TSG-RAN WG4 meeting
26th – 29th October 1999
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Agenda item: AH01
Source: NTT DoCoMo
Title: Link level simulation results for UL performance requirements (FDD)
Document for: Discussion

1.Introduction

Last AH01 meeting agreed detailed simulation assumptions such as the number of diversity branch and values for DPCCH/DPDCH [1]. This paper shows the revised results of UL link level simulations in FDD mode based on the assumptions that have been agreed in AH01.

2.Simulation assumption

Table 1 shows simulation assumptions.

Table 1. Simulation assumptions

Parameter	Assumption
Measurement channels	As specified in Annex A of TS25.101 v2.3.0
Closed power control	Off
AGC	Off
Channel estimation	Ideal
Number of samples per chip	1[sample/chip]
Propagation condition	As specified in Annex B of TS25.101 v2.3.0
Number of bits in AD converter	Floating point simulations
Number of Rake fingers	Equals to number of taps in propagation condition models
Number of Block error	>100
Turbo decoding	Max log-MAP with 8 iterations
Antenna Diversity	2 branch(Eb/Io value is calculated for 1 antenna)

3.Simulation results

In this section, simulation results for both static channel and multi-path fading propagation channels (CASE1,2,3). BLER and BER performance for 4 data rates (12.2kbps, 64kbps, 144kbps, 384kbps) can be seen.

3.1 Static propagation conditions

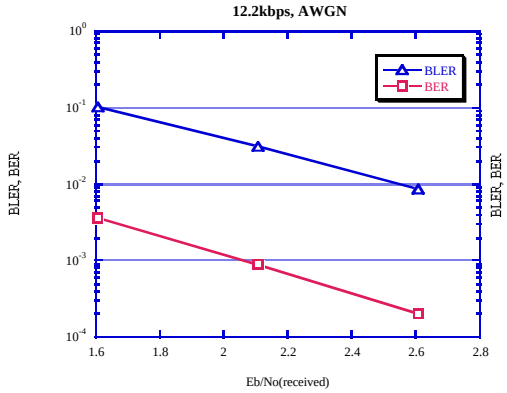


Figure 1. 12.2kbps (AWGN)

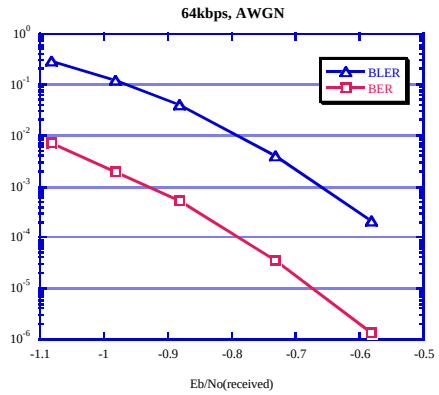


Figure 2. 64kbps (AWGN)

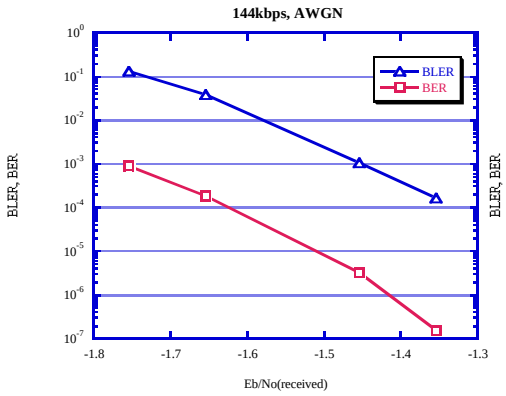


Figure 3. 144kbps (AWGN)

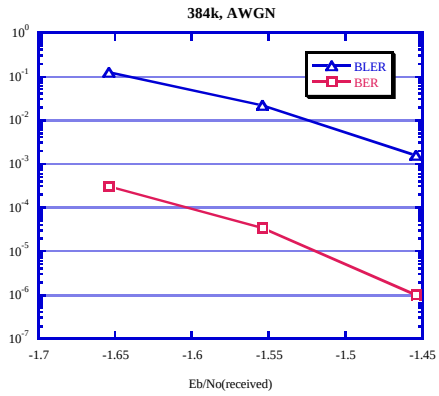


Figure 4. 384kbps (AWGN)

3.2 Multi-path fading propagation conditions, CASE1

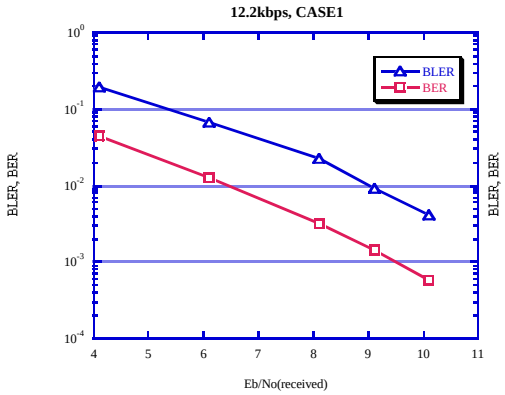


Figure 5. 12.2kbps (CASE1)

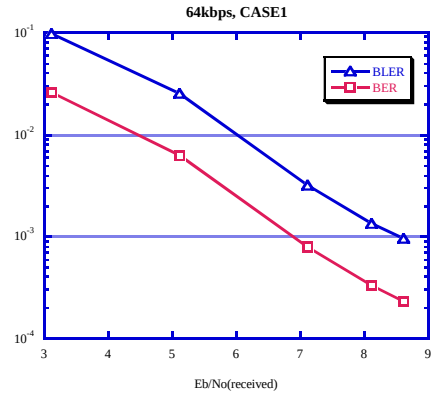


Figure 6. 64kbps (CASE1)

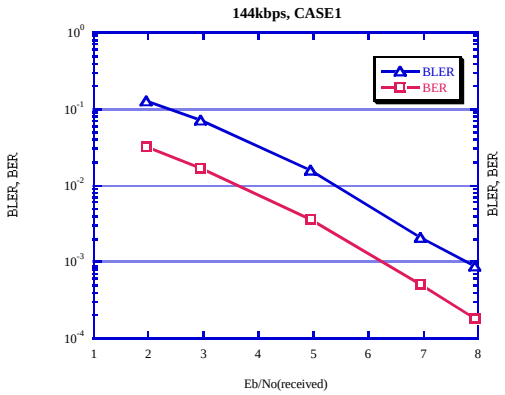


Figure 7. 144kbps (CASE1)

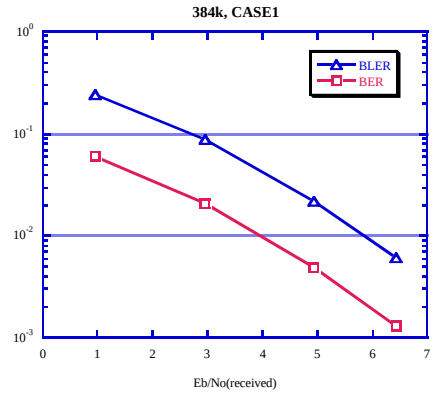


Figure 8. 384kbps (CASE1)

3.3 Multi-path fading propagation conditions, CASE2

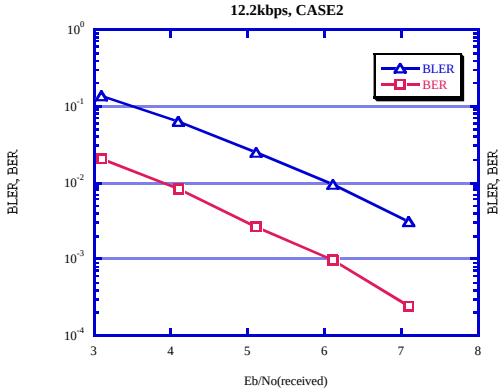


Figure 9. 12.2kbps (CASE2)

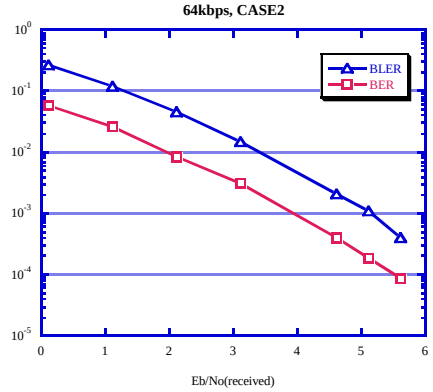


Figure 10. 64kbps (CASE2)

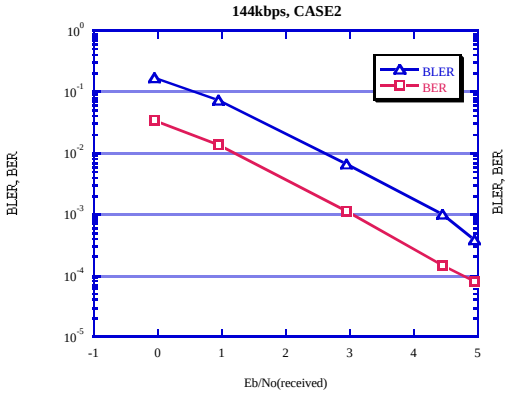


Figure 11. 144kbps (CASE2)

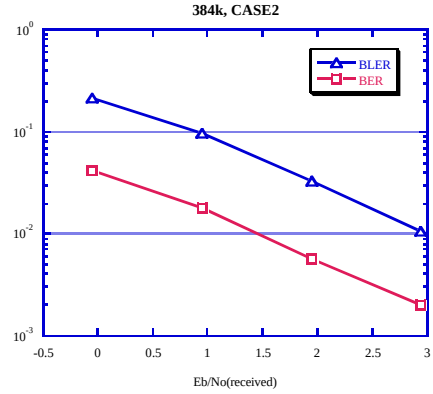


Figure 12. 384kbps (CASE2)

3.4 Multi-path fading propagation conditions, CASE3

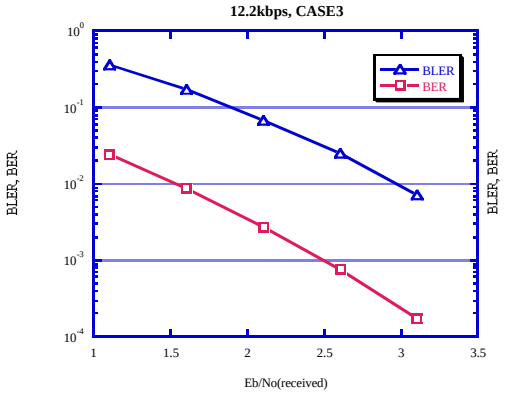


Figure 13. 12.2kbps (CASE3)

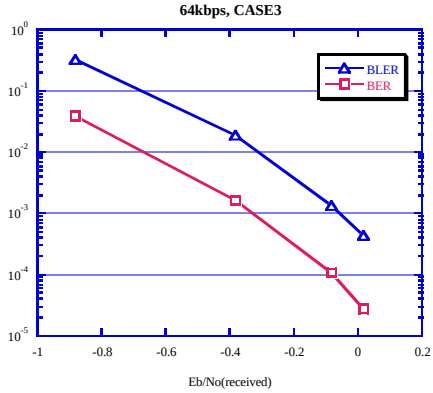
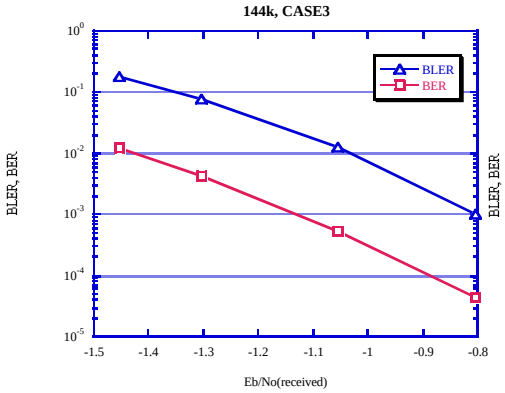


Figure 14. 64kbps (CASE3)



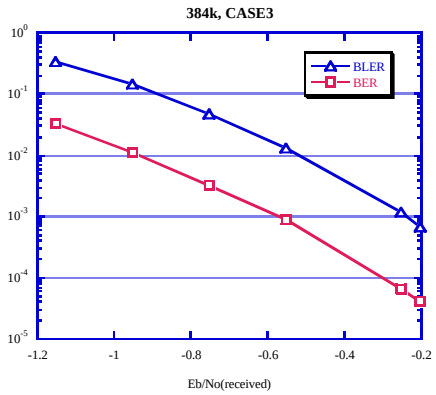


Figure 15. 144kbps (CASE3) Figure 16. 384kbps (CASE3)

4.Conclusion

Table 2 shows the required E_b/N_0 for BLER=10^{-1} to 10^{-3}.

Table 2 Required E_b/N_0 for BLER=10^{-1} to 10^{-3}

	static		CASE 1		CASE 2		CASE 3		
	BLER@ E-1	BLER@ E-2	BLER@ E-1	BLER@ E-2	BLER@ E-1	BLER@ E-2	BLER@ E-1	BLER@ E-2	BLER@ E-3
12.2kbps	1.6	2.5	5.5	8,8	3.5	6.0	1.8	2.9	
64kbps	-1.0	-0.8	3.1	6.0	1.0	3.3	-0.7	-0.3	-0.1
144kbps	-1.75	-1.58	2.5	5.4	0.6	2.6	-1.4	-1.1	-0.8
384kbps	-1.65	-1.53	2.6	5.8	0.8	3.0	-0.9	-0.6	-0.25

This document shows simulation results for BS performance requirements. We propose to decide the specification values for FDD BS performance requirements based on these results with some appropriate implementation margins.

Reference

[1] R4-99595, “Report AH01 meeting” (AH01 secretary)