TSG-RAN Working Group 4 meeting #6
Queensferry, Scotland
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**TSGR4#6(99) 360**

**Agenda Item:**

**Source:** Siemens

**Title:** Proposed changes due to Timing Advance in the TDD Mode

**Document for:** Decision

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## Introduction

In TDD mode, timing advance can be used to serve cells without increasing the midamble length or the guard periods. The timing advance procedure is described in the TSG RAN WG1 document [1]. According to [2] presented and agreed in principle during the last WG4 meeting, TA should be included in the relevant WG4 specification.

## Discussion

The timing advance granularity in TSG RAN WG1 [1] is currently defined as multiple of 4 chips (= 1.04 µs), with a parameter range from 0 to 255. The responsibility of WG4 is to define the measurement error of the TA value. In GSM the corresponding values are: 1 bit ( = 3.69µs) TA with less than ½ bit period (1.85 µs) assessment error for stationary MS. For MS moving at 500 km/h the additional error shall be less than ¼ bit period (0.92µs). In particular this requirement needs to be met at 3 dB below reference sensitivity !
For UTRA TDD it is proposed to allow an measurement error of 2 chips (= 521 ns). Since the TA procedure is already included in WG1 specification, it is only necessary to add the requirement on the measurement error to the relevant WG4 specification TS25.105 “BS Radio Transmission and Reception TDD”. Additionally a test case to verify the TA procedure needs to be added to TS25.142 “BS Conformance Testing TDD”.
More information on timing advance from higher layer point of view is included in [3] and [4].

## Text proposal for TS 25.105

It is proposed to add a new section 7.9 “Timing Advance (TA) Requirements” as follows:
The conditions under the requirements which must be met shall be 3dB below reference sensitivity level in section 7.2.

- On request the BS shall measure the delay of the received signal relative to the expected signal from an UE at zero distance under static channel conditions. This delay, called the timing advance, shall be rounded to the nearest value corresponding to 4 chips period. The delay shall be assessed in such a way that the measurement error (due to noise and interference) is less than 2 chips periods for stationary UE.

## Conclusion

Text to include the requirements on Timing Advance in accordance with the principles given in TSG RAN WG4 Tdoc 337/99 is proposed and should be included in the relevant WG4 standard specification.

## References


[1] 3GPP TSG RAN WG1 TS25.224, V 1.0.0, Physical Layer Procedures (TDD)
[2] 3 GPP TSG RAN WG4 Tdoc 337/99 “Application of Timing Advance (TA) in the TDD mode”
[3] 3 GPP TSG RAN WG2 Tdoc 633/99 “Introduction of Timing Advance for TDD”
[4] 3 GPP TSG RAN WG3 Tdoc 604/99 “Timing Advance for TDD”