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Introduction

This paper describes the characters of the common physical channels in the low chip rate TDD option.

Conclusion

It is proposed to discuss and include the following text into the corresponding section in TR25.928.

---------- changes to TR25.928 begin ----------

7.2.3 Common physical channels

7.2.3.1 Primary common control physical channels (P-CCPCH)

[Description:]
The BCH as described in subclause 7.3.2 'Common Transport Channels' is mapped onto the Primary Common Control Physical Channels (P-CCPCH1 and P-CCPCH2). The position (time slot / code) of the P-CCPCHs is fixed in low chip rate TDD option, see subclause 7.3.2 'Common Transport Channels'. An encoded bit identifies whether the interleaving frame in the P-CCPCH contains a BCH (1) or not (0).

[Rationale:]
7.2.3.1.1 P-CCPCH Spreading
The P-CCPCHs use fixed spreading with a spreading factor SF = 16. The P-CCPCH1 and P-CCPCH2 always use channelisation code 0 and 1 respectively.

7.2.3.1.2 P-CCPCH Training sequences
The training sequences, i.e. midambles, as described in the MA-generation chapter are used for the P-CCPCHs. The basic midamble code $m^{(1)}$ is used for P-CCPCHs as training sequence.
As mentioned in sub clause of P-CCPCH in 25.928, P-CCPCHs are mapped onto first two code channels of Ts0 with spreading factor of 16. Other code channel in Ts0 should also use spreading factor of 16.
Each transport channel assigned in TS0 has channel impulse responses of length W=16 such that there are 8 midamble codes used for TS0.
Ts0 is configured in the following way: Each of the 8 midamble codes is assigned to 2 code channels of spreading factor 16. The first midamble code is assigned to the first 2 code channels of spreading factor 16. The next midamble code to the next 2 code channels of spreading factor 16 and so forth. The P-CCPCHs are assigned to the first midamble code. In order to provide flexibility, it is possible that the Node B uses – for channels other than P-CCPCHs - a certain midamble code assigned to only 1 code channel of spreading factor 16. In that case, the

second code that is assigned to the same midambles is not used by another UE.

[Explanation difference:]
In high chip rate option, the P-CCPCH always contains only the BCH . The position (time slot / code) of the P-CCPCH is known from the Synchronisation Channel (SCH).

In low chip rate option, the P-CCPCH can also contain the PCH and FACH as well as the BCH. The P-CCPCHs are mapped onto two code channels of the DL time slot (time slot 0) which is followed by the DwPTS

There are two kinds of burst types in high chip option and the burst type 1 is used for the P-CCPCH.
There is only one burst type in the low chip rate option.

Because both the uplink and downlink physical channels are work under the synchronization mode and "smart antenna" method is strongly recommended to be used, so the interference on P-CCPCH is thought to be very little in low chip rate TDD option. As a result, "Tx diversity" has not been considered to be applied in low chip rate TDD. BSTTD applied for P-CCPCH can be taking into consideration.

7.2.3.2 Secondary common control physical channel (S-CCPCH)

[Description:]
PCH and FACH can be mapped onto one or more secondary common control physical channels (S-CCPCH). In this way the capacity of PCH and FACH can be adapted to the different requirements. The time slot and codes used for the S-CCPCH are broadcast via cell information. An encoded bit identifies that the interleaving frame in the S-CCPCH contains no BCH. This bit is always 0.

[Rationale:]
7.2.3.2.1 S-CCPCH Spreading
There are two S-CCPCHs (S-CCPCH 1 and S-CCPCH 2) mapped onto two codes of spreading factor 16.

7.2.3.2.3 S-CCPCH Training sequences
The training sequences, i.e. midambles as described in the MA-generation chapter, are used for the S-CCPCH.

7.2.3.3 The physical random access channel (PRACH)
[Description:]
The RACH is mapped onto one or more uplink physical random access channels (PRACH). In such a way the capacity of the RACH can be flexibly scaled depending on the operators need.

[Rationale:]
7.2.3.3.1 PRACH Spreading
The uplink PRACH uses either spreading factor SF=16 or SF=8 as described in subclause 7.3.2.3 ‘The Random Access Channel (RACH)’. The PRACH configuration (time slot number and assigned spreading codes) is broadcast through the BCH information

7.2.3.3.2 PRACH Burst Types
The burst type used on the PRACH is the same as for a traffic channel.

7.2.3.3.3 PRACH Training sequences
The training sequences, i.e. midambles as described in the MA-generation chapter, are used for the PRACH.

7.2.3.3.4 Association between Training Sequences and Channelisation Codes

In the low chip rate TDD option there is a different concept for the RACH. Resource units on the traffic time slots are used for the random access channels. For this reason the PRACH is described and allocated as e.g. the DPCH. Thus, there is no additional association between training sequences and channelisation codes like in the high chip rate TDD option.

[Explanation difference:]

In subclause 10.6.2 “random access procedure”, it has been mentioned that the random access procedure of low chip rate option has two-step approach. The SYNC1 word is used to carry out uplink synchronisation and to resolve the access collision. This two-step procedure enables the ~~P-RACH~~PRACH to be transmitted with high synchronisation precision as DPCH.

So in low chip rate TDD option, the ~~P-RACH~~PRACH is uplink synchronized with other uplink traffic, the burst type used on the ~~P-RACH~~PRACH is the same as for DPCH while in high chip rate TDD option the burst type of the PRACH is a little different from that of DPCH.

7.2.3.4 The synchronisation channel (SCH)

[Description:]

There are two dedicated physical synchronisation channels —DwPTS and UpPTS in each subframe of the low chip rate option as described in subclause 7.2.1 ‘Frame Structure’ and 7.2.2.2 ‘Burst Types’.

[Rationale:]

The burst structures used for DwPTS and UpPTS are different from that used for other physical channels. The detailed description of the burst structure of DwPTS and UpPTS can be found in subclause 7.2.2.2 ‘Burst Types’.

As described in subclause 7.2.2.2 ‘Burst Types’, there are no training sequences in DwPTS and UpPTS. The SYNC code in DwPTS and the SYNC1 code in UpPTS are not spread.

[Explanation difference:]

In low chip rate option, there are two dedicated Physical Synchronisation Channels, DwPTS for the down link synchronisation and UpPTS for the uplink synchronisation.

In high chip rate option, there is only one dedicated Physical Synchronisation Channel for down link synchronisation

---------- changes to TR25.928 end ----------