3GPP TSG RAN WG1 ***TSGR1#16(00)1198***
Pusan, Korea, 10th – 13th October, 2000

Agenda item:

Source: **Philips**

Title: **UE transmit timing in soft handover**

Document for: **Discussion and Decision**

1. Introduction

A number of issues relating to UE transmit and receive timing are described in [1]. One problem relates to the combined effect of the UL Tx timing reference and the valid window for DL Rx timing, which together can cause the UE transmit timing to slew continuously.

The present document continues the discussion on this issue, and suggests some possible alternative solutions.

2. Summary of the problem

TS25.211 section 7.6.3 states that the UE uplink DPCH transmission takes place approximately T_0 chips after the reception of the first significant path of the corresponding downlink DPCH frame. TS25.133 section 7.1 specifies the maximum and minimum rates of transmit timing adjustment which the UE shall use in order to adjust the uplink Tx timing to T_0 ? 1.5 chips from the first significant received path, where T_0 = 1024 chips.

This appears to be satisfactory while the UE is not in soft handover, when it is only communicating with one BS.

However, the required behaviour in soft handover appears not to be clearly defined.

One interpretation would be that when more than one cell is in the active set the UE transmit timing should always be adjusted to T_0 ? 1.5 chips from the first significant received path from *any* of the cells.

The UE is also required to report when the receive-timing of any DL DPCH in the current active set has drifted outside a pre-determined range, known as the “valid range” or “reporting range”.

When a BS is notified that its DL DPCH has drifted outside this range, it can adjust the DL transmit timing by 256 chips to bring the receive timing back into the valid range.

It has been pointed out in [1] that the combination of the uplink timing adjustment and the downlink timing adjustment can result in a situation where a UE continually reports BSs in the active set as being outside the valid range. The problem is illustrated in Figure 1, where DL signals are received from 3 cells A, B and C:

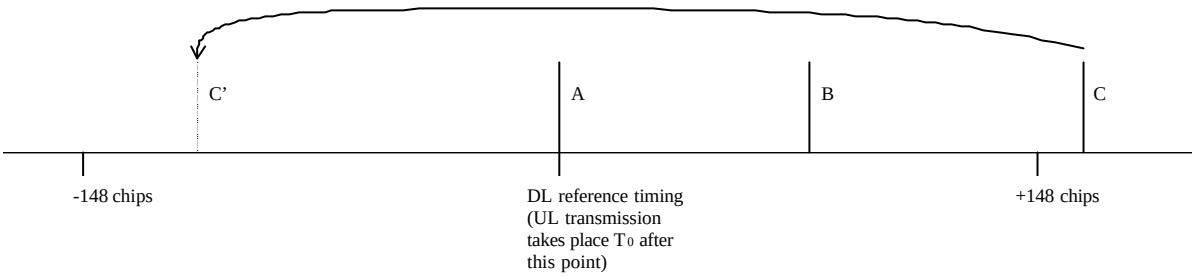

Figure 1

The valid range is shown by way of example as ?148 chips from the UL timing reference. The receive-timing of cell C has drifted outside this range, and the UE reports it to the BS, so its timing is adjusted by 256 chips to position C'. The UE then begins to adjust its timing towards C' + T_0, which causes cell B to go outside the reporting window. This process can repeat continually, with the UE continually advancing its transmit timing.

3. Discussion and possible solutions

A useful goal for the solution would be to minimise the frequency of unnecessarily reporting cells as being outside the valid range.

Option 1

One possible solution to this problem which was proposed in [1] consists of setting the UE timing to T_0 + 128 chips after the first significant path is received, instead of T_0 chips after the first significant path.

This solution relies on the assumption that the reporting range is symmetric with respect to T_0. However, according to the current version of TS25.331, this will not necessarily be the case, as both the upper and lower thresholds of the reporting range can take any value between T_0 – 256 chips and T_0 + 256 chips. Thus it is possible to signal an asymmetric reporting range, for example from T_0 to T_0 + 256 chips.

In this case, setting the UE transmit timing to T_0 + 128 chips after the first significant path would result in a similar problem to that described above:

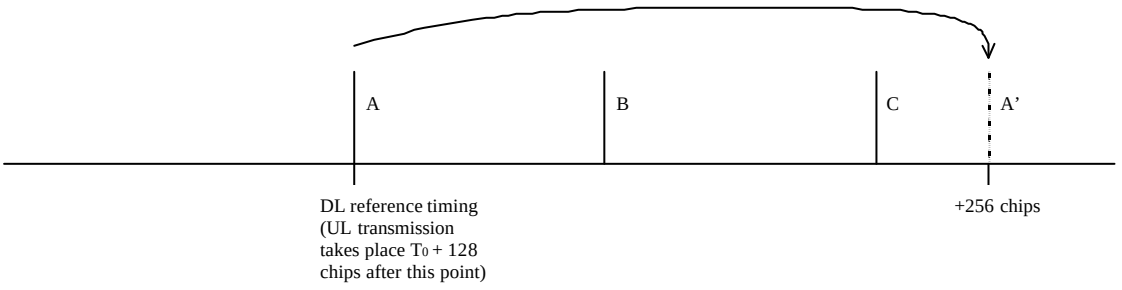

Figure 2

As the UE adjusts its transmit timing to be T_0 + 128 chips after cell A is received, cell A goes outside the reporting range. The network moves A to A', and the UE starts adjusting its transmit timing to T_0 + 128 chips after cell B is received. Cell B goes outside the reporting range, and so on.

Thus a fixed offset does not always solve the problem.

Option 2

In soft handover it may not be necessary to specify the precise method which the UE should use to calculate the UL Tx timing reference. A very simple solution to the problem is therefore to allow the UE to apply an additional variable offset ? between the first received DL path and the UL transmission – i.e. the UE would set the UL Tx timing to be T_0 + ? after the first significant received path of the first cell. This would allow the UE to choose a suitable value for ? which avoided continuously-slewing Tx timing given the current upper and lower thresholds of the reporting range, as well as being appropriate to the requirements of closed-loop power control.

In practice it would be necessary to set limits on the range of ? in order to ensure sensible UE behaviour.

These limits could be set in terms of the time-difference of arrival between the first significant path of the first cell and the first significant path of the last cell, for example:
-20 ? ? ? $|DL_n - DL_1| + 20$
where DL_n is the time of arrival of the first significant path from the last cell and DL_1 is the first significant path from the first cell.

In the case of the "first significant paths" from each cell being received very close together, this would converge to give ? in the range ?20 chips. The additional offset ? would not apply when only 1 cell was in the active set.

Examples of how the two extremities of the range of ? can be useful in adapting to different reporting ranges are shown shown in Figure 3 and Figure 4:

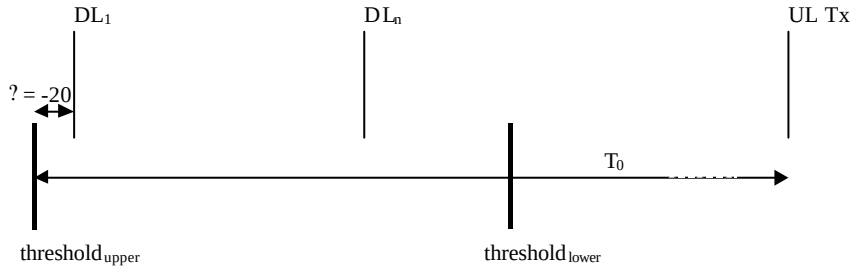

Figure 3

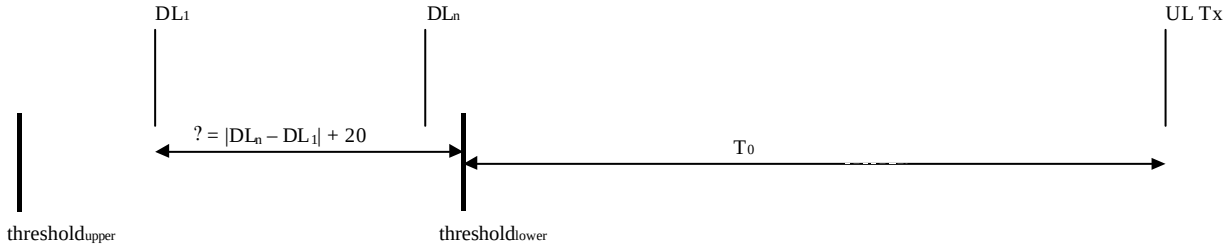

Figure 4

A draft CR for this solution is contained in [2].

Option 3

It may not be desirable to allow the UE to have so much flexibility in determining the timing of the UL transmissions in soft handover. It could be preferable to specify precisely the algorithm which the UE must use in soft handover.

If this is the case, an optimal method would take into account the timings of the received DL signals, the thresholds of the reporting range, and the time required to decode TPC commands, as well as providing a small amount of hysteresis.

A formula which takes all these issues into account and resolves the problem of continual slewing for any valid dimensions of the reporting range is as follows:

$$? = \left\lfloor \frac{threshold_{upper} - T_0}{threshold_{upper} - threshold_{lower}} \times \left| DL_n - DL_1 \right| - 40 \right\rfloor - 20 \quad \text{.....Equation (1)}$$

The resulting offset is shown in Figure 5, Figure 6 and Figure 7. These figures show how the term $\frac{threshold_{upper} - T_0}{threshold_{upper} - threshold_{lower}}$ in equation (1) is used to adjust the position of the reporting range relative to the DL Rx timings depending on the symmetry of the signalled reporting range, so as to prevent continual slewing of UL Tx timing, while also optimising the time available for decoding TPC commands. A 20-chip hysteresis margin is included.

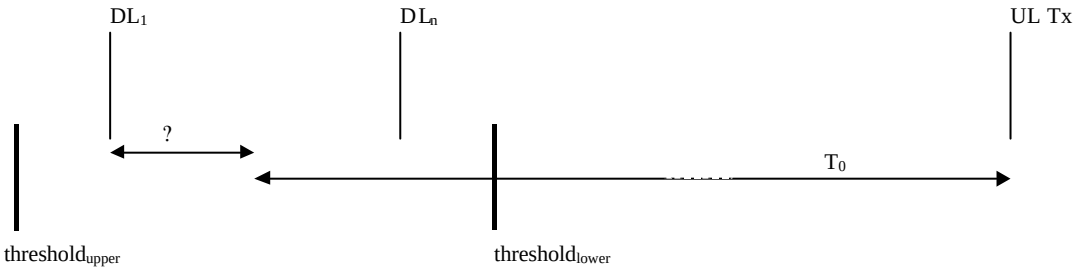

Figure 5: Symmetric reporting range

If the signalled reporting range is symmetric as in Figure 5, the value of ? is adjusted to position the DL paths centrally within the reporting range.

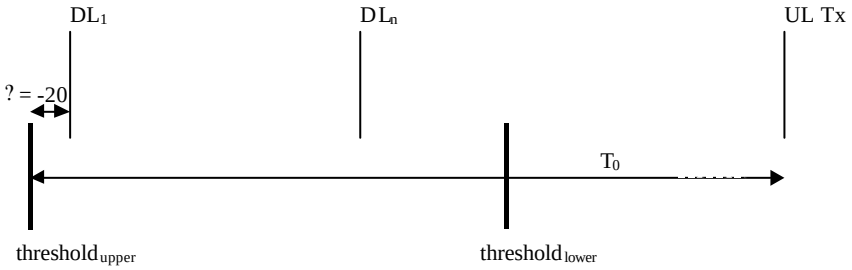

Figure 6: Asymmetric reporting range – case 1

If the signalled reporting range is biased in the direction shown in Figure 6, the value of ? is adjusted to maximise the time available for decoding TPC commands and to prevent continual UL Tx time slewing.

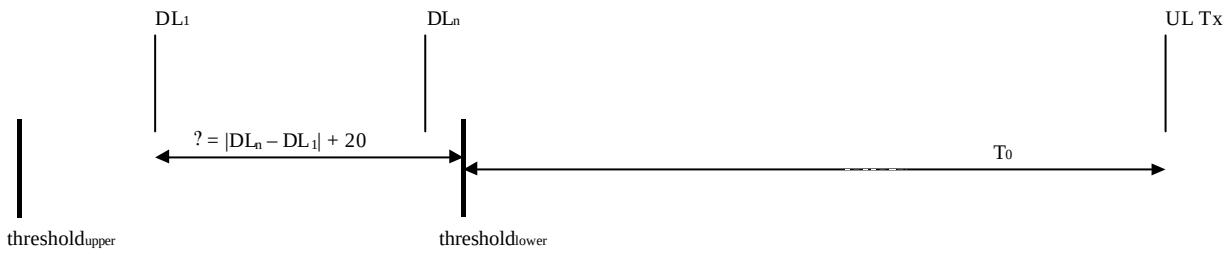

Figure 7: Asymmetric reporting range – case 2

If the signalled reporting range is biased in the direction shown in Figure 7, the value of ? is adjusted to minimise the delay between DL Rx and UL Tx and to prevent continual UL Tx time slewing.

A draft CR for this solution is contained in [3].

4. Size of reporting range

According to TS25.331, the upper and lower thresholds of the reporting range can be set to any value within the range ?256 chips from T_0 (i.e. between 769 and 1280 chips).

The main constraints on the values of the reporting thresholds are as follows:

1. The difference between the upper and lower thresholds should be greater than or equal to 256 chips if the network is to be able to adjust the DL timings so as to arrive inside the reporting range.
2. The lower threshold should be high enough to allow adequate time for decoding TPC commands in the UE.

It is suggested in [1] that the values which the reporting thresholds can take should be more restricted.

The second of the above constraints would appear to be the most critical, and one way of alleviating this could be simply to place a restriction on the *lower* threshold, e.g. not more than 148 chips less than T_0 (i.e. a range of 876 chips to 1280 chips). This minimises the loss of flexibility in setting the reporting range, while avoiding unnecessary intrusion into the time available for processing TPC commands in the UE.

5. Conclusions

Some alternative solutions have been proposed to the problem of continually-slewing UE timing and continuous reporting of downlink signals as out-of-range.

Option (1) does not solve the problem if the reporting range is asymmetric. Option (2) gives flexibility to the UE to solve the problem, but does not fully specify how the UE should calculate the required offset. Option (3) specifies a formula by which the offset can be calculated to solve the problem.

Two alternative draft CRs are provided in [2] and [3] for TS25.211 for each of options 2 and 3.

If either of these CRs are accepted, a LS to RAN WG4 would be required, to request corresponding changes in TS25.133.

If a further restriction is to be applied to the lower reporting threshold (as discussed in section 4 above), a LS would be required to RAN WG2.

References

[1] R1-00-1100, *"UE timing related issues"*, Qualcomm

[2] R1-00-1199, *"Clarification of UL timing reference"*, Philips

[3] R1-00-1200, *"Improvement of UL timing reference*", Philips