TSG-RAN Working Group 1 Meeting #16 ***TSGR1#16(00)1182***

Pusan, Korea
September 10-13, 2000

Agenda Item: **AH24: High Speed Downlink Packet transmission**
Source: **Panasonic**
Title: **Link level simulation results of HSDPA**
Document for: **Discussion**

1 Introduction

In TSG-R1 meeting #15 link level simulation assumptions for High Speed Down Link Packet Access (HSDPA) were presented [1]. This contribution presents a simulation result of HSDPA according to the assumption that was presented in the last meeting. This contribution also points out some simulation assumptions that should be cleared.

2 Simulation parameters

2.1 General simulation parameters

Simulation parameters were set according to the presented assumptions [1]. The shaded parts are different from the presented assumptions.
In this contribution the simulation was run in AWGN channel and without HARQ.

Parameter	Value	Comments
Carrier Frequency	2GHz	
Propagation conditions	AWGN	
Vehicle Speed for Flat Fading	None	Only AWGN
CPICH power	10%(-10dB)	10% of Ior (Ior is Maximum Transmission power of NodeB)
Closed loop Power Control	OFF	
HSDPA frame Length	3.33 ms	
Ior/Ioc	Variable	
Channel Estimation	Non-Ideal (using CPICH)	
Fast fading model	Jakes spectrum	
Channel coding	Turbo code (PCCC), rate 1/2, 3/4, etc.	Rate ¼ was not simulated see 4.1 about turbo encoder structure
Tail bits	6	Only input bits for turbo encoder for trellis termination are sent
Max no. of iterations for Turbo Coder	8	
Metric for Turbo Coder	Max	
Input to Turbo Decoder	Soft	
Turbo Interleaver	Random	
Number of Rake fingers	1	AWGN channel
Hybrid ARQ	None	
Max number of frame transmissions for H-ARQ	None	
Information Bit Rates (Kbps)	As defined	
Number of Multicodes Simulated	1	Only 1 code
TFCI model	None	Associated downlink DPCH is not transmitted

STTD	Off	AWGN channel
Other L1 Parameters	As Specified in Release-99 Specification	
Pilot Ec/Ior	-7dB	As specified in R1-00-727

2.2 Power allocation at Node B

Transmission power allocation in this simulation is shown in Fig1. CPICH is transmitted at 10% of Maximum transmission power of NodeB. DSCH is transmitted at 40% of Maximum transmission power of NodeB. 50% of Maximum transmission power of NodeB is allocated for the other channels, but in this simulation other channels are not transmitted. In this simulation Ec/Ior is calculated as –4dB(40% of NodeB's maximum transmission power).

E_c / I_{or} ? ?4*dB*

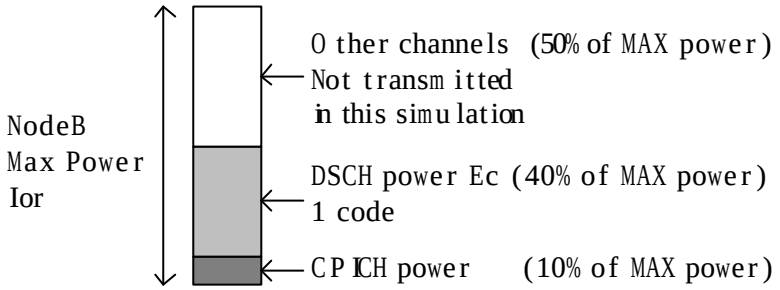

Fig 1 Transmission Power allocation at NodeB

2.3 Number of information bit and puncturing parameters

Simulation was run without rate matching to remove the effect of rate matching algorithm. Therefore the numbers of information bits were decided according to the number of bits of PDSCH. Dummy bits were added to adjust the number of bit per frame in MCS2,4,6,8. Channel codec block diagram is shown in Fig3.

For further simulation, we will use rate-matching algorithm which is specified in 25.212. Using the specified rate matching algorithm, number of information bits will be set according to MCS which was shown by proposed assumption [1].

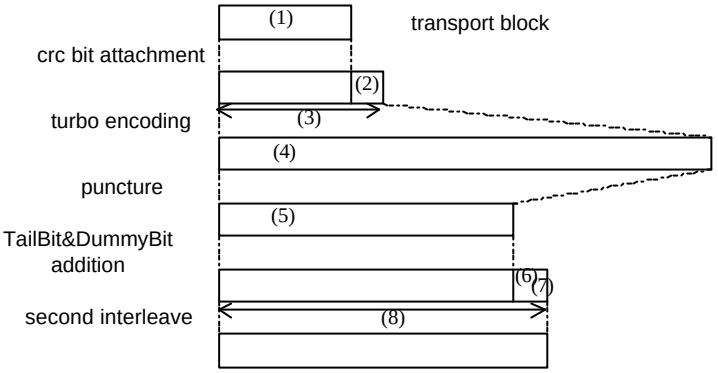

Fig 2 Number of bits in turbo encoder

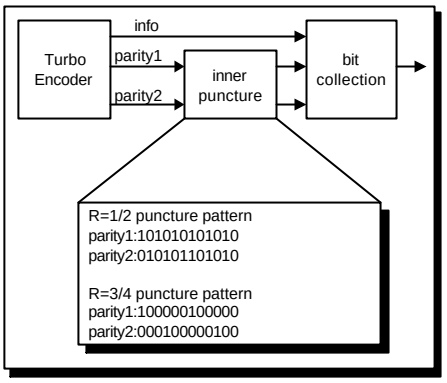

Fig 3 Rate Matching Block Diagram

Table 1. Number of bits for each block

MCS	Modulation	Rate	InfoBit (1)	CRC Bit (2)	Info+CRC (3)	Enced Bit (4)	Punced Bit (5)	TailBit (6)	Dummy Bit (7)	OutPut(Bit) (8)	Info Rate(Mbps)
8	64	¾	1770	24	1794	5382	2392	6	2	2400	0.53
7	64	½	1173	24	1197	3591	2394	6	0	2400	0.35
6	16	¾	1170	24	1194	3582	1592	6	2	1600	0.35
5	16	½	773	24	797	2391	1594	6	0	1600	0.23
4	8	¾	870	24	894	2682	1192	6	2	1200	0.26
3	8	½	573	24	597	1791	1194	6	0	1200	0.17
2	4	¾	570	24	594	1782	792	6	2	800	0.17
1	4	½	373	24	397	1191	794	6	0	800	0.11

3 Simulation Results

FER vs. Eb/No is shown in Fig.4 In comparison to Motorola's simulation results [2] is shown in Table. 2. FER vs. Ior/(Ioc+No) is shown in Fig.5. note that Ec/Ior is fixed to -4dB in this simulation.

Table. 2 Simulation results

MCS	Eb/No when FER = 1%		
	Panasonic	Motorola[2]	Difference between Motorola[2] and Panasonic
1	2.5 dB	2.1 dB	0.4 dB
2	3.6 dB	3.5 dB	0.1 dB
3	3.8 dB	Not simulated	Not simulated
4	5.8 dB	Not simulated	Not simulated
5	4.2 dB	4.2 dB	0.0 dB
6	6.1 dB	6.4 dB	0.3 dB
7	7.0 dB	6.8 dB	0.2 dB
8	9.9 dB	10.0 dB	0.1 dB

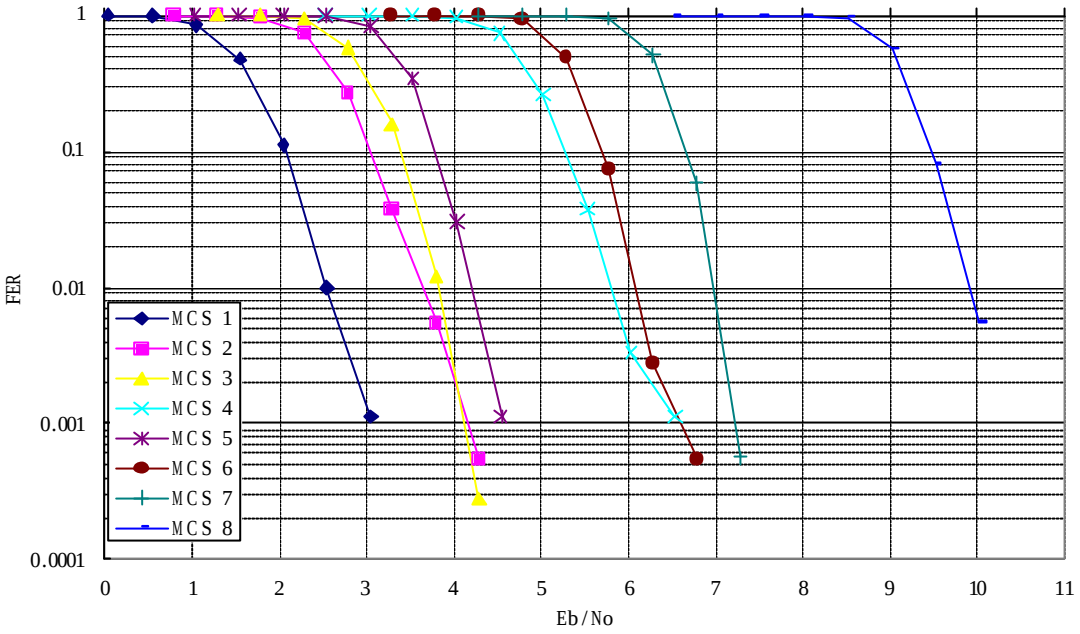

Fig 4 Static (AWGN) Channel FER VS. Eb/No

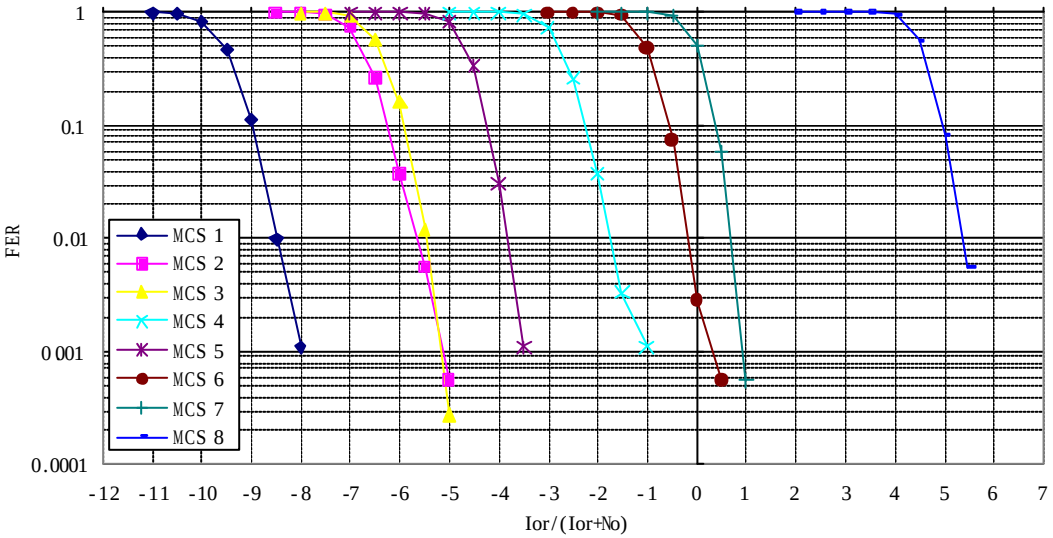

Fig.5 Static (AWGN) Channel FER VS. Ior/(Ior+No)

4 Simulation parameters to be fixed

4.1 Rate ¼ Turbo encoder structure

There are two methods to generate ¼ turbo encoder.
One is to use two different interleavers in turbo encoder, and the other is to use one interleaver and employ repetition to increase parity bits (Fig.6).
We propose to use turbo encoder with repetition (Fig.6) and to be added to the simulation assumption list.

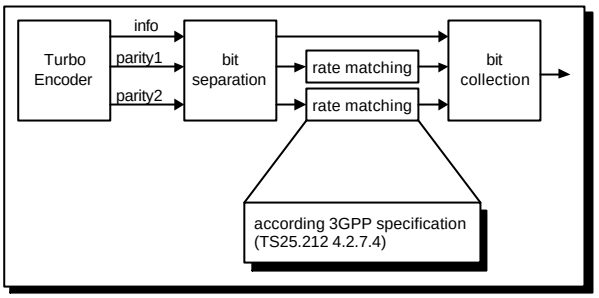

Fig 6 Turbo encoder with repetition

5 Conclusion

We present the simulation results of HSDPA according to the proposed simulation assumptions [1]. The results are found to be close (from 0.0dB to 0.4dB differences) to Motorola's simulation results. [2]
We proposed a simulation assumption of ¼ turbo encoder, which should be writen in simulation assumption document.

6 References

[1] R1-00-1093, "Link Evaluation Methods for High Speed Downlink Packet Access (HSDPA)" Berlin, Germany, August 21-24, 2000.
[2] R1-00-727, Motorola "High Speed Downlink Packet Access", Tokyo, Japan May 22-25, 2000