TSG-RAN Working Group 1 meeting #14 *TSGR1(00)0937*
Oulu, Finland, July 4-7, 2000

Agenda Item: AH21

Source: CWTS

To: TSG RAN WG1

Title: Frame structure for low chip rate TDD option

Document for: Decision

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1. Summary

UTRA has two modes, FDD (Frequency Division Duplex) & TDD (Time Division Duplex), and the TDD mode has two options, high chip rate option (with 3.84 Mcps) and low chip rate option (with 1.28 Mcps). Because of the different transmitting rate, the frame structure of the two options has some difference. In high chip rate option, a 10 ms radio frame is divided into 15 slots (2560 chip/slot at the chip rate 3.84 Mcps). While in low chip rate option, a 10 ms radio frame is subdivided into 2 equal 5 ms sub-frames. Each sub-frame is divided into 7 normal traffic slots (864 chip/slot), two pilot slots (one is 96 chips, the other is 160 chips) and one special guard period (96 chips). There are total 6400 chips/5 ms at the chip rate 1.28 Mcps.

2. Introduction and comparison with high chip option

As in high chip rate TDD option, all physical channels in low chip rate option take three-layer structure with respect to timeslots, radio frames and system frame numbering (SFN). The length of the radio frame is 10 ms both in high and low chip rate TDD option. But in low chip rate TDD option, this 10 ms radio frame is subdivided into 2 equal 5 ms sub-frame to allow the fast update of power control, uplink synchronization, and smart antenna beamforming.

The time slots are used in the sense of a TDMA component to separate different user signals in the time and the code domain. In high chip option, the 10 ms radio frame is subdivided into 15 time slots (TS) of $2560*T_c$ duration each. A time slot corresponds to 2560 chips. All the time slots in the radio frame are same.

While in low chip rate option, a 5 ms sub-frame is subdivided into 7 normal traffic time slots (each corresponds to 864 chips) with 2 pilot time slots and 1 special guard period. The 2 pilot time slots (DwPTS and UpPTS) are used for downlink and uplink synchronisation. (Note that the UpPTS is not continuously transmitted and the DwPTS is not continuously received.) The special guard period is used as a switching point to separate the uplink and downlink. Its 96 chips length ensures that the UpPTS transmitted by one UE will not disturb the reception of the DwPTS for other UEs being close by and the 96 chips length can support the cell radius up to about 11km. If the distortion is accepted in the network the cell radius can be bigger.

In high chip rate option, each of the 15 time slots in one radio frame can be allocated to either the uplink or the downlink which means that there can be multiple switching points in one radio frame.

In low chip rate option, among the 7 normal traffic time slot in the 5 ms sub-frame, Ts0 is always allocated as downlink while Ts1 is always allocated as uplink. The time slots for the uplink and the time slots for the downlink are separated by the switching point. Between the downlink time slots and uplink time slots, the special guard period is the switching point to separate the uplink and downlink. In each 5ms sub-frame, there are two switching points (uplink to downlink and vice versa). This is to ensure that Node B can update the smart antenna's beamforming in 5 ms. And it is also based on the consideration of decrease the interference between different UE in an synchronized TDD mode(e.g. an UE may need to pre-transmit its signal due to the uplink synchronisation requirement, if multiple switching points are assigned, this pre-transmitted signal may cause some serious interference to other downlink time slot). Using the above frame structure, the low chip rate TDD option can operate on both symmetric and asymmetric mode by properly configuring the number of downlink and uplink time slots; (note that whatever the time slot configuration will be, the

GP and DwPTS position within the frame should not change in order not to desynchronise the UEs and in order to allow Node B on air synchronisation procedures which make use of the DwPTS channel!) . It should be noted that in asymmetric operation mode, at least one normal uplink time slot and one downlink time slot will be allocated for traffic (Ts0 for downlink and Ts1 for uplink).

3. Proposal

We propose to modify following paragraphs in the TS25.221 as the description of the frame structure of the low chip rate TDD option.

3GPP Meeting #14
Oulu, Finland, 04-07 Jul 2000

Document R1-00-
e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

25.221	CR		Current Version:	3.2.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to:	RAN#10	for approval	X	strategic		(for SMG use only)
list expected approval meeting # here ↑		for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)* (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]

Source: CWTS **Date:** 29.06.2000

Subject: Inclusion of the low chiprate TDD option frame structure into 25.221

Work item: Low Chiprate TDD option

Category: *(only one category shall be marked with an X)*

F	Correction		**Release:**	Phase 2	
A	Corresponds to a correction in an earlier release			Release 96	
B	Addition of feature	X		Release 97	
C	Functional modification of feature			Release 98	
D	Editorial modification			Release 99	
				Release 00	X

Reason for change: The frame structure of the low chiprate TDD option is different to that of the high chiprate TDD option and has therefore to be specified separately.

Clauses affected:

Other specs affected:

Other 3G core specifications	[ ]	→ List of CRs:
Other GSM core specifications	[ ]	→ List of CRs:
MS test specifications	[ ]	→ List of CRs:
BSS test specifications	[ ]	→ List of CRs:
O&M specifications	[ ]	→ List of CRs:

Other comments:

help.doc

<--------- double-click here for help and instructions on how to create a CR.

5 Physical channels

All physical channels take three-layer structure with respect to timeslots, radio frames and system frame numbering (SFN), see [14]. Depending on the resource allocation, the configuration of radio frames or timeslots becomes different. All physical channels need guard symbols in every timeslot. The time slots are used in the sense of a TDMA component to separate different user signals in the time and the code domain. The physical channel signal format for high and low chip rate TDD option are ~~is~~ presented in figure 1 and figure 2 respectively.~~.~~

A physical channel in TDD is a burst, which is transmitted in a particular timeslot within allocated Radio Frames. The allocation can be continuous, i.e. the time slot in every frame is allocated to the physical channel or discontinuous, i.e. the time slot in a subset of all frames is allocated only. A burst is the combination of a data part, a midamble and a guard period. The duration of a burst is one time slot. Several bursts can be transmitted at the same time from one transmitter. In this case, the data part must use different OVSF channelisation codes, but the same scrambling code. The midamble part has to use the same basic midamble code, but can use different midambles.

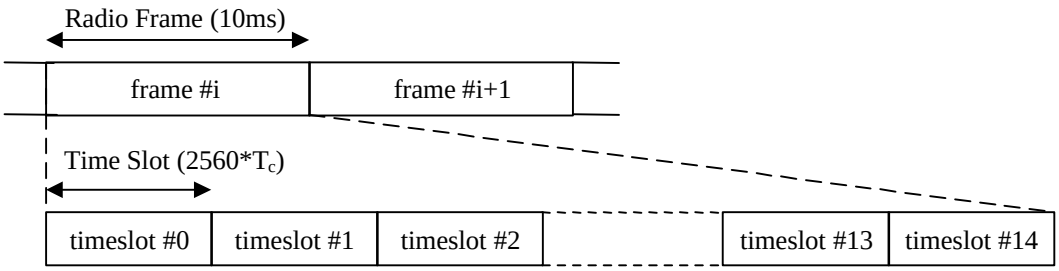


Figure 1: Physical channel signal format for the high chiprate TDD option

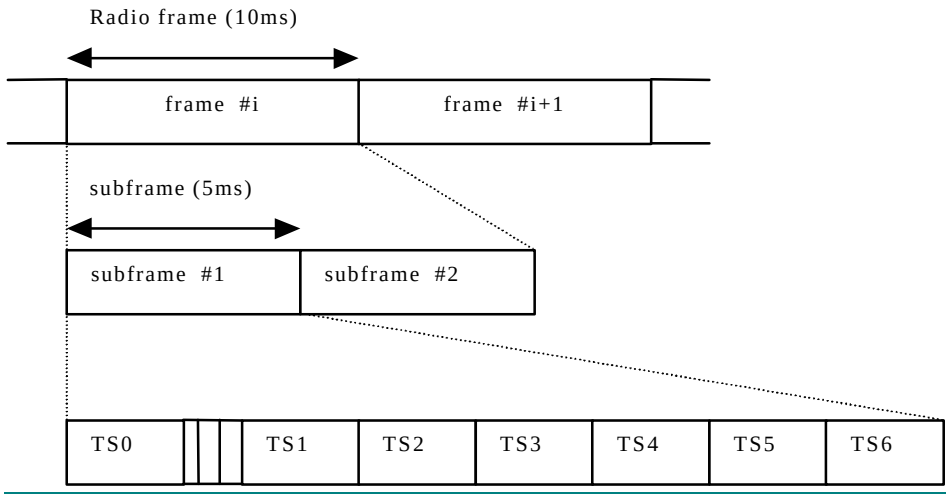


Figure 2: Physical channel signal format for the low chiprate TDD option

The data part of the burst is spread with a combination of channelisation code and scrambling code. The channelisation code is a OVSF code, that can have a spreading factor of 1, 2, 4, 8, or 16. The data rate of the physical channel is depending on the used spreading factor of the used OVSF code.

~~The midamble part of the burst can contain two different types of midambles: a short one of length 256 chips, or a long one of 512 chips. The data rate of the physical channel is depending on the used midamble length.~~

So a physical channel is defined by frequency, timeslot, channelisation code, burst type and Radio Frame allocation The scrambling code and the basic midamble code are broadcast and may be constant within a cell. When a physical channel

is established, a start frame is given. The physical channels can either be of infinite duration, or a duration for the allocation can be defined.

5.1 Frame structure

5.1.1 Frame structure for the high chiprate TDD option

The TDMA frame has a duration of 10 ms and is subdivided into 15 time slots (TS) of 2560*T_c duration each. A time slot corresponds to 2560 chips. The physical content of the time slots are the bursts of corresponding length as described in subclause 5.2.2.

Each 10 ms frame consists of 15 time slots, each allocated to either the uplink or the downlink (figure 2). With such a flexibility, the TDD mode can be adapted to different environments and deployment scenarios. In any configuration at least one time slot has to be allocated for the downlink and at least one time slot has to be allocated for the uplink.

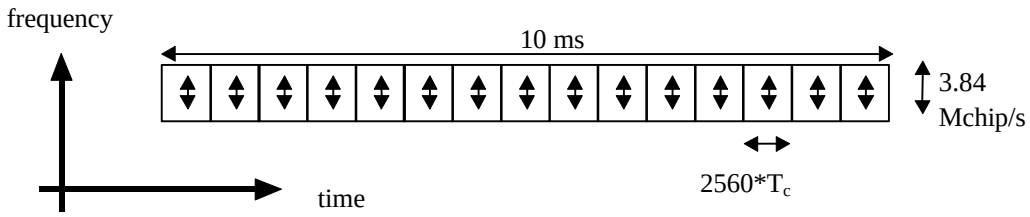
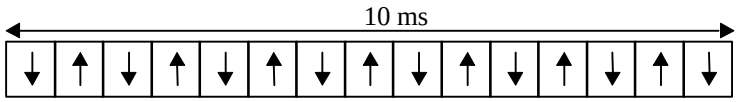
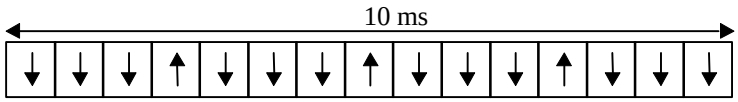


Figure ~~23~~ : The TDD frame structure for the high chiprate TDD option

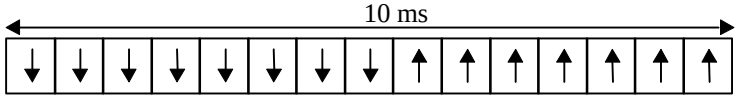
Examples for multiple and single switching point configurations as well as for symmetric and asymmetric UL/DL allocations are given in figure ~~34~~.



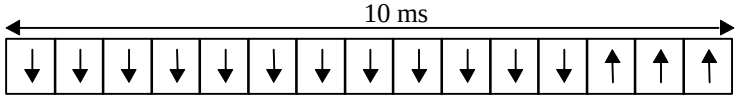
Multiple-switching-point configuration (symmetric DL/UL allocation)



Multiple-switching-point configuration (asymmetric DL/UL allocation)



Single-switching-point configuration (symmetric DL/UL allocation)



Single-switching-point configuration (asymmetric DL/UL allocation)

~~Figure 3~~Figure 4: TDD frame structure examples

5.1.2 Frame structure for the low chiprate TDD option

The TDMA frame has a duration of 10 ms and is divided into 2 sub-frames of 5ms. The frame structure for each sub-frame in the 10ms frame length is the same.

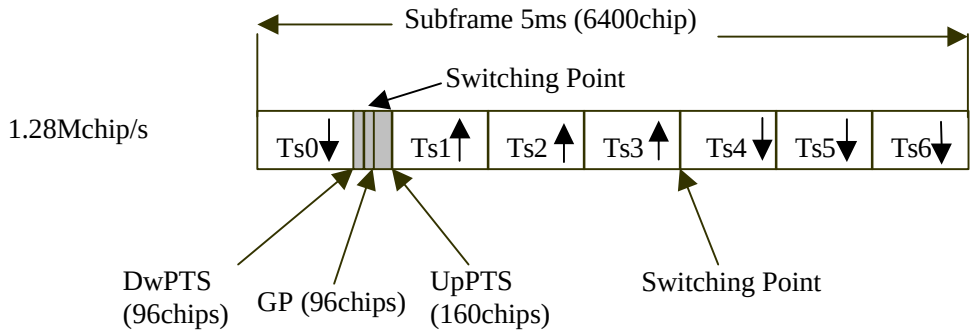


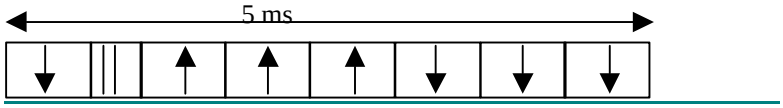
Figure 5 Structure of the sub-frame for low chip rate option

Tsn (n from 0 to 6): the nth normal time slot, 864 chips duration;
DwPTS: downlink pilot time slot, 96 chips duration;
UpPTS: uplink pilot time slot, 160 chips duration;
GP: main guard period for TDD operation, 96 chips duration;

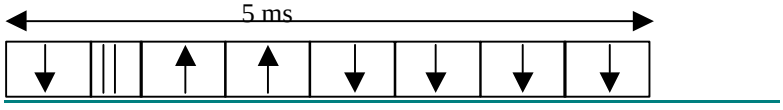
In Figure 5, the total number of normal traffic time slot for uplink and downlink is 7, and the length for each normal time slot is 864 chips duration. Among the 7 normal traffic time slot, Ts0 is always allocated as downlink while Ts1 is always allocated as uplink. The time slots for the uplink and the downlink are separated by a switching point. Between the downlink time slots and uplink time slots, the special period is the switching point to separate the uplink and downlink. In each sub-frame of 5ms for low chip rate option, there are two switching points (uplink to downlink and vice versa).

Using the above frame structure, the low chip rate TDD option can operate on both symmetric and asymmetric mode by properly configuring the number of downlink and uplink time slots. In any configuration at least one time slot (TS0) has to be allocated for the downlink and at least one time slot has to be allocated for the uplink (TS1).

Examples for symmetric and asymmetric UL/DL allocations are given in figure 6.



symmetric DL/UL allocation



asymmetric DL/UL allocation

Figure 6: low chip rate TDD sub-frame structure examples