TSG-RAN Working Group 1 meeting #14 ***TSGR1#14(00)0903***
Oulu, FINLAND, July 4 - July 7, 2000

Agenda Item:

Source: **SK Telecom**

Title: **Uplink Synchronous Transmission Scheme (USTS)**

Document for: **Discussion**

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1. Introduction

Uplink Synchronous Transmission Scheme (USTS) is an alternative technology applicable for low mobility terminals, especially in indoor and WLL-like environments. USTS can reduce uplink intra-cell interference by means of making a cell receive orthogonalized signals from UEs. And accordingly, USTS is expected to yield better performance. This feature is intended to support uplink synchronous transmission with low overhead, good capacity characteristics, and minimal impact on hardware and software resources at the UE and in the UTRAN [1-10].

USTS was proposed to WG1 and once included in Release 99. However, it is postponed to Release 2000 and it is now one of study items mainly because of missing support from other WGs about the impact on higher layers, e.g.,RRC, Iu, Iur, and Iub interfaces.

2. Study Issues

To include the support for USTS, the following issues need to be discussed [1-10]:

1. Transmission time control of each UE to orthogonalize receiving signals from UEs.
   - Initial synchronisation
   - Tracking process : closed loop timing control by using Time Alignment Bit (TAB)
2. Code usage to discriminate physical channels and cells for USTS mode.
   - Scrambling code generation to align a common scrambling code of different UEs
   - Channelisation code allocation to maximise the number of supportable users with one scrambling code

3 Uplink Synchronous Transmission Scheme (USTS)

3.1 General

To orthogonalize receiving signals from UEs,

- The network may allocate the same scrambling code to more than one UE. In case of USTS, the long scrambling code described in section 4.3.2.2. of TS 25.213 is used. However, this long scrambling code is not UE specific, but cell specific. In order to generate the cell specific long scrambling code, the initial loading value of PN generator is determined by the network. Scrambling code needs to be aligned to guarantee orthogonality among channels. The spreading and modulation scheme for USTS is same as section 4 of TS 25.213. Additional scrambling codes can be assigned to prevent channelisation code shortage problem.

- Basically the channelisation code allocation for USTS is very similar to that for downlink because the same OVSF code is used for both cases. However, a special code allocation scheme is required for USTS due to the following facts:

  - A whole set of OVSF code are shared by all UEs in a cell.
  - At least two codes should be needed to each UE for DPCCH and DPDCH.

Therefore, different channelization codes are allocated to all dedicated physical channels across all UEs in a cell and the spreading factor and node number of channelization code are delivered from network to each UE.

- The signal transmission time of each UE is adjusted.

3.2. Transmission time control

In a USTS mode, time alignment is required to preserve orthogonality between channelisation codes from different UEs and also to properly despread the cell-specific long scrambling code. The transmission time control is carried out by two steps. The first step is Initial synchronization and the second is tracking.

1) Initial synchronization: Adjust transmission time through the initial timing control information given by higher layer

2) Tracking process (Closed Loop Timing control): Adjust the transmission time through the Time Alignment Bit (TAB) over DPCCH.

First, let's make clear the definition of the reference time. The reference time (T_{ref}) is mainly dependent of the round trip propagation delay (RTPD) of first significant path, where RTPD is a function of the distance between Node B and UE, and the first significant path variation due to fading as well. The cell size is the main design parameter for T_{ref}, however, it is up to network operators to determine the value of T_{ref}. One simple way is to set T_{ref} to the average value of the RTPD.

Figures 3.1 and 3.2 explain the measurement of RTPD and the timing control, respectively, where the timing counter increases by one every (1/oversamples) chip interval. In both figures, Node B and UE have their local timing and the timing of UE is lagging $T_{p,d}$ behind the timing of Node B, where $T_{p,d}$ is the propagation time in downlink. In Figure 3.1, UE can start to transmit RACH message at the beginning of any access slot. After measuring $T_{measure}$ at Node B, we can calculate RTPD as

$$RTPD = T_{p,d} + T_{p,u} = T_{measure} \mod (5120 * \text{oversamples}), \tag{3.1}$$

where $T_{p,d}$ and $T_{p,u}$ are the propagation delays in downlink and uplink, respectively. The size of one access slot is 5120 chips. And hence the initial synchronization time is obtained by

$$T_{INIT\_SYNC} = T_{ref} - RTPD. \tag{3.2}$$

In Figure 3.2, before adjustment, DPCH message is expected to arrive at point A, where $\tau_{DPCH,n}$ is a multiple of 256 chips offset and T_0 is constant. After adjustment according to T_{INIT_SYNC}, the arrival at Node B is scheduled to occur at point B, $\tau_{DPCH,n} + T_0 + T_{ref}$ later from the beginning of each frame. There may be variation around point B due to movement of UE and this can be overcome by Tracking process using TAB commands. And accordingly, it keeps the uplink DPCCH/DPDCH frame arrive at Node B at the same point of each frame which is determined during Initial synchronisation process.

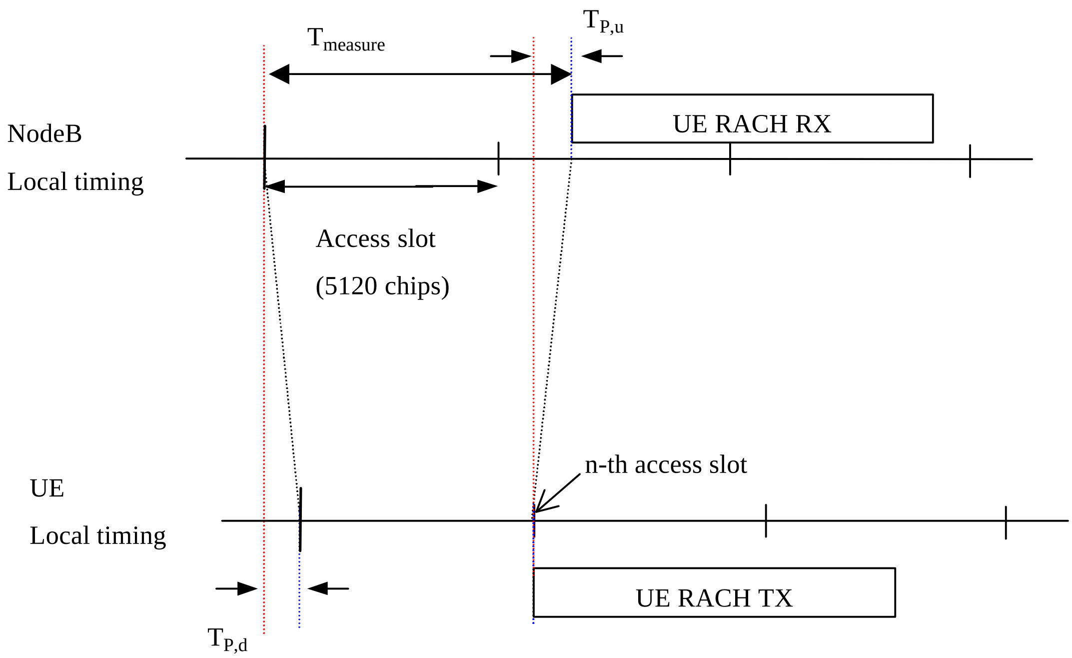

Figure 3.1 Measurement of RTPD

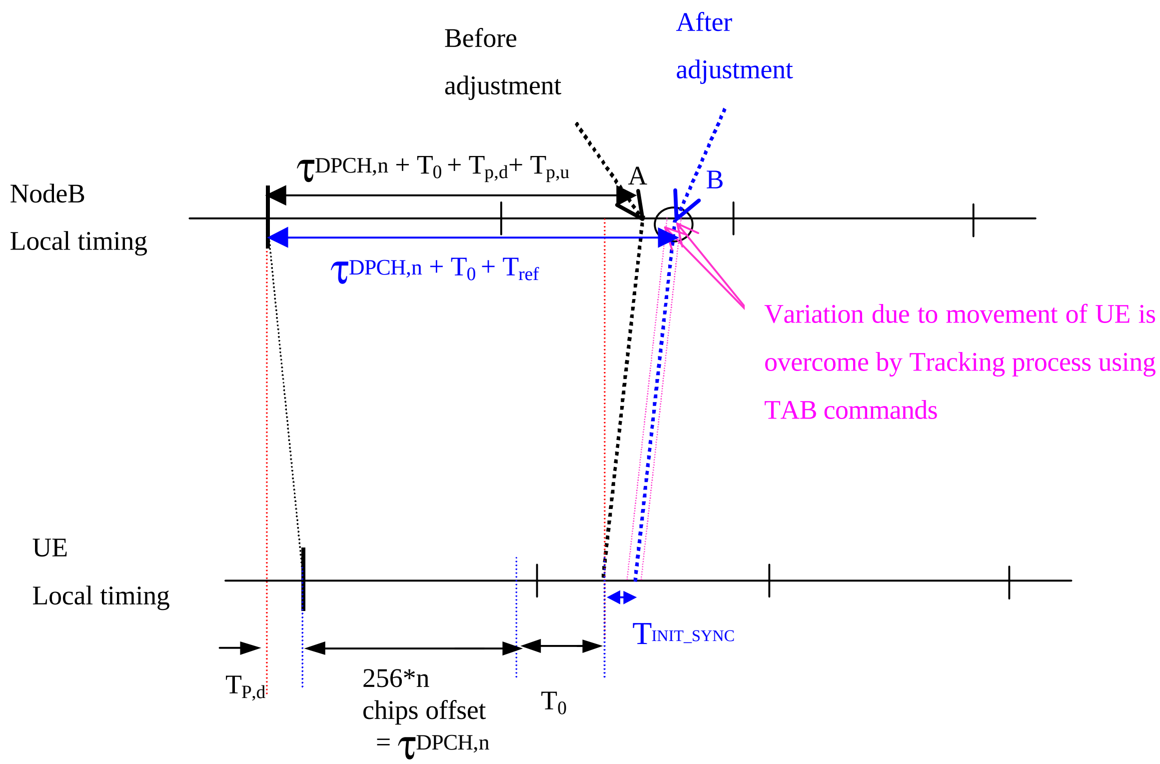

Figure 3.2 Initial synchronisation and Tracking for DPDCH/DPCCH

3.2.1 Initial synchronisation

- UTRAN measures the RTPD and set T_{INIT_SYNC} to compensate the difference between the measured RTPD and T_{ref} .

- UE adjust its transmission time according to T_{INIT_SYNC} delivered from UTRAN.

3.2.2 Tracking process

This is very like closed loop power control

- Node B compares the desired receiving time with received signal timing from UE every 20msec.

- The desired receiving time comes to T_0+T_{ref}, offset by $\tau_{DPCH,n}$ from the beginning of each DPCCH/DPDCH frame.

- When the received timing is earlier than the desired receiving time at a Node B, Time Alignment Bit (TAB) = "0". When this is later than the desired receiving time, TAB = "1".

- TAB replaces the TPC bit in slot #14 in frames with CFN mod 2 = 0.

- At the UE, hard decision on the TAB shall be performed. When it is judged as "0", the transmission time shall be delayed by δT, whereas if it is judged as "1", the transmission time shall be advanced by δT. δT is the timing control step size, whose minimum value depends on the oversampling rate.

3.3 Scrambling code alignment

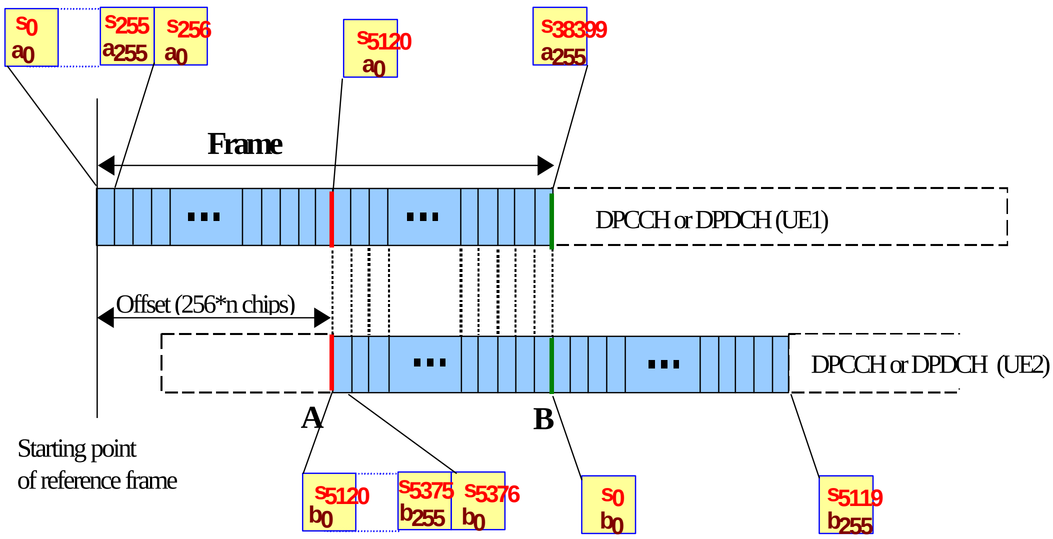

Figure 3.3 Timing at Node B and usage of scrambling and orthogonal codes in case of two UEs (a,b : orthogonal codes, s : scrambling code, SF = 256)

Figure 3.3 shows a simple example with two UEs. Different UE uses different orthogonal codes to discriminate UE (exactly speaking, discriminate channel) and the UEs in the same cell use a same scrambling code (cell-specific not UE-specific for USTS mode). Therefore, orthogonal codes repeat every 256 chips when SF = 256 but a scrambling code repeats every 10 msec (38400 chips). To obtain the orthogonality property in USTS mode, the scrambling code has to be aligned at chip level as described in the above Figure. Accordingly, all UEs are modulated with a same scrambling chip value if they are at the same time point.

- Reference frame : frame with offset = 0
- Code generators are reset not at their frame starting points but at the starting point of the reference frame
- Offsets are needed at the initial stage of each scrambling code generation

References

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