**3GPP TSG RAN WG1 #113** **R1-230xxxx**

**Incheon, Korea, May 22nd – 26th, 2023**

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| *CR-Form-v12.2* |
| **DRAFT CHANGE REQUEST** |
|  |
|  | **38.213** | **CR** |  | **rev** |  | **Current version:** | **17.5.0** |  |
|  |
| *For* [***HELP***](http://www.3gpp.org/3G_Specs/CRs.htm#_blank)*on using this form: comprehensive instructions can be found at* [*http://www.3gpp.org/Change-Requests*](http://www.3gpp.org/Change-Requests)*.* |
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| ***Proposed change affects:*** | UICC apps |  | ME |  | Radio Access Network |  | Core Network |  |

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|  |
| ***Title:***  | Introduction of NR support for dedicated spectrum less than 5MHz for FR1 |
|  |  |
| ***Source to WG:*** | Samsung |
| ***Source to TSG:*** |  |
|  |  |
| ***Work item code:*** | NR\_ FR1\_lessthan\_5MHz\_BW-Core |  | ***Date:*** | 2023-06-04 |
|  |  |  |  |  |
| ***Category:*** | B |  | ***Release:*** | Rel-18 |
|  | *Use one of the following categories:****F*** *(correction)****A*** *(mirror corresponding to a change in an earlier release)****B*** *(addition of feature),* ***C*** *(functional modification of feature)****D*** *(editorial modification)*Detailed explanations of the above categories canbe found in 3GPP [TR 21.900](http://www.3gpp.org/ftp/Specs/html-info/21900.htm). | *Use one of the following releases:Rel-8 (Release 8)Rel-9 (Release 9)Rel-10 (Release 10)Rel-11 (Release 11)…Rel-16 (Release 16)Rel-17 (Release 17)Rel-18 (Release 18)Rel-19 (Release 19)* |
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| ***Reason for change:*** | Introduction of NR support for dedicated spectrum less than 5MHz for FR1. |
|  |  |
| ***Summary of change:*** |  Introduce NR support for dedicated spectrum less than 5MHz for FR1.  |
|  |  |
| ***Consequences if not approved:*** | No NR support for dedicated spectrum less than 5MHz for FR1. |
|  |  |
| ***Clauses affected:*** | 13  |
|  |  |
|  | **Y** | **N** |  |  |
| ***Other specs*** |  |  |  Other core specifications  | TS 38.211 |
| ***affected:*** |  |  |  Test specifications | TS/TR ... CR ...  |
| ***(show related CRs)*** |  |  |  O&M Specifications | TS/TR ... CR ...  |
|  |  |
| ***Other comments:*** |  |
|  |  |
| ***This CR's revision history:*** |  |

\*\*\* Unchanged parts are omitted \*\*\*

# 13 UE procedure for monitoring Type0-PDCCH CSS sets

If during cell search a UE determines from *MIB* that a CORESET for Type0-PDCCH CSS set is present, as described in clause 4.1, the UE determines a number of consecutive resource blocks and a number of consecutive symbols for the CORESET of the Type0-PDCCH CSS set from *controlResourceSetZero* in *pdcch-ConfigSIB1*, as described in Tables 13-0 through 13-10, for operation without shared spectrum channel access in FR1 and FR2-1, or as described in Tables 13-1A and 13-4A for operation with shared spectrum channel access in FR1, or as described in Table 13-10A for FR2-2, and determines PDCCH monitoring occasions from *searchSpaceZero* in *pdcch-ConfigSIB1*, included in *MIB*, as described in Tables 13-11 through 13-15A. and are the SFN and slot index within a frame of the CORESET based on SCS of the CORESET and and are the SFN and slot index based on SCS of the CORESET, respectively, where the SS/PBCH block with index overlaps in time with system frame and slot . The symbols of the CORESET associated with *pdcch-ConfigSIB1* in *MIB* or with *searchSpaceSIB1* in *PDCCH-ConfigCommon* have normal cyclic prefix.

For operation with shared spectrum channel access in FR2-2 and for operation without shared spectrum channel access, a UE assumes that the offset in Tables 13-0 through 13-10A is defined with respect to the SCS of the CORESET for Type0-PDCCH CSS set from the smallest RB index of the CORESET for Type0-PDCCH CSS set to the smallest RB index of the common RB overlapping with the first RB of the corresponding SS/PBCH block after truncation, if any [4, TS 38.211]. The SCS of the CORESET for Type0-PDCCH CSS set is provided by *subCarrierSpacingCommon* for FR1 and FR2-1 and same as the SCS of the corresponding SS/PBCH block for FR2-2. In Tables 13-7, 13-8, and 13-10, is defined in [4, TS 38.211].

For operation with shared spectrum channel access in FR1, a UE determines an offset from a smallest RB index of the CORESET for Type0-PDCCH CSS set to a smallest RB index of the common RB overlapping with a first RB of the corresponding SS/PBCH block

- according to the offset in Table 13-1A or Table 13-4A, if the frequency position of the SS/PBCH block corresponds to the GSCN of a synchronization raster entry as defined in [8-1, TS 38.101-1], and

- according to a sum of a first offset and a second offset if the frequency position of the SS/PBCH block is provided by *ssbFrequency* in a measurement configuration associated with a reporting configuration providing *reportCGI* and does not correspond to the GSCN of a synchronization raster entry as defined in [8-1, TS 38.101-1], where

- the first offset is provided in Table 13-1A or Table 13-4A, and

- the second offset is determined as the offset from a smallest RB index of the common RB overlapping with the first RB of the SS/PBCH block indicated in the measurement configuration to a smallest RB index of the common RB overlapping with the first RB of a SS/PBCH block hypothetically located at the GSCN of a synchronization raster entry, where the single synchronization raster entry is located in the same channel as the SS/PBCH block used for the shared spectrum channel access procedure, as described in [15, TS 37.213]

where the offsets are defined with respect to the SCS of the CORESET for Type0-PDCCH CSS set that is same as the SCS of the corresponding SS/PBCH block.

For operation without shared spectrum channel access and for the SS/PBCH block and CORESET multiplexing pattern 1, a UE monitors PDCCH in the Type0-PDCCH CSS set over two slots. For SS/PBCH block with index , the UE determines an index of slot as that is in a frame with system frame number (SFN) satisfying if , or in a frame with SFN satisfying if where based on the SCS for PDCCH receptions in the CORESET [4, TS 38.211].

- For and for a SS/PBCH block index , the two slots including the associated Type0-PDCCH monitoring occasions are slots and . , , and the index of the first symbol of the CORESET in slots and are provided by Table 13-11 and Table 13-12.

- For and for a SS/PBCH block index , the two slots including the associated Type0-PDCCH monitoring occasions are slots and . , , and the index of the first symbol of the CORESET in slots and are provided by Table 13-12A, where .

- For and for a SS/PBCH block index , the two slots including the associated Type0-PDCCH monitoring occasions are slots and . , , and the index of the first symbol of the CORESET in slots and are provided by Table 13-12A, where .

For operation with shared spectrum channel access and for the SS/PBCH block and CORESET multiplexing pattern 1, a UE monitors PDCCH in the Type0-PDCCH CSS set over slots that include Type0-PDCCH monitoring occasions associated with SS/PBCH blocks that are quasi co-located with the SS/PBCH block that provides a CORESET for Type0-PDCCH CSS set with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable [6, TS 38.214]. For a candidate SS/PBCH block index , where , two slots include the associated Type0-PDCCH monitoring occasions. The UE determines an index of slot as that is in a frame with system frame number (SFN) satisfying if , or in a frame with SFN satisfying if where based on the SCS for PDCCH receptions in the CORESET [4, TS 38.211].

- For and for a candidate SS/PBCH block index , the two slots including the associated Type0-PDCCH monitoring occasions are slots and . , , and the index of the first symbol of the CORESET in slots and are provided by Table 13-11. The UE does not expect to be configured with , or with , when .

- For and for a candidate SS/PBCH block index , the two slots including the associated Type0-PDCCH monitoring occasions are slots and . , , and the index of the first symbol of the CORESET in slots and are provided by Table 13-12.

- For and for a candidate SS/PBCH block index , the two slots including the associated Type0-PDCCH monitoring occasions are slots and . , , and the index of the first symbol of the CORESET in slots and are provided by Table 13-12A, where .

- For and for a candidate SS/PBCH block index , the two slots including the associated Type0-PDCCH monitoring occasions are slots and . , , and the index of the first symbol of the CORESET in slots and are provided by Table 13-12A, where .

For operation without shared spectrum channel access and for the SS/PBCH block and CORESET multiplexing patterns 2 and 3, a UE monitors PDCCH in the Type0-PDCCH CSS set over one slot with Type0-PDCCH CSS set periodicity equal to the periodicity of SS/PBCH block. For a SS/PBCH block with index , the UE determines the slot index and based on parameters provided by Tables 13-13 through 13-15A.

For operation with shared spectrum channel access and for SS/PBCH block and CORESET multiplexing pattern 3, a UE monitors PDCCH in the Type0-PDCCH CSS set over slots that include Type0-PDCCH monitoring occasions associated with SS/PBCH blocks that are quasi co-located with the SS/PBCH block that provides a CORESET for Type0-PDCCH CSS set with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable. For a candidate SS/PBCH block index , where , the periodicity of the slot including the associated Type0-PDCCH monitoring occasion is same as the periodicity of the candidate SS/PBCH block, and the UE determines the slot index and based on parameters provided by Tables 13-15 and 13-15A, where is replaced by for operation with shared spectrum channel access in FR2-2.

For the SS/PBCH block and CORESET multiplexing patterns 2 and 3, if the active DL BWP is the initial DL BWP, the UE is expected to be able to perform radio link monitoring, as described in clause 5, and measurements for radio resource management [10, TS 38.133] using a SS/PBCH block that provides a CORESET for Type0-PDCCH CSS set.

Table 13-0: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {15, 15} kHz for frequency bands with minimum channel bandwidth 3 MHz and channel bandwidth 3 MHz. Non-interleaved CCE-to-REG mapping applies for entries 4 and 5.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Index | SS/PBCH block and CORESET multiplexing pattern  | Number of RBs  | Number of Symbols  | Offset (RBs)  |
| 0 | 1  | 12  | 2  | 0  |
| 1 | 1  | 12  | 3  | 0  |
| 2 | 1  | 24  | 2  | 0  |
| 3 | 1  | 24  | 3  | 0  |
| 4 | 1  | 24  | 2  | 0  |
| 5 | 1  | 24  | 3  | 0  |
| 6 | Reserved |
| 7 | Reserved |
| 8 | Reserved  |
| 9 | Reserved  |
| 10 | Reserved  |
| 11 | Reserved  |
| 12 | Reserved |
| 13 | Reserved  |
| 14 | Reserved |
| 15 | Reserved |

Table 13-1: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {15, 15} kHz for frequency bands with minimum channel bandwidth 5 MHz or 10 MHz or with minimum channel bandwidth 3 MHz and channel bandwidth larger than 3 MHz

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Index | SS/PBCH block and CORESET multiplexing pattern  | Number of RBs  | Number of Symbols  | Offset (RBs)  |
| 0 | 1  | 24  | 2  | 0  |
| 1 | 1  | 24  | 2  | 2  |
| 2 | 1  | 24  | 2  | 4  |
| 3 | 1  | 24  | 3  | 0  |
| 4 | 1  | 24  | 3  | 2  |
| 5 | 1  | 24  | 3  | 4  |
| 6 | 1  | 48  | 1  | 12  |
| 7 | 1  | 48  | 1  | 16  |
| 8 | 1  | 48  | 2  | 12  |
| 9 | 1  | 48  | 2  | 16  |
| 10 | 1  | 48  | 3  | 12  |
| 11 | 1  | 48  | 3  | 16  |
| 12 | 1  | 96  | 1  | 38  |
| 13 | 1  | 96  | 2  | 38  |
| 14 | 1  | 96  | 3  | 38  |
| 15 | Reserved |

\*\*\* Unchanged parts are omitted \*\*\*