**3GPP TSG RAN WG1 Meeting #107bis-e R1-2200689**

**e-Meeting, January 17 – 25, 2022**

**Source: Moderator (Intel Corporation)**

**Title: Summary #1 of email discussion on initial access aspect of NR extension up to 71 GHz**

**Agenda item: 8.2.1**

**Document for: Discussion**

# Introduction

In this contribution, moderator summarize discussions on remaining issues related to initial access for extending NR up to 71 GHz based submitted contributions and email discussions from RAN1 #107-bis-e.

# Summary of issues

## 2.1 DBTW applicability to licensed operation

* From [1] Futurewei:
  + Support DBTW for FR2-2 licensed bands.
  + For FR2-2 licensed bands reuse the and the ssb-PositionsInBurst as defined for shared spectrum in 60 GHz.
  + Change the Draft 38.213 h00 text “For operation without shared spectrum channel access, in FR1 and FR2, and for operation with shared spectrum channel access in FR2-2” to “For operation without shared spectrum channel access, in FR1 and FR2, and for operation in FR2-2”
* From [2] Huawei/HiSilicon:
  + For UE operation with shared spectrum in FR2-2, UE assumes the default DBTW lengths of 5ms for 120kHz and 1.25 ms for 480 and 960 kHz when DBTW is not indicated.
  + UE is expected to be configured with =64 in licensed operations
  + Agree to TP#1-4
* From [4] vivo
  + DBTW should apply to all of FR2-2.
  + Agree to TP#1-2
* From [7] Samsung
  + No need to support DBTW for licensed operation in FR2-2.
    - No specification impact.
  + Agree to TP#1-3
* From [8] NTT Docomo
  + Agree to TP#1-2
* From [9] ZTE/Sanechips
  + There are two alternatives to solve inconsistencies of supporting DBTW and the indication of between RAN1’s agreements and the description of 38213\_CR0271\_(Rel-17)\_R1-2112931.
    - Alt 1: Do not support DBTW in licensed spectrum. UE can judge whether the operation is in licensed spectrum or shared spectrum before decoding MIB (may depend on sync raster design by RAN4 or implementation).
    - Alt 2: Delete the restriction “with shared spectrum channel access” for the indication of in the CR.
* From [10] Spreadtrum
  + It is general view that both LBT and no LBT is supported for SSB transmission. For DBTW, we should consider these two cases both.
  + The reserved codepoint for Q value indication can be used to distinguish the operation in licensed operation and the operation with the short control signalling in unlicensed operation.
* From [14] Ericsson
  + RAN1 to conclude that the DBTW procedure in 38.213 is not applicable to operation without shared spectrum channel access and no further spec changes are needed for that case.
* From [17] LGE
  + Agree to TP#1-5

#### TP# 1-1 for TS38.213

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| 4.1 Cell search <unchanged part omitted>  The candidate SS/PBCH blocks in a half frame are indexed in an ascending order in time from 0 to , where is determined according to SS/PBCH block patterns for Cases A through G. is a maximum number of SS/PBCH block indexes in a cell, and the maximum number of transmitted SS/PBCH blocks within a half frame is .  - For operation without shared spectrum channel access, in FR1 and FR2, and for operation ~~with shared spectrum channel access~~ in FR2-2  - For operation with shared spectrum channel access in FR1, for and 15 kHz SCS of SS/PBCH blocks and for and 30 kHz SCS of SS/PBCH blocks  <unchanged part omitted> |

#### TP# 1-2 for TS38.213 [4][8]

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| 4.1 Cell search <unchanged part omitted>  ~~For operation with shared spectrum channel access in FR2-2,~~ For operation in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  <unchanged part omitted> |

#### TP# 1-3 for TS38.213 [7]

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| 13 UE procedure for monitoring Type0-PDCCH CSS sets  ============= Unchanged Text Omitted =============  For operation without shared spectrum channel access and for operation with shared spectrum channel access in FR2-2, a UE assumes that the offset in Tables 13-1 through 13-10C is defined with respect to the SCS of the CORESET for Type0-PDCCH CSS set from the smallest RB index of the CORESET for Type0-PDCCH CSS set to the smallest RB index of the common RB overlapping with the first RB of the corresponding SS/PBCH block. The SCS of the CORESET for Type0-PDCCH CSS set is provided by *subCarrierSpacingCommon* for FR1 and FR2-1 and same as the SCS of the corresponding SS/PBCH block for FR2-2. In Tables 13-7, 13-8, and 13-10 is defined in [4, TS 38.211].  ============= Unchanged Text Omitted ===================== |

#### TP# 1-4 for TS38.213 [2]

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| 4.1 Cell search \*\*\* Unchanged text is omitted \*\*\*  Table 4.1-2: Mapping between the combination of *subCarrierSpacingCommon* and *spare* to for operation with and without shared spectrum channel access in FR2-2  \*\*\* Unchanged text is omitted \*\*\* |

#### TP# 1-5 for TS38.213 [17]

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| 4.1 Cell search \*\*\* Unchanged text is omitted \*\*\*  Table 4.1-2: Mapping between the combination of *subCarrierSpacingCommon* and *spare* to ~~for operation with shared spectrum channel access~~ in FR2-2  \*\*\* Unchanged text is omitted \*\*\* |

### Summary of Discussions

The following is a summary of company position of various aspects of DRS.

* Several companies commented that DBTW should be applicable to licensed cases for FR2-2 as well. Two companies commented that applicability of DBTW should be only for unlicensed operation.

### 1st Round Discussion

Discuss further on whether or not to allow applicability of DBTW for licensed operations

Please comment on whether DBTW should be applicable for licensed operations as well (from specification perspective). Please further comment on TP#1-6, which is the combined TP of 1-1, 1-2, 1-3, 1-4, and 1-5.

#### TP# 1-6 for TS38.213

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| 4.1 Cell search <unchanged part omitted>  ~~For operation with shared spectrum channel access in FR2-2,~~ For operation in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  The candidate SS/PBCH blocks in a half frame are indexed in an ascending order in time from 0 to , where is determined according to SS/PBCH block patterns for Cases A through G. is a maximum number of SS/PBCH block indexes in a cell, and the maximum number of transmitted SS/PBCH blocks within a half frame is .  - For operation without shared spectrum channel access, in FR1 and FR2, and for operation ~~with shared spectrum channel access~~ in FR2-2  - For operation with shared spectrum channel access in FR1, for and 15 kHz SCS of SS/PBCH blocks and for and 30 kHz SCS of SS/PBCH blocks  <unchanged part omitted>  Table 4.1-2: Mapping between the combination of *subCarrierSpacingCommon* and *spare* to ~~for operation with shared spectrum channel access~~ in FR2-2  <unchanged part omitted> |

#### Company Comments/Inputs

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| --- | --- |
| Company | Comments |
| Samsung | We believe these things are coupled and should be discussed together, and the following options are reasonable proposals for discussion:   * Option 1: Don’t support DBTW for licensed operation, and the definition of is not applicable for licensed operation (no need to specify its indication). For this option, no spec change is needed. * Option 2: Support DBTW for licensed operation, and the indication of for licensed operation needs to be added to TS 38.213. Further specify that for licensed operation. * Option 3: Support DBTW for licensed operation, and the indication of for licensed operation needs to be added to TS 38.213. No need to further specify that for licensed operation (but as a note in chairman note for guidance of gNB’s implementation).   We don’t think the option of defining and/or specifying for licensed operation without supporting DBTW for licensed band is one valid option, since based on current specification, is only applicable to the text that associated with unlicensed band.  Within these three options, we prefer Option 1, since the UE behavior for all the options are exactly the same, due to the fact that supporting =64 with DBTW is exactly the same as not supporting DBTW at all. Also, since there is no spec change needed in Option 1, we prefer to keep current text in the spec.  Regarding TP#1-6, we don’t support the changes other than the second one, which is not related to above discussion, but some imperfectness of the wording in the spec. We believe the following reorder of the sentence is more clear (just some rewording, no change to the technical points):  - For operation without shared spectrum channel access~~,~~  in FR1 and FR2, and for operation with shared spectrum channel access in FR2-2, . |

### <Summary of 1st Round Discussion>

*[Summary to be provided by moderator after discussion]*

## 2.2 Q=64 expectation in licensed operation

* From [1] Futurewei:
  + For FR2-2 licensed bands reuse the and the ssb-PositionsInBurst as defined for shared spectrum in 60 GHz.
  + For FR2-2 licensed band UE expects that , which implies that UE cannot assume a QCL-D relationship between SSB(s) with different block indices.
* From [2] Huawei/HiSilicon:
  + Regarding, agree with the following point from the “Note” in the agreement in RAN1 107-e and include it in 38.213:
  + UE is expected to be configured with =64 in licensed operations
  + Agree to TP#2-1
* From [8] NTT Docomo
  + Agree to TP#2-1

#### TP# 2-1 for TS38.213 [2][8]

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| 4.1 Cell search \*\*\* Unchanged text is omitted \*\*\*  For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  UE is expected to be configured with =64 for operation without shared spectrum in FR2-2.  \*\*\* Unchanged text is omitted \*\*\* |

#### TP# 2-2 for TS38.213 [17]

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| 4.1 Cell search \*\*\* Unchanged text is omitted \*\*\*  For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  For operation without shared spectrum channel access in FR2-2, a UE expects that is indicated as 64, where is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2.  \*\*\* Unchanged text is omitted \*\*\* |

### Summary of Discussions

The following is a summary of company position of various aspects of DRS.

* Companies commented we should capture the expected parameters for Q in licensed operation cases to the specification.

### 1st Round Discussion

Discuss further on the TP#2-1 and #2-2.

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| --- | --- |
| Company | Comments |
| Samsung | As commented in section 2.1, this discussion is only applicable when we agree to supported DBTW for licensed band. |

### <Summary of 1st Round Discussion>

*[Summary to be provided by moderator after discussion]*

## 2.3 Q parameter signaling for DRS

* From [2] Huawei/HiSilicon:
  + Support 8 as the fourth value of and the minimum DBTW length of 0.0625 to reduce the latency of initial access procedure.
  + Regarding, agree with the following point from the “Note” in the agreement in RAN1 107-e and include it in 38.213:
  + UE is expected to be configured with =64 in licensed operations
  + Agree to TP#1-1
* From [3] Interdigital
  + Support values of {8,16,32,64} for SSB blocks with all supported SCS 120kHz, 480kHz, and 960kHz in operation with shared spectrum.
* From [10] Spreadtrum
  + The reserved codepoint for Q value indication can be used to distinguish the operation in licensed operation and the operation with the short control signalling in unlicensed operation.
* From [15] Apple
  + For 480/960kHz SCS, support in addition to : {16, 32, 64}.
* From [16] Sharp
  + Use 1 MIB payload bit to partially indicate Q values of {16, 32, 64} and the full indication for Q and DBTW enabled/disabled can be complemented by SIB1. Adopt the following text proposal (TP#3-3).

#### TP# 3-1 for TS38.213 [2][3]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 4.1 Cell search \*\*\* Unchanged text is omitted \*\*\*  Table 4.1-2: Mapping between the combination of *subCarrierSpacingCommon* and *spare* to for operation with shared spectrum channel access in FR2-2   |  |  |  | | --- | --- | --- | | *subCarrierSpacingCommon* | *spare* |  | | scs15or60 | 0 | ~~16~~8 | | scs15or60 | 1 | ~~32~~16 | | scs30or120 | 0 | ~~64~~32 | | scs30or120 | 1 | ~~reserved~~64 |   \*\*\* Unchanged text is omitted \*\*\* |

#### TP# 3-2 for TS38.213 [15]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 4.1 Cell search \*\*\* Unchanged text is omitted \*\*\*  Table 4.1-2: Mapping between the combination of *subCarrierSpacingCommon* and *spare* to for operation with shared spectrum channel access in FR2-2   |  |  |  | | --- | --- | --- | | *subCarrierSpacingCommon* | *spare* |  | | scs15or60 | 0 | 16 | | scs15or60 | 1 | 32 | | scs30or120 | 0 | ~~64~~48 | | scs30or120 | 1 | ~~reserved~~64 |   \*\*\* Unchanged text is omitted \*\*\* |

#### TP# 3-3 for TS38.213 [16]

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| 4.1 Cell search \*\*\* Unchanged text is omitted \*\*\*  For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. In a case that only *subCarrierSpacingCommon* is used for indication, ‘scs15or60’ indicates and ‘scs30or120’ indicates . The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  \*\*\* Unchanged text is omitted \*\*\* |

### Summary of Discussions

The following is a summary of company views on Q parameter signaling for DRS.

* Support 8 in addition to {16,32,64}
  + Huawei/HiSilicon, Interdigital
* Support 48 in addition to {16,32,64}
  + Apple
* Superposition multiple hypothesis for Q=16/32 into a single entry
  + Sharp
* Reserved codepoint used to indicate licensed or unlicensed operation
  + Spreadtrum

### 1st Round Discussion

Discuss further on the TP#3-1, 3-2, and 3-3. Please also further comment on any changes to Q parameters values in this sub-section as well.

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| Company | Comments |
| Samsung | We don’t think changes to current specification are needed, but open to the discussion. |

### <Summary of 1st Round Discussion>

*[Summary to be provided by moderator after discussion]*

## 2.4 DBTW Length

* From [2] Huawei/HiSilicon:
  + For UE operation with shared spectrum in FR2-2, UE assumes the default DBTW lengths of 5ms for 120kHz and 1.25 ms for 480 and 960 kHz when DBTW is not indicated.
  + Support 8 as the fourth value of and the minimum DBTW length of 0.0625 to reduce the latency of initial access procedure.
* From [6] Nokia/NSB
  + For 480 and 960 kHz, confirm that supported DBTW lengths are {1.25, 1, 0.75, 0.5, 0.25, 0.125}.
* From [7] Samsung
  + Keep 5 ms as the default duration for DBTW in FR2-2, if no higher layer parameter is provided.
    - No specification impact.
* From [9] ZTE/Sanechips
  + If the DBTW length is not configured (i.e. discoveryBurstWindowLength is not provided), UE can assume the DBTW length for all supported SCSs (120/480/960 kHz) in FR2-2 is a half frame.

### Summary of Discussions

The following is a summary of company views on DBTW lengths.

* Two companies commented that default value for DBTW should be 5 msec.
* One company commented that default value for DBTW should be 5 msec for 120 kHz, 1.25 msec for 480 and 960 kHz.
* One companies commented we should confirm that 0.0625 msec should be removed. One company commented we should keep 0.0625 msec (along with Q=8) for DBTW length.

### 1st Round Discussion

Discuss further on the following proposals.

#### Proposal# 4-1

* If the DBTW length is not configured (i.e. discoveryBurstWindowLength is not provided), UE assumes the default DBTW lengths of 5ms for 120kHz and 1.25 ms for 480 and 960 kHz.

#### Proposal# 4-2

* If the DBTW length is not configured (i.e. discoveryBurstWindowLength is not provided), UE can assume the DBTW length for all supported SCSs (120/480/960 kHz) in FR2-2 is a half frame.

As for whether or not to keep 0.0625 msec, as per RAN1 agreement this depends on whether Q=8 is supported or not. This is being discussed in section 2.2, and once concluded we can prepare appropriate changes to 38.213, if needed.

#### Company Comments/Inputs

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| Company | Comments |
| Samsung | We support Proposal# 4-2, and want to add a further note that “no change in TS 38.213 is needed” (maybe this is only a conclusion for clarification).  The UE behavior of Proposal# 4-1 and Proposal# 4-2 are exactly the same, since there is no candidate SSB locations after 1.25 ms for 480 and 960 kHz SCS. |

### <Summary of 1st Round Discussion>

*[Summary to be provided by moderator after discussion]*

## 2.5 Other DRS Aspects

* From [1] Futurewei:
  + For FR2-2 licensed band UE expects that , which implies that UE cannot assume a QCL-D relationship between SSB(s) with different block indices.
* From [2] Huawei/HiSilicon:
  + Add the following note to the comment section of discoveryBurstWindowLength-r17 row in RRC parameter list: “Note: This parameter is to be included in both SIB1 and the common serving cell configuration parameters”.
  + Support adding "SSB-PositionQCL-Relation-r17" to RRC parameter list as both UE-specific and cell-specific parameter.
* From [10] Spreadtrum
  + The candidate SSB positions for 120kHz SCS follows the current spec.
* From [14] Ericsson
  + Inform RAN2 that the either the value range of the information element SSB-PositionQCL-Relation-r16 needs to be extended, or a new Rel-17 IE need to be defined to allow configuration of Q = 16, 32, or 64 in SIB2, SIB3, SIB4, MeasObjectNR, and ServingCellConfigCommon for RRM measurements when operating with shared spectrum channel access in FR2-2.

### Summary of Discussions

The following is a summary of company position of various aspects of DRS.

* Add the following note to the comment section of discoveryBurstWindowLength-r17 row in RRC parameter list: “Note: This parameter is to be included in both SIB1 and the common serving cell configuration parameters”.
* Support adding "SSB-PositionQCL-Relation-r17" to RRC parameter list as both UE-specific and cell-specific parameter.
* Inform RAN2 that the either the value range of the information element SSB-PositionQCL-Relation-r16 needs to be extended, or a new Rel-17 IE need to be defined to allow configuration of Q = 16, 32, or 64 in SIB2, SIB3, SIB4, MeasObjectNR, and ServingCellConfigCommon for RRM measurements when operating with shared spectrum channel access in FR2-2.

### 1st Round Discussion

Discuss further on the following proposals. Moderator assumes the if the proposals are agreeable, we could add the notes to the RRC parameter list.

#### Proposal# 5-1

* Add the following note to the comment section of discoveryBurstWindowLength-r17 row in RRC parameter list
  + “Note: This parameter is to be included in both SIB1 and the common serving cell configuration parameters”.

#### Proposal# 5-2

* Support adding "SSB-PositionQCL-Relation-r17" to RRC parameter list as both UE-specific and cell-specific parameter.

#### Proposal# 5-3

* Inform RAN2 (by adding notes to RRC parameter list) that the either the value range of the information element SSB-PositionQCL-Relation-r16 needs to be extended, or a new Rel-17 IE need to be defined to allow configuration of Q = 16, 32, or 64 in SIB2, SIB3, SIB4, MeasObjectNR, and ServingCellConfigCommon for RRM measurements when operating with shared spectrum channel access in FR2-2.

#### Company Comments/Inputs

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| Company | Comments |
| Samsung | We support Proposal# 5-1, 5-2, and 5-3.  After we concluded issues in 2.1, maybe it’s also good to clarify whether Proposal# 5-1, 5-2 are also restricted to unlicensed operation only. |

### <Summary of 1st Round Discussion>

*[Summary to be provided by moderator after discussion]*

## 2.6 CORESET#0 Configuration

* From [2] Huawei/HiSilicon:
  + Support the following CORESET#0 RB offsets for {SSB, CORESET#0} SCS={120, 120} kHz:
    - For CORESET#0 with 24 RBs: The same as supported values in Table 13-8 of 38.213.
    - For CORESET#0 with 48 RBs: The same as supported values in Table 13-8 of 38.213 in addition to RB offset values of [0] and [28] RBs for multiplexing pattern 1.
    - For CORESET#0 with 96 RBs: RB offsets of [0] and [76] RBs for multiplexing pattern 1.
  + Support the following CORESET#0 RB offsets values for {SSB, CORESET#0} SCS={480, 480} kHz and {960, 960} kHz:
    - For CORESET#0 with 24 RBs: The same as supported values in Table 13-8 of 38.213.
    - For CORESET#0 with 48 RBs: The same as supported values in Table 13-8 of 38.213 in addition to RB offset values of [0] and [28] RBs for multiplexing pattern 1.
    - For CORESET#0 with 96 RBs: RB offsets of [0] and [76] RBs for multiplexing pattern 1.
* From [3] Interdigital
  + Support multiplexing pattern 3 for SSB-CORESERT#0, only for ={24,48} and only with {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz and {480, 480} kHz.
  + Do not support 96RBs for CORESERT#0 with {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz.
  + Do not support additional RB offsets for the {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, and use the same supported values in Table 13-8 of TS 38.213.
* From [4] vivo
  + Do not support Multiplexing pattern 3 for SCS 480 kHz and 960 kHz.
  + Support 96 RB for SCS 120kHz and 480 kHz and do not support 96 RB for SCS 960kHz.
  + For ‘controlResourceSetZero’ configuration for {120K, 120K} pair in FR2-2:
    - Support 2 RB offset values for multiplexing pattern 1 with 24 PRB cases: [0] and [4]
    - Support 3 RB offset values for multiplexing pattern 1 with 48 PRB cases: [0], [14], and [28]
    - Support 2 RB offset values for multiplexing pattern 1 with 96 PRB cases: [0], and [76]
    - Support following two RB offset values for multiplexing pattern 3: -20 if kssb=0, -21 if kssb>0
  + For ‘controlResourceSetZero’ configuration for {480K, 480K} pair in FR2-2:
    - Support 2 RB offset values for multiplexing pattern 1 with 24 PRB cases: [0] and [4]
    - Support 3 RB offset values for multiplexing pattern 1 with 48 PRB cases: [0], [14], and [28]
    - Support 2 RB offset values for multiplexing pattern 1 with 96 PRB cases: [0], and [76]
  + For ‘controlResourceSetZero’ configuration for {960K, 960K} pair in FR2-2:
    - Support 2 RB offset values for multiplexing pattern 1 with 24 PRB cases: [0] and [4]
    - Support 3 RB offset values for multiplexing pattern 1 with 48 PRB cases: [0], [14], and [28]
* From [5] CATT
  + For CORESET#0 configuration, reusing of legacy RB offset values are preferred.
  + If multiplexing pattern 3 for 480 kHz and 960 kHz is supported, the first symbols index of Type0-PDCCH monitoring occasions can be 2 for even SSB index and can be 9 for odd SSB index.
* From [6] Nokia/NSB
  + 120 kHz SCS
    - 24 PRB CORESET#0: RB offsets 0, 4
    - 48 PRB CORESET#0: RB offsets 0, 14, 28
    - 96 PRB CORESET#0: RB offsets 0, 76
  + 480 kHz SCS
    - 24 PRB CORESET#0: RB offsets 0, 4
    - 48 PRB CORESET#0: RB offsets 0, 14, 28
    - 96 PRB CORESET#0: RB offsets 0, 36, 40, 76
  + 960 kHz SCS
    - 24 PRB CORESET#0: RB offsets 0, 4
    - 48 PRB CORESET#0: RB offsets 0, 14, 28
    - 96 PRB CORESET#0: RB offsets FFS
  + For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, support multiplex pattern 3 with 24 PRB and 2 symbol duration, and multiplexing pattern 3 with 48 PRB and 2 symbol duration.
  + At least for 480 kHz, support multiplexing pattern 1 with 96 PRB with 2-symbol duration, with four RB offsets.
  + Confirm the support of CORESET#0 with = {96} for 120kHz and 480kHz sub-carrier spacing.
  + The Type0-PDCCH CSS set for multiplexing pattern 3 for 480kHz and 960kHz is defined as follows:

|  |  |  |
| --- | --- | --- |
| **Index** | **PDCCH monitoring occasions (SFN and slot number)** | **First symbol index**  **(*k* = 0, 1, … 31)** |
| 0 |  | 2, 9 in |
| 1 ~ 15 | Reserved | |

* From [7] Samsung
  + For 120 kHz SCS:
    - Support one RB offset for 24 RB CORESET#0 bandwidth in Pattern 1;
    - Support two RB offsets for 48 RB CORESET#0 bandwidth in Pattern 1;
    - Support one RB offset for 96 RB CORESET#0 bandwidth in Pattern 1;
    - Support same RB offsets as Rel-15 FR 2-1 in Pattern 3;
    - Adopt TP#3-2 for TS 38.213.
  + For 480 kHz and 960 kHz SCS:
    - Support the same CORESET#0 configuration table;
    - Support multiplexing pattern 3 with same RB offsets as in Rel-15 FR2-1;
    - Support two RB offsets for 24 RB CORESET#0 bandwidth in Pattern 1;
    - Support three RB offsets for 48 RB CORESET#0 bandwidth in Pattern 1;
    - Support two RB offsets for 48 RB CORESET#0 bandwidth in Pattern 1;
    - Support 1 symbol for CORESET#0 when the bandwidth of CORESET#0 is 96;
    - Adopt TP#3-3 for TS 38.213.
* From [11] OPPO
  + Support RB offset values to configure the start or end RB of the SSB pattern aligned with the start or end RB of the CORESET#0 for 24 PRB configuration.
  + Support RB offset values to configure the SSB pattern located in the central RBs of the CORESET#0 resource for 48 PRB and 96 PRB configuration.
  + Whether to support additional RB offset values should be based on RAN4 channelization design outcome.
  + Whether to support multiplexing pattern 1 with 96 PRB and 2 symbol duration for {480, 480} kHz and {960, 960} kHz should be decided after the completion of entries for required RB offsets for 24 PRB and 48 PRB configuration.
* From [12] ETRI
  + Agree to TP#3-4
  + Removal of M=2 cases
* From [13] Intel
  + Confirm WAs on ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz.
  + Support the following RB offset values for CORESET#0 configured in MIB:
    - Multiplexing pattern 1 with 120 kHz SCS and 24 or 96 RBs: 0 RB offset
    - Multiplexing pattern 1 with 120 kHz SCS and 48 RBs: 14 RB offset
    - Multiplexing pattern 1 with 480 kHz SCS and 24, 48, or 96 RBs: 0 RB offset
    - Multiplexing pattern 1 with 960 kHz SCS and 24, 48, or 96 RBs: 0 RB offset
    - Multiplexing pattern 3 with 120, 480, or 960 kHz SCS: -20 or -21 (depending on k\_ssb) RB offset

#### TP# 6-1 for TS38.213 [4]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| <unchanged part omitted>  Table 13-10A: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 0 | | 3 | 1 | 48 | 2 | 0 | | 4 | 1 | 48 | 1 | 14 | | 5 | 1 | 48 | 2 | 14 | | 6 | 1 | 48 | 1 | 28 | | 7 | 1 | 48 | 2 | 28 | | 8 | 1 | 96 | 1 | 0 | | 9 | 1 | 96 | 2 | 0 | | 10 | 1 | 96 | 1 | 76 | | 11 | 1 | 96 | 2 | 76 | | 12 | 3 | 24 | 2 | -20 if  -21 if | | 13 | 3 | 48 | 2 | -20 if  -21 if | | 14 |  |  |  |  | | 15 |  |  |  |  |   <unchanged part omitted>  Table 13-10B: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {480, 480} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 0 | | 3 | 1 | 48 | 2 | 0 | | 4 | 1 | 48 | 1 | 14 | | 5 | 1 | 48 | 2 | 14 | | 6 | 1 | 48 | 1 | 28 | | 7 | 1 | 48 | 2 | 28 | | 8 | 1 | 96 | 1 | 0 | | 9 | 1 | 96 | 2 | 0 | | 10 | 1 | 96 | 1 | 76 | | 11 | 1 | 96 | 2 | 76 | | 12 |  |  |  |  | | 13 |  |  |  |  | | 14 |  |  |  |  | | 15 |  |  |  |  |   <unchanged part omitted>  Table 13-10C: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {960, 960} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 0 | | 3 | 1 | 48 | 2 | 0 | | 4 | 1 | 48 | 1 | 14 | | 5 | 1 | 48 | 2 | 14 | | 6 | 1 | 48 | 1 | 28 | | 7 | 1 | 48 | 2 | 28 | | 8 |  |  |  |  | | 9 |  |  |  |  | | 10 |  |  |  |  | | 11 |  |  |  |  | | 12 |  |  |  |  | | 13 |  |  |  |  | | 14 |  |  |  |  | | 15 |  |  |  |  |   <unchanged part omitted> |

#### TP# 6-2 for TS38.213 [7]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ============= Unchanged Text Omitted ================  Table 13-10A: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 2 | | 1 | 1 | 48 | 1 | 0 | | 2 | 1 | 48 | 1 | 28 | | 3 | 1 | 48 | 2 | 0 | | 4 | 1 | 48 | 2 | 28 | | 5 | 1 | 96 | 1 | 38 | | 6 | 1 | 96 | 2 | 38 | | 7 | 3 | 24 | 2 | -20 if ,  -21 if | | 8 | 3 | 24 | 2 | 24 | | 9 | 3 | 48 | 2 | -20 if ,  -21 if | | 10 | 3 | 48 | 2 | 48 | | 11 | Reserved | | | | | 12 | Reserved | | | | | 13 | Reserved | | | | | 14 | Reserved | | | | | 15 | Reserved | | | |   =============== Unchanged Text Omitted =================== |

#### TP# 6-3 for TS38.213 [7]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ========== Unchanged Text Omitted ============  Table 13-10B: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {480, 480} kHz or {960, 960} for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 0 | | 3 | 1 | 48 | 1 | 14 | | 4 | 1 | 48 | 1 | 28 | | 5 | 1 | 48 | 2 | 0 | | 6 | 1 | 48 | 2 | 14 | | 7 | 1 | 48 | 2 | 28 | | 8 | 1 | 96 | 1 | 0 | | 9 | 1 | 96 | 1 | 76 | | 10 | 1 | 96 | 2 | 0 | | 11 | 1 | 96 | 2 | 76 | | 12 | 3 | 24 | 2 | -20 if ,  -21 if | | 13 | 3 | 24 | 2 | 24 | | 14 | 3 | 48 | 2 | -20 if ,  -21 if | | 15 | 3 | 48 | 2 | 48 |   ================Unchanged Text Omitted =================== |

#### TP# 6-4 for TS38.213 [7][12]

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| =========== Unchanged Text Omitted ===========  Table 13-15A: PDCCH monitoring occasions for Type0-PDCCH CSS set - SS/PBCH block and CORESET multiplexing pattern 3 and {SS/PBCH block, PDCCH} SCS {480, 480} kHz or {960, 960} kHz   |  |  |  | | --- | --- | --- | | Index | PDCCH monitoring occasions (SFN and slot number) | **First symbol index**  **( = 0, 1, …, 31)** | | 0 |  | 2, 9 in  , |   ============ Unchanged Text Omitted ============ |

#### TP# 6-5 for TS38.213 [11]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Table 13-10A: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz for FR2-2**   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **Index** | **SS/PBCH block and CORESET multiplexing pattern** | **Number of RBs** | **Number of Symbols** | **Offset (RBs)** | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 48 | 1 | 14 | | 2 | 1 | 48 | 2 | 14 | | 3 | 1 | 96 | 1 | 38 | | 4 | 1 | 96 | 2 | 38 | | 5 | 3 | 24 | 2 | 24 | | 6 | 3 | 48 | 2 | 48 | | 7 | 1 | 24 | 2 | 4 | | 8 | 1 | 24 | 2 | [RAN4 outcome] | | 9 | 1 | 48 | 1 | [RAN4 outcome] | | 10 | 1 | 48 | 2 | [RAN4 outcome] | | 11 | 1 | 96 | 1 | [RAN4 outcome] | | 12 | 1 | 96 | 2 | [RAN4 outcome] | | 13 | 3 | 24 | 2 | -20 if kSSB = 0;  -21 if kSSB > 0 | | 14 | 3 | 48 | 2 | -20 if kSSB = 0;  -21 if kSSB > 0 | | 15 |  |  |  |  |   **Table 13-10B: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {480, 480} kHz for FR2-2**   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **Index** | **SS/PBCH block and CORESET multiplexing pattern** | **Number of RBs** | **Number of Symbols** | **Offset (RBs)** | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 48 | 1 | 14 | | 2 | 1 | 48 | 2 | 14 | | 3 | [1] | [96] | [2] | [38] | | 4 | 3 | 24 | 2 | 24 | | 5 | 3 | 48 | 2 | 48 | | 6 | 1 | 24 | 2 | 4 | | 7 | 1 | 24 | 2 | [RAN4 outcome] | | 8 | 1 | 48 | 1 | [RAN4 outcome] | | 9 | 1 | 48 | 2 | [RAN4 outcome] | | 10 | [1] | [96] | [2] | [RAN4 outcome] | | 11 | 3 | 24 | 2 | -20 if kSSB = 0;  -21 if kSSB > 0 | | 12 | 3 | 48 | 2 | -20 if kSSB = 0;  -21 if kSSB > 0 | | 13 |  |  |  |  | | 14 |  |  |  |  | | 15 |  |  |  |  |   **Table 13-10C: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {960, 960} kHz for FR2-2**   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **Index** | **SS/PBCH block and CORESET multiplexing pattern** | **Number of RBs** | **Number of Symbols** | **Offset (RBs)** | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 48 | 1 | 14 | | 2 | 1 | 48 | 2 | 14 | | 3 | [1] | [96] | [2] | [38] | | 4 | 3 | 24 | 2 | 24 | | 5 | 3 | 48 | 2 | 48 | | 6 | 1 | 24 | 2 | 4 | | 7 | 1 | 24 | 2 | [RAN4 outcome] | | 8 | 1 | 48 | 1 | [RAN4 outcome] | | 9 | 1 | 48 | 2 | [RAN4 outcome] | | 10 | [1] | [96] | [2] | [RAN4 outcome] | | 11 | 3 | 24 | 2 | -20 if kSSB = 0;  -21 if kSSB > 0 | | 12 | 3 | 48 | 2 | -20 if kSSB = 0;  -21 if kSSB > 0 | | 13 |  |  |  |  | | 14 |  |  |  |  | | 15 |  |  |  |  | |

#### TP# 6-6 for TS38.213 [13]

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Table 13-10A: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 48 | 1 | 14 | | 2 | 1 | 48 | 2 | 14 | | 3 | 1 | 96 | 1 | 0 | | 4 | 1 | 96 | 2 | 0 | | 5 | 3 | 24 | 2 | -20 if k\_ssb =0  -21 if k\_ssb >0 | | 6 | 3 | 48 | 2 | -20 if k\_ssb =0  -21 if k\_ssb >0 | | 7 |  |  |  |  | | 8 |  |  |  |  | | 9 |  |  |  |  | | 10 |  |  |  |  | | 11 |  |  |  |  | | 12 |  |  |  |  | | 13 |  |  |  |  | | 14 |  |  |  |  | | 15 |  |  |  |  |   Table 13-10B: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {480, 480} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 48 | 1 | 0 | | 2 | 1 | 48 | 2 | 0 | | 3 | 1 | 96 | 2 | 0 | | 4 | 3 | 24 | 2 | -20 if k\_ssb =0  -21 if k\_ssb >0 | | 5 | 3 | 48 | 2 | -20 if k\_ssb =0  -21 if k\_ssb >0 | | 6 |  |  |  |  | | 7 |  |  |  |  | | 8 |  |  |  |  | | 9 |  |  |  |  | | 10 |  |  |  |  | | 11 |  |  |  |  | | 12 |  |  |  |  | | 13 |  |  |  |  | | 14 |  |  |  |  | | 15 |  |  |  |  |   Table 13-10C: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {960, 960} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 48 | 1 | 0 | | 2 | 1 | 48 | 2 | 0 | | 3 | 1 | 96 | 2 | 0 | | 4 | 3 | 24 | 2 | -20 if k\_ssb =0  -21 if k\_ssb >0 | | 5 | 3 | 48 | 2 | -20 if k\_ssb =0  -21 if k\_ssb >0 | | 6 |  |  |  |  | | 7 |  |  |  |  | | 8 |  |  |  |  | | 9 |  |  |  |  | | 10 |  |  |  |  | | 11 |  |  |  |  | | 12 |  |  |  |  | | 13 |  |  |  |  | | 14 |  |  |  |  | | 15 |  |  |  |  | |

### Summary of Discussions

The following is a summary of company views on the CORESET#0 configuration in MIB.

* CORESET#0 RB offsets for {SSB, CORESET#0} SCS={120, 120} kHz
  + Mux pattern 1, 24 RB:
    - 0, 4 (Same as Table 13-8): Huawei/HiSilicon, vivo, [CATT], Nokia/NSB, OPPO
    - 0: Intel
    - one value: Samsung
  + Mux pattern 1, 48 RB:
    - 0, 14, 28: Huawei/HiSilicon, vivo, Nokia/NSB
    - 14 (Same as Table 13-8): Intel, [CATT], OPPO
    - two values: Samsung
  + Mux pattern 1, 96 RB:
    - 0, 76: Huawei/HiSilicon, vivo, Nokia/NSB
    - 38: OPPO
    - 0: Intel
    - one value: Samsung
  + Mux pattern 3: -20 if kssb=0, -21 if kssb>0
    - vivo, Intel
* CORESET#0 RB offsets for {SSB, CORESET#0} SCS={480, 480} kHz
  + Mux pattern 1, 24 RB:
    - 0, 4: Huawei/HiSilicon, vivo, Nokia/NSB, OPPO
    - 0: Intel
  + Mux pattern 1, 48 RB:
    - 0, 14, 28: Huawei/HiSilicon, vivo, Nokia/NSB
    - 14: OPPO
    - 0: Intel
  + Mux pattern 1, 96 RB:
    - 0, 76: Huawei/HiSilicon, vivo, Nokia/NSB
    - 38: OPPO
    - 0: Intel
  + Mux pattern 3:
    - -20 if kssb=0, -21 if kssb>0: Intel
    - Same as Rel-15: Samsung
* CORESET#0 RB offsets for {SSB, CORESET#0} SCS={960, 960} kHz
  + Mux pattern 1, 24 RB:
    - 0, 4: Huawei/HiSilicon, vivo, Nokia/NSB, OPPO
    - 0: Intel
  + Mux pattern 1, 48 RB:
    - 0, 14, 28: Huawei/HiSilicon, vivo, Nokia/NSB
    - 14: OPPO
    - 0: Intel
  + Mux pattern 1, 96 RB:
    - 0, 76: Huawei/HiSilicon
    - 38: OPPO
    - 0: Intel
  + Mux pattern 3:
    - -20 if kssb=0, -21 if kssb>0: Intel
    - Same as Rel-15: Samsung
* Do not support 96 RB for 480, 960 kHz
  + Interdigital
* Support mux pattern 3 with 24 and 48 RB for 120 and 480 kHz only
  + Interdigital
* Do not support mux pattern 3 for 480 and 960 kHz
  + vivo
* Support 96 RB for 120 and 480 kHz, and do not support 96 RB for 960 kHz
* Support mux pattern 3 with 24 and 48 RB for 480 and 960 kHz
  + Nokia/NSB
* At least for 480 kHz, support multiplexing pattern 1 with 96 PRB with 2-symbol duration, with four RB offsets.
  + Nokia/NSB
* Confirm WAs on ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz.
  + Intel

### 1st Round Discussion

Discuss further on the following proposals and issues.

For the RB offsets, while actual required RB offsets will require channelization in RAN4 to be complete, companies provided some suggestions. Proposal #6-1 is moderator’s attempt based on companies inputs. Moderator notes that there are few companies who expressed different views on RB offsets. Please comment further on RB offsets, or whether RAN1 should wait until RAN4 concludes on the channelization.

#### Proposal# 6-1

* CORESET#0 RB offsets for {SSB, CORESET#0} SCS={120, 120} kHz
  + Mux pattern 1, 24 RB with 2 symbols: 0, 4
  + Mux pattern 1, 48 RB with 1 and 2 symbol: 0, 14, 28
  + Mux pattern 1, 96 RB with 1 and 2 symbols: 0, 76
  + Mux pattern 3, 24 RB with 2 symbols: -20 if kssb=0, -21 if kssb>0
  + Mux pattern 3, 48 RB with 2 symbols: -20 if kssb=0, -21 if kssb>0
  + Total 14 entries (=2 + 3 + 3 + 2 + 2 + 1 + 1)
* CORESET#0 RB offsets for {SSB, CORESET#0} SCS={480, 480} kHz
  + Mux pattern 1, 24 RB with 2 symbols: 0, 4
  + Mux pattern 1, 48 RB with 1 and 2 symbol: 0, 14, 28
  + Mux pattern 1, 96 RB with 2 symbols: 0, 76
  + Mux pattern 3, 24 RB with 2 symbols: -20 if kssb=0, -21 if kssb>0
  + Mux pattern 3, 48 RB with 2 symbols: -20 if kssb=0, -21 if kssb>0
  + Total 12 entries (=2 + 3 + 3 + 2 + 1 + 1)
* CORESET#0 RB offsets for {SSB, CORESET#0} SCS={960, 960} kHz
  + Mux pattern 1, 24 RB with 2 symbols: 0, 4
  + Mux pattern 1, 48 RB with 1 and 2 symbol: 0, 14, 28
  + Mux pattern 1, 96 RB with 2 symbols: 0, 76
  + Mux pattern 3, 24 RB with 2 symbols: -20 if kssb=0, -21 if kssb>0
  + Mux pattern 3, 48 RB with 2 symbols: -20 if kssb=0, -21 if kssb>0
  + Total 12 entries (=2 + 3 + 3 + 2 + 1 + 1)

There are several companies proposing to support or not support specific cases. There has been RAN1 agreement/working assumption on this before. So unless there are critical problems, moderator suggests not to revisit previously agreed aspects. Below is a copy of relevant WA for CORESET#0. Companies to provide comments on what the concern are and reasons and motivation to change previous WA.

|  |
| --- |
| Working assumption:   * For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz, support multiplexing pattern 1 with 96 PRB CORESET#0, and {1, 2} symbol durations * Note: the working assumption can be confirmed once RAN1 agrees on the number of needed SSB-CORESET0 offsets for 24 and 48 RB CORESET0 based on RAN4 channelization design   **Working assumption**  For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,   * After supporting entries for multiplexing pattern 1 for the agreed pairs of (, ) ={(24, 2), (48, 1), (48,2)} (with required RB offsets), if additional entries are left, support multiplex pattern 3 with 24 PRB and 2 symbol duration, and multiplexing pattern 3 with 48 PRB and 2 symbol duration.   **Working assumption**  For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,   * After supporting entries for multiplexing pattern 1 for the agreed pairs of (, ) ={(24, 2), (48, 1), (48,2)} (with required RB offsets) and multiplex pattern 3 with 24 and 48 PRB and 2 symbol duration (with required RB offsets), if additional entries are left, support multiplexing pattern 1 with 96 PRB and 2 symbol duration   + Note: the working assumption can be confirmed once RAN1 agrees on the number of needed SSB-CORESET0 offsets for 24 and 48 RB CORESET0 based on RAN4 channelization design. |

#### Company Comments/Inputs

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | Although the Proposal# 6-1 is not exactly the same as our proposal, we are ok with the directional in general to make a conservative design that is applicable regardless of RAN4 decisions. There are some further comments:   * For Pattern 3, our proposal is not included, and revised the summary to reflect so. Basically, we prefer to keep the same configurations as Rel-15, and didn’t the reason to remove one of the configurations. * For Pattern 1 with 96 RBs for 480 kHz and 960 kHz, we are wondering whether we can also support 1 symbol such that the configuration tables for 120/480/960 kHz are exactly the same. |

### <Summary of 1st Round Discussion>

*[Summary to be provided by moderator after discussion]*

## 2.7 SS#0 Configuration

* From [6] Nokia/NSB
  + The Type0-PDCCH CSS set for multiplexing pattern 3 for 480kHz and 960kHz is defined as follows:

|  |  |  |
| --- | --- | --- |
| **Index** | **PDCCH monitoring occasions (SFN and slot number)** | **First symbol index**  **(*k* = 0, 1, … 31)** |
| 0 |  | 2, 9 in |
| 1 ~ 15 | Reserved | |

* From [12] ETRI
  + Agree to TP#7-1
  + Removal of M=2 cases
* From [13] Intel
  + Agree to TP# 7-2

#### TP# 7-1 [7][12]

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| =========== Unchanged Text Omitted ===========  Table 13-15A: PDCCH monitoring occasions for Type0-PDCCH CSS set - SS/PBCH block and CORESET multiplexing pattern 3 and {SS/PBCH block, PDCCH} SCS {480, 480} kHz or {960, 960} kHz   |  |  |  | | --- | --- | --- | | Index | PDCCH monitoring occasions (SFN and slot number) | **First symbol index**  **( = 0, 1, …, 31)** | | 0 |  | 2, 9 in  , |   ============ Unchanged Text Omitted ============ |

#### TP# 7-2 [13]

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Table 13-15A: PDCCH monitoring occasions for Type0-PDCCH CSS set - SS/PBCH block and CORESET multiplexing pattern 3 and {SS/PBCH block, PDCCH} SCS {480, 480} kHz or {960, 960} kHz   |  |  |  | | --- | --- | --- | | Index | PDCCH monitoring occasions (SFN and slot number) | **First symbol index**  **(k=0,1, … 31)** | | 0 |  | 2, 9 in | |

#### TP# 7-3 for TS38.213 [12]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***TS 38.213 Subclause 13, Start of Text Proposal* ---------------------------------------------**  Table 13-12A: Parameters for PDCCH monitoring occasions for Type0-PDCCH CSS set - SS/PBCH block and CORESET multiplexing pattern 1 and {SS/PBCH block, PDCCH} SCS {480, 480} kHz or {960, 960} kHz in FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index |  | Number of search space sets per slot |  | **First symbol index** | | 0 | 0 | 1 | 1 | 0 | | 1 | 0 | 2 | 1/2 | {0, if is even}, {7, if is odd} | | 2 | X | 1 | 1 | 0 | | 3 | X | 2 | 1/2 | {0, if is even}, {7, if is odd} | | 4 | 5 | 1 | 1 | 0 | | 5 | 5 | 2 | 1/2 | {0, if is even}, {7, if is odd} | | 6 | 0 | 2 | 1/2 | {0, if is even}, {, if is odd} | | 7 | X | 2 | 1/2 | {0, if is even}, {, if is odd} | | 8 | 5 | 2 | 1/2 | {0, if is even}, {, if is odd} | | 9 | 5+X | 1 | 1 | 0 | | 10 | 5+X | 2 | 1/2 | {0, if is even}, {7, if is odd} | | 11 | 5+X | 2 | 1/2 | {0, if is even}, {, if is odd} | | 12 | ~~0~~ | ~~1~~ | ~~2~~ | ~~0~~ | | Reserved | | | | | 13 | ~~5~~ | ~~1~~ | ~~2~~ | ~~0~~ | | Reserved | | | | | 14 | Reserved | | | | | 15 | Reserved | | | |   ***TS 38.213 Subclause 13, End of Text Proposal* ---------------------------------------------** |

### Summary of Discussions

The following is a summary of company position of various aspects of SS#0 configuration.

* Three companies provided TP (#7-1) for starting OFDM symbol position for multiplexing pattern 3 for 480 and 960 kHz.
  + TP#7-2 seems to conceptually same as TP# 7-1.
* One company suggested removing M=2 from the SS#0 configuration.

### 1st Round Discussion

Discuss further on the TP#7-1 and #7-3

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | We support TP#7-1 (corrected the font color in the TP).  We didn’t see an essential issue with the aspect concerned by TP#7-3. |

### <Summary of 1st Round Discussion>

*[Summary to be provided by moderator after discussion]*

## 2.8 ANR/CGI Reporting Aspects

* From [2] Huawei/HiSilicon:
  + In operation with shared spectrum in FR2-2, when a UE is configured to report the CGI associated with an off-synch raster SSB, the UE finds the frequency offset from CORESET#0 to the off-synch raster SSB according to a sum of the following first offset and the second offset:
    - First offset: Provided in Table 13-10A, Table 13-10B, Table 13-10C of 38.213 and
    - Second offset: Determined as the offset from a smallest RB index of the common RB overlapping with the first RB of the off-synch raster SSB indicated in the measurement configuration to a smallest RB index of the common RB overlapping with the first RB of a SSB hypothetically located at the GSCN of the synch raster entry closest to 120th RE of the SSB indicated in the measurement configuration in the same channel where the synch raster entry is located in the same 100 or 400MHz channel as the 120 or 480kHz SSB.
* From [6] Nokia/NSB
  + For operation with and without shared spectrum access on FR2-2, apply the method defined for FR2-1 to acquire the SIB1 when the SSB is not directly associated to the SIB1.
* From [7] Samsung
  + No need to support Rel-16 NR-U method for determining the RB offset for ANR purpose.
    - Adopt TP#8-1 for TS 38.213.
* From [14] Ericsson
  + Adopt TP#8-2 to correct Section 13 in 38.213 so that the Rel-16 ANR procedure for shared spectrum channel access is not applicable to FR2-2.

#### TP# 8-1 for TS38.213 [7]

|  |
| --- |
| 13 UE procedure for monitoring Type0-PDCCH CSS sets  ============= Unchanged Text Omitted =============  For operation without shared spectrum channel access and for operation with shared spectrum channel access in FR2-2, a UE assumes that the offset in Tables 13-1 through 13-10C is defined with respect to the SCS of the CORESET for Type0-PDCCH CSS set from the smallest RB index of the CORESET for Type0-PDCCH CSS set to the smallest RB index of the common RB overlapping with the first RB of the corresponding SS/PBCH block. The SCS of the CORESET for Type0-PDCCH CSS set is provided by *subCarrierSpacingCommon* for FR1 and FR2-1 and same as the SCS of the corresponding SS/PBCH block for FR2-2. In Tables 13-7, 13-8, and 13-10 is defined in [4, TS 38.211].  For operation with shared spectrum channel access in FR1, a UE determines an offset from a smallest RB index of the CORESET for Type0-PDCCH CSS set to a smallest RB index of the common RB overlapping with a first RB of the corresponding SS/PBCH block  - according to the offset in Table 13-1A or Table 13-4A, if the frequency position of the SS/PBCH block corresponds to the GSCN of a synchronization raster entry as defined in [8-1, TS 38.101-1], and  - according to a sum of a first offset and a second offset if the frequency position of the SS/PBCH block is provided by *ssbFrequency* in a measurement configuration associated with a reporting configuration providing *reportCGI* and does not correspond to the GSCN of a synchronization raster entry as defined in [8-1, TS 38.101-1], where  - the first offset is provided in Table 13-1A or Table 13-4A, and  - the second offset is determined as the offset from a smallest RB index of the common RB overlapping with the first RB of the SS/PBCH block indicated in the measurement configuration to a smallest RB index of the common RB overlapping with the first RB of a SS/PBCH block hypothetically located at the GSCN of a synchronization raster entry, where the single synchronization raster entry is located in the same channel as the SS/PBCH block used for the shared spectrum channel access procedure, as described in [15, TS 37.213]  where the offsets are defined with respect to the SCS of the CORESET for Type0-PDCCH CSS set that is same as the SCS of the corresponding SS/PBCH block.  ============= Unchanged Text Omitted ===================== |

#### TP# 8-2 for TS38.213 [14]

|  |
| --- |
| >>> Text Proposal (TP#1) for 38.213, Section 13 >>>  \*\*\* Unchanged text omitted \*\*\*  For operation without shared spectrum channel access and in FR2-2, a UE assumes that the offset in Tables 13-1 through 13-10C is defined with respect to the SCS of the CORESET for Type0-PDCCH CSS set from the smallest RB index of the CORESET for Type0-PDCCH CSS set to the smallest RB index of the common RB overlapping with the first RB of the corresponding SS/PBCH block. The SCS of the CORESET for Type0-PDCCH CSS set is provided by *subCarrierSpacingCommon* for FR1 and FR2-1 and same as the SCS of the corresponding SS/PBCH block for FR2-2. In Tables 13-7, 13-8, and 13-10 is defined in [4, TS 38.211].  For operation with shared spectrum channel access in FR1, a UE determines an offset from a smallest RB index of the CORESET for Type0-PDCCH CSS set to a smallest RB index of the common RB overlapping with a first RB of the corresponding SS/PBCH block  - according to the offset in Table 13-1A or Table 13-4A, if the frequency position of the SS/PBCH block corresponds to the GSCN of a synchronization raster entry as defined in [8-1, TS 38.101-1], and  - according to a sum of a first offset and a second offset if the frequency position of the SS/PBCH block is provided by *ssbFrequency* in a measurement configuration associated with a reporting configuration providing *reportCGI* and does not correspond to the GSCN of a synchronization raster entry as defined in [8-1, TS 38.101-1], where  - the first offset is provided in Table 13-1A or Table 13-4A, and  - the second offset is determined as the offset from a smallest RB index of the common RB overlapping with the first RB of the SS/PBCH block indicated in the measurement configuration to a smallest RB index of the common RB overlapping with the first RB of a SS/PBCH block hypothetically located at the GSCN of a synchronization raster entry, where the single synchronization raster entry is located in the same channel as the SS/PBCH block used for the shared spectrum channel access procedure, as described in [15, TS 37.213]  where the offsets are defined with respect to the SCS of the CORESET for Type0-PDCCH CSS set that is same as the SCS of the corresponding SS/PBCH block.  \*\*\* Unchanged text omitted \*\*\*  >>> End Text Proposal >>> |

### Summary of Discussions

The following is a summary of company inputs on ANR/CGI reporting aspects.

* Few companies provided views on how to handle the second offset indication for CORESET#0 intended to support other means of ANR/CGI reporting for neighbor cells for FR2-2.

### 1st Round Discussion

Discuss further on TP#8-1 and #8-2.

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | We corrected TP#8-1 in the summary (one change is loss), and we believe it’s the same as TP#8-2, but using a better wording what editors used in current spec ^^. |

### <Summary of 1st Round Discussion>

*[Summary to be provided by moderator after discussion]*

## 2.9 NR Carrier RSSI measurement

* From [7] Samsung
  + For 480 and 960 kHz:
    - Support the following 4 configurations for NR carrier RSSI measurement:
      * Configuration #0: {0, 1};
      * Configuration #1: {0, 1, …, 5};
      * Configuration #2: {0, 1, …, 8};
      * Configuration #3: {0, 1, …, 12};
    - Adopt TP#5 for TS 38.215.
* From [15] Apple
  + For 480 and 960 kHz SCS, support the following 4 configurations for NR carrier RSSI measurement:

#### TP# 9-1 for TS38.215 [7]

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 5.1.3 SS reference signal received quality (SS-RSRQ)  =========== Unchanged Text Omitted ===========  Table 5.1.3-1: NR Carrier RSSI measurement symbols   |  |  | | --- | --- | | **OFDM signal indication *endSymbol*** | **Symbol indexes** | | | 0 | {0,1} | | 1 | For 480 kHz and 960 kHz {0,1,2,..,10,12}; otherwise {0,1,2,..,10,11} | | 2 | {0,1,2,…, 5} | | 3 | For 480 kHz and 960 kHz {0,1,2,..,8}; otherwise {0,1,2,…, 7} |   ============ Unchanged Text Omitted ============ |

#### TP# 9-2 for TS38.215 [15]

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  | | --- | --- | | **OFDM signal indication end Symbol** | **Symbol indexes** | | 0 | {0,1} | | 1 | For 480 kHz/960 kHz: {0,1,2 ,…, 11,12},  otherwise: {0,1,2,…,10,11} | | 2 | {0,1, 2,…, 5} | | 3 | {0, 1, 2,…, 7} | |

### Summary of Discussions

The following is a summary of company inputs on updates to NR RSSI.

* Two companies provide suggestions to updates to NR RSSI.

### 1st Round Discussion

Discuss further on TP#9-1 and #9-2.

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | We support TP#9-1 for the best technical merit, and can be ok with TP#9-2 as a compromise. |

### <Summary of 1st Round Discussion>

*[Summary to be provided by moderator after discussion]*

## 2.10 PRACH

* From [3] Interdigital
  + For 52.6 – 71 GHz, support sharing and extending the COT for LBT-free PRACH transmission in the consecutive ROs. Consider using preambles scrambled with cover codes in PRACH transmission to inform an ongoing RACH occasion. As such, upon successful detection of the cover code, the UE could consider extending the initiated COT for LBT-free PRACH transmission.
* From [14] Ericsson
  + Agree to TP#10-1
* From [17] LGE
  + Agree to TP#10-1, #10-3

#### TP# 10-1 for TS38.211 [14][17]

|  |
| --- |
| \*\*\* Unchanged text omitted \*\*\*  5.3.2 OFDM baseband signal generation for PRACH  The time-continuous signal  on antenna port for PRACH is defined by  \*\*\* Unchanged text omitted \*\*\* |

#### TP# 10-2 for TS38.211 [17]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| \*\*\* Unchanged text omitted \*\*\*  **Table 6.3.3.2-1: Supported combinations of and , and the corresponding value of .**   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | **for PRACH** | **for PUSCH** | **, allocation expressed in number of RBs for PUSCH** |  | | … | … | … | … | … | | 139 | 480 | 120 | 47~~48~~ | 1~~2~~ | | … | … | … | … | … | | 139 | 960 | 120 | 94~~96~~ | 1~~2~~ | | … | … | … | … | … | | 571 | 480 | 120 | 191~~192~~ | 1~~2~~ | | … | … | … | … | … |   \*\*\* Unchanged text omitted \*\*\* |

### Summary of Discussions

The following is a summary of company inputs on PRACH.

* One company commented that cover code multiplied PRACH format shout be supported for sharing and extending COT
* Two companies provided editorial correction to PRACH sequence length application for TS38.211
* One company suggested updated to the number of RB for PRACH

### 1st Round Discussion

Discuss further on the TP#10-1 and #10-2. Also please comment further on Proposal #10-1.

#### Proposal# 10-1

* For 52.6 – 71 GHz, support sharing and extending the COT for LBT-free PRACH transmission in the consecutive ROs. Consider using preambles scrambled with cover codes in PRACH transmission to inform an ongoing RACH occasion. As such, upon successful detection of the cover code, the UE could consider extending the initiated COT for LBT-free PRACH transmission.

|  |  |
| --- | --- |
| Company | Comments |
|  |  |

### <Summary of 1st Round Discussion>

*[Summary to be provided by moderator after discussion]*

## 2.11 Other PRACH aspects

### Summary of Discussions

* From [3] Interdigital
  + Do not support gap insertion between consecutive ROs in time domain as it causes inefficiency and application ambiguity.
  + Consider decomposing the PRACH occasions in time and frequency for operation without beam switching gaps between consecutive ROs. As such, the beam switching corresponding to each RO could be accomplished along with the preceding time-domain RO.
* From [9] ZTE/Sanechips
  + The ra-ResponseWindow and msgB-ResponseWindow value should be updated for Rel-17 above 52.6GHz.
    - The value of {sl240, sl320, sl640, sl960, sl1280,sl1920,sl2560} should be added for ra-ResponseWindow-17.
    - The value of {sl640, sl960,sl1280,sl1920,sl2560} should be added for msgB-ResponseWindow-r17.
  + The ra-ResponseWindow-r17 and msgB-ResponseWindow-r17 should be included in the RRC parameters for Rel-17 above 52.6GHz.
  + The msgA-PRACH-RootSequenceIndex-r16 should be included in the RRC parameters for Rel-17 above 52.6GHz.
* From [14] Ericsson
  + Add the parameter msgA-PRACH-RootSequeceIndex for configuring the root sequence index and sequence length for 2-step RACH to the higher layer parameter spreadsheet and send update to RAN2.

### 1st Round Discussion

Discuss further on the following updates to RRC parameters. Moderator assumes company can actually provide comments on these RRC parameters directly to the RRC parameter discussion. Therefore, moderator only ask companies to provide input on the proposed updates and ask ZTE and Ericsson (original proponents) to provide inputs to the RRC parameter discussion directly.

Also please provide information on per UE/cell/TRP information for RRC parameters below.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Sub-feature group** | **Parameter name in the spec** | **New or existing?** | **Description/Notes** | **Value range** | **Per (UE, cell, TRP, …)** | **UE-specific or Cell-specific** |
| SSB and RACH | ra-ResponseWindow-17 | New | From Conclusion:  For FR2-2, support the same mechanism as in Rel-16 for extended RAR window for both 4-step and 2-step RACH. | {sl240, sl320, sl640, sl960，sl1280,sl1920,sl2560.} |  |  |
| SSB and RACH | msgB-ResponseWindow-r17 | New | From conclusion: Conclusion:  For FR2-2, support the same mechanism as in Rel-16 for extended RAR window for both 4-step and 2-step RACH. | {sl640, sl960,sl1280,sl1920,sl2560} |  |  |
| SSB and RACH | msgA-PRACH-RootSequeceIndex-r16 | existing | May not need to change the IE, but need to add in the note on the limitation to be used with SCS. Field description requires updating to capture that L = 1151 is not supported for SCS 480 and 960 kHz and L = 571 is not supported for 960 kHz. | CHOICE { l571 INTEGER {0..569}, l1151 INTEGER {0..1149}} | RACH-ConfigCommonTwoStepRA-r16 | Cell-specific |

#### Company Comments/Inputs

|  |  |
| --- | --- |
| Company | Comments |
|  |  |

### <Summary of 1st Round Discussion>

*[Summary to be provided by moderator after discussion]*

## 2.12 Intra-Cell guard band

### Summary of Discussions

One company provided editorial correction to guard band for shared spectrum cases.

* From [14] Ericsson
  + Agree to TP#12-1

#### TP# 12-1 for TS38.214 [14]

|  |
| --- |
| \*\*\* Unchanged text omitted \*\*\*  7 UE procedures for transmitting and receiving on a carrier with intra-cell guard bands  For operation with shared spectrum channel access in FR1, when the UE is configured with any of *IntraCellGuardBandsPerSCS* for UL carrier and for DL carrier with SCS configuration , the UE is provided with intra-cell guard bands on a carrier with , each defined by start CRB and size in number of CRBs, and , provided by higher layer parameters *startCRB* and *nrofCRBs*, respectively, where . The subscript *x* is set to DL and UL for the downlink and uplink, respectively. Where there is no risk of confusion, the subscript *x* can be dropped. The intra-cell guard bands separate RB sets, each defined by start and end CRB, and , respectively. The UE does not expect that *nrofCRBs* is configured with non-zero value smaller than the applicable intra-cell guard bands as specified in [8, TS 38.101-1] corresponding to and carrier size . The UE determines the start and end CRB indices for as  \*\*\* Unchanged text omitted \*\*\* |

### 1st Round Discussion

Discuss further on the TP#12-1

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | Should this issue be discussed in initial access agenda? |

### <Summary of 1st Round Discussion>

*[Summary to be provided by moderator after discussion]*

## 2.13 Others Aspects

* From [1] Futurewei:
  + Indication of LBT/No-LBT mode of channel access per cell is provided in SIB1.
  + The SIB1 LBT/No-LBT indication is used by UE for channel access until it receives a dedicated channel access indication or configuration, which takes precedence over the LBT/No-LBT SIB1 indication.
  + Define or extend the LBT channel access mode indication in DCI for FR2-2.
  + If the short control signaling exempt is supported for msg1 and msgA, the indication of the short control signaling LBT exemption support should be provided in SIB1.
* From [3] Interdigital
  + Support indicating the license regime in initial access operations based on different sync raster sets.
* From [10] Spreadtrum
  + Supporting initial cell selection with 480kHz SSB should be an optional UE capability separately from supporting other processing with 480/960kHz SCS.
  + The SSB-based TRS/CSI-RS validation can be supported.
* From [11] OPPO
  + Support indication of short control signalling transmission related parameters.

### 1st Round Discussion

Please note the following:

* For issues related to channel access, such as parameters for short control signaling or LBT, moderator asks proponent companies to bring the issue up in channel access agenda.
* For issues related to making some UE features/capability optional/mandatory, moderator asks proponent companies to bring the issue up in UE feature discussion directly, unless the proposal to create a new UE capability.
* For channelization aspects, moderator assumes this is in RAN4 domain, and moderator asks proponent companies to bring the issue up in RAN4.

Companies are asked to provide comments on any other issues that needs to be addressed or any other proposal the moderator has missed.

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | We agree with moderator’s comments. |

### <Summary of 1st Round Discussion>

*[Summary to be provided by moderator after discussion]*

# Summary of Proposals for Email Approval

*[Summary to be provided by moderator]*

# Summary of Agreements from RAN1 #107-bis-e

*[Summary to be provided by moderator]*

# Reference

1. R1-2200024, “On remaining issues for initial access for Beyond 52.6GHz,” FUTUREWEI
2. R1-2200044, “Remaining issue of initial access signals and channels for 52-71GHz spectrum,” Huawei, HiSilicon
3. R1-2200059, “Remaining issues for initial access operation in 52.6-71GHz,” InterDigital, Inc.
4. R1-2200074, “Remaining issues on initial access aspects for NR operation from 52.6GHz to 71GHz,” vivo
5. R1-2200142, “Remaining issues on Initial access aspects for up to 71GHz operation,” CATT
6. R1-2200183, “Initial access aspects,” Nokia, Nokia Shanghai Bell
7. R1-2200192, “Maintenance on initial access aspects for NR from 52.6 GHz to 71 GHz,” Samsung
8. R1-2200226, “Remaining issues on initial access aspects for NR in FR2-2,” NTT DOCOMO, INC.
9. R1-2200259, “Remaining issues on the initial access aspects for 52.6 to 71GHz,” ZTE, Sanechips
10. R1-2200273, “Discussion on initial access aspects for NR for 60GHz,” Spreadtrum Communications
11. R1-2200324, “Discusson on remaining issue for initial access aspects,” OPPO
12. R1-2200355, “Remaining issues on initial access aspects for NR from 52.6 to 71GHz,” ETRI
13. R1-2200366, “Discussion on initial access aspects for extending NR up to 71 GHz,” Intel Corporation
14. R1-2200400, “Initial Access Aspects,” Ericsson
15. R1-2200409, “On remaining issues for initial access,” Apple
16. R1-2200494, “Initial access aspects,” Sharp
17. R1-2200564, “Initial access aspects to support NR above 52.6 GHz,” LG Electronics

# List of RAN1 Agreements on initial access

## RAN1 #104-e

**R1-2102073** [Draft] LS on beam switching gap for 60 GHz band Intel Corporation

Final LS endorsed in R1-2102202

Agreement:

Send an LS to RAN4 to get input on gap required for gNBs and UEs for beam switching and for UL/DL and DL/UL switching.

Agreement:

Whether or not to support 240 kHz, 480kHz and 960kHz SCS for SSB and the conditions under which SSB for 240 kHz, 480 kHz and 960 kHz may be supported will be decided no later than RAN1#104bis-e.

Agreement:

For an unlicensed band that requires LBT, further study whether/how to support discovery burst (DB) and discovery burst transmission window (DBTW) at least for 120 kHz SSB SCS

* If DB supported
  + FFS: What signals/channels are included in DB other than SS/PBCH block
* If DBTW is supported
  + Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs
    - FFS: how to support UEs performing initial access that do not have any prior information on DBTW.
  + PBCH payload size is no greater than that for FR2
  + Duration of DBTW is no greater than 5 ms
  + Number of PBCH DMRS sequences is the same as for FR2
* The following points are additionally FFS:
  + How to indicate candidate SSB indices and QCL relation without exceeding limit on PBCH payload size
  + Details of the mechanism for enabling/disabling DBTW considering LBT exempt operation and overlapping licensed/unlicensed bands
  + Whether or not to support DBTW for SSB SCS(s) other than 120 kHz if other SSB SCS(s) are supported

Agreement:

For CORESET#0 and Type0-PDCCH search space configured in MIB:

* Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {120, 120} kHz
  + Support at least SSB and CORESET#0 multiplexing patterns, number of RBs for CORESET#0, number of symbols (duration of CORESET#0) that are supported in Rel-15/16 for {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS = {120, 120} kHz.
    - FFS: Supporting additional values
  + FFS: Supported values for SSB to CORESET#0 offset RBs
* If 480kHz SSB SCS that configures CORESET#0 and Type0-PDCCH CSS in MIB is agreed to be supported,
  + Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {480, 480} kHz
* If 960 kHz SSB SCS that configures CORESET#0 and Type0-PDCCH CSS in MIB is agreed to be supported,
  + Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {960, 960} kHz
* If 240 kHz SSB SCS is agreed to be supported,
  + Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {240, 120} kHz
* FFS: any other combinations between one of SSB SCS (120, 240, 480, 960) and one of CORESET#0 SCS (120, 480, 960)
  + FFS: initial timing resolution based on low SCS (120 kHz) and its impact on the performance of higher SCS (480/960 kHz)

Agreement:

For 480 kHz and 960 kHz SSB SCS (if agreed)

* Study further on reserving symbol gap between SSB positions with different SSB index (and possibly between SSB position and other signal/channels)
  + FFS: whether symbol gap is needed for only 960 kHz or both 480 and 960 kHz.
* Study further on reserving gap for UL/DL switching within the pattern accounting possibility for reserving UL transmission occasions in the SSB pattern
* Study should account for inputs from RAN4

Agreement:

* For initial access and non-initial access use cases, support 120kHz PRACH SCS with sequence length L=571, 1151 (in addition to L=139) for PRACH Formats A1~A3, B1~B4, C0, and C2.
* For non-initial access use cases,
  + if 480kHz and/or 960 kHz SSB SCS is agreed to be supported, support 480 and/or 960 kHz PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively.
    - FFS: support of sequence length L = 571, 1151
* FFS: Support of 480 and/or 960 kHz PRACH SCS for initial access use cases, if 480 and/or 960 kHz SSB SCS is agreed to be supported for initial access

Agreement:

If 480 and/or 960 kHz PRACH SCS is supported, RAN1 should study whether or not the current RA-RNTI calculation and PRACH identification in RAR correctly provides unique identification of PRACH.

## RAN1 #104-bis-e

Agreement:

For the case where SSB location and SCS are explicitly provided to the UE (non-initial access) and SSB does not configure Type-0 PDCCH, support 480 kHz and 960 kHz numerologies for the SSB

* Note: Strive to minimize specification impact due to the new SCS for SSB

Agreement:

* For operation with shared spectrum channel access of NR 52.6 – 71 GHz, support discovery burst (DB) and define the DB same as in Rel-16 37.213 Section 4.0
* FFS: Support discovery burst transmission window (DBTW) at least for SSB with 120 kHz SCS with the following requirements
  + PBCH payload size is no greater than that for FR2
  + Duration of DBTW is no greater than 5 ms
  + Number of PBCH DMRS sequences is the same as for FR2
  + FFS: applicability of DBTW design for 120kHz to SSB with 480kHz and 960kHz SCS
  + Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs
    - FFS: how to support UEs performing initial access that do not have any prior information on DBTW.
    - FFS: details of the mechanism for enabling/disabling DBTW considering LBT exempt operation and overlapping licensed/unlicensed bands
    - FFS: details of how to inform UEs of the configuration of DBTW

Agreement:

For SSB with 120kHz SCS for NR 52.6 GHz to 71 GHz,

* 120 kHz SCS: the first symbols of the candidate SS/PBCH blocks have indexes {4, 8,16, 20} + 28×n, where index 0 corresponds to the first symbol of the first slot in a half-frame.
* For carrier frequencies within 52.6 GHz to 71GHz, support at least 𝑛 = 0, 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 15, 16, 17, 18.
  + Other values of *n* (if any) are FFS, and support of additional n values are subject to support of DBTW for 120kHz SSB

Agreement:

* PRACH configuration for 480/960 kHz SCS (if agreed)
  + The minimum PRACH configuration period is 10 ms (as in FR2)
  + For RO configuration for PRACH with 480/960kHz SCS,
    - FFS: details of how to configure the 480/960 kHz PRACH ROs using [60 or 120 kHz] reference slot considering at least:
      * location of 480/960 kHz PRACH slot per reference slot
      * location of duration containing 480/960khz PRACH slot pattern within 10ms
      * potential impact to RA-RNTI calculation

## RAN1 #105-e

Agreement:

For 480kHz/960kHz SSB, select one of the following alternatives:

* ALT 1) First symbols of the candidate SSB have index {X, Y} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
  + value of X and Y are identical for 480kHz and 960kHz
    - FFS: exact value of X and Y
* ALT 2) First symbols of the candidate SSB have index {4, 8, 16,20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
* Values of n for 480kHz and 960kHz for ALT 1 and 2
  + FFS: whether number of values for ‘n’ depend on LBT operation (i.e. LBT vs no-LBT)
  + FFS: exact values of ‘n’ for each SCS
  + Values of ‘n’ for one mode of operation shall be strictly a subset of values for another mode of operation, if two mode of operation exist for number of candidate SSBs
  + FFS: whether values of ‘n’ shall not be all consecutive integer values (i.e. non-candidate SSB slots are positioned every few candidate SSB slots)

Proposal:

In addition to 120kHz, support **480** kHz SSB for initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with following constraints.

* Limited sync raster entry numbers
  + It is assumed that RAN4 supports a channelization design which results in the total number of synchronization raster entries considering both licensed and unlicensed operation in a 52.6 – 71 GHz band no larger than 665 (Note: the total number of synchronization raster entries in FR2 for band n259 + n261 is 602). If the assumption cannot be satisfied, it’s up to RAN4 to decide its applicability to bands in 52.6 – 71 GHz.
* only 480kHz CORESTE#0/Type0-PDCCH SCS supported for 480 kHz SSB SCS.
* SSB time domain candidate resource pattern (within a slot or pair of slots) for 480 and 960kHz SSB are identical
* Prioritize support SSB-CORESET0 multiplexing pattern 1. Other patterns discussed on a best effort basis.
* Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible

Formal objection sustained by: Huawei, MediaTek (would like to discuss at next meeting)

Proposal:

In addition to 120kHz, support **both** **480 and 960** kHz SSB for initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with following constraints.

* Limited sync raster entry numbers
  + It is assumed that RAN4 supports a channelization design which results in the total number of synchronization raster entries considering both licensed and unlicensed operation in a 52.6 – 71 GHz band no larger than 665 (Note: the total number of synchronization raster entries in FR2 for band n259 + n261 is 602). If the assumption cannot be satisfied, it’s up to RAN4 to decide its applicability to bands in 52.6 – 71 GHz.
* only 1 CORESTE#0/Type0-PDCCH SCS supported for each SSB SCS i.e., (480,480) and (960,960).
* SSB time domain candidate resource pattern (within a slot or pair of slots) for 480 and 960kHz SSB are identical
* Prioritize support SSB-CORESET0 multiplexing pattern 1. Other patterns discussed on a best effort basis.
* Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible

Formal objection sustained by: Huawei, MediaTek (object to 960 kHz)

Proposal:

To support ANR and PCI confusion detection for 480/960kHz SCS based SSB, support CORESET#0/Type0-PDCCH configuration in MIB of 480 and 960kHz SSB

* FFS: additional method(s) to enable support to obtain neighbor cell PCI and SIB1 contents related to CGI reporting
* Only 1 CORESTE#0/Type0-PDCCH SCS supported for each SSB SCS, i.e., (480,480) and (960,960).
* Prioritize support SSB-CORESET0 multiplexing pattern 1. Other patterns discussed on a best effort basis.
* Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible
* Note: From UE perspective, ANR detection for 480/960kHz SCS based SSB is not supported if the UE does not support 480/960 SCS for SSB.
* Note: for ANR, when reading the MIB, the cell containing the SSB is known to the UE, as defined in 38.133 specification.

Formal objection sustained by: Huawei

Agreement:

For the case agreed in RAN1 #104bis-e where 480/960 kHz SSB location and SCS are explicitly provided to the UE (non-initial access)

* Support configuring CORESET#0/Type0-PDCCH for the purpose of ANR/PCI confusion detection by down selecting from the following two alternatives
  + Alt 1) Using dedicated signaling
  + Alt 2) Using configuration in MIB
    - Note: for ANR, when reading the MIB, the cell containing the SSB is known to the UE, as defined in 38.133 specification.

Agreement:

For 480kHz and 960kHz PRACH,

* Down-select among option 1 and 2
  + Option 1) The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.
    - FFS: supported values of the starting PRACH slot index within reference slot and whether or not the ROs for a given PRACH configuration can span more than one PRACH slot if gaps between consecutive ROs are supported for LBT and/or beam switching purposes
  + Option 2) Each 120kHz RO corresponds to 4 and 8 candidate RO positions for 480kHz and 960kHz PRACH, respectively. Information about the number and locations of 480/960kHz candidate RO(s) are configured or pre-selected within each 120kHz RO. The reference 120kHz RO is determined by the current PRACH configuration method in Rel-15/16 specification.
* Following alternatives are considered on PRACH density
  + ALT 1) At least the same density (i.e. number of PRACH slots per reference slot) as for 120kHz PRACH in FR2 is supported
    - FFS: support for higher PRACH slot density (number of PRACH slots per reference slot)
  + ALT 2) at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
    - FFS: support for higher RO density
  + An “example” illustration of PRACH slots for 480/960kHz is shown below:



* FFS: whether and how to account for LBT in RO configuration (if needed)
* FFS: whether and how to account for beam switching gap in RO configuration (if needed)

Agreement:

FFS: Support DBTW at least for 120kHz

* FFS whether DBTW will be applicable for 480/960 kHz SSB SCS
  + If DBTW is supported for 480/960kHz SSB:
    - For the case agreed in RAN1 #104bis-e where 480/960 kHz SSB location and SCS are explicitly provided to the UE (non-initial access), indication of DBTW configuration (e.g. enable/disable of DBTW,  , and DBTW length) are supported by dedicated signaling.
* For 120kHz SSB, support mechanism to distinguish at least the following scenarios:
  + Case 1) (Unlicensed with LBT off) + DBTW disabled
  + Case 2) (Unlicensed with LBT on) + DBTW enabled
  + Case 3) (Unlicensed with LBT on) + DBTW disabled
  + Case 4) (Licensed) + DBTW disabled
  + FFS: Whether/how LBT on/off is indicated in MIB
    - If not indicated in MIB, then FFS whether/how the UE determines different sizes of DCI 1\_0 with CRC scrambled by SI-RNTI
  + FFS: whether any case(s) can be combined for DBTW signaling design and how to handle implications to DCI 1\_0 size ambiguity if is not distinguished in signaling
  + FFS: whether all above cases need an explicit indication
  + FFS: Whether a single indication can be used for combination of more than one cases
* For 120 kHz SSB, enable/disable of DBTW is indicated by one or more of the following methods:
  + Option 1) signaling in MIB
    - Option 1-1) disabling DBTW is jointly coded with
    - Option 1-2) indicated by other bit fields in MIB
    - FFS: among options 1-1 and 1-2
  + Option 2) distinct GSCN used by the SSB
  + Option 3) By comparing the value of  in MIB and DBTW length after UE reads SIB1 or by comparing the value of  in MIB and default DBTW length of 5 ms before UE reads SIB1.
  + FFS: whether to support option 1, 2, 3, or any combination of the options.
  + Note: enable/disable signaling of DBTW by MIB or GSCN does not preclude other signaling methods

Agreement:

If DBTW is supported,

* Working assumption: MIB signaling to support
  + Alt A) indication of at least for 120kHz SSB
    - In this case, the total number of values of to not exceed 4
  + Alt B) Explicit indication of SSB index and/or SSB candidate location
    - FFS on the details of signaling
  + FFS betweenAlt A, or B, or supporting both
* Supported DBTW lengths
  + Alt 1) 0.5, 1, 2, 3, 4, 5 msec
    - Note: same as Rel-16 FR1 NR-U
  + Alt 2) maximum 5 msec
    - FFS other values
  + FFS between Alt 1 and 2
* Number of candidate positions when DBTW is enabled
  + For 120kHz SSB
    - FFS between 64 or 80
  + If DBTW is additionally supported for 480/960kHz SSB
    - FFS between 64 or 128

## RAN1 #106-e

Conclusion:

RAN1 will continue discussions to develop solutions for supporting DBTW

Agreement:

* For 480 and 960kHz PRACH:
  + The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.



Agreement:

* For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, X} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame.



* Alt 1: X = 8
* Alt 2: X = 9

Agreement:

For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame.

Working assumption:

For 120kHz SSB, the number of candidates SSBs in a half frame is 64.

Agreement:

For DBTW with 120kHz SCS (if supported), support DBTW lengths {0.5, 1, 2, 3, 4, 5} msec

* Note: this should be the same as Rel-16 NR-U DBTW lengths.

Agreement:

For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,

* Support the following set of parameters.

|  |  |  |
| --- | --- | --- |
| SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols |
| 1 | 24 | 2 |
| 1 | 48 | 1 |
| 1 | 48 | 2 |

* + Note: the number of entries corresponding the same {mux pattern, number of RB, number of symbol} tuple (listed above) will depend on required RB offsets that needs to be supported based on channel and sync raster design.
* FFS: addition other set of parameters

Agreement:

Do not support PRACH length L=571, 1151 for 960kHz PRACH and at least L =1151 for 480kHz PRACH.

Agreement:

For 480 and 960kHz PRACH:

* At least the same RO density in time domain (i.e. number of specified RO per reference slot according the PRACH configuration index) as for 120kHz PRACH in FR2 is supported
  + FFS: Support gap between consecutive ROs in time domain and the details to derive the gap

Agreement:

For 480 and 960kHz PRACH,

* When a PRACH slot can contain all time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching,
  + and when number of PRACH slots in a reference slot is 1,
    - for 480kHz and for 960kHz PRACH
  + and when the number of PRACH slots in a reference slot is 2,
    - for 480kHz and for 960kHz PRACH
* FFS: values, when a PRACH slot cannot contain all time domain PRACH occasions~~,~~ corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching.
* FFS: whether to allow for additional values if the maximum that can be configured for the number of FD RO’s is less than 8 (due to BW limitation)

## RAN1 #106-bis-e

Working assumption:

Support DBTW for 120 kHz.

* FFS: Support for 480 kHz and 960 kHz

Conclusion:

Do not support gap between consecutive ROs for 480kHz and 960kHz

Agreement:

Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off).

* Existing DCI size alignment in TS38.212 applies to DCI 1\_0 and 0\_0 in CSS.

Agreement:

* Indication of licensed and unlicensed operation is not explicitly indicated in MIB or PBCH payload.
  + FFS: Whether or not to indicate licensed regime by different synchronization raster entries.
* Indication of use of LBT or no-LBT is not explicitly indicated in MIB or PBCH payload.

Agreement:

No other values of n other than agreed previously is supported for 120kHz SCS, where parameter ‘n’ is the set of values to determine the first symbols of the candidate SSB blocks for 120kHz SCS in agreement from RAN1 #104-bis-e.

Working assumption:

* For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz, support multiplexing pattern 1 with 96 PRB CORESET#0, and {1, 2} symbol durations
* Note: the working assumption can be confirmed once RAN1 agrees on the number of needed SSB-CORESET0 offsets for 24 and 48 RB CORESET0 based on RAN4 channelization design

Agreement:

Additionally, support PRACH length L=571 for 480kHz

Agreement:

Support 120 kHz and 480 kHz subcarrier spacing for initial UL BWP for PCell.

Working assumption:

For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW

* If only 1 bit is needed: subCarrierSpacingCommon
* If 2 bits is needed: subCarrierSpacingCommon, and 1 bit from pdcch-ConfigSIB1 (pending CORESET0 or search space design would allows for this bit), else, use the spare-bit (not the Msg Extension bit)
  + The design of CORESET0 and search space shall be done without any consideration to this proposal
  + If 2 bits are needed for both 120kHz and 480/960kHz cases, then use the same bit field combination (i.e. use pdcch-ConfigSIB1 bit for 120/480/960 kHz or spare-bit for 120/480.960 kHz)
  + Note: If pdcch-ConfigSIB1 bit is used, the use of controlResourceSetZero (searchSpaceZero) for 120 kHz and   searchSpaceZero (controlResourceSetZero) for 480/960 kHz is not precluded
* FFS: if 3 bits are required
* Note: the working assumption can be confirmed after RAN1 agrees on the number of needed SSB-CORESET0 offsets based on RAN4 channelization design

Agreement:

For 120kHz SCS, for  values:

* If 2 bits are available in MIB for , at least support {16, 32, 64}
* If 1 bit is available in MIB for , support {32, 64}
  + FFS: methods to indicate more  values without increasing used number of bits, e.g., {16, 32, 64}
* Note: value  < 64 indicates DBTW enabled/supported and operation with shared spectrum.
* Note: For operation without shared spectrum channel access, a UE expects to be configured with  = 64. Use of =64 in shared spectrum is not precluded.
* FFS: 1 bit or 2 bits used for 

Agreement:

Supported value of n for 480/960kHz SSB slot pattern:

* ALT A) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB
  + same pattern will apply to 480kHz and 960kHz (i.e same N and M for 480 and 960 kHz)
  + N = 2, M = 8
  + FFS: starting position of n
* ALT B) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB
  + scaled version pattern will apply between 480 and 960 kHz (i.e. N and M for 480kHz, 2N and 2M for 960 kHz)
  + N = 2, M = 8
  + FFS: starting position of n
* ALT C) slots that do not contain SSB correspond to the slots that do not contain SSB in 120 kHz Case D.
  + Note: ALT 4 means that only slots 32-39 for 480 kHz SSB pattern are reserved for UL and 960 kHz SSB pattern is contiguous.

Agreement:

For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 1:

* FFS: The value of X (> 0)
* FFS: whether or not to use different X value depending on whether DBTW is ON/OFF
* FFS: whether or not to use same or different X value for 480 and 960 kHz
* FFS: whether Y = , or Y=, or whether to remove entries with Y

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Index** |  | **Number of search space sets per slot** |  | **First symbol index** |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | X | 1 | 1 | 0 |
| 3 | X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 4 | 5 | 1 | 1 | 0 |
| 5 | 5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 6 | 0 | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 7 | X | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 8 | 5 | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 9 | 5 + X | 1 | 1 | 0 |
| 10 | 5 + X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 11 | 5 + X | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 12 | 0 | 1 | 2 | 0 |
| 13 | 5 | 1 | 2 | 0 |
| 14 | Reserved | | | |
| 15 | Reserved | | | |

## RAN1 #107-e

**Agreement**

* Support DBTW with 480 and 960 kHz SCS.
* For licensed and unlicensed operation, support 64 candidate SSB positions in a half frame
* Working assumption: Use 2 bits for Q:
  + SubcarrierSpacingCommon
  + spare bit in MIB
* Send LS to RAN2 for confirming the use of the spare bit in MIB
  + The use of 2 bits for Q can be revisited if RAN2 tells RAN1 that the spare bit cannot be used

R1-2112614 [Draft] LS on initial access for 60 GHz Intel Corporation

Final LS endorsed in R1-2112805.

**Agreement**

Confirm the following working assumptions:

* (From #106-bis-e) Support DBTW for 120 kHz.
* (From #106-e) For 120kHz SSB, the number of candidates SSBs in a half frame is 64.

**Agreement**

For SCS that support DBTW, UE derives the QCL relation between candidate SSBs by the value of , where is the candidate SSB index.

**Conclusion**

* The bit-width of ssb-PositionsInBurst in SIB1 and ServingCellConfigCommon is kept the same as in Rel-15 (i.e., 16-bits in SIB1 and 64-bits in ServingCellConfigCommon).

**Agreement**

If multiplexing pattern 3 for 480 and 960 kHz is supported, the TDRA allocation table C is updated as follows:

* Row index 6 (previously reserved) is set to
  + Dmrs-TypeA-Position: 2,3
  + PDSCH mapping type: Type B
  + K0 : 0
  + S = 11
  + L = 2

**Agreement**

Finalizing PRACH slot index for 480 and 960 kHz (removal of bracket of previous agreement)

* when number of PRACH slots in a reference slot is 1,
  + for 480kHz and for 960kHz PRACH
* when the number of PRACH slots in a reference slot is 2,
  + for 480kHz and for 960kHz PRACH

**Agreement**

Update the Table 8.1-2 in TS38.213 to indicate the Ngap (gap between valid RO and SS/PBCH) for 480 kHz and 960 kHz SCS as follows:

* for 480 kHz
* for 960 kHz;

**Agreement**

For single cell operation or for operation with carrier aggregation in a same frequency band, a UE does not transmit PRACH and PUSCH/PUCCH/SRS in a same slot or when a gap between the first or last symbol of a PRACH transmission in a first slot is separated by less than 𝑁 symbols from the last or first symbol, respectively, of a PUSCH/PUCCH/SRS transmission in a second slot where 𝑁=16 for 𝜇=5, 𝑁=32 for 𝜇=6, and 𝜇 is the SCS configuration for the active UL BWP. For a PUSCH transmission with repetition Type B, this applies to each actual repetition for PUSCH transmission [6, TS 38.214].

**Conclusion:**

as part of gap between last symbol of PDCCH order reception and first symbol of the PRACH transmission for FR2-2 uses the same value as FR2-1 (i.e. single value for FR2).

**Agreement**

* For 480 kHz, slot index, n, that contain SSB are:
  + n = {0,1,2,3,4,5,6,7, 8,9,10,11,12,13,14,15, 16,17,18,19,20,21,22,23, 24,25,26,27,28,29,30,31}
* For 960 kHz, slot index, n, that contain SSB are:
  + n = {0,1,2,3,4,5,6,7, 8,9,10,11,12,13,14,15, 16,17,18,19,20,21,22,23, 24,25,26,27,28,29,30,31}

**Agreement**

For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz,

* use Table 13-12 in TS38.213 for multiplexing pattern 1,
* use Table 13-15 in TS38.213 for multiplexing pattern 3.

**Agreement**

For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, parameter X from previous RAN1 agreement is set to:

* X = 1.25 for 480 kHz
* X = 0.625 for 960 kHz

**Conclusion:**

For FR2-2, support the same mechanism as in Rel-16 for extended RAR window for both 4-step and 2-step RACH.

**Agreement**

For a Type-2 random access procedure, a UE transmits a PUSCH, when applicable, after transmitting a PRACH. The UE encodes a transport block provided for the PUSCH transmission using redundancy version number 0. The PUSCH transmission is after the PRACH transmission by at least symbols where for and for , and is the SCS configuration for the active UL BWP.

**Agreement**

For 480 and 960 kHz, supported DBTW lengths are:

* {1.25, 1, 0.75, 0.5, 0.25, 0.125, X} ms, where X = 0.0625 if Q=8 is supported and X is removed if Q=8 is not supported.

**Agreement**

SSB-PositionQCL-Relation IE to indicate QCL relationship between SSB positions for FR2-2 are same set of values supported for in MIB.

**Agreement**

For operation with shared spectrum access, for SS/PBCH block and CORESET#0 multiplexing pattern 3, a UE monitors PDCCH in the Type0-PDCCH CSS set over slots that include Type0-PDCCH monitoring occasions associated with SS/PBCH blocks that are quasi co-located with the SS/PBCH block that provides a CORESET for Type0-PDCCH CSS set.

**Agreement**

For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, parameter Y from previous RAN1 agreement is Y = .

**Agreement**

* For 480kHz and 960kHz PRACH, reuse the RA-RNTI and MSGB-RNTI formula as FR2 and express the slot indexes t\_id based on 120kHz SCS:
  + RA-RNTI =1+s\_id+14×t\_id+14×80×f\_id +14×80×8×ul\_carrier\_id
  + MSGB-RNTI = 1 + s\_id + 14 × t\_id + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id + 14 × 80 × 8 × 2
    - where the subcarrier spacing to determine t\_id is based on the value of µ specified in clause 5.3.2 in TS 38.211 [8] for µ = {0, 1, 2, 3}
    - for µ = {5, 6}, t\_id is the index of the 120 kHz slot in a system frame that contains the PRACH occasion (0 ≤ t\_id < 80).
  + Note: As per previous RAN1 agreement, there is only one 480 or 960 kHz PRACH slot in a 120kHz slot, such that RA-RNTI and MSGB-RNTI does not result in ID collision.
* Send LS to RAN2 on the updates on RA-RNTI and MSGB-RNTI.

R1-2112734 [Draft] LS on RA-RNTI and MSGB-RNTI for 480 and 960 kHz Intel Corporation

Final LS endorsed in R1-2112832 (with removal of “first” in text referring to the captured agreement)

**Agreement**

* Same values using the same set of signaling bits are supported for 120, 480, and 960 kHz.
* Supported values of : {16, 32, 64}
  + Note:
    - For operation with shared spectrum channel access, any supported value of can be indicated and value < 64 indicates DBTW enabled
    - UE is expected to be configured with =64 in licensed operations
    - For operation with and without shared spectrum channel access, =64 indicates that the SS/PBCH block index and the candidate SS/PBCH block index have a one-to-one mapping relationship.

**Working assumption**

For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,

* After supporting entries for multiplexing pattern 1 for the agreed pairs of (, ) ={(24, 2), (48, 1), (48,2)} (with required RB offsets), if additional entries are left, support multiplex pattern 3 with 24 PRB and 2 symbol duration, and multiplexing pattern 3 with 48 PRB and 2 symbol duration.

**Working assumption**

For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,

* After supporting entries for multiplexing pattern 1 for the agreed pairs of (, ) ={(24, 2), (48, 1), (48,2)} (with required RB offsets) and multiplex pattern 3 with 24 and 48 PRB and 2 symbol duration (with required RB offsets), if additional entries are left, support multiplexing pattern 1 with 96 PRB and 2 symbol duration
  + Note: the working assumption can be confirmed once RAN1 agrees on the number of needed SSB-CORESET0 offsets for 24 and 48 RB CORESET0 based on RAN4 channelization design.

**Agreement**

* If is indicated, the same interpretation of ssb-PositionsInBurst in SIB1 or ServingCellConfigCommon as in Rel-16 is supported, i.e.:
  + A bit set to 1 at position indicates SS/PBCH block index k-1
  + The UE assumes that a bit at position k > is set to 0
    - For ssb-PositionsInBurst in SIB1, the UE assumes that a bit at *groupPresence* corresponding to a SS/PBCH block index ≥ is set to 0
  + Note: for ssb-PositionsInBurst in SIB1, position k corresponds to the SS/PBCH block index indicated by a bit in inOneGroup and a bit in groupPresence
* In operation with shared spectrum in 60 GHz, for ssb-PositionsInBurst in ServingCellConfigCommonSIB,
  + for MSB k, k≥1, of inOneGroup and MSB m, m≥1, of groupPresense of ssb-PositionsInBurst:
    - if MSB k of inOneGroup and MSB m of groupPresense are set to 1, the UE assumes that SSB(s) within DBTW with ‘candidate SSB index(es)’ corresponding to ‘SSB index’ equal to k-1+(m-1)×8 may be transmitted;
    - if MSB k of inOneGroup or MSB m of groupPresense is set to 0, the UE assumes that SSB(s) within DBTW with ‘candidate SSB index(es)’ corresponding to ‘SSB index’ equal to k-1+(m-1)×8 is not transmitted;
* In operation with shared spectrum in 60 GHz, for ssb-PositionsInBurst in ServingCellConfigCommon,
  + ssb-PositionsInBurst bits correspond to supported ‘SSB indices’,
    - and UE assumes that SSB(s) within DBTW with ‘candidate SSB index(es)’ corresponding to indicated bit(s) may be transmitted;
    - and UE assumes that SSB(s) within DBTW with ‘candidate SSB index(es)’ corresponding to not indicated bit(s) are not transmitted
* Note to spec editor: The above three bullets maintain the same behavior as Rel-16 NR-U

**Agreement**

Update the Table 6.3.3.2-1 in TS 38.211 as follows:

* Table 6.3.3.2-1: Supported combinations of and , and the corresponding value of .

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | for PRACH | for PUSCH | , allocation expressed in number of RBs for PUSCH |  |
| ... | ... | ... | ... | ... |
| 139 | 120 | 120 | 12 | 2 |
| 139 | 120 | 480 | 3 | 1 |
| 139 | 120 | 960 | 2 | 23 |
| 139 | 480 | 120 | 48 | 2 |
| 139 | 480 | 480 | 12 | 2 |
| 139 | 480 | 960 | 6 | 2 |
| 139 | 960 | 120 | 96 | 2 |
| 139 | 960 | 480 | 24 | 2 |
| 139 | 960 | 960 | 12 | 2 |
| 571 | 120 | 120 | 48 | 2 |
| 571 | 120 | 480 | 12 | 1 |
| 571 | 120 | 960 | 7 | 47 |
| 571 | 480 | 120 | 192 | 2 |
| 571 | 480 | 480 | 48 | 2 |
| 571 | 480 | 960 | 24 | 2 |
| 1151 | 120 | 120 | 97 | 6 |
| 1151 | 120 | 480 | 25 | 23 |
| 1151 | 120 | 960 | 13 | 45 |