**3GPP TSG RAN WG1 Meeting #107-e R1-2112451**

**e-Meeting, November 11 – 19, 2021**

**Source: Moderator (Intel Corporation)**

**Title: Summary #1 of email discussion on initial access aspect of NR extension up to 71 GHz**

**Agenda item: 8.2.1**

**Document for: Discussion**

# Introduction

In this contribution, we summarize discussions aspects related to initial access for extending NR up to 71 GHz based for RAN1 #107-e. The main issues discussed in the following section for initial access are detailed design for synchronization signal block (SSB), CORESET#0, PRACH related issues, and discovery reference signal (DRS) related operations.

# Summary of issues

## 2.1 SSB Aspects

### 2.1.1 DRS Related Aspects (and other MIB design other than CORESET#0/Type0-PDCCH)

* From [1] Huawei/HiSilicon:
  + For SSB with 120 kHz SCS, confirm the working assumption on 64 candidate SSBs within a half frame.
  + For SSB with 480 kHz and 960 kHz SCS, 64 candidate SSBs is sufficient for operation without shared spectrum while 128 candidate SSBs should be supported for operation with shared spectrum.
  + For operation with shared spectrum and for 480 kHz and 960 kHz SSBs, indicate the 7th bit of the candidate SSB index by borrowing the 4th LSB of SFN in the PBCH payload. Indicate the 4th LSB of SFN with spare bit in MIB payload.
  + Confirm the working assumption to support DBTW for 120 kHz and further support DBTW for 480 kHz and 960 kHz SSB.
  + At least should be indicated in MIB for all three numerologies.
  + UE should be able to identify DBTW enable/disable before acquiring SIB1. A specific entry of in MIB should be reserved to disable DBTW if the number of candidate SSB positions is larger than 64 for 480 kHz and 960 kHz SCS.
  + Configure DBTW length in SIB1 for operation with shared spectrum in 52.6GHz to 71GHz with the following values:
    - 480 kHz SCS: {72, 32, 24, 16, 8, 4} slots = {2.25, 1, 0.75, 0.5, 0.25, 0.125} ms
    - 960 kHz SCS: {64, 32, 24, 16, 8, 4} slots = {1, 0.5, 0.375, 0.25, 0.125, 0.0625} ms
  + The MIB content and PBCH payload in Table [1]-5 and Table [1]-6 should be supported for 120 kHz, 480 kHz and 960 kHz SSB.
    - Table [1]-5 uses subCarrierSpacingCommon and pdcch-ConfigSIB1 for Q
    - Table [1]-6 uses subCarrierSpacingCommon and pdcch-ConfigSIB1 for Q, 1 spare bit for 4th LSB of SFN, 4th LSB of SFN for 7th candidate SSB index.
* From [3] vivo:
  + The number of candidate SSBs for 480/960KHz should be increased into 128.
  + Support DBTW for 480/960KHz SSB in unlicensed operation from 52.6GHz to 71GHz.
  + Whether or not to indicate licensed regime by different synchronization raster entries is depending on the RAN 4 synchronization raster design.
  + Support to use DBTW lengths {0.5, 1, 2, 3, 4, 5} msec for SCS 120 kHz, and the maximum DBTW length for SCS 480 kHz and 960 kHz should be 1.25ms and 0.625ms when the number of candidate SSBs is 64, 2.5ms and 1.25ms in unlicensed scenario the number of candidate SSBs is 128.
* From [4] ZTE/Sanechips
  + Confirm the working assumption:
    - Support DBTW for 120 kHz, 480 kHz and 960 kHz.
  + In order to reduce the impact of standardization caused by indicating candidate SSB indices, the maximum number of candidate SSBs defined in the half-frame can be kept unchanged (maintain 64) or limited to 128 for 480/960 kHz SSB SCS.
  + Four candidate values {8,16,32,64} for and two bits for the indication are preferred.
  + For Rel-17 above 52.6GHz, it is recommended that the UE derives the QCL relation between candidate SSBs by the value of , where is the candidate SSB index.
  + For 480 kHz and 960 kHz SCS, if DBTW and 64 SSB candidate positions are supported, the same mechanism for DBTW operation as 120 kHz can be adopted.
    - Value <64 indicates DBTW enabled/supported and operation with shared spectrum.
    - For operation without shared spectrum channel access, a UE expects to be configured with =64.
    - If =64, DBTW can be seen as disabled as the effect of DBTW enabled is the same as DBTW disabled
  + For 480 kHz and 960 kHz SCS, if DBTW and 128 SSB candidate positions are supported, the following DBTW operation can be considered.
    - Value <64 indicates DBTW enabled/supported and operation with shared spectrum.
    - For operation without shared spectrum channel access, a UE expects to be configured with =64.
    - If =64, enable/disable of DBTW can be implicitly indicated by comparing the value of  in MIB and DBTW length
* From [5] Spreadtrum
  + Confirm the working assumption that DBTW is supported for 120kHz SCS.
  + DBTW is supported for 480/960kHz SCS.
  + DBTW length for 480/960kHz can be {4, 8, 16, 24, 32, 40} slots.
  + Confirm the working assumption that the number of candidate SSBs in a half frame is 64 for 120kHz SCS.
  + The number of candidate SSBs in a half frame is more than 64 and not great than 128 for 480/960kHz SCS.
* From [7] Nokia/NSB
  + The design for DBTW, if supported, is common to different sub-carrier spacings.
  + For 480kHz and 960kHz, the number of SSB candidate locations in a half frame is 64.
  + If DBTW is supported,  are supported. subCarrierSpacingCommon and spare-bit are used for indication of . implies that DBTW is not assumed.
  + If DBTW is supported, the supported values for discoveryBurstWindowLength are same as used for Rel-16 NR-U also for 480kHz and 960kHz: 0.5, 1, 2, 3, 4, 5 ms
* From [8] CATT
  + The work assumption of support DBTW for 120 kHz is confirmed.
  + To increase the number of actual SSB transmission, sub-set of SSBs can be transmitted as NO-LBT and the other sub-set SSBs are transmitted as DBTW if the exempt Short Control Signaling rules can be applied by local region rule.
  + DBTW for 480/960 kHz SSB SCS can be supported with up to 128 candidate SSB index.
  + To indicate 7th bit of the candidate SSB index for 480/960 kHz SSB SCS, following schemes can be further considered and down-selected:
    - Borrowing the subCarrierSpacingCommon in MIB
    - Borrowing the 4th LSB of SFN, and move 4th LSB of SFN to subCarrierSpacingCommon in MIB
    - Borrowing half frame bit  , with all candidate SSBs are assumed to be put in first half frame when DBTW is enabling.
  + On DBTW length for SCS 480/960 KHz (if supported), scale factor is applied comparing to value of SCS 120 KHz,
  + 2 bits used for ，and four states {16, 32, 64, reserved/DBTW disabled} is recommend.
* From [10] Sony
  + Discovery Burst Transmission Window should be supported for all SCSs.
  + 2 bits should be supported for indication of
    - values should support {8, 16, 32, 64}
* From [11] Ericsson
  + Support DBTW for 120/480/960 given that 1) no additional (compared to the already supported 64) candidate SS/PBCH block positions are introduced and 2) a common design (e.g. value range of Q, DBTW length, repurposed bits etc.) for all SCS is used.
  + Q is signaled by repurposing subCarrierSpacingCommon (1 bit) for 120/480/960 kHz SCS.
  + If RAN1 decides to use two bits to signal Q (not our preference) add either 24 or 48 as a value of Q for 120/480/960 kHz SCS.
  + The value range for Q is the same for 120/480/960 kHz SCS.
  + The value range for the DBTW length is the same for 120/480/960 kHz SCS.
* From [12] Intel
  + For DRS based on SSBs with SCS 120 kHz:

    - is indicated in MIB
      * At least the subCarrierSpacingCommon bit from MIB is reinterpreted to indicate
      * Consider 1 bit from pdcch-ConfigSIB1 in MIB to indicate from the extended set, e.g.,
        + Alternatively, the spare bit from PBCH payload could be used to indicate in addition to the subCarrierSpacingCommon bit from MIB
    - DBTW on/off is identified based on comparison of the DBTW length with the time duration occupied by transmission of SSBs
    - DBTW length is signalled in SIB1
  + For DRS based on SSBs with SCS 480 kHz/960 kHz:
    - and SSB candidate slots are arranged according to Proposal 2
    - One bit from MIB is used for indexing additional SSB candidates
      * The subCarrierSpacingCommon bit from MIB is reinterpreted for this purpose
    - is indicated in MIB
      * One bit from pdcch-ConfigSIB1 in MIB is repurposed to indicate at least
      * The spare bit from PBCH payload could be used to indicate in addition to 1 bit from pdcch-ConfigSIB1 in MIB
    - DBTW length is fixed and not signalled
    - DBTW on/off is explicitly signalled in SIB1
* From [14] NEC
  + Confirm the working assumption that Support DBTW for 120 kHz.
  + DBTW should be supported for 480kHz and 960 kHz SCS.
  + If DBTW is supported for 480/960kHz SCS SSB transmission, 128 SSB candidates should be supported.
  + The long term sensing could be considered as an approach to enabling/disabling DBTW.
  + For the value set of Q, {16, 32, 64} should be supported, namely 2 bits are needed for Q value indication.
  + Confirm the working assumption about parameters related to operation of DBTW for SCS that DBTW is supported.
* From [15] Samsung
  + Support discovery burst transmission window for all SCSs on the 60 GHz unlicensed spectrum.
    - The indication of Q can be in MIB for a best effort, and if not possible, in SIB1;
    - For 480 kHz and 960 kHz SCS, support 128 candidate SS/PBCH block locations within a half frame, and use one PHY bit in PBCH payload to indicate the extra candidate SS/PBCH block index (e.g. 7th LSB);
    - If supporting more than 64 candidate SS/PBCH block locations, support DBTW off indication jointly coded with 3 numerical values of Q.
* From [16] Panasonic
  + DBTW is supported for 480 and 960 kHz and supports 64 candidate SSB positions. If 128 candidate SSB positions are required, the signaling method needs to be clarified.
  + For 480/960 kHz, DBTW lengths scaled from 120 kHz are baseline.
  + For for 480/960 kHz SCS, the same indication and values as 120 kHz SCS are supported at least for the case where 64 candidate SSB positions are supported.
  + For the indication of , 4 states (2 bits) are supported.
* From [17] Interdigital
  + Support Discovery Burst Transmission Window (DBTW) for SCS 120kHz, 480kHz, and 960kHz in shared spectrum operations that require LBT to enhance the initial access operation in beyond 52.6GHz spectrum.
  + Support using the combination of 1 bit from subCarrierSpacingCommon, and 1 bit from pdcch-ConfigSIB1 to indicate the DBTW parameters.
  + For SCS 120kHz, 480kHz, and 960kHz, if 2 bits are available in MIB for , below table can be used to indicate DBTW enabled/disabled along with the parameter, while supporting up to 128 candidate SSB positions:

|  |  |  |  |
| --- | --- | --- | --- |
| *1st bit* | *2nd bit* | *Codepoint* | *Description* |
| *0* | *0* | *00* | *DBTW is disabled* |
| *0* | *1* | *01* | *- DBTW is enabled and .*  *- 2nd bit is used to indicate the 7th bit for SSB candidate indexes.* |
| *1* | *0 or 1* | *10 or 11* | *- DBTW is enabled and .*  *- 2nd bit is used to indicate the 7th bit for SSB candidate indexes.* |

* + Support candidate SSB positions more than 64 for SCS 120kHz, 480kHz, and 960kHz.
* From [19] ETRI
  + Support DBTW for all SSB SCSs.
  + Support 64 SSB candidate positions for all SCS as the first priority, however also can live with 128 SSB candidate positions if the one bit for SSB index is available.
* From [20] Sharp
  + Confirm the working assumption on supporting DBTW for 120kHz. In addition, support DBTW for SSB with 480 or 960 kHz SCS in FR2-2 operation.
  + Support 128 candidate SSBs for 480 or 960 kHz SCS in FR2-2 operation.
  + For 120 kHz SCS, use 1 MIB payload bit to indicate Q values of {16, 32, 64}. For 480 kHz/960kHz SCS supporting 120 candidate SSBs, use 1 MIB payload bit to indicate Q values of {32, 64, 128}. The full indication for Q and DBTW enabled/disabled can be complemented by SIB1.
* From [21] Convida Wireless
  + If impact of LBT failure is not addressed, increasing the number of SSB candidate positions to larger than 64 e.g., 128 to increase transmission opportunities to cope with LBT failure could be considered.
  + Increased number of candidate SSB positions larger than 64, e.g., 128 for shared spectrum channel access for SCSs of 480KHz and 960KHz for 52.6 GHz-71 GHz.
  + Support DBTW for SCS 120kHz, 480kHz and 960kHz in shared spectrum operations for 52.6 GHz-71 GHz.
* From [22] LGE
  + Confirm the following working assumption made in RAN1#106-e.
    - For 120kHz SSB, the number of candidates SSBs in a half frame is 64.
  + Confirm the following working assumption made in RAN1#106bis-e.
    - Support DBTW for 120 kHz.
  + If DBTW is supported for 480 kHz and 960 kHz SSB, the number of candidates SSBs in a half frame is 64 for all SCSs in FR2-2.
  + Total of 4 states (i.e., {8, 16, 32, 64}) of values are supported by using 2 bits in MIB of the followings.
    - subCarrierSpacingCommon
    - spare-bit (not the Msg Extension bit)
* From [23] NTT Docomo
  + DBTW should be supported irrespective of SCS, i.e., confirm the WA on the support of DBTW without any restriction on SCS.
    - In a certain region, e.g., Japan, sensing needs to be performed for initiating any transmission by any device in 60 GHz.
  + Support to confirm the working assumption that the number of candidate SSB positions with 120 kHz SCS in a half frame is 64
  + On the number of candidate SSB positions:
    - Prefer to support 64 candidate SSB positions for both 480 and 960 kHz SCS
    - Fine to support 128 candidate SSB positions for 480 and 960 kHz SCS, if and only if it is achieved by the limited amount of specification impacts
  + For DBTW to be supported in Rel-17 NR 52.6 – 71 GHz, similar to Rel-16 NR-U, support to indicate QCL parameter in MIB
    - Regardless of the number of candidate SSB positions, support to use only subCarrierSpacingCommon for DBTW related parameter indication in MIB
* From [24] Qualcomm
  + if DBTW is supported for 480 kHz/960 kHz SSB, use 64 candidate SSB positions
  + for 120kHz SCS, consider using only 1 bit in MIB to indicate the , where:
    - ∈ {32, 64}
    - subCarrierSpacingCommon is used to signal the 1 bit for
  + for SCS 480 and 960 kHz, do not support discovery burst transmission window (DBTW) for SSB
  + for operation with shared spectrum, modify the QCL derivation equation to (), where is the candidate SSB index
* From [25] Mediatek
  + RAN 1 to clarify the support of DBTW for 120 kHz SCS.
* From [26] WILUS
  + It should be confirmed to support discovery burst transmission window (DBTW) for at least 120kHz SCS. In addition to 120kHz SCS, DBTW should be applicable for 480/960 kHz SSB SCS on supporting NR above 52.6GHz.

#### Summary of Discussions

The following is a summary of company position of various aspects of DRS.

* Confirm WA
  + DBTW for 120kHz
    - Huawei/HiSilicon, Spreadtrum, CATT, NEC, Sharp, LGE
  + 64 candidates for 120kHz
    - Huawei/HiSilicon, LGE
* Supporting DBTW for 480/960 kHz
  + Support: Huawei/HiSilicon, vivo, ZTE/Sanechips, Spreadtrum, CATT, Sony, NEC, Samsung, Panasonic, [Nokia/NSB (conditioned on supporting 64 candidate SSB)], Ericsson (conditioned on supporting 64 candidate SSB), Interdigital, ETRI, Sharp, Convida Wireless, LGE (conditioned on supporting 64 candidate SSB), NTT Docomo, WILUS
  + Not Support: Qualcomm
* Number of SSB candidates for DBTW
  + 64: Huawei/HiSilicon (licensed), Nokia/NSB, Panasonic, ETRI (1st preference), Docomo (1st preference), Qualcomm
  + 128: Huawei/HiSilicon (unlicensed), vivo, [ZTE/Sanechips], [Spreadtrum], CATT, Intel, NEC, Samsung, Interdigital, ETRI (2nd preference), Convida Wireless, Docomo (2nd preference)
* SSB index indication for 7th SSB index bit (if >64 candidate SSB)
  + use 4th LSB of SFN, (4th LSB of SFN moves to MIB)
    - Huawei/HiSilicon, CATT, Samsung
  + subCarrierSpacingCommon
    - CATT, Intel
  + Use half frame bit (assume SSB are always in first half radio frame)
    - CATT
* Supported values:
  + 1 bit {32, 64}: Ericsson, [Docomo?], Qualcomm (for 120kHz)
  + 1 bit {16, 64} (different from RAN1 agreement): Intel
  + 2 bits, {16, 32, 64} : Huawei/HiSilicon, NEC, Samsung
  + 2 bits, {8,16,32,64} : ZTE/Sanechips, Nokia/NSB, CATT, Sony, Intel, LGE
  + 2 bits: Panasonic
  + 2 bits {32, 64}: Interdigital (2 bit is re-used to indicate 7th bit of SSB index)
    - 00 : DBTW disable (or Q=64 with SSB in first 64 candidate position)
    - 01 : Q=64, SSB in second SSB position)
    - 10 : Q=32, SSB in first 64 SSB position
    - 11 : Q=32, SSB in second 64 SSB position
  + 1 bit {16, 32, 64} : Sharp
    - UE assumes 32 or 64 depending on indication
    - IF Q=32 is indicated, UE performs double hypothesis (Q=16 and 32) during PDCCH monitoring
    - gNB uses 16 or 32 when indicated as 32, 64 when indicated as 64
* Indication of DBTW
  + Explicit disable indication: Huawei/HiSilicon (if >64 candidate SSB), Samsung (assuming 128 candidate SSB)
  + Q=64 can be understood as disabled : ZTE/Sanechips, Nokia/NSB
* Signaling bits used for DBTW operation
  + subCarrierSpacingCommon and 1 bit from pdcch-ConfigSIB1 : Huawei/HiSilicon (for 120kHz), Intel, Interdigital
  + subCarrierSpacingCommon, 1 bit from pdcch-ConfigSIB1, spare bit : Huawei/HiSilicon (for 480/960 kHz), Intel (for 2 bit Q)
  + subCarrierSpacingCommon and spare bit: Nokia/NSB, Intel (for 120kHz), LGE
  + subCarrierSpacingCommon: Intel, Docomo, Qualcomm
* Supported DBTW lengths for 480/960 kHz (if supported)
  + For 480kHz:
    - {2.25, 1, 0.75, 0.5, 0.25, 0.125} ms : Huawei/HiSilicon
    - Max 1.25ms or 2.5ms (depending on 64 or 128 candidate SSB): vivo
    - {4, 8, 16, 24, 32, 40} slots : Spreadtrum
    - {0.5, 1, 2, 3, 4, 5} ms : Nokia/NSB, Ericsson
    - Scaled of 120kHz case : CATT
    - Single value: Intel
  + For 960kHz:
    - {1, 0.5, 0.375, 0.25, 0.125, 0.0625} ms : Huawei/HiSilicon
    - Max 0.625ms or 1.25ms (depending on 64 or 128 candidate SSB): vivo
    - {4, 8, 16, 24, 32, 40} slots : Spreadtrum
    - {0.5, 1, 2, 3, 4, 5} ms : Nokia/NSB, Ericsson
    - Scaled of 120kHz case : CATT
    - Single value: Intel
* QCL derivation
  + UE derives the QCL relation between candidate SSBs by the value of , where is the candidate SSB index
    - ZTE/Sanechips, Qualcomm

#### [ACTIVE] 1st Round Discussion

Discuss further on the following proposals and issues.

##### Issue #1) confirming WA

Companies should had time to review the Working assumptions made, it would be good to confirm the working assumption. If not agreeable, companies should present critical reasons why it should not be confirmed.

###### Proposal 1.1-1

* Confirm WA of the following:
  + (From #106-bis-e) Support DBTW for 120 kHz.
  + (From #106-e) For 120kHz SSB, the number of candidates SSBs in a half frame is 64.

##### Issue #2) Whether or not to support DBTW and number of SSB candidates

Great majority of the companies support DBTW for 480 and 960 kHz. We could try to make some progress here. Some companies stated that they are only supportive of DBTW for 480 and 960 kHz if RAN1 supports 64 SSB candidates. So we may need to discuss the support of DBTW and number of SSB candidates together.

###### Proposal 1.1-2

* Support DBTW for SSB with 480 and 960 kHz SCS.

In terms of support for 64 vs 128 candidate positions for SSB with 480 and 960 kHz (unlicensed operation), the following is a summary:

* 64 candidates: 6 companies
* 128 candidates: 12 companies (excluding companies who listed 128 as 2nd preference)

While there seems to be larger number of support for 128 candidates, moderator suspects discussions are needed. Moderator has formulated Proposal 1.1-2A and 1.1-2B.

###### Proposal 1.1-2A

* For unlicensed operation, support 64 candidate SSB positions within DBTW.

###### Proposal 1.1-2B

* For unlicensed operation, support 128 candidate SSB positions within DBTW.

##### Issue #3) SSB index indication for max 128 candidates SSB (if supported)

If 128 candidate SSB positions are supported, RAN1 needs to resolve how to indicate the signaling for the 7th SSB index bit. So far, three options has been presented.

Option 1) use 4th LSB of SFN (the 4th LSB of SFN will move to MIB, using one of the leftover bits)

Option 2) subCarrierSpacingCommon

Option 3) use half radio frame bit (SSB are only carried in the first half radio frames)

Please comment further on which options is acceptable if 128 candidates SSB positions are supported.

###### [draft] Proposal 1.1-3

* [Moderator to suggest proposal based on company feedback]

##### Issue #4) Indication of DBTW &

Moderator assumes if only 64 candidate SSBs are supported then same signaling will be applied to 120, 480, and 960 kHz. If 128 candidate SSBs are supported, there may need to be discussion on whether same or different number of values are to be supported for 120kHz and 480/960kHz, respectively.

Moderator has drafted few options for proposals based on comments received. The main issues that requires resolutions are:

* Number of bits for Q
* Whether same number of bits for Q for 120 and 480/960kHz
* Which bits are used to convey Q

Please comment further on the issues above, based on it moderator will update proposal 1.1-4, 1.1-4A, and/or 1.1-4B.

###### [draft] Proposal 1.1-4

* For 480 and 960kHz, if DBTW is supported and 64 candidate SSB position are supported,
  + Same values using the same set of signaling bits are supported for 120, 480, and 960 kHz.
  + Supported values of : {8,16, 32, 64}
    - =64 is also used to indicate disable of DBTW by gNB
    - UE is expected to be configured with =64 in licensed operations
  + 2 bits required for are taken from
    - subCarrierSpacingCommon
    - [spare bit (note: not the MIB extension bit)]
      * *Moderator to update the second bit based on company feedback*

###### [draft] Proposal 1.1-4A

* For 480 and 960kHz, if DBTW is supported and 128 candidate SSB position are supported,
  + Supported values of for 120 kHz: {[8],16, 32, 64}
    - =64 is also used to indicate disable of DBTW by gNB
    - UE is expected to be configured with =64 in licensed operations
  + Supported values of for 480 and 960 kHz: {16, 32, 64}
    - 1 state of is used to indicate disable of DBTW
    - UE is expected to be configured with disable of DBTW in licensed operations
    - UE does not expect SSB index to be for the second set of 64 candidates SSB positions (i.e. 7th SSB index bit set to 1) in licensed operations
  + 2 bits required for are taken from
    - subCarrierSpacingCommon
    - [spare bit (note: not the MIB extension bit)]
      * *Moderator to update the second bit based on company feedback*

###### [draft] Proposal 1.1-4B

* For 480 and 960kHz, if DBTW is supported and 128 candidate SSB position are supported,
  + Supported values of for 120, 480, and 960 kHz: {32, 64}
    - =64 is also used to indicate disable of DBTW by gNB
    - UE is expected to be configured with =64 in licensed operations
    - For 480 and 960 kHz, if SSB index is for second set of 64 candidate SSB position (i.e. 7th SSB index bit set to 1), UE may assume DBTW is enabled.
    - For 480 and 960 kHz, UE does not expect SSB index to be for the second set of 64 candidates SSB positions (i.e. 7th SSB index bit set to 1) in licensed operations
  + 1 bits required for are taken from
    - [spare bit (note: not the MIB extension bit)]
      * *Moderator to update the second bit based on company feedback*

##### Issue #5) DBTW lengths for 480/960 kHz

Company views are somewhat split on the supported DBTW lengths. Few companies prefer to keep the same as 120kHz cases, few companies prefer to scale the DBTW lengths accordingly. One company prefers to have single window as the total duration for DBTW is small.

There seems to be no clear option that has majority support. Companies advocated for scaling the length to account for reduction in total time duration for SSB, keeping same length between different SCS. Given that having certain measurement/processing window lengths that are too small in time isn’t great for implementation. Moderator has put a suggest potentially compromise proposal 1.1-5, that has not been proposed any company. Please comment further whether this is ok. If not please, suggest alternative proposals that you believe could be acceptable by all.

###### Proposal 1.1-5

* If DBTW is supported for 480 and 960 kHz, supported DBTW lengths are:
  + {2.25, 1, 0.75, 0.5, 0.25, 0.125} ms

##### Issue #6) QCL derivation

For the for QCL derivation when DBTW is used, it looks like agreement to re-use the NR-U like approach was not agreed. Few companies proposed to agree on this as well. Moderator has formulated proposal 1.1-6 based on suggestions from the companies.

###### Proposal 1.1-6

* For SCS that support DBTW, UE derives the QCL relation between candidate SSBs by the value of , where is the candidate SSB index.

##### Company Comments/Inputs

|  |  |
| --- | --- |
| Company | Comments |
|  |  |

#### <Summary of 1st Round Discussion>

*[To be filled by moderator]*

### 2.1.2 SSB Resource Pattern

* From [1] Huawei/HiSilicon:
  + Support following patterns (ALT C) for SSB with 480 kHz and 960 kHz SCS:
    - For operations without shared spectrum:
      * {2,9}+14n, (n=0,1,2,…,31) for both 480 kHz and 960 kHz SCS.
    - For operations with shared spectrum:
      * {2,9}+14n, (n=0,1,2,…,31,40,…,71) for 480 kHz SCS;
      * {2,9}+14n, (n=0,1,2,…,63) for 960 kHz SCS.
* From [2] Futurewei:
  + For SS/PBCH transmission at 480kHz and respectively 960kHz use the same gaps as in SCS 120 kHz, i.e. (Alt C) slots that do not contain SSB correspond to the slots that do not contain SSB in 120 kHz Case D.
* From [3] vivo
  + Support non-contiguous slot pattern for 480/960KHz SSB to reserve time for UL transmission, i.e. ALT A (1st preference) and ALT B (2nd preference).
* From [4] ZTE/Sanechips:
  + The ALT B (N=2, M=8) for 480/960 kHz SSB slot pattern design in a half frame should be supported: First symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
    - If DBTW is not supported or DBTW is disabled
      * For 480kHz SCS, 64 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, (gap) 10,11,12,13, 14,15,16,17, (gap) 20,21,22,23, 24,25,26,27, (gap) 30,31,32,33, 34,35,36,37}
      * For 960kHz SCS, 64 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, (gap) 20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35}
    - If DBTW is supported and it is enabled
      * Additional 64 candidate SSB can be defined after the above original 64 candidate SSBs in the half frame
* From [5] Spreadtrum
  + Support ALT C) for slot pattern for 480/960kHz SSB.
* From [7] Nokia/NSB:
  + Define SSB slot pattern for 480kHz and 960kHz sub-carrier spacing so that 8 consecutive slots are contain SSB candidate locations, followed by 4 slots are left unoccupied (by SSBs), until all SSBs locations are accounted. Determine the slot indexes n for candidate locations as follows:
    - The slot indexes n={0,1,2,3,4,5,6,7,
    - 12,13,14,15,16,17,18,19,
    - 24,25,26,27,28,29,30,31,
    - 36,37,38,39,40,41,42,43}
* From [8] CATT
  + 480/960kHz SSB slot pattern, ALT B is preferred:
    - ALT B) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB, scaled version pattern will apply between 480 and 960 kHz (i.e. N and M for 480kHz, 2N and 2M for 960 kHz), N = 2, M = 8
* From [9] OPPO
  + Support ALT A) or ALT B), i.e., non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB.
* From [11] Ericsson
  + For operation with 480kHz and 960kHz sub-carrier spacing, support an SSB pattern according to Alt C.
* From [12] Intel
  + Consider SSB pattern in a slot with 8 SSB containing slots, each slot with 2 SSB position, followed by 2 non-SSB carrying slots for 480 kHz and 960kHz. Supported value of n for 480/960kHz SSB slot pattern is
    - n = {0,1,2,3,4,5,6,7, 10,11,12,13,14,15,16,17, 20,21,22, 23,24,25,26,27, 30,31,32,33,34,35,36,37}, {40, 41,42, 43,44,45,46,47, 50,51,52,53,54,55,56,57, 60,61,62, 63,64,65,66,67, 70,71,72,73,74, 75,76,77}.
    - The second set of n values could be used to enable larger number of candidate SSBs, i.e.,
* From [15] Samsung
  + For 480 kHz and 960 kHz, support (Alt C in the previous agreement):
    - for 480 kHz SCS and operation without shared spectrum channel access;
    - for 480 kHz SCS and operation with shared spectrum channel access;
    - for 960 kHz SCS and operation without shared spectrum channel access;
    - for 960 kHz SCS and operation with shared spectrum channel access.
* From [16] Panasonic
  + For SSB slot pattern for 480/960 kHz, N slot gap (slots that do not contain SSB) every M slot that contain SSB are supported (i.e., ALT A or ALT B agreed in RAN1#106bis-e).
* From [17] Interdigital
  + Support using gap slots in Case D SSB pattern in SCS 120kHz for the candidate SSB positions, wherein multiple subsets of candidate SSB indexes per gap slot are considered.
  + In SCS 120kHz, the SSB pattern in gap slots for the candidate SSB positions can be different from Case D SSB pattern to allow more number of candidate SSB positions per gap slot.
  + Consider a combination of Alt. B and Alt. C, where the gaps slots corresponding to 120kHz gap slots are preserved, e.g., gap slots 32-39 for 480 kHz SSB.
* From [18] Apple
  + Reserve 2 slots for UL transmissions every 8 consecutive slots that contains SSB for both 480kHz SCS and 960kHz SCS.
* From [19] ETRI
  + Support ALT B) for SSB patterns.
    - ALT B) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB
      * *scaled version pattern will apply between 480 and 960 kHz (i.e. N and M for 480kHz, 2N and 2M for 960 kHz)*
      * *N = 2, M = 8*
      * *starting position of n = 0*
* From [20] Sharp
  + Regarding supported value of n for 480/960kHz SSB slot pattern, our first preference is ALT C and second preference is ALT B.
* From [22] LGE
  + For 480/960 kHz SSB, first symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame (as per agreement in RAN1#106-e), and values of ‘n’ are consecutive integers (i.e., n = 0, 1, 2, …, 31), which is ALT C of agreement in RAN1#106bis-e.
* From [23] NTT Docomo
  + For 480/960 kHz SSB slot pattern, slightly prefer ALT C
* From [24] Qualcomm
  + for 480 kHz/960 kHz SSB pattern, support the following alternative:
    - ALT B) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB
    - scaled version pattern will apply between 480 and 960 kHz (i.e. N and M for 480kHz, 2N and 2M for 960 kHz)
    - N = 2, M = 8
    - Starting position of n = 0
* From [25] Mediatek
  + For SSB pattern of 480 and 960 kHz SCS, support Alt A.
* From [26] WILUS
  + We support Alt-C as SSB slot pattern for 480/960kHz SCS, i.e., slots that do not contain SSB correspond to the slots that do not contain SSB in 120 kHz Case D.

#### Summary of Discussions

Among the three alternatives agreed in last meeting, summary of company views are as follows:

* ALT A) non-contiguous, N=2 slot gap (slots that do not contain SSB) every M=8 slots that contain SSB for 480/960 kHz
  + vivo (1st preference), OPPO, Intel, Panasonic, Apple, Mediatek
* ALT B) non-contiguous, N=2,4 slot gap (slots that do not contain SSB) every M=8,16 slots that contain SSB for 480 and 960, respectively.
  + Vivo (2nd preference), ZTE/Sanechips, CATT, OPPO, Panasonic, ETRI, Sharp (2nd preference), Qualcomm
* ALT C) slots that do not contain SSB correspond to the slots that do not contain SSB in 120 kHz Case D.
  + Huawei/HiSilicon, Futurewei, Spreadtrum, Ericsson, Samsung, Sharp (1st preference), NTT Docomo, WILUS
* non-contiguous, N=4 slot gap (slots that do not contain SSB) every M=8 slots that contain SSB for 480/960 kHz.
  + Nokia/NSB
* non-contiguous, N=2,4 slot gap (slots that do not contain SSB) every M=8,16 slots that contain SSB for 480 and 960, respectively, and slots that overlap with slots not occupied case D SSB pattern are also unoccupied by SSB (ALT B + C)
  + Interdigital

#### [ACTIVE] 1st Round Discussion

Alt C is preferred by the most number of companied followed by Alt B. Moderator suggests trying to discuss around Alt B or C. Moderator would like to ask companies who preferred other alternatives, whether they would be ok to accept Alt B and/or Alt C.

Discuss further on the following proposal.

##### Proposal 1.2-1

* ALT B)
  + For 480 kHz, slot index, n, that contain SSB are:
    - If 64 candidate SSB, n = {0,1,2,3,4,5,6,7, (gap) 10,11,12,13,14,15,16,17, (gap) 20,21,22,23,24,25,26,27, (gap) 30,31,32,33,34,35,36,37}
    - If 128 candidate SSB, n = {0,1,2,3,4,5,6,7, (gap) 10,11,12,13,14,15,16,17, (gap) 20,21,22,23,24,25,26,27, (gap) 30,31,32,33,34,35,36,37}, (gap) {40,41,42,43,44,45,46,47, (gap) 50,51,52,53,54,55,56,57, (gap) 60,61,62,63,64,65,66,67, (gap) 70,71,72,73,74, 75,76,77}
  + For 960 kHz, slot index, n, that contain SSB are:
    - If 64 candidate SSB, n = {0,1,2,3,4,5,6,7, 8,9,10,11,12,13,14,15, (gap) 20,21,22,23,24,25,26,27, 28,29,30,31,32,33,34,35}
    - If 128 candidate SSB, n = {0,1,2,3,4,5,6,7, 8,9,10,11,12,13,14,15, (gap) 20,21,22,23,24,25,26,27, 28,29,30,31,32,33,34,35}, (gap) {40,41,42,43,44,45,46,47, 48,49,50,51,52,53,54,55, (gap) 60,61,62, 63,64,65,66,67, 68,69,70,71,72,73,74,75}

##### Proposal 1.2-1A

* ALT C)
  + For 480 kHz, slot index, n, that contain SSB are:
    - If 64 candidate SSB, n = {0,1,2,3,4,5,6,7, 8,9,10,11,12,13,14,15, 16,17,18,19,20,21,22,23, 24,25,26,27,28,29,30,31}
    - If 128 candidate SSB, n = {0,1,2,3,4,5,6,7, 8,9,10,11,12,13,14,15, 16,17,18,19,20,21,22, 23, 24,25,26,27,28,29,30,31}, (gap) {40,41,42,43,44,45,46,47, 48,49,50,51,52,53,54,55, 56,57,58,59,60,61,62,63, 64,65,66,67,68,69,70,71}
  + For 960 kHz, slot index, n, that contain SSB are:
    - If 64 candidate SSB, n = {0,1,2,3,4,5,6,7, 8,9,10,11,12,13,14,15, 16,17,18,19,20,21,22,23, 24,25,26,27,28,29,30,31}
    - If 128 candidate SSB, n = {0,1,2,3,4,5,6,7, 8,9,10,11,12,13,14,15, 16,17,18,19,20,21,22,23, 24,25,26,27,28,29,30,31}, {32,33,34,35,36,37,38,39, 40,41,42,43,44,45,46,47, 48,49,50,51,52,53,54,55, 56,57,58,59,60,61,62,63}

##### Company Comments/Inputs

|  |  |
| --- | --- |
| Company | Comments |
|  |  |

#### <Summary of 1st Round Discussion>

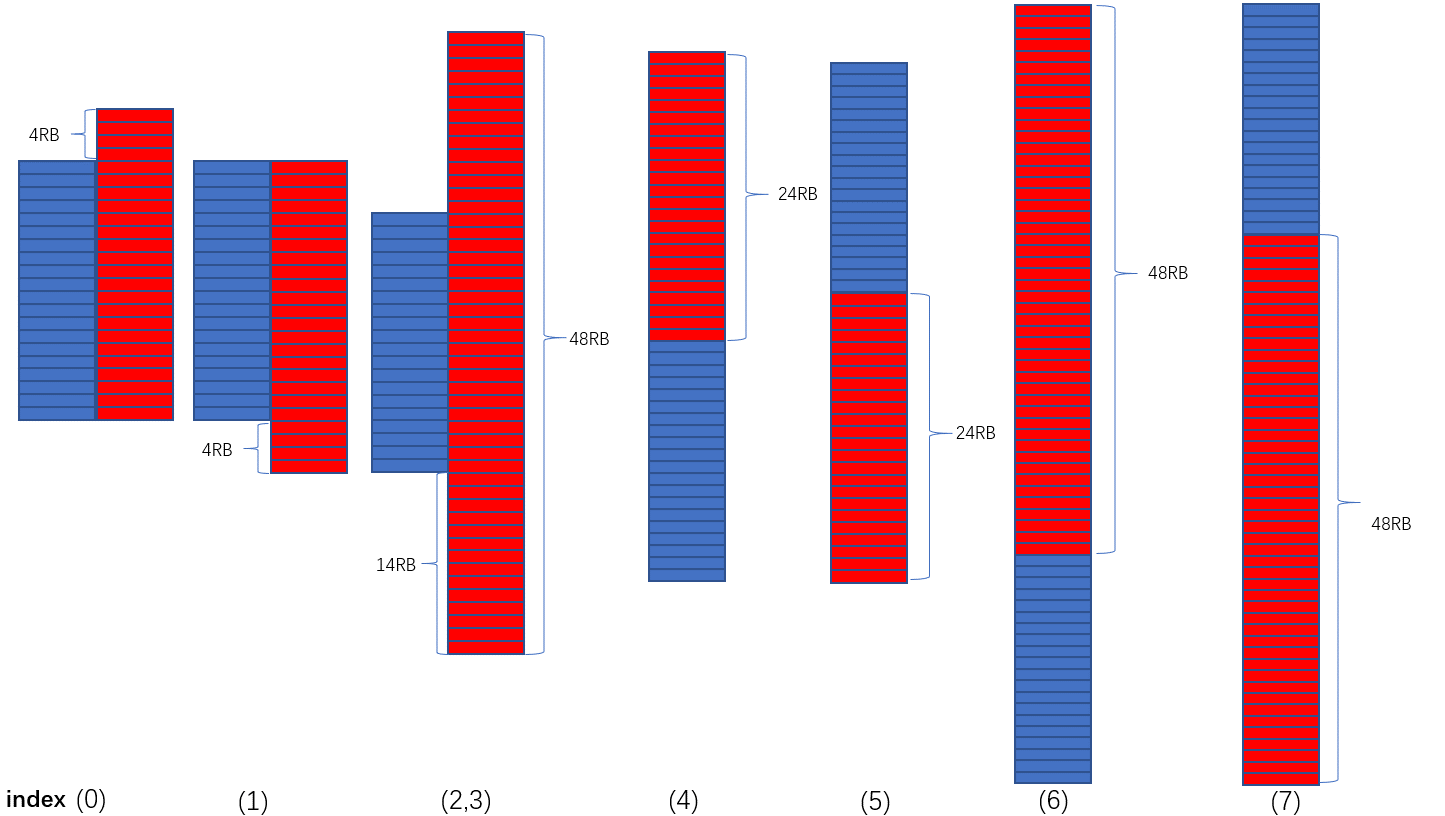
*[To be filled by moderator]*

### 2.1.3 CORESET#0/SS#0 Configuration

* From [1] Huawei/HiSilicon:
  + For CORESET for Type0-PDCCH in 52.6GHz to 71GHz spectrum, support the following:
    - For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {120, 120} kHz, support multiplexing pattern 1 and multiplexing pattern 3 as per Agreement in RAN1 104-e.
    - For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {480, 480} kHz, support multiplexing pattern 1 only.
    - For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {960, 960} kHz, support multiplexing pattern 1 only.
  + Support the following CORESET#0 RB offsets values for {SSB, CORESET#0} SCS={120, 120} kHz:
    - For CORESET#0 with 24 RBs and 48 RBs: the same as supported values in Table 13-8 of 38.213.
    - For CORESET#0 with 48 RBs: additional RB offsets values of 0 and 28 RBs can be considered for multiplexing pattern 1.
    - For CORESET#0 with 96 RBs: RB offsets values of 0 and 76 RBs can be considered for multiplexing pattern 1.
    - Note: All above RB offsets are nominal and may need to be modified after finalizing synch raster and channel raster design in FR2-2.
  + Support the following CORESET#0 RB offsets values for {SSB, CORESET#0} SCS={480, 480} kHz and {960, 960} kHz:
    - For CORESET#0 with 24 RBs: the same as supported values in Table 13-8 of 38.213.
    - For CORESET#0 with 48 RBs: In addition to the offset of 14 RBs already supported in Rel-16, additional values of 0 and 28 RBs can be considered for multiplexing pattern 1.
  + The parameters for PDCCH monitoring occasions for Type0-PDCCH CSS set - SS/PBCH block and CORESET multiplexing pattern 1 with {120, 120} kHz in Table [1]-3should be supported.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Index |  | Number of search space sets per slot |  | **First symbol index** |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 5 | 1 | 1 | 0 |
| 2 | 0 | 2 | 1/2 | {0, if is even}, {7, if is odd} |
| 3 | 5 | 2 | 1/2 | {0, if is even}, {7, if is odd} |
| 4 | 0 | 2 | 1/2 | {0, if is even}, {, if is odd} |
| 5 | 5 | 2 | 1/2 | {0, if is even}, {, if is odd} |
| 6 | 0 | 1 | 2 | 0 |
| 7 | 5 | 1 | 2 | 0 |

* + Support the parameters for PDCCH monitoring occasions for Type0-PDCCH CSS set - SS/PBCH block and CORESET multiplexing pattern 1 with {480, 480} kHz and {960, 960} kHz in Table 4 that is obtained from the agreed Table in RAN1 106b-e by selecting when DBTW is OFF and when DBTW is ON and removing entries with Y.
    - Note: DBTW OFF is indicated in MIB using a value of
* From [2] Futurewei:
  + Rel 17 FR2-2 the SS/PBCH and CORESET#0 for Type0-PDCCH should have only the same SCS.
  + Confirm working assumption for {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz, support multiplexing pattern 1.
  + Use O from the set {0, 5, 2.5, 5+2.5} for 120 kHz, {0, 5, X, 5+X} for 480 kHz, and {0, 5, (2\*X), 5 + (2\*X)} for 960 kHz, with X values TBD.
* From [3] vivo:
  + Support Multiplexing pattern 1 and 3 for SCS 120 kHz, and support Multiplexing pattern 3 for SCS 480 kHz and 960 kHz when operation in FR2-2.
  + Support 96 RB for SCS 120kHz and 480 kHz. Do not support 96 RB for SCS 960kHz.
  + If the sync raster/ channel raster is designed with the same way as in FR 2-1, the existing RB offset design can be reused for SCS 480 kHz and 960 kHz. Otherwise, the RB offset should be re-designed .



* + Set ‘O’ as 1.25 and 2.5 for SCS 480 kHz, 0.625 and 1.25 for SCS 960 kHz.
  + Support remove entries with Y.
* From [4] ZTE/Sanechips
  + For {SSB, CORESET# for Type0-PDCCH} SCS = {120, 120} kHz, even though RAN4 has agreed the minimum CBW is increased to 100 MHz, at least SSB and CORESET#0 multiplexing patterns, number of RBs for CORESET#0, number of symbols (duration of CORESET#0) that are supported in Rel-15/16 should still be supported.
  + For {SSB, CORESET#0 for Type0-PDCCH} SCS= {480, 480} kHz and {960, 960} kHz, RAN1 should also support the following set of parameters of ‘controlResourceSetZero’ configuration.
    - Mux pattern 3 with 24 PRB and 2 symbols
    - Mux pattern 3 with 48 PRB and 2 symbols
  + Adopt same Table 13-12 in TS 38.213 for ‘searchSpaceZero’ configuration for 120/480/960 kHz SCS. For the four FFSs, the following views can be considered.
    - FFS: The value of X (> 0)
      * Proposal: X = 2.5 ms
    - FFS: whether or not to use different X value depending on whether DBTW is ON/OFF
      * Proposal: Same value for DBTW is ON/OFF
    - FFS: whether or not to use same or different X value for 480 and 960 kHz
      * Proposal: Same value for 480 and 960 kHz
    - FFS: whether Y = , or Y=, or whether to remove entries with Y
      * Proposal: Prefer to maintain Y = 
* From [7] Nokia/NSB
  + Support the following RB offsets:
    - 120 kHz SCS
    - 24 PRB CORESET#0: RB offsets 0, 4
      * 48 PRB CORESET#0: RB offsets 0, 14, 28
      * 96 PRB CORESET#0: RB offsets 0, 76
    - 480 kHz SCS
      * 24 PRB CORESET#0: RB offsets 0, 4
      * 48 PRB CORESET#0: RB offsets 0, 14, 28
    - 960 kHz SCS
      * 24 PRB CORESET#0: RB offsets 0, 4
      * 48 PRB CORESET#0: RB offsets 0, 14, 28
    - Note: Numbers could be had in square brackets until RAN4 has confirmed the spectrum utilization assumption.
  + Confirm the support of CORESET#0 with ={96} for 120kHz sub-carrier spacing.
  + Support the following ’O’ values for both 480 and 960 kHz sub-carrier options: {0, 1.5, 5, 6.5} ms.
  + If configuration with consecutive PDCCH monitoring occasions are supported, we would have slight preference to define the first symbol index as {0, if i is even}, {, if i is odd}
  + For SSB and CORESET#0 with 480kHz sub-carrier spacing with SSB and CORESET#0 multiplexing pattern 3, following configuration options could be considered:
    - ={2}
    - ={24, 48}.
  + The Type0-PDCCH CSS set for multiplexing pattern 3 for 480kHz could be designed as follows:

|  |  |  |
| --- | --- | --- |
| **Index** | **PDCCH monitoring occasions (SFN and slot number)** | **First symbol index**  **(*k* = 0, 1, … 31)** |
| 0 |  | 2, 9 in |
| 1 ~ 15 | Reserved | |

* + If contiguous SSB slot pattern is supported for 480kHz and 960kHz, configuration of multiplexing pattern 1 could be used to multiplex SSB and RMSI to same slot.
* From [8] CATT
  + the same X value is used for both DBTW ON/OFF configuration, and following X values can be supported for different SCSs
    - For SCS=480 kHz, value of X can be 2.5ms
    - For SCS=960 kHz, value of X can be 1.25ms
  + The configuration of {0, if  is even}, {, if  is odd} can be supported, considering for SCS=120 KHz use case, the gNB could use implementation to avoid beam switching gap issue if it choose to.
* From [9] OPPO
  + The value of X should be discussed after the candidate SSB number and SSB slot pattern are determined.
  + Support for both 480kHz SCS and 960kHz SCS for Type0-PDCCH CSS.
* From [11] Ericsson
  + Use existing Table 13-12 and Table 13-15 in 38.213 "as is" for operation with 120 kHz SCS in the FR2-2 frequency range. No table entries should be removed.
  + In the table in the RAN1#106b-e agreement, select X=2.5 for both 480 and 960 kHz, and for both DBTW ON/OFF, select , and keep row entries with .
  + For the 57 – 71 GHs band, the following SSB-CORESET0 offsets are sufficient to ensure that all ARFCNs in the floating channelization design in [R1-2111470] are usable:
    - 120/480 kHz SCS: [2 14 26] RBs for 48 RB CORESET0
    - 960 kHz SCS: [0 4] RBs for 24 RB CORESET0
  + If RAN4 defines a floating channelization with a sync raster granularity in line with the design in [R1-2111470], reserve space in the CORESET configuration tables for 3 SSB-CORESET0 offsets for the case of 48 RB CORESET0 for 120/480 kHz.
  + Do not confirm the Working Assumption to support 96 RB CORESET for 120 kHz SCS operation until the RAN4 channelization design is known and it is known how many SSB-CORESET0 offsets are needed for 24 and 48 RB CORESET0.
* From [12] Intel
  + Support 96 PRB CORESET for {SS/PBCH, PDCCH} equal to {480,480} and {960,960} kHz with = {1, 2}.
  + Support the following CORESET#0 RB offset values for {120, 120} kHzkHz for multiplexing patterns 1 and 3:
    - For CORESET#0 with 24 RBs: [0] for multiplexing pattern 1 and –20 if kssb =0 (-21 if kssb > 0) for multiplexing pattern 3.
    - For CORESET#0 with 48 RBs: [0], for multiplexing pattern 1 and –20 if kssb =0 (-21 if kssb > 0) for multiplexing pattern 3.
    - For CORESET#0 with 96 RBs: [0] for multiplexing pattern 1 and –20 if kssb =0 (-21 if kssb > 0) for multiplexing pattern 3.
  + Modify Table 13.8 in TS 38.213 to support the proposed RB offset when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz
  + Support the following CORESET#0 RB offset values for {480, 480}, {960, 960} kHz for multiplexing patterns 1 and 3:
    - For CORESET#0 with 24 RBs: [0] for multiplexing pattern 1 and –20 if kssb =0 (-21 if kssb > 0) for multiplexing pattern 3.
    - For CORESET#0 with 48 RBs: [0], for multiplexing pattern 1 and –20 if kssb =0 (-21 if kssb > 0) for multiplexing pattern 3.
    - For CORESET#0 with 96 RBs: [0] for multiplexing pattern 1 and –20 if kssb =0 (-21 if kssb > 0) for multiplexing pattern 3.
  + Support addition of a new table in 38.213 for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {480, 480} kHz or {960, 960} kHz.
  + Send an LS to RAN4 to consider raster design where RB offset [0] is sufficient for lower spectrum utilization.
  + For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} SCS = {120, 120} kHz,
    - use Table 13-12 in TS38.213 for multiplexing pattern 1.
      * Note: Preference to exclude the rows corresponding to O=2.5 and O=7.5, but would be ok to leave them as is.
    - use Table 13-15 in TS38.213 for multiplexing pattern 3.
  + For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
    - Support O = {0, 2.5, 5, 7.5} for 480kHz (in case Lmax = 128)
    - Support O = {0, 1.25, 5, 6.25} for 960kHz {in case Lmax = 128)
    - Support same O values for DBTW on/off
    - Remove entries for Y= in the table
  + If a non-contiguous SSB slot pattern is supported for {SSB, Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, the equation for determining the slot number for PDCCH monitoring is modified to allow colocation of Type-0 PDCCCH and the corresponding SSB.
    - Support the following modified equation:
    - For 480 kHz and 960 kHz: where and
* From [15] Samsung
  + For CORESET#0 configuration with 120 kHz SCS,
    - support one RB offset for 24 RB CORESET#0 bandwidth in Pattern 1; (e.g. 2 PRB)
    - support two RB offsets for 48 RB CORESET#0 bandwidth in Pattern 1; (e.g. 0, 28 PRB)
    - support one RB offset for 96 RB CORESET#0 bandwidth in Pattern 1; (e.g. 0, 38 PRB)
    - support same RB offsets as Rel-15 FR 2-1 in Pattern 3.
  + For CORESET#0 configuration with 480 kHz and 960 kHz SCS,
    - support the same CORESET#0 configuration table;
    - support multiplexing pattern 3 with same RB offsets as in Rel-15 FR2-1;
    - support two RB offsets for 24 RB CORESET#0 bandwidth in Pattern 1; (e.g. 0, 4 PRB)
    - support three RB offsets for 48 RB CORESET#0 bandwidth in Pattern 1; (e.g. 0, 14, 28 PRB)
  + For Type0-PDCCH configuration:
    - For 480 kHz, ;
    - For 960 kHz, ;
    - .
  + For SS/PBCH block and CORESET#0 multiplexing pattern 3, a UE monitors PDCCH in the Type0-PDCCH CSS set over slots that include Type0-PDCCH monitoring occasions associated with SS/PBCH blocks that are quasi co-located with the SS/PBCH block that provides a CORESET for Type0-PDCCH CSS set.
* From [17] Interdigital
  + Introduce the enhancements on SS/PBCH block transmission patterns to deliberately include the CORESET#0 and SIB1 in fixed time locations along with the corresponding SS/PBCH block to ensure the channel occupancy as much as possible, in the initial access operations with 120kHz SCS for unlicensed spectrum in beyond 52.6GHz.
* From [18] Apple
  + For Type0-PDCCH MOs determination, the offset values are defined as for 480kHz and 960kHz SCS respectively, where .
* From [20] Sharp
  + Regarding the offset value O, our first preference is X = 1 for 480kHz and DBTW off; X = 2.5 for 480kHz and DBTW on; X = 0.5 for 960kHz and DBTW off; X = 1 for 960 and DBTW on. Our second preference is X = 2.5 independent of SCS and DBTW on/off.
  + For Type0-PDCCH CSS set configuration rows where the first symbol index is given by {0, if i is even}, {, if i is odd}, for O = 0, Y = . For O > 0, Y=.
* From [22] LGE
  + Reuse Table 13-12 in TS 38.213 specification for type0-PDCCH CSS set configuration with 120/480/960 kHz, except for O values for 480/960 kHz.
    - For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, in the table of agreement in RAN1#106bis-e
    - X=1.25 for 480 kHz and X=0.625 for 960 kHz, regardless of whether DBTW is enabled or disabled
    - Y = as in Rel-15
* From [23] NTT Docomo
  + For 120 kHz SCS, reuse Table 13-8 and 13-12 as they are.
  + For ‘controlResourceSetZero’ configuration for 480/960 kHz SCS:
    - Reuse the existing RB offsets in FR2-1 with 120 kHz SCS
  + For ‘searchSpaceZero’ configuration for 480/960 kHz SCS:
    - X should follow the SSB slot pattern to be supported
    - X can be dependent on SCS in a simple scaling manner, while no need to depend on DBTW enabled/disabled as it seems too much optimization given the limited time in Rel-17
    - The rows with Y should be kept, and Y should be
* From [24] Qualcomm
  + for FR2-2, CORESET0 SCS = SSB SCS for all SCSs
  + consider minimizing the overhead of beam switching gaps by supporting multiplexing pattern 3
  + for ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, the following parameters from the agreement can be used:
    - Y =
    - “X” may be selected from these 2 options:
      * Option A: 1.25 ms and 0.625 ms for 480 and 960 kHz, respectively
      * Option B: 2.5 ms and 1.25 ms for 480 and 960 kHz, respectively
* From [25] Mediatek
  + For the value of “O”, which represents time-domain offset between SSB and type-0 PDCCH monitoring occasion, support O.

#### Summary of Discussions

Quick recap of previous agreements.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Agreement:  For CORESET#0 and Type0-PDCCH search space configured in MIB:   * Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {120, 120} kHz   + Support at least SSB and CORESET#0 multiplexing patterns, number of RBs for CORESET#0, number of symbols (duration of CORESET#0) that are supported in Rel-15/16 for {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS = {120, 120} kHz.     - FFS: Supporting additional values   + FFS: Supported values for SSB to CORESET#0 offset RBs   Agreement:  For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 1:   * FFS: The value of X (> 0) * FFS: whether or not to use different X value depending on whether DBTW is ON/OFF * FFS: whether or not to use same or different X value for 480 and 960 kHz * FFS: whether Y = , or Y=, or whether to remove entries with Y  |  |  |  |  |  | | --- | --- | --- | --- | --- | | **Index** |  | **Number of search space sets per slot** |  | **First symbol index** | | 0 | 0 | 1 | 1 | 0 | | 1 | 0 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} | | 2 | X | 1 | 1 | 0 | | 3 | X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} | | 4 | 5 | 1 | 1 | 0 | | 5 | 5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} | | 6 | 0 | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} | | 7 | X | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} | | 8 | 5 | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} | | 9 | 5 + X | 1 | 1 | 0 | | 10 | 5 + X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} | | 11 | 5 + X | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} | | 12 | 0 | 1 | 2 | 0 | | 13 | 5 | 1 | 2 | 0 | | 14 | Reserved | | | | | 15 | Reserved | | | | |

The following are a summary of company views on CORESET#0 configuration aspects.

* For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz
  + controlResourceSetZero
  + searchSpaceZero
    - Use Table 13-12 and 13-15 for mux pattern 1 and 3, respectively
      * Ericsson, Intel (2nd preference)
      * *Moderator note: moderator assumes this is by default what will happen when there are lack of any further agreements in RAN1.*
    - use Table 13-12 in TS38.213 for multiplexing pattern 1 excluding the rows corresponding to O=2.5 and O=7.5,
      * Huawei/HiSiliconx, Intel (1st preference)
    - use Table 13-15 in TS38.213 for multiplexing pattern 3.
      * Hiawei/HiSilicon
* For {SSB, CORESET#0/Type0-PDCCH} = {480, 480} and {960, 960} kHz
  + controlResourceSetZero
    - only mux pattern 1
      * Huawei/HiSilicon
    - Mux pattern 1 & 3
      * vivo, [ZTE/Sanechips], Nokia/NSB, Samsung
      * mux pattern 3 with 24 PRB, 48 PRB: ZTE/Sanechips, Nokia/NSB
    - Support 96 PRB
      * vivo, Intel
  + searchSpaceZero
    - O values:
      * X = 1.25 with DBTW is ON, X = 0.625 with DBTW is OFF: Huawei/HiSilicon
      * X=1.25, 2.5 for 480kHz, X=0.625, 1.25 for 960 kHz: vivo
      * X = 2.5: ZTE/Sanechips
      * X = 2.5 for 480kHz, 1.25 for 960kHz: CATT, Intel, Qualcomm
      * X = 1.25 for 480kHz and 0.625 for 960kHz: Samsung, Apple, LGE, Qualcomm
      * X = 1.5: Nokia/NSB
      * X = 1.25: Mediatek
      * X = 1 for 480 kHz and DBTW OFF, X = 2.5 with 480kHz and DBTW ON, 0.5 for 960 kHz and DBTW OFF, 1 for 960 kHz and DBTW ON: Sharp
    - Different X values for O signaling depending on DBTW
      * Yes (different): CATT
      * No (same): ZTE/Sanechips, Nokia/NSB, Intel, LGE
    - Entries with Y
      * Remove: vivo, Intel
      * Y = N\_symb^CORESET: ZTE/Sanechips, Nokia/NSB, Ericsson, Samsung, Sharp (for O=0), LGE, Docomo
      * Y = N\_symb^CORESET + 1: OPPO, Sharp(for O>0), Qualcomm
  + Other proposals
    - If a non-contiguous SSB slot pattern is supported for {SSB, Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, the equation for determining the slot number for PDCCH monitoring is modified to allow colocation of Type-0 PDCCCH and the corresponding SSB.
      * Intel
    - For SS/PBCH block and CORESET#0 multiplexing pattern 3, a UE monitors PDCCH in the Type0-PDCCH CSS set over slots that include Type0-PDCCH monitoring occasions associated with SS/PBCH blocks that are quasi co-located with the SS/PBCH block that provides a CORESET for Type0-PDCCH CSS set.
      * Samsung
* RB offset
  + RB offsets for mux pattern 1
    - 120kHz with 24 PRB
      * {0, 4} (Table 13-8): Huawei/HiSilicon, Docomo
      * {0}: Intel
      * {2}: Samsung (1 offset)
    - 120kHz with 48 PRB
      * {14} (Table 13-8): Docomo
      * {0, 14, 28}: Huawei/HiSilicon, Nokia/NSB
      * {2, 14, 26}: Ericsson
      * {0}: Intel
      * {0, 28}: Samsung (2 offset)
    - 120kHz with 96 PRB
      * {0, 76}: Huawei/HiSilicon, Nokia/NSB
      * {0}: Intel
      * {0, 39}: Samsung (2 offset)
    - 480/960kHz with 24 PRB
      * {0, 4}: Nokia/NSB, Ericsson, Samsung (2 offset), Docomo
      * {0}: Intel
    - 480/960kHz with 48 PRB
      * {14} : Docomo
      * {0, 14, 28} : Nokia/NSB, Samsung (3 offset)
      * {0}: Intel
    - 480/960kHz with 96 PRB
      * {0}: Intel
  + RB offset for mux pattern 3
    - Only -20 (or -21 if kssb>0)
      * Intel
    - Both -20 (or -21 if kssb>0) and (N\_RB)
      * Samsung

#### [ACTIVE] 1st Round Discussion

##### Issue #1) SS#0 for 120kHz

Few companies mentioned using Table 13-12 and 13-15 as is for {120, 120} kHz, and few companies mentioned removal of O=2.5 and 7.5 entries from Table 13-12. As Ericsson mentions, the WID states to try to reuse tables for CORESET#0 and SS#0 as much as possible. Moderator asks companies to see, if they can accept Proposal 1.3-2. Moderator assumes by default in lack of agreement, Proposal 1.3-2 is what we will end up with in the specification. However, it would be still good to get agreement on this for clarity.

###### Proposal 1.3-1

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz,
  + use Table 13-12 in TS38.213 for multiplexing pattern 1,
  + use Table 13-15 in TS38.213 for multiplexing pattern 3.

##### Issue #2) CORESET#0 for 480/960kHz

One company commented that only multiplexing pattern 1 should be supported for 480 and 960 kHz. The WID explicitly states multiplexing pattern 1 should be prioritized. However, there are several companies who commented support of multiplexing pattern 3. Therefore, moderator has formulated Proposal 1.3-2 and 1.3-2A based on comments received. Please check to see if the proposal is acceptable.

###### Proposal 1.3-2

* For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, Support multiplexing pattern 1 with 96 PRB and 2 symbol duration

###### Proposal 1.3-2A

* For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + After supporting entries for multiplexing pattern 1 (with required RB offsets), if additional entries are left, support multiplex pattern 3 with 24 PRB and 2 symbol duration, and multiplexing pattern 3 with 48 PRB and 2 symbol duration.

##### Issue #3) SS#0 for 480/960kHz

Proposed O values from companies seem to be bit diverse. Among the proposals, (X = 2.5 for 480kHz, 1.25 for 960kHz) and (X = 1.25 for 480kHz and 0.625 for 960kHz) seems to have more support. While some companies suggested changing O value depending on whether DBTW is enabled or disabled, majority of the companies proposed same O value regardless of DBTW. Based on this moderator suggest Proposal 1.3-3 and Proposal 1.3-3A. Let’s try to down-select among the two proposals.

###### Proposal 1.3-2

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, parameter X from previous RAN1 agreement is set to:
  + X = 1.25 for 480 kHz
  + X = 0.625 for 960 kHz

###### Proposal 1.3-2A

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, parameter X from previous RAN1 agreement is set to:
  + X = 2.5 for 480 kHz
  + X = 1.25 for 960 kHz

##### Issue #4) SSB/CORESET RB offset for 120 kHz

As of November 11, RAN4 still has not concluded on the channel raster design for band n263 (the 60 GHz band). Therefore, RAN1 may need to pre-populate some entries and revise them accordingly after Ran4 finalizes the channelization design. Moderator has suggested Proposal 1.3-4 based on inputs received. Please check to see if this is acceptable.

###### Proposal 1.3-4

* For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz,
  + Reserve 2 RB offset values for multiplexing pattern 1 with 24 PRB cases
    - Tentative placeholder values: [0] and [4]
  + Reserve 3 RB offset values for multiplexing pattern 1 with 48 PRB cases
    - Tentative placeholder values: [0], [14], and [28]
  + Reserve 2 RB offset values for multiplexing pattern 1 with 96 PRB cases
    - Tentative placeholder values: [0], and [76]
  + Note: the tentative placeholder values are agreed with the understanding the values shall be revisited and updated once RAN4 concludes channel and sync raster design for band n263. Removal and voiding (as reserved states) of RB offset not required by RAN4 design is not precluded and shall be revisited.

Moderator has suggested Proposal 1.3-4A and 1.3-4B based on inputs received. RAN1 should down-select among the two proposals.

###### Proposal 1.3-4A

* For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz,
  + Support following two RB offset values for multiplexing pattern 3
    - -20 if kssb=0, -21 if kssb>0
    - N\_RB , where N\_RB is the number of PRB for CORESET#0

###### Proposal 1.3-4B

* For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz,
  + Support following one RB offset value for multiplexing pattern 3
    - -20 if kssb=0, -21 if kssb>0

##### Issue #5) SSB/CORESET RB offset for 480/960 kHz

As of November 11, RAN4 still has not concluded on the channel raster design for band n263 (the 60 GHz band). Therefore, RAN1 may need to pre-populate some entries and revise them accordingly after Ran4 finalizes the channelization design. Moderator has suggested Proposal 1.3-5 based on inputs received. Please check to see if this is acceptable.

###### Proposal 1.3-5

* For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Reserve 2 RB offset values for multiplexing pattern 1 with 24 PRB cases
    - Tentative placeholder values: [0] and [4]
  + Reserve 2 RB offset values for multiplexing pattern 1 with 48 PRB cases
    - Tentative placeholder values: [0], and [14]
  + Reserve 1 RB offset values for multiplexing pattern 1 with 96 PRB cases (if supported)
    - Tentative placeholder values: [0]
  + Note: the tentative placeholder values are agreed with the understanding the values shall be revisited and updated once RAN4 concludes channel and sync raster design for band n263. Removal and voiding (as reserved states) of RB offset not required by RAN4 design is not precluded and shall be revisited.

Moderator has suggested Proposal 1.3-5A and 1.3-5B based on inputs received. RAN1 should down-select among the two proposals.

###### Proposal 1.3-5A

* For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support following two RB offset values for multiplexing pattern 3 (if supported)
    - -20 if kssb=0, -21 if kssb>0
    - N\_RB , where N\_RB is the number of PRB for CORESET#0

###### Proposal 1.3-5B

* For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support following one RB offset value for multiplexing pattern 3 (if supported)
    - -20 if kssb=0, -21 if kssb>0

##### Issue #6) other issues

There are two proposals related to CORESET#0/SS#0 that was proposed. Moderator suggest discussing the two proposals further.

###### Proposal 1.3-6

* If a non-contiguous SSB slot pattern is supported for {SSB, Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, the equation for determining the slot number for PDCCH monitoring is modified to allow colocation of Type-0 PDCCCH and the corresponding SSB

###### Proposal 1.3-6A

* For SS/PBCH block and CORESET#0 multiplexing pattern 3, a UE monitors PDCCH in the Type0-PDCCH CSS set over slots that include Type0-PDCCH monitoring occasions associated with SS/PBCH blocks that are quasi co-located with the SS/PBCH block that provides a CORESET for Type0-PDCCH CSS set.

##### Company Comments/Inputs

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| --- | --- |
| Company | Comments |
|  |  |

#### <Summary of 1st Round Discussion>

*[To be filled by moderator]*

### 2.1.4 ssb-PositionsInBurst configuration & related aspects

* From [1] Huawei/HiSilicon:
  + In operation with shared spectrum in 60 GHz, for MSB k, k≥1, of inOneGroup and MSB m, m≥1, of groupPresense of ssb-PositionsInBurst:
    - if MSB k of inOneGroup and MSB m of groupPresense are set to 1, the UE assumes that SSB(s) within DBTW with candidate SSB index(es) corresponding to SSB index equal to k-1+(m-1)×8 may be transmitted;
    - if MSB k of inOneGroup or MSB m of groupPresense are set to 0, the UE assumes that the SSB(s) are not transmitted.
  + Regardless of the value of the MSB k of inOneGroup and MSB m of groupPresense in ssb-PositionsInBurst configured in SIB1, if > , UE assumes that candidate SSB index(es) corresponding to SSB index equal to are not transmitted.
* From [3] vivo:
  + One solution is to ensure how many bits in the groupPresence are valid in terms of the value of Q. For instance, if Q=32, then the valid bits in the groupPresence are 4 (Q/8).
  + Another solution is to re-define the groupPresence and inOneGroup in terms of Q. That is, determine the number of SSBs represented by each bit in groupPresence and inOneGroup according to the value of Q. For instance, if Q=32, Q/8=4, then 1 bit represent 4 SSBs.
* From [7] Nokia/NSB:
  + Consider signalling of the valid and invalid candidate SSB indices (associated Type0-PDCCH monitoring occasions) via bits in groupPresence denoting SSB indices greater than . FFS for the case of 128 candidate SSB positions with 480 and 960 kHz SCS.
* From [11] Ericsson
  + The mechanism in Rel-16 (adapted to the restricted ssbPositionInBust signaling using inOneGroup and groupPresence) can be used also for FR2-2 to map SSB candidate positions to ssb-PositionsInBurst.
* From [19] ETRI
  + The interpretation of ssb-PositionsInBurst can be changed depending on .
    - When =16, ssb-PositionsInBurst can be interpreted as full bitmap for indicating 16 SSBs
    - When =32, different number of bits for inOneGroup and groupPresense can be assigned (e.g., 4 bits for inOneGroup, 12 bits for groupPresense), alternatively each bit corresponds to a slot containing 2 SSBs
* From [22] LGE
  + The bit-width of ssb-PositionsInBurst in SIB1 and ServingCellConfigCommon is kept the same as in Rel-15 (i.e., 16-bit bitmap in SIB1 and 64-bit bitmap in ServingCellConfigCommon).
    - For ssb-PositionsInBurst in SIB1, if is indicated as 64, the same method with Rel-15 is applied. If is indicated as less than 64,
    - Alt 1: UE expects a bit at groupPresence corresponding to a SS/PBCH block index k (≥ Q) is set to 0.
    - Alt 2: A bit in 16-bit bitmap corresponds to N (= max {Q/16, 1}) SS/PBCH block index(es).
    - For ssb-PositionsInBurst in ServingCellConfigCommon, UE expects that the k-th bit in the bitmap is set to 0, where k > Q.
* From [23] NTT Docomo
  + For ssb-PositionInBurst in ServingCellConfigCommon and ServingCellConfigCommonSIB, Rel-16 NR-U approach can be reused for the interpretation when DBTW is supported
    - In case of 64 candidate SSB positions, assuming the actual number of SSB beams could be smaller than 64 when DBTW is enabled, some bits in this parameter could be left unused (i.e., always 0)

#### Summary of Discussions

While the formulation from companies are slightly different. Companies generally seem to agree that SSB indices larger than indicated value of should be set to 0. There are other proposals such as re-using the same number of bits as in Rel-15, and proposals to support bitmap approach ssb-PositionInBurst for when Q=16 is indicated.

#### [ACTIVE] 1st Round Discussion

Moderator has formulated the following proposals based on inputs received. Please discuss the proposals.

###### Proposal 1.4-1

* The bit-width of ssb-PositionsInBurst in SIB1 and ServingCellConfigCommon is kept the same as in Rel-15 (i.e., 16-bits in SIB1 and 64-bits in ServingCellConfigCommon).

###### Proposal 1.4-2

* If is indicated, UE expects bits of ssb-PositionsInBurst corresponding to SSB index k larger than indicated is set to 0.

###### Proposal 1.4-3

* In operation with shared spectrum in 60 GHz, for ssb-PositionsInBurst in ServingCellConfigCommonSIB,
  + If ,
    - 16 bits ssb-PositionsInBurst correspond to ‘SSB index’ 0 to 15, and UE assumes that SSB(s) within DBTW with ‘candidate SSB index(es)’ corresponding to indicated bit(s) are transmitted.
  + if > 16, for MSB k, k≥1, of inOneGroup and MSB m, m≥1, of groupPresense of ssb-PositionsInBurst:
    - if MSB k of inOneGroup and MSB m of groupPresense are set to 1, the UE assumes that SSB(s) within DBTW with ‘candidate SSB index(es)’ corresponding to ‘SSB index’ equal to k-1+(m-1)×8 may be transmitted;

###### Proposal 1.4-4

* In operation with shared spectrum in 60 GHz, for ssb-PositionsInBurst in ServingCellConfigCommon,
  + ssb-PositionsInBurst bits correspond to supported ‘SSB indices’, and UE assumes that SSB(s) within DBTW with ‘candidate SSB index(es)’ corresponding to indicated bit(s) are transmitted

##### Company Comments/Inputs

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| --- | --- |
| Company | Comments |
|  |  |

#### <Summary of 1st Round Discussion>

*[To be filled by moderator]*

### 2.1.5 TDRA Enhancements

* From [5] Nokia/NSB:
  + To align PDSCH allocation with the new SSB pattern for SSB and CORESET#0 multiplexing pattern 3 starting symbol S and number of consecutive symbols L values {4,2} and {11,2} would need to be supported.
* From [8] CATT
  + Symbol #6 and symbol #13 can be reserved for beam switching. Neither PDCCH nor PDSCH can be transmitted on the reserved symbols.
  + The default TDRA table for pattern 1 in TS 38.214 can be enhanced, e,g at least {S=6 ,L=7}, {S=2，L=11} is supported
* From [12] Intel
  + For 480 and 960 kHz, no need to enhance or modify TDRA allocation A table.
  + Modify TDRA allocation C table to add S=11 and L =2.
* From [23] NTT Docomo
  + For ‘controlResourceSetZero’ configuration for 480/960 kHz SCS:
    - Enhance Default PDSCH TDRA Table A
      * E.g., {S, L}={8, 6} and {9, 5} can be considered
* From [24] Qualcomm
  + for TDRA C for SI-RNTI PDSCH, consider ways to support the values of S = 11 and L = 2

#### Summary of Discussions

Company views on enhancing TDRA allocation A table is split. However, for TDRA allocation C table, if multiplexing pattern 3 is supported for 480 and 960 kHz SCS, then inclusion of S=11, L=2 was proposed by few companies.

#### [ACTIVE] 1st Round Discussion

Moderator suggest to discuss further on the following proposals. For Proposal 1.5-1A, moderator would like to ask proponent company to enhance TDRA table A, the exact details that would need to agreed such that editor can implement the proposal into the specification.

###### Proposal 1.5-1

* Conclusion:
  + TDRA allocation table A is unchanged for 480 and 960 kHz SCS.

###### [draft] Proposal 1.5-1A

* For 480 and 960 kHz SCS, the TDRA allocation table A used for PDSCH scheduled by SI-RNTI scrambled PDCCH is updated as follows:
  + [proponent to suggest the changes]

###### Proposal 1.5-2

* If multiplexing pattern 3 for 480 and 960 kHz is supported, the TDRA allocation table C is updated as follows:
  + Row index 6 (previously reserved) is set to
    - Dmrs-TypeA-Position: 2,3
    - PDSCH mapping type: Type B
    - K0 : 0
    - S = 11
    - L = 2

##### Company Comments/Inputs

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| --- | --- |
| Company | Comments |
|  |  |

#### <Summary of 1st Round Discussion>

*[To be filled by moderator]*

### 2.1.6 ANR/CGI Reporting Aspects

* From [1] Huawei/HiSilicon:
  + To find the offset between an off-synch raster SSB and the corresponding CORESET#0 in 60GHz unlicensed spectrum, RAN1 should uniquely determine the hypothetical on-synch raster SSB that serves as the reference for the offset to the off-synch raster SSB in case more than one synch rasters are included in a channel bandwidth.
* From [5] Spreadtrum:
  + The mechanism of two offsets in MIB defined for NR-U, i.e. Alt 2), can be reused for UE to determine CORESET#0/Type0-PDCCH.
* From [8] CATT
  + There is no need to study additional method(s) to enable support to obtain neighbor cell SIB1 contents related to CGI reporting in Rel-17.
* From [9] OPPO
  + For ANR design, RAN1 considers one of the two options
    - Option 1: RAN1 holds ANR discussion until RAN4 concludes the channelization, LBT bandwidth and sync raster relationship.
    - Option 2: RAN1 does not follow R16 baseline solution and redesign ANR.
* From [15] Samsung
  + Rel-16 NR-U scheme of using a secondary frequency offset is not applicable for Rel-17 FR2-2 unlicensed bands.
  + No need to support extra method for providing the CORESET#0/Type0-PDCCH configuration for ANR purpose.
* From [26] Qualcomm
  + for ANR, do not consider additional methods (compared to current NR) to signal the NCGI

#### Summary of Discussions

Several companies commented further methods to aupport ANR/CGI reporting is should not be considered. While few companies commented NR-U like approaches to determine offset can be used for 60 GHz as well.

#### [ACTIVE] 1st Round Discussion

Given that NR-U like approach is only made possible with specific channel raster design, and the exact channel raster design is not complete in RAN4 (as of November 11), moderator suggest to conclude RAN1 will no further discuss additional methods for ANR/CGI reporting for 60 GHz.

###### Proposal 1.6-1

* Conclusion:
  + Do not consider additional method for providing the CORESET#0/Type0-PDCCH configuration for ANR/CGI reporting purpose.

##### Company Comments/Inputs

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| --- | --- |
| Company | Comments |
|  |  |

#### <Summary of 1st Round Discussion>

*[To be filled by moderator]*

### 2.1.7 NR Carrier RSSI measurement

* From [15] Samsung
  + For 480 and 960 kHz, support the following 4 configurations for NR carrier RSSI measurement:
    - Configuration #0: {0, 1};
    - Configuration #1: {0, 1, …, 5};
    - Configuration #2: {0, 1, …, 8};
    - Configuration #3: {0, 1, …, 12}.

#### Summary of Discussions

Samsung has brought the issue on NR carrier RSSI measurement. Samsung has pointed out the existing RSSI measurement symbols do not line up with SSB positions for 480 and 960kHz. Therefore, specification update is needed.



#### [ACTIVE] 1st Round Discussion

Suggest discussing proposal from Samsung.

###### Proposal 1.7-1

* For 480 and 960 kHz, support the following 4 configurations for NR carrier RSSI measurement:
  + Configuration #0: {0, 1};
  + Configuration #1: {0, 1, …, 5};
  + Configuration #2: {0, 1, …, 8};
  + Configuration #3: {0, 1, …, 12}

##### Company Comments/Inputs

|  |  |
| --- | --- |
| Company | Comments |
|  |  |

#### <Summary of 1st Round Discussion>

*[To be filled by moderator]*

### 2.1.8 Various other aspects on SSB Design

* From [1] Huawei/HiSilicon:
  + Use of LBT should be indicated in SIB1 to help UE determine the existence of “ChannelAccess-CPext” field in DCI format 1-0/0-0 scrambled with TC-RNTI and in RAR UL grant.
* From [5] Spreadtrum
  + SSB with 240kHz SCS can be down-prioritized.
  + Supporting initial cell selection with 480kHz SSB should be an optional UE capability separately from supporting other processing with 480/960kHz SCS.
  + The SSB-based TRS/CSI-RS validation can be supported.
* From [9] OPPO
  + The raster step size for 120kHz and 480kHz are 3\*17.28MHz and 15\*17.28MHz, respectively, leading to a total number of raster entries 428.
* From [13] Lenovo/Motorola Mobility
  + For NR operation in unlicensed bands between 52.6 GHz and 71 GHz, potential enhancements related to periodic transmission of DRS such as SSB/PBCH/CORESET#0 are needed including:
    - performing directional LBT prior to the transmission of SSB according to the ssb-PositionsInBurst
    - directional LBT on multiple beams at the same time at the beginning of the DRS window
    - Cat 2 LBT (depending on the gap) before actual transmission
  + For initial access in NR unlicensed bands between 52.6 GHz and 71 GHz, with directional LBT based channel access mechanism, indication of sensing beams can be considered during the initial access
  + For supporting NR from 52.6 GHz to 71 GHz in Rel. 17, with higher subcarrier spacings (numerologies), coverage enhancement of channels and signals used for initial access should be considered for NR beyond 52.6 GHz
* From [17] Interdigital
  + Consider indicating the license regime in initial access operations based on different sync raster sets.
* From [21] Convida Wireless
  + SSB coverage enhancement should be studied for higher SCS.

#### Summary of Discussions

* Companies have provided the following issues
  + LBT aspects for SIB1
  + 240 kHz SSB down prioritization
  + Initial cell selection for 480kHz SCS as a separate UE capability
  + Sync raster design
  + LBT before DRS
  + Coverage enhancements

#### [ACTIVE] 1st Round Discussion

For issues brought up, the issue should be discussed in appropriate WG or agenda.

* Raster design
  + Should be discussed in RAN4
* Capability aspect for initial access
  + Should be discussed in 8.16.2
* LBT related aspects
  + Should be discussed in 8.2.6 channel access agenda
* Coverage enhancement
  + Moderator suggest to de-prioritize this discussion as coverage enhancement was explicitly de-scoped from the WID

If there are other issues that require solution in order for RAN1 to complete the WI, please provide comments and inputs.

##### Company Comments/Inputs

|  |  |
| --- | --- |
| Company | Comments |
|  |  |

#### <Summary of 1st Round Discussion>

*[To be filled by moderator]*

## 2.2 PRACH Aspects

### 2.2.1 PRACH Sequence and Format

* From [4] ZTE/Sanechips:
  + Update the Table 6.3.3.2-1 in TS 38.211 as follows:
    - Table 6.3.3.2-1: Supported combinations of and , and the corresponding value of .

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | for PRACH | for PUSCH | , allocation expressed in number of RBs for PUSCH |  |
| ... | ... | ... | ... | ... |
| 139 | 120 | 120 | 12 | 2 |
| 139 | 120 | 480 | 3 | 2 |
| 139 | 120 | 960 | 2 | 2 |
| 139 | 480 | 120 | 48 | 2 |
| 139 | 480 | 480 | 12 | 2 |
| 139 | 480 | 960 | 6 | 2 |
| 139 | 960 | 120 | 96 | 2 |
| 139 | 960 | 480 | 24 | 2 |
| 139 | 960 | 960 | 12 | 2 |
| 571 | 120 | 120 | 48 | 2 |
| 571 | 120 | 480 | 12 | 2 |
| 571 | 120 | 960 | 6 | 2 |
| 571 | 480 | 120 | 192 | 2 |
| 571 | 480 | 480 | 48 | 2 |
| 571 | 480 | 960 | 24 | 2 |
| 1151 | 120 | 120 | 96 | 1 |
| 1151 | 120 | 480 | 24 | 1 |
| 1151 | 120 | 960 | 12 | 1 |

#### Summary of Discussions

* K bar values and N\_RB allocation for PRACH for 480 and 960 kHz is missing. ZTE has provided a table to review and agree to.

#### [ACTIVE] 1st Round Discussion

Further discussion on following proposals.

###### Proposal 2.1-1

* + Update the Table 6.3.3.2-1 in TS 38.211 as follows:
    - Table 6.3.3.2-1: Supported combinations of and , and the corresponding value of .

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | for PRACH | for PUSCH | , allocation expressed in number of RBs for PUSCH |  |
| ... | ... | ... | ... | ... |
| 139 | 120 | 120 | 12 | 2 |
| 139 | 120 | 480 | 3 | 2 |
| 139 | 120 | 960 | 2 | 2 |
| 139 | 480 | 120 | 48 | 2 |
| 139 | 480 | 480 | 12 | 2 |
| 139 | 480 | 960 | 6 | 2 |
| 139 | 960 | 120 | 96 | 2 |
| 139 | 960 | 480 | 24 | 2 |
| 139 | 960 | 960 | 12 | 2 |
| 571 | 120 | 120 | 48 | 2 |
| 571 | 120 | 480 | 12 | 2 |
| 571 | 120 | 960 | 6 | 2 |
| 571 | 480 | 120 | 192 | 2 |
| 571 | 480 | 480 | 48 | 2 |
| 571 | 480 | 960 | 24 | 2 |
| 1151 | 120 | 120 | 96 | 1 |
| 1151 | 120 | 480 | 24 | 1 |
| 1151 | 120 | 960 | 12 | 1 |

##### Company Comments/Inputs

|  |  |
| --- | --- |
| Company | Comments |
|  |  |

#### <Summary of 1st Round Discussion>

*[To be filled by moderator]*

### 2.2.2 RACH Occasion Resources

* From [2] Futurewei:
  + For 480kHz and 960 kHz SCS reuse Table 6.3.3.2-4: Random access configurations for FR2 and unpaired spectrum, where the slot index is scaled up by 4 and respectively by 8 as per prior agreement. For 120 kHz SCS use the Table 6.3.3.2-4 as is.
* From [7] Nokia/NSB:
  + Support the following PRACH slot configuration for 480 and 960 kHz PRACH:
    - when number of PRACH slots in a reference slot is 1,
      * for 480kHz and for 960kHz PRACH
    - and when the number of PRACH slots in a reference slot is 2,
      * for 480kHz and for 960kHz PRACH
* From [8] CATT
  + The reference slot duration corresponds to 60 kHz SCS. PRACH slot index corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.
  + For 480/960 kHz PRACH slots configuration, higher PRACH slot density or higher RO density in time domain can be supported to compensate the impact from decreasing MSGS–FDM and LBT/beam switching GAP.
    - For 480KHz SCS, PRACH slot density can be 2 or 4 times comparing to than 120KHz SCS
    - For 960KHz SCS, PRACH slot density can be 4 times comparing to 120KHz SCS
  + If gap for LBT or beam switching is needed before UE transmit an msg-1, one RO can be disabled by RRC in a 60 KHz reference slot, and UE can perform LBT or beam switching on the disable RO.
* From [11] Ericsson
  + Confirm the values for from the RAN1#106-e agreement for both the case of 1 and 2 PRACH slots per reference slot.
* From [17] Interdigital
  + Do not support gap insertion between consecutive ROs in time domain as it causes inefficiency and application ambiguity.
  + Consider the enhancements to RO configuration without inserting gaps in between consecutive ROs.
  + Consider decomposing the PRACH occasions in time and frequency for operation without beam switching gaps between consecutive ROs. As such, the beam switching corresponding to each time-domain RO could be accomplished along with the preceding time-domain RO.
* From [19] ETRI
  + Propose to remove the square bracket for values in the previous agreement.
* From [22] LGE
  + For 480 and 960 kHz PRACH, for 480 kHz and for 960 kHz PRACH when number of PRACH slots in a reference slot is 1, and for 480 kHz and for 960 kHz PRACH when the number of PRACH slots in a reference slot is 2.
* From [24] Qualcomm
  + a maximum of 4 and 2 FD multiplexed ROs for SCS = 120 kHz and sequence length = 571 and 1151, respectively

#### Summary of Discussions

The following is a summary of company views.

* Confirmation of WA on PRACH slots for 480 and 960 kHz
  + Nokia/NSB, Ericsson, ETRI, LGE
* Maximum of 4 and 2 FDM ROs for 120 kHz and sequence length L= 571 and 1151, respectively
  + Qualcomm

#### [ACTIVE] 1st Round Discussion

Suggest discussing on the following proposals.

###### Proposal 2.2-1

* Finalizing PRACH slot index for 480 and 960 kHz (removal of bracket of previous agreement)
  + when number of PRACH slots in a reference slot is 1,
    - for 480kHz and for 960kHz PRACH
  + when the number of PRACH slots in a reference slot is 2,
    - for 480kHz and for 960kHz PRACH

###### Proposal 2.2-2

* Support maximum of 4 and 2 FD multiplexed ROs for SCS = 120 kHz and sequence length = 571 and 1151, respectively

##### Company Comments/Inputs

|  |  |
| --- | --- |
| Company | Comments |
|  |  |

#### <Summary of 1st Round Discussion>

*[To be filled by moderator]*

### 2.2.3 RA Preamble ID

* From [1] Huawei/HiSilicon:
  + The RA-RNTI corresponding to 480 kHz and 960 kHz ROs can be generated according to equation (3) by compressing the t\_id to .
* From [3] vivo:
  + For 480kHz and 960kHz PRACH, reuse the RA-RNTI formula as FR2 and express the slot indexes t\_id based on 120kHz SCS:
    - RA-RNTI=1+s\_id+14×t\_id+14×80×f\_id +14×80×8×ul\_carrier\_id
    - where t\_id can be the index of the first 120kHz slot contains the PRACH occasion in a system frame (0 ≤ t\_id < 80).
* From [4] ZTE/Sanechips
  + For higher PRACH SCS (480 and/or 960 kHz), consider the following options for further down-selection of RA-RNTI enhancements:
    - Option 3)
      * Segment the PRACH into N segments
      * is the index of the PRACH slot that contains the PRACH occasion in a segment.
      * In DCI: RA-indication = Segment index
    - Option 7)
      * is the index of the first 120kHz slot that contains the PRACH occasion in a system frame.
      * is the index of the first OFDM symbol of the PRACH occasion based on the value of specified in clause 5.3.2 of TS 38.211.
  + Reuse the maximum of 40 ms for ra-ResponseWindow for unlicensed band and the same window size for msgB-ResponseWindow for both licensed and unlicensed band in 52.6GHz and 71GHz.
* From [6] Fujitsu
  + When calculating RA-RNTI for 480kHz and 960kHz PRACH, the following should be considered to uniquely identify a RO:
    - t\_id is determined in a way that more than one slot can have the same t\_id; and
    - DCI scheduling RAR indicates the local index among the slots having the same t\_id.
* From [7] Nokia/NSB
  + Reuse RA-RNTI formula defined for 120 kHz SCS also for the cases PRACH is configured with 480 or 960 kHz SCS where
    - assumes 480/960 kHz SCS
    - assumes 120 kHz SCS
* From [8] CATT
  + For supporting Msg1 transmission with 480 KHz/960 KHz SCS, RA-RNTI is divided into two parts. One part of RA-RNTI is carried by DCI, and the remaining 16-bit of RA-RNTI could be used to scramble CRC of the DCI1. Two possible options are:
    - Option A:
      * RA-RNTI = (1 + s\_id + 14 × t\_id + 14 ×× f\_id + 14 × × 8 × ul\_carrier\_id) mod
      * inDCI\_bit = floor ((1 + s\_id + 14 × t\_id + 14 ×× f\_id + 14 × × 8 × ul\_carrier\_id) /)
      * s\_id is the index of the first OFDM symbol of the PRACH occasion (0 ≤ s\_id < 14)
      * t\_id is the index of the first slot of the PRACH occasion in a system frame (0 ≤ t\_id < 640)
    - Option B:
      * RA-RNTI = 1 + s\_id + 14 ×(t\_id mod 80) + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id
      * inDCI\_bit =
      * s\_id is the index of the first OFDM symbol of the PRACH occasion (0 ≤ s\_id < 14)
      * t\_id is the index of the first slot of the PRACH occasion in a system frame (0 ≤ t\_id < 640)
* From [11] Ericsson
  + For 480/960 kHz PRACH, reuse the RA-RNTI expressions from Rel-15/16, with the additional statement that for 480/960 kHz PRACH, t\_id should be determined based on a subcarrier spacing of 120 kHz.
* From [12] Intel
  + RA-RNTI computation equation should be adjusted to avoid overflow in case of PRACH SCS 480 kHz and 960 kHz;
    - Support the following modified equation for RA-RNTI computation:
    - ,
    - where t\_id is based on the value of specified in clause 5.3.2 of TS 38.211.
* From [18] Apple
  + modifying the existing calculation equation or redefine t\_id based on 120kHz SCS to solve the RA-RNTI overflowing problem:
* From [19] ETRI
  + Propose to reuse the current equation with minor modifications for RA preamble ID calculation.
    - RA-RNTI = 1 + s\_id + 14 × t\_id + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id
    - *t\_id is the index of 120kHz slot that contains RO in a system frame*
    - s\_id is the index of the first OFDM symbol of RO based on the value of specified in clause 5.3.2 of TS 38.211
* From [20] Sharp
  + Assuming RO density per reference slot is unchanged, without modifying the formula and definition of s\_id, modify the definition of t\_id as the slot index referring to 120kHz SCS.
* From [22] LGE
  + Reuse the existing RA-RNTI/MSGB-RNTI equation by reinterpreting the slot indexes t\_id based on a new specific subcarrier spacing as the slot indexes of 120 kHz SCS (e.g., floor(t\_id/n) where n=4 for 480 kHz SCS and n=8 for 960 kHz).
  + In the case of mapping RA-RNTI to actual 480/960 kHz PRACH slot, the RAR window segmentation as well as DCI indication can be considered:
    - Divide the RAR window for RA-RNTI (or msg2 window for MSGB-RNTI) into N sub-periods (where each sub-period is 80 slots using the used SCS) + signal the sub-period index using bit-field with ceiling{log2(N)} bits in the DCI that schedules the MSG2/MSGB.
  + If the modulo operation is adopted instead of the RAR window segmentation method to calculate RA-RNTI for 480/960 kHz PRACH, the following aspects should be considered: 1) valid RNTI value range (starting from 1 and not from 0) and 2) offset value for MSGB-RNTI to be separated from RA-RNTI.
* From [24] Qualcomm
  + for SCS = 480/960 kHz, reuse the Rel-15 RA-RNTI equation with redefining the t\_id definition as:
    - t\_id is the index of the first slot (based on 120 kHz numerology) of the PRACH occasion in a system frame (0 ≤ t\_id < 80)

#### Summary of Discussions

Companies seem to be converging on re-using the existing RA-RNTI calculation formula with a minor update to t\_id. While companies have slightly different formulation of the resolution, the end result seems to be the same. From the proposal, description from vivo and Intel seems to be most clear. Suggest to down-select among the two descriptions.

#### [ACTIVE] 1st Round Discussion

Discuss further on the following proposals, and down-select among Proposal 2.3-2 and 2.3-2A. Once agreed, need to send a LS to RAN2 so that the update can be captured in RAN2 specification. From moderator’s understanding proposal 2.3-2 and 2.3-2A have completely identical functionality, and the only difference is how it is described. Suggest to simply pick by majority among the two options.

###### Proposal 2.3-2

* + For 480kHz and 960kHz PRACH, reuse the RA-RNTI formula as FR2 and express the slot indexes t\_id based on 120kHz SCS:
    - RA-RNTI=1+s\_id+14×t\_id+14×80×f\_id +14×80×8×ul\_carrier\_id
    - where t\_id can be the index of the first 120kHz slot contains the PRACH occasion in a system frame (0 ≤ t\_id < 80).
  + Send LS to RAN2 on the updates on RA-RNTI.

###### Proposal 2.3-2A

* + RA-RNTI computation equation should be adjusted to avoid overflow in case of PRACH SCS 480 kHz and 960 kHz;
    - Support the following modified equation for RA-RNTI computation:
    - ,
    - where t\_id is based on the value of specified in clause 5.3.2 of TS 38.211.
  + Send LS to RAN2 on the updates on RA-RNTI.

##### Company Comments/Inputs

|  |  |
| --- | --- |
| Company | Comments |
|  |  |

#### <Summary of 1st Round Discussion>

*[To be filled by moderator]*

### 2.2.3 RAR Window

* From [1] Huawei/HiSilicon:
  + Support maximum of 40 ms for ra-ResponseWindow for operation with shared spectrum and msgB-ResponseWindow for both operations with and without shared spectrum. Support indicating two LSBs of SFN at which gNB has received msg1 (MsgA) in DCI format 1\_0 with CRC scrambled by RA-RNTI (MsgB-RNTI).
* From [4] ZTE/Sanechips
  + Reuse the maximum of 40 ms for ra-ResponseWindow for unlicensed band and the same window size for msgB-ResponseWindow for both licensed and unlicensed band in 52.6GHz and 71GHz.

#### Summary of Discussions

Few companies commented on the RAR window size for 60 GHz, and suggested to use 40 msec window. This also requires support of 2 bits in DCI format 1\_0 indicating the two LSB of the SFN that PRACH was sent.

#### [ACTIVE] 1st Round Discussion

Discuss on the following proposal.

###### Proposal 2.3-3

* Support maximum of 40 ms for ra-ResponseWindow for operation with shared spectrum and msgB-ResponseWindow for both operations with and without shared spectrum. Support indicating two LSBs of SFN at which gNB has received msg1 (MsgA) in DCI format 1\_0 with CRC scrambled by RA-RNTI (MsgB-RNTI).

##### Company Comments/Inputs

|  |  |
| --- | --- |
| Company | Comments |
|  |  |

#### <Summary of 1st Round Discussion>

*[To be filled by moderator]*

### 2.2.4 Ngap between PRACH-SSB and PRACH-PUSCH/PUCCH/SRS

There PRACH validation is considered in [TS 38.213]

*“A PRACH occasion in a PRACH slot is valid if it does not precede a SS/PBCH block in the PRACH slot and starts at least symbols after a last SS/PBCH block reception symbol, where is provided in Table 8.1-2”*

Table 8.1-2: values for different preamble SCS

|  |  |
| --- | --- |
| Preamble SCS |  |
| 1.25 kHz or 5 kHz | 0 |
| 15 kHz or 30 kHz or 60 kHz or 120 kHz | 2 |

*“For single cell operation or for operation with carrier aggregation in a same frequency band, a UE does not transmit PRACH and PUSCH/PUCCH/SRS in a same slot or when a gap between the first or last symbol of a PRACH transmission in a first slot is separated by less than symbols from the last or first symbol, respectively, of a PUSCH/PUCCH/SRS transmission in a second slot where for or 1, for or , and is the SCS configuration for the active UL BWP. For a PUSCH transmission with repetition Type B, this applies to each actual repetition for PUSCH transmission [6, TS 38.21*4].”

* From [2] Futurewei:
  + Update the table 8.1-2 to indicate the necessary Ngap for higher SCS.
* From [4] ZTE/Sanechips
  + Update Table 8.1-2 in TS 38.213 as follows:
    - For 480 and 960kHz, Ngap = 16
  + Define the symbol level gap N =32 between PRACH and PUSCH/PUCCH/SRS for 480kHz and 960kHz.
* From [15] Samsung
  + For FR2-2,
    - Minimum gap between a valid RO and a SS/PBCH block for 120 kHz, for 480 kHz, and for 960 kHz;
    - Minimum gap separating PRACH transmission and PUSCH/PUCCH/SRS transmission for 120 kHz, for 480 kHz, and for 960 kHz;
    - The term when determining the gap between a PDCCH order and the PRACH transmission for FR2-2.
* From [25] Mediatek
  + RAN 1 to discuss the value of for NR operation in 52.6-71 GHz.

#### Summary of Discussions

The symbol gap between PRACH and other signals/channels are required to be defined for 480 and 960 kHz case. Several companies provided resolution for this issue.

#### [ACTIVE] 1st Round Discussion

Discuss on the following proposals. As for delta\_delay between PDCCH order and PRACH of 0.25msec. FR2 covers both FR2-1 and FR2-2. Therefore, instead of agreement, conclusion might suffice.

###### Proposal 2.3-4

* Update the Table 8.1-2 in TS38.213 to indicate the Ngap (gap between valid RO and SS/PBCH) for 480 kHz and 960 kHz SCS as follows:
  + for 480 kHz
  + for 960 kHz;

###### Proposal 2.3-4A

* For single cell operation or for operation with carrier aggregation in a same frequency band, a UE does not transmit PRACH and PUSCH/PUCCH/SRS in a same slot or when a gap between the first or last symbol of a PRACH transmission in a first slot is separated by less than 𝑁 symbols from the last or first symbol, respectively, of a PUSCH/PUCCH/SRS transmission in a second slot where 𝑁=16 for 𝜇=5, 𝑁=32 for 𝜇=6, and 𝜇 is the SCS configuration for the active UL BWP. For a PUSCH transmission with repetition Type B, this applies to each actual repetition for PUSCH transmission [6, TS 38.214].

###### Proposal 2.3-4B

* Conclusion:
  + as part of gap between last symbol of PDCCH order reception and first symbol of the PRACH transmission for FR2-2 uses the same value as FR2-1 (i.e. single value for FR2).

##### Company Comments/Inputs

|  |  |
| --- | --- |
| Company | Comments |
|  |  |

#### <Summary of 1st Round Discussion>

*[To be filled by moderator]*

### 2.2.4 Other aspects on PRACH

* From [2] Futurewei:
  + Support short control signaling LBT exception for RACH transmissions.
* From [17] Interdigital
  + For 52.6 – 71 GHz, support sharing and extending the COT for LBT-free PRACH transmission in the consecutive ROs. Consider using preambles scrambled with cover codes in PRACH transmission to inform an ongoing RACH occasion. As such, upon successful detection of the cover code, the UE could consider extending the initiated COT for LBT-free PRACH transmission.

#### Summary of Discussions

Companies provide some inputs related to LBT aspects for PRACH. Moderator think better agenda item for discussion is A.I. 8.2.6.

#### [ACTIVE] 1st Round Discussion

Moderator suggest discussing LBT aspects under 8.2.6 channel access agenda.

##### Company Comments/Inputs

|  |  |
| --- | --- |
| Company | Comments |
|  |  |

#### <Summary of 1st Round Discussion>

*[To be filled by moderator]*

## 2.3 Others Aspects

#### [ACTIVE] 1st Round Discussion

Companies are asked to provide comments on any other issues that needs to be addressed in order to complete the WI.

##### Company Comments/Inputs

|  |  |
| --- | --- |
| Company | Comments |
|  |  |

#### <Summary of 1st Round Discussion>

*[To be filled by moderator]*

# Reference

1. R1-2110827, “Initial access signals and channels for 52-71GHz spectrum,” Huawei, HiSilicon
2. R1-2110872, “Initial access for Beyond 52.6GHz,” FUTUREWEI
3. R1-2110998, “Remaining issues on initial access aspects for NR operation from 52.6GHz to 71GHz,” vivo
4. R1-2111074, “Discussion on the initial access aspects for 52.6 to 71GHz,” ZTE, Sanechips
5. R1-2111091, “Discussion on initial access aspects for NR for 60GHz,” Spreadtrum Communications
6. R1-2111146, “Considerations on initial access for NR from 52.6GHz to 71 GHz,” Fujitsu
7. R1-2111195, “Initial access aspects,” Nokia, Nokia Shanghai Bell
8. R1-2111241, “Initial access aspects for up to 71GHz operation,” CATT
9. R1-2111307, “Discusson on initial access aspects,” OPPO
10. R1-2111385, “Considerations on initial access aspects for NR from 52.6 GHz to 71 GHz,” Sony
11. R1-2111463, “Initial Access Aspects,” Ericsson
12. R1-2111483, “Discussion on initial access aspects for extending NR up to 71 GHz,” Intel Corporation
13. R1-2111641, “Initial access aspects for NR from 52.6 GHz to 71GHz,” Lenovo, Motorola Mobility
14. R1-2111701, “Discussion on initial access aspects supporting NR from 52.6 to 71 GHz,” NEC
15. R1-2111725, “Initial access aspects for NR from 52.6 GHz to 71 GHz,” Samsung
16. R1-2111788, “Initial access aspects for NR from 52.6 GHz to 71 GHz,” Panasonic Corporation
17. R1-2111832, “Discussion on initial access channels and signals for operation in 52.6-71GHz,” InterDigital, Inc.
18. R1-2111861, “Initial access signals and channels,” Apple
19. R1-2111987, “Discussion on initial access aspects for NR from 52.6 to 71GHz,” ETRI
20. R1-2112011, “Initial access aspects,” Sharp
21. R1-2112029, “NR SSB design consideration for 52.6 GHz to 71 GHz,” Convida Wireless
22. R1-2112045, “Initial access aspects to support NR above 52.6 GHz,” LG Electronics
23. R1-2112096, “Initial access aspects for NR from 52.6 to 71 GHz,” NTT DOCOMO, INC.
24. R1-2112203, “Initial access aspects for NR in 52.6 to 71GHz band,” Qualcomm Incorporated
25. R1-2112290, “Remaining issues on initial access of 52.6-71 GHz NR operation,” MediaTek Inc.
26. R1-2112384, “Remaining issues on initial access aspects for NR beyond 52.6GHz,” WILUS Inc.

# List of RAN1 Agreements on initial access

## RAN1 #104-e

**R1-2102073** [Draft] LS on beam switching gap for 60 GHz band Intel Corporation

Final LS endorsed in R1-2102202

Agreement:

Send an LS to RAN4 to get input on gap required for gNBs and UEs for beam switching and for UL/DL and DL/UL switching.

Agreement:

Whether or not to support 240 kHz, 480kHz and 960kHz SCS for SSB and the conditions under which SSB for 240 kHz, 480 kHz and 960 kHz may be supported will be decided no later than RAN1#104bis-e.

Agreement:

For an unlicensed band that requires LBT, further study whether/how to support discovery burst (DB) and discovery burst transmission window (DBTW) at least for 120 kHz SSB SCS

* If DB supported
  + FFS: What signals/channels are included in DB other than SS/PBCH block
* If DBTW is supported
  + Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs
    - FFS: how to support UEs performing initial access that do not have any prior information on DBTW.
  + PBCH payload size is no greater than that for FR2
  + Duration of DBTW is no greater than 5 ms
  + Number of PBCH DMRS sequences is the same as for FR2
* The following points are additionally FFS:
  + How to indicate candidate SSB indices and QCL relation without exceeding limit on PBCH payload size
  + Details of the mechanism for enabling/disabling DBTW considering LBT exempt operation and overlapping licensed/unlicensed bands
  + Whether or not to support DBTW for SSB SCS(s) other than 120 kHz if other SSB SCS(s) are supported

Agreement:

For CORESET#0 and Type0-PDCCH search space configured in MIB:

* Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {120, 120} kHz
  + Support at least SSB and CORESET#0 multiplexing patterns, number of RBs for CORESET#0, number of symbols (duration of CORESET#0) that are supported in Rel-15/16 for {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS = {120, 120} kHz.
    - FFS: Supporting additional values
  + FFS: Supported values for SSB to CORESET#0 offset RBs
* If 480kHz SSB SCS that configures CORESET#0 and Type0-PDCCH CSS in MIB is agreed to be supported,
  + Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {480, 480} kHz
* If 960 kHz SSB SCS that configures CORESET#0 and Type0-PDCCH CSS in MIB is agreed to be supported,
  + Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {960, 960} kHz
* If 240 kHz SSB SCS is agreed to be supported,
  + Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {240, 120} kHz
* FFS: any other combinations between one of SSB SCS (120, 240, 480, 960) and one of CORESET#0 SCS (120, 480, 960)
  + FFS: initial timing resolution based on low SCS (120 kHz) and its impact on the performance of higher SCS (480/960 kHz)

Agreement:

For 480 kHz and 960 kHz SSB SCS (if agreed)

* Study further on reserving symbol gap between SSB positions with different SSB index (and possibly between SSB position and other signal/channels)
  + FFS: whether symbol gap is needed for only 960 kHz or both 480 and 960 kHz.
* Study further on reserving gap for UL/DL switching within the pattern accounting possibility for reserving UL transmission occasions in the SSB pattern
* Study should account for inputs from RAN4

Agreement:

* For initial access and non-initial access use cases, support 120kHz PRACH SCS with sequence length L=571, 1151 (in addition to L=139) for PRACH Formats A1~A3, B1~B4, C0, and C2.
* For non-initial access use cases,
  + if 480kHz and/or 960 kHz SSB SCS is agreed to be supported, support 480 and/or 960 kHz PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively.
    - FFS: support of sequence length L = 571, 1151
* FFS: Support of 480 and/or 960 kHz PRACH SCS for initial access use cases, if 480 and/or 960 kHz SSB SCS is agreed to be supported for initial access

Agreement:

If 480 and/or 960 kHz PRACH SCS is supported, RAN1 should study whether or not the current RA-RNTI calculation and PRACH identification in RAR correctly provides unique identification of PRACH.

## RAN1 #104-bis-e

Agreement:

For the case where SSB location and SCS are explicitly provided to the UE (non-initial access) and SSB does not configure Type-0 PDCCH, support 480 kHz and 960 kHz numerologies for the SSB

* Note: Strive to minimize specification impact due to the new SCS for SSB

Agreement:

* For operation with shared spectrum channel access of NR 52.6 – 71 GHz, support discovery burst (DB) and define the DB same as in Rel-16 37.213 Section 4.0
* FFS: Support discovery burst transmission window (DBTW) at least for SSB with 120 kHz SCS with the following requirements
  + PBCH payload size is no greater than that for FR2
  + Duration of DBTW is no greater than 5 ms
  + Number of PBCH DMRS sequences is the same as for FR2
  + FFS: applicability of DBTW design for 120kHz to SSB with 480kHz and 960kHz SCS
  + Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs
    - FFS: how to support UEs performing initial access that do not have any prior information on DBTW.
    - FFS: details of the mechanism for enabling/disabling DBTW considering LBT exempt operation and overlapping licensed/unlicensed bands
    - FFS: details of how to inform UEs of the configuration of DBTW

Agreement:

For SSB with 120kHz SCS for NR 52.6 GHz to 71 GHz,

* 120 kHz SCS: the first symbols of the candidate SS/PBCH blocks have indexes {4, 8,16, 20} + 28×n, where index 0 corresponds to the first symbol of the first slot in a half-frame.
* For carrier frequencies within 52.6 GHz to 71GHz, support at least 𝑛 = 0, 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 15, 16, 17, 18.
  + Other values of *n* (if any) are FFS, and support of additional n values are subject to support of DBTW for 120kHz SSB

Agreement:

* PRACH configuration for 480/960 kHz SCS (if agreed)
  + The minimum PRACH configuration period is 10 ms (as in FR2)
  + For RO configuration for PRACH with 480/960kHz SCS,
    - FFS: details of how to configure the 480/960 kHz PRACH ROs using [60 or 120 kHz] reference slot considering at least:
      * location of 480/960 kHz PRACH slot per reference slot
      * location of duration containing 480/960khz PRACH slot pattern within 10ms
      * potential impact to RA-RNTI calculation

## RAN1 #105-e

Agreement:

For 480kHz/960kHz SSB, select one of the following alternatives:

* ALT 1) First symbols of the candidate SSB have index {X, Y} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
  + value of X and Y are identical for 480kHz and 960kHz
    - FFS: exact value of X and Y
* ALT 2) First symbols of the candidate SSB have index {4, 8, 16,20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
* Values of n for 480kHz and 960kHz for ALT 1 and 2
  + FFS: whether number of values for ‘n’ depend on LBT operation (i.e. LBT vs no-LBT)
  + FFS: exact values of ‘n’ for each SCS
  + Values of ‘n’ for one mode of operation shall be strictly a subset of values for another mode of operation, if two mode of operation exist for number of candidate SSBs
  + FFS: whether values of ‘n’ shall not be all consecutive integer values (i.e. non-candidate SSB slots are positioned every few candidate SSB slots)

Proposal:

In addition to 120kHz, support **480** kHz SSB for initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with following constraints.

* Limited sync raster entry numbers
  + It is assumed that RAN4 supports a channelization design which results in the total number of synchronization raster entries considering both licensed and unlicensed operation in a 52.6 – 71 GHz band no larger than **665** (Note: the total number of synchronization raster entries in FR2 for band n259 + n261 is 602). If the assumption cannot be satisfied, it’s up to RAN4 to decide its applicability to bands in 52.6 – 71 GHz.
* only 480kHz CORESTE#0/Type0-PDCCH SCS supported for 480 kHz SSB SCS.
* SSB time domain candidate resource pattern (within a slot or pair of slots) for 480 and 960kHz SSB are identical
* Prioritize support SSB-CORESET0 multiplexing pattern 1. Other patterns discussed on a best effort basis.
* Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible

Formal objection sustained by: Huawei, MediaTek (would like to discuss at next meeting)

Proposal:

In addition to 120kHz, support **both** **480 and 960** kHz SSB for initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with following constraints.

* Limited sync raster entry numbers
  + It is assumed that RAN4 supports a channelization design which results in the total number of synchronization raster entries considering both licensed and unlicensed operation in a 52.6 – 71 GHz band no larger than **665** (Note: the total number of synchronization raster entries in FR2 for band n259 + n261 is 602). If the assumption cannot be satisfied, it’s up to RAN4 to decide its applicability to bands in 52.6 – 71 GHz.
* only 1 CORESTE#0/Type0-PDCCH SCS supported for each SSB SCS i.e., (480,480) and (960,960).
* SSB time domain candidate resource pattern (within a slot or pair of slots) for 480 and 960kHz SSB are identical
* Prioritize support SSB-CORESET0 multiplexing pattern 1. Other patterns discussed on a best effort basis.
* Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible

Formal objection sustained by: Huawei, MediaTek (object to 960 kHz)

Proposal:

To support ANR and PCI confusion detection for 480/960kHz SCS based SSB, support CORESET#0/Type0-PDCCH configuration in MIB of 480 and 960kHz SSB

* FFS: additional method(s) to enable support to obtain neighbor cell ~~PCI and~~ SIB1 contents related to CGI reporting
* Only 1 CORESTE#0/Type0-PDCCH SCS supported for each SSB SCS, i.e., (480,480) and (960,960).
* Prioritize support SSB-CORESET0 multiplexing pattern 1. Other patterns discussed on a best effort basis.
* Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible
* Note: From UE perspective, ANR detection for 480/960kHz SCS based SSB is not supported if the UE does not support 480/960 SCS for SSB.
* Note: for ANR, when reading the MIB, the cell containing the SSB is known to the UE, as defined in 38.133 specification.

Formal objection sustained by: Huawei

Agreement:

For the case agreed in RAN1 #104bis-e where 480/960 kHz SSB location and SCS are explicitly provided to the UE (non-initial access)

* Support configuring CORESET#0/Type0-PDCCH for the purpose of ANR/PCI confusion detection by down selecting from the following two alternatives
  + Alt 1) Using dedicated signaling
  + Alt 2) Using configuration in MIB
    - Note: for ANR, when reading the MIB, the cell containing the SSB is known to the UE, as defined in 38.133 specification.

Agreement:

For 480kHz and 960kHz PRACH,

* Down-select among option 1 and 2
  + Option 1) The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.
    - FFS: supported values of the starting PRACH slot index within reference slot and whether or not the ROs for a given PRACH configuration can span more than one PRACH slot if gaps between consecutive ROs are supported for LBT and/or beam switching purposes
  + Option 2) Each 120kHz RO corresponds to 4 and 8 candidate RO positions for 480kHz and 960kHz PRACH, respectively. Information about the number and locations of 480/960kHz candidate RO(s) are configured or pre-selected within each 120kHz RO. The reference 120kHz RO is determined by the current PRACH configuration method in Rel-15/16 specification.
* Following alternatives are considered on PRACH density
  + ALT 1) At least the same density (i.e. number of PRACH slots per reference slot) as for 120kHz PRACH in FR2 is supported
    - FFS: support for higher PRACH slot density (number of PRACH slots per reference slot)
  + ALT 2) at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
    - FFS: support for higher RO density
  + An “example” illustration of PRACH slots for 480/960kHz is shown below:



* FFS: whether and how to account for LBT in RO configuration (if needed)
* FFS: whether and how to account for beam switching gap in RO configuration (if needed)

Agreement:

FFS: Support DBTW at least for 120kHz

* FFS whether DBTW will be applicable for 480/960 kHz SSB SCS
  + If DBTW is supported for 480/960kHz SSB:
    - For the case agreed in RAN1 #104bis-e where 480/960 kHz SSB location and SCS are explicitly provided to the UE (non-initial access), indication of DBTW configuration (e.g. enable/disable of DBTW,  , and DBTW length) are supported by dedicated signaling.
* For 120kHz SSB, support mechanism to distinguish at least the following scenarios:
  + Case 1) (Unlicensed with LBT off) + DBTW disabled
  + Case 2) (Unlicensed with LBT on) + DBTW enabled
  + Case 3) (Unlicensed with LBT on) + DBTW disabled
  + Case 4) (Licensed) + DBTW disabled
  + FFS: Whether/how LBT on/off is indicated in MIB
    - If not indicated in MIB, then FFS whether/how the UE determines different sizes of DCI 1\_0 with CRC scrambled by SI-RNTI
  + FFS: whether any case(s) can be combined for DBTW signaling design and how to handle implications to DCI 1\_0 size ambiguity if is not distinguished in signaling
  + FFS: whether all above cases need an explicit indication
  + FFS: Whether a single indication can be used for combination of more than one cases
* For 120 kHz SSB, enable/disable of DBTW is indicated by one or more of the following methods:
  + Option 1) signaling in MIB
    - Option 1-1) disabling DBTW is jointly coded with
    - Option 1-2) indicated by other bit fields in MIB
    - FFS: among options 1-1 and 1-2
  + Option 2) distinct GSCN used by the SSB
  + Option 3) By comparing the value of  in MIB and DBTW length after UE reads SIB1 or by comparing the value of  in MIB and default DBTW length of 5 ms before UE reads SIB1.
  + FFS: whether to support option 1, 2, 3, or any combination of the options.
  + Note: enable/disable signaling of DBTW by MIB or GSCN does not preclude other signaling methods

Agreement:

If DBTW is supported,

* Working assumption: MIB signaling to support
  + Alt A) indication of at least for 120kHz SSB
    - In this case, the total number of values of to not exceed 4
  + Alt B) Explicit indication of SSB index and/or SSB candidate location
    - FFS on the details of signaling
  + FFS betweenAlt A, or B, or supporting both
* Supported DBTW lengths
  + Alt 1) 0.5, 1, 2, 3, 4, 5 msec
    - Note: same as Rel-16 FR1 NR-U
  + Alt 2) maximum 5 msec
    - FFS other values
  + FFS between Alt 1 and 2
* Number of candidate positions when DBTW is enabled
  + For 120kHz SSB
    - FFS between 64 or 80
  + If DBTW is additionally supported for 480/960kHz SSB
    - FFS between 64 or 128

## RAN1 #106-e

Conclusion:

RAN1 will continue discussions to develop solutions for supporting DBTW

Agreement:

* For 480 and 960kHz PRACH:
  + The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.



Agreement:

* For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, X} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame.



* Alt 1: X = 8
* Alt 2: X = 9

Agreement:

For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame.

Working assumption:

For 120kHz SSB, the number of candidates SSBs in a half frame is 64.

Agreement:

For DBTW with 120kHz SCS (if supported), support DBTW lengths {0.5, 1, 2, 3, 4, 5} msec

* Note: this should be the same as Rel-16 NR-U DBTW lengths.

Agreement:

For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,

* Support the following set of parameters.

|  |  |  |
| --- | --- | --- |
| SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols |
| 1 | 24 | 2 |
| 1 | 48 | 1 |
| 1 | 48 | 2 |

* + Note: the number of entries corresponding the same {mux pattern, number of RB, number of symbol} tuple (listed above) will depend on required RB offsets that needs to be supported based on channel and sync raster design.
* FFS: addition other set of parameters

Agreement:

Do not support PRACH length L=571, 1151 for 960kHz PRACH and at least L =1151 for 480kHz PRACH.

Agreement:

For 480 and 960kHz PRACH:

* At least the same RO density in time domain (i.e. number of specified RO per reference slot according the PRACH configuration index) as for 120kHz PRACH in FR2 is supported
  + FFS: Support gap between consecutive ROs in time domain and the details to derive the gap

Agreement:

For 480 and 960kHz PRACH,

* When a PRACH slot can contain all time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching,
  + and when number of PRACH slots in a reference slot is 1,
    - for 480kHz and for 960kHz PRACH
  + and when the number of PRACH slots in a reference slot is 2,
    - for 480kHz and for 960kHz PRACH
* FFS: values, when a PRACH slot cannot contain all time domain PRACH occasions~~,~~ corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching.
* FFS: whether to allow for additional values if the maximum that can be configured for the number of FD RO’s is less than 8 (due to BW limitation)

## RAN1 #106-bis-e

Working assumption:

Support DBTW for 120 kHz.

* FFS: Support for 480 kHz and 960 kHz

Conclusion:

Do not support gap between consecutive ROs for 480kHz and 960kHz

Agreement:

Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off).

* Existing DCI size alignment in TS38.212 applies to DCI 1\_0 and 0\_0 in CSS.

Agreement:

* Indication of licensed and unlicensed operation is not explicitly indicated in MIB or PBCH payload.
  + FFS: Whether or not to indicate licensed regime by different synchronization raster entries.
* Indication of use of LBT or no-LBT is not explicitly indicated in MIB or PBCH payload.

Agreement:

No other values of n other than agreed previously is supported for 120kHz SCS, where parameter ‘n’ is the set of values to determine the first symbols of the candidate SSB blocks for 120kHz SCS in agreement from RAN1 #104-bis-e.

Working assumption:

* For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz, support multiplexing pattern 1 with 96 PRB CORESET#0, and {1, 2} symbol durations
* Note: the working assumption can be confirmed once RAN1 agrees on the number of needed SSB-CORESET0 offsets for 24 and 48 RB CORESET0 based on RAN4 channelization design

Agreement:

Additionally, support PRACH length L=571 for 480kHz

Agreement:

Support 120 kHz and 480 kHz subcarrier spacing for initial UL BWP for PCell.

Working assumption:

For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW

* If only 1 bit is needed: subCarrierSpacingCommon
* If 2 bits is needed: subCarrierSpacingCommon, and 1 bit from pdcch-ConfigSIB1 (pending CORESET0 or search space design would allows for this bit), else, use the spare-bit (not the Msg Extension bit)
  + The design of CORESET0 and search space shall be done without any consideration to this proposal
  + If 2 bits are needed for both 120kHz and 480/960kHz cases, then use the same bit field combination (i.e. use pdcch-ConfigSIB1 bit for 120/480/960 kHz or spare-bit for 120/480.960 kHz)
  + Note: If pdcch-ConfigSIB1 bit is used, the use of controlResourceSetZero (searchSpaceZero) for 120 kHz and   searchSpaceZero (controlResourceSetZero) for 480/960 kHz is not precluded
* FFS: if 3 bits are required
* Note: the working assumption can be confirmed after RAN1 agrees on the number of needed SSB-CORESET0 offsets based on RAN4 channelization design

Agreement:

For 120kHz SCS, for  values:

* If 2 bits are available in MIB for , at least support {16, 32, 64}
* If 1 bit is available in MIB for , support {32, 64}
  + FFS: methods to indicate more  values without increasing used number of bits, e.g., {16, 32, 64}
* Note: value  < 64 indicates DBTW enabled/supported and operation with shared spectrum.
* Note: For operation without shared spectrum channel access, a UE expects to be configured with  = 64. Use of =64 in shared spectrum is not precluded.
* FFS: 1 bit or 2 bits used for 

Agreement:

Supported value of n for 480/960kHz SSB slot pattern:

* ALT A) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB
  + same pattern will apply to 480kHz and 960kHz (i.e same N and M for 480 and 960 kHz)
  + N = 2, M = 8
  + FFS: starting position of n
* ALT B) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB
  + scaled version pattern will apply between 480 and 960 kHz (i.e. N and M for 480kHz, 2N and 2M for 960 kHz)
  + N = 2, M = 8
  + FFS: starting position of n
* ALT C) slots that do not contain SSB correspond to the slots that do not contain SSB in 120 kHz Case D.
  + Note: ALT 4 means that only slots 32-39 for 480 kHz SSB pattern are reserved for UL and 960 kHz SSB pattern is contiguous.

Agreement:

For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 1:

* FFS: The value of X (> 0)
* FFS: whether or not to use different X value depending on whether DBTW is ON/OFF
* FFS: whether or not to use same or different X value for 480 and 960 kHz
* FFS: whether Y = , or Y=, or whether to remove entries with Y

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Index** |  | **Number of search space sets per slot** |  | **First symbol index** |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | X | 1 | 1 | 0 |
| 3 | X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 4 | 5 | 1 | 1 | 0 |
| 5 | 5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 6 | 0 | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 7 | X | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 8 | 5 | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 9 | 5 + X | 1 | 1 | 0 |
| 10 | 5 + X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 11 | 5 + X | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 12 | 0 | 1 | 2 | 0 |
| 13 | 5 | 1 | 2 | 0 |
| 14 | Reserved | | | |
| 15 | Reserved | | | |