**3GPP TSG RAN WG1 Meeting #106-bis-e R1-2110538**

**e-Meeting, October 11 – 19, 2021**

**Source: Moderator (Intel Corporation)**

**Title: Summary #4 of email discussion on initial access aspect of NR extension up to 71 GHz**

**Agenda item: 8.2.1**

**Document for: Discussion**

# Introduction

In this contribution, we discuss aspects related to initial access for extending NR up to 71 GHz based on submitted contributions to RAN1 #106-bis-e. The main issues discussed in the following section for initial access are detailed design for synchronization signal block (SSB), CORESET#0, PRACH related issues, and discovery reference signal (DRS) related operations.

During the last RAN Plenary, the WID has been updated to reflect the approved numerologies for initial access. The following is copy of the WID objectives relevant for initial access.

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| * Physical layer aspects including [RAN1]:   + Support of up to 64 SSB beams for licensed and unlicensed operation in this frequency range.   + Supports 120kHz SCS for SSB and 120kHz SCS for initial access related signals/channels in an initial BWP.     - Study and specify, if needed, additional SCS (480kHz, 960kHz) for SSB for cases other than initial access.     - Note: coverage enhancement for SSB is not pursued.   + In addition to 120kHz, support 480 kHz SSB for initial access with support of CORESET#0/Type0-PDCCH configuration in the MIB with following constraints:     - Limited sync raster entry numbers       * It is assumed that RAN4 supports a channelization design which results in the total number of synchronization raster entries considering both licensed and unlicensed operation in a 52.6 – 71 GHz band no larger than 665 (Note: the total number of synchronization raster entries in FR2 for band n259 + n257 is 599). If the assumption cannot be satisfied, it’s up to RAN4 to decide its applicability to bands in 52.6 – 71 GHz.     - only 480kHz CORESET#0/Type0-PDCCH SCS supported for 480 kHz SSB SCS.     - Prioritize support SSB-CORESET#0 multiplexing pattern 1. Other patterns discussed on a best effort basis.     - 960 kHz numerology for the SSB is not supported by the UE for initial access in Rel-17.     - Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible     - Note: 480 kHz is an optional SSB numerology for initial access for the UE. A UE supporting a band in 52.6-71 GHz must at least support 120 kHz SCS (for initial access and after initial access)     - Note: Dependency or lack thereof for a UE supporting 480kHz and/or 960kHz numerology for data and control to also support 480kHz SSB numerology for initial access is to be tackled as part of UE capability discussion.   + Support ANR and PCI confusion detection for 120, 480 and 960kHz SCS based SSB, support CORESET#0/Type0-PDCCH configuration in MIB of 120, 480 and 960kHz SSB     - FFS: additional method(s) to enable support to obtain neighbour cell SIB1 contents related to CGI reporting     - Only 1 CORESET#0/Type0-PDCCH SCS supported for each SSB SCS, i.e., (120, 120), (480, 480) and (960, 960).     - Prioritize support SSB-CORESET#0 multiplexing pattern 1. Other patterns discussed on a best effort basis.     - Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible     - Note: From UE perspective, ANR detection for 480/960kHz SCS based SSB is not supported if the UE does not support 480/960 SCS for SSB.     - Note: for ANR, when reading the MIB, the cell containing the SSB is known to the UE, as defined in 38.133 specification.   + Specify support for PRACH sequence lengths (i.e. L=139, L=571 and L=1151) and study, if needed, specify support for RO configuration for non-consecutive RACH occasions (RO) in time domain for operation in shared spectrum |

# Summary of issues

## 2.1 SSB Aspects

### 2.1.1 DRS Related Aspects (and other MIB design other than CORESET#0/Type0-PDCCH)

* From [1] Huawei/HiSilicon:
  + For SSB with 120 kHz SCS, confirm the working assumption on 64 candidate SSBs within a half frame.
  + For SSB with 480 kHz and 960 kHz SCS, 64 candidate SSBs is sufficient for operation without shared spectrum while 128 candidate SSBs should be supported for operation with shared spectrum.
  + For operation with shared spectrum and for 480 kHz and 960 kHz SSBs, indicate the 7th bit of the candidate SSB index by borrowing the 4th LSB of SFN in the PBCH payload. Indicate the 4th LSB of SFN with spare bit in MIB payload.
  + Support discovery burst transmission window (DBTW) for all three numerologies in shared spectrum in 52.6GHz to 71GHz. At least should be indicated in MIB for all three numerologies.
  + Configure DBTW length in SIB1 for operation with shared spectrum in 52.6GHz to 71GHz with the following values:
    - 480 kHz SCS: {72, 32, 24, 16, 8, 4} slots = {2.25, 1, 0.75, 0.5, 0.25, 0.125} ms
    - 960 kHz SCS: {64, 32, 24, 16, 8, 4} slots = {1, 0.5, 0.375, 0.25, 0.125, 0.0625} ms
  + No indication for licensed or unlicensed operation is required in MIB.
  + Use of LBT should be indicated in SIB1 to help UE determine the existence of “ChannelAccess-CPext” field in DCI format 1-0/0-0. Common DCI size should be assumed for DCI format 1-0/0-0 in CSS no matter LBT is ON or OFF.
  + In operation with shared spectrum in 60 GHz, for MSB k, k≥1, of inOneGroup and MSB m, m≥1, of groupPresense of ssb-PositionsInBurst:
    - if MSB k of inOneGroup and MSB m of groupPresense are set to 1, the UE assumes that SSB(s) within DBTW with candidate SSB index(es) corresponding to SSB index equal to k-1+(m-1)×8 may be transmitted;
    - if MSB k of inOneGroup or MSB m of groupPresense are set to 0, the UE assumes that the SSB(s) are not transmitted.
  + Regardless of the value of the MSB k of inOneGroup and MSB m of groupPresense in ssb-PositionsInBurst configured in SIB1, if > , UE assumes that candidate SSB index(es) corresponding to SSB index equal to are not transmitted.
  + the MIB content and PBCH payload in Table [1]-6 and Table [1]-7should be supported for 120 kHz, 480 kHz and 960 kHz SSB.
    - Table [1]-6 MIB and PBCH payload bit allocation for 120kHz SCS SSB

|  |  |  |  |
| --- | --- | --- | --- |
| bit | | FR2-1 | FR2-2 |
|  |  | 120kHz | 120kHz |
| MIB | 0 | 10 - 5 MSB of SFN | 10 - 5 MSB of SFN |
| 1 |
| 2 |
| 3 |
| 4 |
| 5 |
| 6 | subCarrierSpacingCommon | 1 bit for (sec 2.2) |
| 7 | ssb-SubcarrierOffset | ssb-SubcarrierOffset |
| 8 |
| 9 |
| 10 |
| 11 | dmrs-TypeA-Position | dmrs-TypeA-Position |
| 12 | pdcch-ConfigSIB1  /controlResourceSetZero | controlResourceSetZero  (Sec 3.1 Table 1) |
| 13 |
| 14 |
| 15 |
| 16 | pdcch-ConfigSIB1  /searchSpaceZero | searchSpaceZero  (Sec 3.3 Table 4) |
| 17 |
| 18 |
| 19 | 1 bit for (sec 2.2) |
| 20 | cellBarred | cellBarred |
| 21 | intraFreqReselection | intraFreqReselection |
| 22 | spare | Spare bit |
| PBCH payload | 23 | 4th LSB of SFN | 4th LSB of SFN |
| 24 | 3th LSB of SFN | 3th LSB of SFN |
| 25 | 2th LSB of SFN | 3th LSB of SFN |
| 26 | 1th LSB of SFN | 3th LSB of SFN |
| 27 | half frame indication | half frame indication |
| 28 | 6th bit of candi. SSB index | 6th bit of candi. SSB index |
| 29 | 5th bit of candi. SSB index | 5th bit of candi. SSB index |
| 30 | 4th bit of candi. SSB index | 4th bit of candi. SSB index |

* + Table [1]-7 MIB and PBCH payload bit allocation 480kHz and 960kHz SCS SSB

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| bit | | FR2-1 | FR2-2 | |
|  |  | 120kHz | 480kHz and 960kHz | |
| DBTW OFF | DBTW ON |
| MIB | 0 | 10 - 5 MSB of SFN | 10 - 5 MSB of SFN | |
| 1 |
| 2 |
| 3 |
| 4 |
| 5 |
| 6 | subCarrierSpacingCommon | 1 bit for (sec 2.2) | |
| 7 | ssb-SubcarrierOffset | ssb-SubcarrierOffset | |
| 8 |
| 9 |
| 10 |
| 11 | dmrs-TypeA-Position | dmrs-TypeA-Position | |
| 12 | pdcch-ConfigSIB1  /controlResourceSetZero | controlResourceSetZero  (sec 3.2 Table 2) | |
| 13 |
| 14 |
| 15 | searchSpaceZero  (Sec 3.3 Table 5) | |
| 16 | pdcch-ConfigSIB1  /searchSpaceZero |
| 17 |
| 18 |
| 19 | 1 bit for (sec 2.2) | |
| 20 | cellBarred | cellBarred | |
| 21 | intraFreqReselection | intraFreqReselection | |
| 22 | spare | Spare bit | 4th LSB of SFN |
| PBCH payload | 23 | 4th LSB of SFN | 4th LSB of SFN | 7th bit of candi. SSB index (sec 2.1) |
| 24 | 3th LSB of SFN | 3th LSB of SFN | |
| 25 | 2th LSB of SFN | 3th LSB of SFN | |
| 26 | 1th LSB of SFN | 3th LSB of SFN | |
| 27 | half frame indication | half frame indication | |
| 28 | 6th bit of candi. SSB index | 6th bit of candi. SSB index | |
| 29 | 5th bit of candi. SSB index | 5th bit of candi. SSB index | |
| 30 | 4th bit of candi. SSB index | 4th bit of candi. SSB index | |

* From [2] Futurewei:
  + For FR2-2 120 kHz SCS support SS/PBCH DBTW.
  + For 480/960 kHz SS/PBCH DBTW should not be supported.
  + If DBTW is supported use where is the candidate SS/PBCH block index to establish a QCL relation between different SS/PBCH indexes.
  + For 120kHz SS/PBCH SCS indicate that DBTW is enabled in SIB1 and indicate LBT disabled either in MIB or in SIB1.
  + For 480/960 kHz SS/PBCH SCS use the field subCarrierSpacingCommon to indicate LBT disabled.
  + Consider whether the ssb-PositionsInBurst definition needs to be updated to support higher SCS SSB.
* From [3] Spreadtrum:
  + Confirm the working assumption that DBTW is supported at least for 120kHz SCS.
  + DBTW is supported for 480/960kHz SCS.
  + Confirm the working assumption that the number of candidate SSBs in a half frame is 64 for 120kHz SCS.
  + The number of candidate SSBs in a half frame is more than 64 and not great than 128 for 480/960kHz SCS.
  + The maximum DBTW length for 480/960kHz SCS can be 2ms and 1ms respectively.
  + The gap slots (slots without SSB) for 480/960kHz SCS can be different from that of 120kHz SCS.
* From [4] ZTE, Sanechips:
  + The following design of candidate SSBs with SCS 480/960 kHz in a half frame can be considered: First symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
    - If DBTW is not supported or DBTW is disabled
      * For 480kHz SCS, the 64 candidate SSBs are located in 32 slots, with 2 slots spacing between every 8 consecutive slots to avoid prolonged occupation, i.e. n=0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 20, 21, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 34, 35, 36, 37
      * For 960kHz SCS, the 64 candidate SSBs are located in 32 slots, with 4 slots spacing between every 16 consecutive slots to avoid prolonged occupation, i.e. n=0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35
    - If DBTW is supported and it is enabled
      * Additional 64 candidate SSB can be defined after the above original 64 candidate SSBs in the half frame
  + Discovery burst transmission window (DBTW) should be supported for all approved SSB SCS in FR2-2, including 120 kHz, 480 kHz and 960 kHz.
  + In order to reduce the impact of standardization caused by indicating candidate SSB indices, the maximum number of candidate SSBs defined in the half-frame can be kept unchanged (maintain 64) or limited to 128 for 480/960 kHz SSB SCS.
  + Four candidate values {8,16,32,64} for are preferred from the perspective of reducing bit overhead.
  + For Rel-17 above 52.6GHz, it is recommended that the UE derives the QCL relation between candidate SSBs by the value of , where is the candidate SSB index.
  + Enable/disable of DBTW can be implicitly indicated by comparing the value of  in MIB and DBTW length, and explicit signaling is not needed for this purpose.
* From [5] vivo:
  + Support DBTW in un-licensed band/LBT case from 52.6 GHz to 71 GHz for SSB with all supported SCSs.
  + Do not support explicit indication of DBTW on/off in MIB.
  + Support to use DBTW lengths {0.5, 1, 2, 3, 4, 5} msec for SCS 120 kHz, and FFS small values for SCS 480 kHz and 960 kHz.
  + Do not support LBT on/off indication in MIB.
  + The following fields could be considered to indicate the value of Q in PBCH:
    - subCarrierSpacingCommon
    - LSB of ssb-SubcarrierOffset
    - Coreset#0 and Type#0 PDCCH indication
  + When DBTW is enabled with indicated value of Q, how to interpret the meaning of ssbPositionsInBurst should be studied.
* From [8] NEC:
  + DBTW should be supported for SSB transmission with 120 kHz and 480/960 kHz SCS.
  + The long term sensing could be considered as an approach to enabling/disabling DBTW.
  + DBTW indication could be indicated per beam for SSB transmission.
  + Unlicensed/licensed operation indication should not be indicated in MIB.
  + LBT on/off indication should not be indicated in MIB.
  + The value of Q should be no lower than 16 at least.
  + The candidate SSB indication in NR-U should be reused with enhancement to indicate DBTW enabling/disabling and Q value jointly in MIB.
  + If DBTW is additionally supported for 480/960kHz SCS SSB transmission, 128 SSB candidates should be supported.
* From [9] CATT:
  + DBTW for 480/960 kHz SSB SCS can be supported with up to 128 candidate SSB index.
  + To indicate 7th bit of the candidate SSB index for 480/960 kHz SSB SCS, following schemes can be further considered and down-selected:
    - Borrowing the subCarrierSpacingCommon in MIB
    - Borrowing the 4th LSB of SFN, and move 4th LSB of SFN to subCarrierSpacingCommon in MIB
    - Borrowing half frame bit  , with all candidate SSBs are assumed to be put in first half frame when DBTW is enabling.
  + For NR operation in 60 GHz unlicensed spectrum, the discovery burst transmission window (DBTW) shall be supported for 120 KHz SSB at least when gNB configures more than 56 SSB transmissions.
  + sub-set of SSBs can be transmitted as NO-LBT and the other sub-set SSBs are transmitted as DBTW if the exempt Short Control Signaling rules can be applied by local region rule.
  + For number of ，four states {16, 32, 64, reserved/DBTW disabled} is recommend.
  + On DBTW length for SCS 480/960 KHz (if supported), scale factor is applied comparing to value of SCS 120 KHz,
  + For 120 kHz SSB, signaling in MIB can indicate enable/disable of DBTW.
  + If LBT ON/OFF state is indicated in MIB/PBCH, joint coding can be used for indication of LBT ON/OFF, DBTW enabling/disabling and one bit information for candidate SSB index.
  + If LBT ON/OFF state is not indicated in MIB/PBCH, it can be indicated in DCI 1\_0 scrambled by SI-RNTI.
* From [11] Ericsson:
  + If a DBTW is supported (not our preference), it should only be supported for 120 kHz SSB SCS and not for 480/960 kHz SSB SCS.
  + Confirm the working assumption that no additional (compared to the already supported 64) candidate SS/PBCH block positions are introduced.
  + Conclude that a DBTW is not supported.
  + If a DBTW is supported (not our preference) select one of the following options:
    - Option 1: Q and DBTW on/off indicated in MIB using the subCarrierSpacingCommon field
      * Q = [64, 32] where Q=64 indicates DBTW off
      * DCI 1\_0 size is the same for LBT on/off (unlicensed/licensed)
    - Option 2: Q and DBTW on/off indicated in SIB1
      * The subCarrierSpacingCommon field is ignored
      * Default assumption for Q depends on the agreed value range of Q and can be left to UE implementation
      * Q = [48, 32, 16, 8]. Absence of the parameter in SIB1 indicates DBTW off.
      * DCI 1\_0 size is the same for LBT on/off (unlicensed/licensed)
    - Option 3: Q indicated in SIB1 and DBTW on/off indicated in MIB using the subCarrierSpacingCommon field
      * Default assumption for Q (if DBTW on) depends on the agreed value range of Q and can be left to UE implementation
      * Q = [48, 32, 16, 8]. The parameter is only configured in SIB1 if DBTW is on
      * DCI 1\_0 size is the same for LBT on/off (unlicensed/licensed)
* From [12] Nokia, NSB:
  + The design for DBTW, if supported, is common to different sub-carrier spacings.
  + Confirm the working assumption on number of SSB candidate locations in a half frame for 120kHz:
  + For 480kHz and 960kHz, the number of SSB candidate locations in a half frame is 64.
  + If DBTW is supported,  is supported. FFS for need for other values.
  + Provide LBT on/off and DBTW indication in SIB1. (Note: licenced/unlicenced operation is assumed to be already part of SIB1 via frequency band information.)
  + Do not provide separate, additional indication for DBTW on/off in MIB. (Note it would be possible to provide the indication implicitly e.g. part of .)
* From [13] Samsung:
  + Support discovery burst transmission window for all SCSs on the 60 GHz unlicensed spectrum.
    - The indication of Q can be in MIB for a best effort, and if not possible, in SIB1;
    - The indication of DBTW disabling can be joint coded with the indication of Q, if Q is indicated in MIB; and the indication can use 1 bit in MIB, if Q is not indicated in MIB;
    - For 480 kHz and 960 kHz SCS, support 128 candidate SS/PBCH block locations within a half frame, and use one PHY bit in PBCH payload to indicate the extra candidate SS/PBCH block index (e.g. 7th LSB);
    - For initial access, different synchronization raster entries are applied for licensed and unlicensed operations; for non-initial access, support an explicit indication of licensed or licensed operation when configuring a cell.
* From [15] Intel:
  + For DRS based on SSBs with SCS 120 kHz:
    - and reuse Case D slot pattern for placement of SSB candidates
    - is indicated in MIB
      * At least the subCarrierSpacingCommon bit from MIB is reinterpreted to indicate
      * Consider 1 bit from pdcch-ConfigSIB1 in MIB to indicate from the extended set, e.g.,
        + Alternatively, the spare bit from PBCH payload could be used to indicate in addition to the subCarrierSpacingCommon bit from MIB
    - DBTW on/off is identified based on comparison of the DBTW length with the time duration occupied by transmission of SSBs
    - DBTW length is signalled in SIB1
    - Licensed vs. unlicensed operation is not signalled in MIB
      * Align sizes of DCI 1\_0 scrambled with SI-RNTI between licensed and unlicensed modes of operation
  + For DRS based on SSBs with SCS 480 kHz/960 kHz:
    - and SSB candidate slots are arranged according to Proposal 2
    - One bit from MIB is used for indexing additional SSB candidates
      * The subCarrierSpacingCommon bit from MIB is reinterpreted for this purpose
    - is indicated in MIB
      * One bit from pdcch-ConfigSIB1 in MIB is repurposed to indicate at least
    - The spare bit from PBCH payload could be used to indicate in addition to 1 bit from pdcch-ConfigSIB1 in MIB
    - DBTW length is fixed and not signalled
    - DBTW on/off is explicitly signalled in SIB1
    - Licensed vs. unlicensed operation is not signalled in MIB
      * Align sizes of DCI 1\_0 scrambled with SI-RNTI between licensed and unlicensed modes of operation
* From [16] NTT Docomo:
  + DBTW should be supported irrespective of SCS.
    - In a certain region, e.g., Japan, sensing needs to be performed for initiating any transmission by any device in 60 GHz.
  + Support to confirm the working assumption that the number of candidate SSBs with 120 kHz SCS in a half frame is 64
  + Support 64 candidate SSBs with both 480 and 960 kHz SCS
  + For DBTW to be supported in Rel-17 NR 52.6 – 71 GHz, similar to Rel-16 NR-U, support to indicate QCL parameter in MIB
    - Support to use subCarrierSpacingCommon for QCL parameter indication in MIB
  + For DBTW to be supported in Rel-17 NR 52.6 – 71 GHz, following information can be implicitly indicated via subCarrierSpacingCommon
    - Enabling/disabling of DBTW
    - Licensed/unlicensed band
    - LBT on/off
* From [17] Pansonic:
  + DBTW is supported regardless of SCS.
  + The number of candidate SSB positions is 64.
  + For values, total of 4 states are supported (e.g., {8, 16, 32, 64}).
  + For the indication of Q, SIB1 is used except the signaling method to use MIB are clarified.
  + If Q is indicated in MIB, DBTW enabled/disabled is indicated in MIB (implicitly Q=64). If Q is indicated in SIB1, DBTW enabled/disabled is indicated in SIB1.
  + DBTW lengths for 480/960 kHz SCS are scaled from 120 kHz SCS.
* From [18] Sony:
  + Discovery Burst Transmission Window should be supported for all SCSs.
  + Enabling/disabling DBTW and should be signalled in MIB
    - Indication of disabling DBTW should be jointly coded with
      * Parameter to signal indicates {8, 16, 32, or 64}
      * = 64 implies disabling DBTW
  + For indication of QCL relation and disabling DBTW in MIB, subCarrierSpacingCommon and reserved state of pdcchConfig-SIB1 should be used.
* From [19] ETRI:
  + Propose to support DBTW for all SSB SCSs and the same DBTW lengths with Rel-16 NR-U.
* From [20] Lenovo, Motorola Mobility:
  + For NR operation in unlicensed bands between 52.6 GHz and 71 GHz, potential enhancements related to periodic transmission of DRS such as SSB/PBCH/CORESET#0 are needed including:
    - performing directional LBT prior to the transmission of SSB according to the ssb-PositionsInBurst
    - directional LBT on multiple beams at the same time at the beginning of the DRS window
    - Cat 2 LBT (depending on the gap) before actual transmission
* From [21] Interdigital:
  + Support Discovery Burst (DB) and Discovery Burst Transmission Window (DBTW) in unlicensed spectrum operations that require LBT to enhance the initial access operation in beyond 52.6GHz spectrum.
  + Consider indicating enable/disable of DBTW in initial access operations based on a range of the sync raster offset.
  + Consider the enhancements to indicate the mode of operation regarding the enable/disable of the DBTW, on/off of the LBT, and the license regime based on the combination of Sync. raster offset and MIB indication.
  + Support enhancements on the reference tables in indication of Q parameter for up to 64 SSB beams in initial access operations for unlicensed spectrum in beyond 52.6GHz, e.g., subsamples of the Q parameter.
  + Support candidate SSB positions more than 64 for 120kHz SSB.
* From [22] LG Electronics:
  + For FR2-2, UE always assumes DBTW is enabled for 120 kHz SSB reception.
  + Total of 4 states (e.g., {8, 16, 32, 64}) of values are supported by using 2 bits of the followings.
    - subCarrierSpacingCommon
    - LSB(s) of ssb-SubcarrierOffset
    - dmrs-TypeA-Position
  + No MIB indication to identify operation with or without shared spectrum channel access, but SIB indication or synchronization raster differentiation to identify operation with or without shared spectrum channel access.
  + Do not indicate LBT on/off in PBCH. DCI format 1\_0 size should be aligned regardless of LBT on or off unless synchronization rasters are used to identify operation with or without shared spectrum channel access.
  + Discuss how to signal actually transmitted SSBs via ssb-PositionsInBurst when can be indicated to be less than 64 in MIB.
* From [23] Sharp:
  + Adopt DBTW for SSB with 120 or 480 or 960 kHz SCS in FR2-2 operation.
  + One MIB payload bit is used for indication of candidate SSB index for . Another MIB payload bit indicates Q related information. DBTW enabled/disabled is not explicitly indicated via MIB. These two bits are repurposed from the bit for subCarrierSpacingCommon indication and the LSB for ssb-SubcarrierOffset indication.
* From [24] Apple:
  + If DBTW is introduced, for above 52.6GHz frequency band, consider the following:
    - Re-purposing the 1-bit 'subCarrierSpacingCommon'
    - If more than one bit is needed, re-purposing 1-bit MSB of controlResourceSetZero in MIB or providing one more bit information by selecting one sequence from two candidates to scramble CRC bits of PBCH payload.
  + LBT on/off can be implicitly indicated based on the indication of DBTW enable/disable.
  + Licensed/unlicensed band can be signaled in SIB1.
  + The same DCI size is used for DCI format 1\_0 monitored in a common search space in both licensed and unlicensed band with existing padding operation.
* From [25] Convida Wireless:
  + If impact of LBT failure is not addressed, increasing the number of SSB candidate positions to above 64 to increase transmission opportunities to cope with LBT failure could be considered.
  + Increased number of candidate SSB positions for unlicensed/shared spectrum channel access with LBT could be considered for SCSs of 480KHz and 960KHz for 52.6 GHz-71 GHz.
* From [26] Qualcomm:
  + do not support discovery burst transmission window (DBTW) for SSB for SCS 480 and 960 kHz
  + for an unlicensed band that requires LBT, if DBTW for SSB is adopted for 120 kHz SSB:
    - MIB signaling to support indication of for 120 kHz SSB
    - Minimize the number of bits needed to signal (1 or 2 bits) and thus the values (2 or 4 values)
    - Enabling/disabling DBTW can be implicit in the value
    - Consider getting the bits needed from one or more of the following: controlResourceSetZero, subCarrierSpacingCommon
    - Confirm the working assumption that the number of candidate positions when DBTW is enabled = 64 for 120 kHz SSB
    - Consider having a subset of the SSBs (< 64) transmitted under the short control signal assumption while another subset can be best effort or have multiple positions per beam (have a within the subset)
  + consider increasing the size of the DCI 1\_0 for NR licensed, by adding a field, to align with the size of the corresponding DCIs for the unlicensed operation.
* From [27] WILUS:
  + We propose to support discovery burst transmission window (DBTW) for at least 120kHz SCS which makes it possible to define candidate SSB positions within the DBTW. In addition to 120kHz SCS, DBTW should be applicable for 480/960 kHz SSB SCS on supporting NR above 52.6GHz.
  + Before confirming the working assumption that the number of candidates SSBs in a half frame is 64 for 120kHz SSB, it would be necessary to consider a method for compensating for the insufficient opportunity of the SSB transmission due to LBT failures in order to perform the operation in the unlicensed band of above 52.6GHz.
  + It should be further considered that the additional candidate SS/PBCH block locations within a DBTW can be set to the closest slot locations after LBT failure at candidate SS/PBCH blocks locations as defined in FR2.

#### Summary of Discussions

The following are previous agreements on DRS aspects.

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| **RAN1 #105e**  **Agreement:**  For an unlicensed band that requires LBT, further study whether/how to support discovery burst (DB) and discovery burst transmission window (DBTW) at least for 120 kHz SSB SCS   * If DB supported   + FFS: What signals/channels are included in DB other than SS/PBCH block * If DBTW is supported   + Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs     - FFS: how to support UEs performing initial access that do not have any prior information on DBTW.   + PBCH payload size is no greater than that for FR2   + Duration of DBTW is no greater than 5 ms   + Number of PBCH DMRS sequences is the same as for FR2 * The following points are additionally FFS:   + How to indicate candidate SSB indices and QCL relation without exceeding limit on PBCH payload size   + Details of the mechanism for enabling/disabling DBTW considering LBT exempt operation and overlapping licensed/unlicensed bands * Whether or not to support DBTW for SSB SCS(s) other than 120 kHz if other SSB SCS(s) are supported   **Agreement:**   * For operation with shared spectrum channel access of NR 52.6 – 71 GHz, support discovery burst (DB) and define the DB same as in Rel-16 37.213 Section 4.0 * FFS: Support discovery burst transmission window (DBTW) at least for SSB with 120 kHz SCS with the following requirements   + PBCH payload size is no greater than that for FR2   + Duration of DBTW is no greater than 5 ms   + Number of PBCH DMRS sequences is the same as for FR2   + FFS: applicability of DBTW design for 120kHz to SSB with 480kHz and 960kHz SCS   + Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs     - FFS: how to support UEs performing initial access that do not have any prior information on DBTW.     - FFS: details of the mechanism for enabling/disabling DBTW considering LBT exempt operation and overlapping licensed/unlicensed bands     - FFS: details of how to inform UEs of the configuration of DBTW   **Agreement:**  FFS: Support DBTW at least for 120kHz   * FFS whether DBTW will be applicable for 480/960 kHz SSB SCS   + If DBTW is supported for 480/960kHz SSB:     - For the case agreed in RAN1 #104bis-e where 480/960 kHz SSB location and SCS are explicitly provided to the UE (non-initial access), indication of DBTW configuration (e.g. enable/disable of DBTW,  , and DBTW length) are supported by dedicated signaling.  * For 120kHz SSB, support mechanism to distinguish at least the following scenarios:   + Case 1) (Unlicensed with LBT off) + DBTW disabled   + Case 2) (Unlicensed with LBT on) + DBTW enabled   + Case 3) (Unlicensed with LBT on) + DBTW disabled   + Case 4) (Licensed) + DBTW disabled   + FFS: Whether/how LBT on/off is indicated in MIB     - If not indicated in MIB, then FFS whether/how the UE determines different sizes of DCI 1\_0 with CRC scrambled by SI-RNTI   + FFS: whether any case(s) can be combined for DBTW signaling design and how to handle implications to DCI 1\_0 size ambiguity if is not distinguished in signaling   + FFS: whether all above cases need an explicit indication   + FFS: Whether a single indication can be used for combination of more than one cases * For 120 kHz SSB, enable/disable of DBTW is indicated by one or more of the following methods:   + Option 1) signaling in MIB     - Option 1-1) disabling DBTW is jointly coded with  * + - Option 1-2) indicated by other bit fields in MIB     - FFS: among options 1-1 and 1-2   + Option 2) distinct GSCN used by the SSB   + Option 3) By comparing the value of  in MIB and DBTW length after UE reads SIB1 or by comparing the value of  in MIB and default DBTW length of 5 ms before UE reads SIB1.  * + FFS: whether to support option 1, 2, 3, or any combination of the options.   + Note: enable/disable signaling of DBTW by MIB or GSCN does not preclude other signaling methods   **Agreement:**  If DBTW is supported,   * Working assumption: MIB signaling to support   + Alt A) indication of at least for 120kHz SSB  * + - In this case, the total number of values of to not exceed 4  * + Alt B) Explicit indication of SSB index and/or SSB candidate location     - FFS on the details of signaling   + FFS betweenAlt A, or B, or supporting both * Supported DBTW lengths   + Alt 1) 0.5, 1, 2, 3, 4, 5 msec     - Note: same as Rel-16 FR1 NR-U   + Alt 2) maximum 5 msec     - FFS other values   + FFS between Alt 1 and 2 * Number of candidate positions when DBTW is enabled   + For 120kHz SSB     - FFS between 64 or 80   + If DBTW is additionally supported for 480/960kHz SSB     - FFS between 64 or 128   **RAN1 #106e**  Conclusion:  RAN1 will continue discussions to develop solutions for supporting DBTW  **Agreement:**  For DBTW with 120kHz SCS (if supported), support DBTW lengths {0.5, 1, 2, 3, 4, 5} msec   * Note: this should be the same as Rel-16 NR-U DBTW lengths.   Working assumption:  For 120kHz SSB, the number of candidates SSBs in a half frame is 64. |

The following is a summary of company position of various aspects of DRS.

* Supporting DBTW
  + Support: Huawei/HiSilicon, Futurewei (120kHz only), ZTE/Sanechips, vivo, NEC, Intel, Docomo, Panasonic, Sony, ETRI, Interdigital, Sharp, WILUS, LGE
  + Do not support: Ericsson (if supported only for 120kHz only), Qualcomm (not support for 480/960kHz)
* Indication of DBTW (for initial access)
  + in MIB (either explicit or implicit with Q=64):
    - implicit: ZTE/Sanechip, NEC, Samsung (if Q is indicated in MIB), Docomo, Panasonic, Sony, Sharp, Apple, Qualcomm (for 120kHz), Huawei/HiSilicon (for 120 kHz), Nokia/NSB (if number of candidate locations is restricted for 480/960kHz scs to 64)
    - no explicit signaling in MIB: vivo
    - explicit: CATT, Samsung (if Q is not indicated in MIB), Huawei/HiSilicon (for 480/960 kHz)
  + in SIB1:
    - Futurewei, Nokia/NSB
  + raster:
    - Interdigital, Samsung
  + UE always assumes DBTW is enabled for 120 kHz SSB reception, w/o indication of DBTW
    - LGE
* Supporting means of conveying candidate SSB location & SSB beams
  + Supported values:
    - 120kHz {16,32,64} : Huawei/HiSilicon
    - 480/960kHz {16,32,64} : Huawei/HiSilicon
    - {8,16,32,64}: ZTE/Sanechips, Intel (if 2 bit for Q), Panasonic, Sony, LGE
    - Min 16: NEC
    - {16, 32, 64, reserved/DBTW disabled}: CATT
    - {32, 64} 64 serves DBTW disable: Ericsson (if DBTW supported, if Q indicated in MIB, as one option)
    - {8,16,32,48} : Ericsson (if DBTW supported, if Q indicated in SIB1, as one option)
    - {32, 64}: Nokia/NSB
    - {16,64}: Intel (if 1 bit for Q)
  + Potential bits for required signaling (e.g. additional SSB index, Q) for supporting DBTW in MIB
    - subCarrierSpacingCommon: Huawei/HiSilicon, vivo, Ericsson (if DBTW supported, as one option), Intel, Docomo, Sony, LGE, Apple, Qualcomm (for 120kHz), Futurewei (for 120 kHz only)
    - controlResourceSetZero: vivo, Intel (for 480/960kHz), Sony, Apple, Qualcomm (for 120kHz), Huawei/HiSilicon (for 480/960 kHz)
    - searchSpaceZero: Huawei/HiSilicon (for 120 kHz only), vivo
    - some bits of k\_SSB: vivo, LGE
    - dmrs-typeA-position: LGE
    - spare bit (not the Msg Extension bit): Intel
    - LSB of *ssb-SubcarrierOffset* Futurewei (120 kHz only)
  + Placement of candidate SSB index in PHY portion of PBCH (not in MIB) (requires moving 1 bit of SFN from PHY portion of PBCH to MIB.
    - Support: Huawei/HiSilicon, Samsung
    - FFS: CATT
  + indication in SIB1
    - Ericsson (if DBTW supported, as one option)
* Supported DBTW lengths for 480/960 kHz (if supported)
  + For 480kHz:
    - {2.25, 1, 0.75, 0.5, 0.25, 0.125} ms : Huawei/HiSilicon
    - Max 2 ms: Spreadtrum
    - Scaled version of 120kHz case: CATT, Panasonic
    - Fixed to single value: Intel
    - Same as for 120kHz i.e. {0.5, 1, 2, 3, 4, 5} ms: Nokia
  + For 960kHz:
    - {1, 0.5, 0.375, 0.25, 0.125, 0.0625} ms : Huawei/HiSilicon
    - Max 1ms: Spreadtrum
    - Scaled version of 120kHz case: CATT, Panasonic
    - Fixed to single value: Intel
    - Same as for 120kHz i.e. {0.5, 1, 2, 3, 4, 5} ms: Nokia
* Number of SSB candidates for DBTW
  + For 120kHz:
    - confirm WA
      * Huawei/HiSilicon, Spreadtrum, Ericsson, Nokia/NSB, Intel, Docomo, Qualcomm, ETRI, LGE, Sharp
    - Wait for confirming WA after decision for 480/960kHz is made:
      * CATT
    - Support additional values of n
      * NEC
  + For 480/960kHz:
    - 64: Huawei/HiSilicon (licensed), ZTE (if DBTW not supported/disabled), Docomo, Panasonic, LGE (if supported), Nokia (if supported)
    - 64 < 128 ≤ 128: Spreadtrum
    - < 64: Interdigital,
    - 128: Huawei/HiSilicon (unlicensed), ZTE (if DBTW supported/enabled), NEC, CATT, Samsung, Intel, Convida, Sharp
* *ssb-PositionsInBurst* in SIB1
  + if MSB k of inOneGroup and MSB m of groupPresense are set to 1, the UE assumes that SSB(s) within DBTW with candidate SSB index(es) corresponding to SSB index equal to k-1+(m-1)×8 may be transmitted; if MSB k of inOneGroup or MSB m of groupPresense are set to 0, the UE assumes that the SSB(s) are not transmitted.
    - Huawei/HiSilicon
  + FFS: Futurewei, vivo, LGE
* Indication of licensed and unlicensed operation in MIB:
  + Support: [Docomo]
  + Not support: Huawei/HiSilicon, NEC, Intel, LGE, Apple, Sharp
* Indication of LBT
  + MIB: Futurewei (480/960kHz), [Docomo], Apple (implicit with DBTW)
  + SIB1: Nokia/NSB, Intel, [LGE], Sharp
  + If indicated, joint encoding with DBTW enable/disable: CATT
  + If not indicated, provide indication in DCI 1\_0 scrambled by SI-RNTI: CATT
* DCI sizes between licensed and unlicensed
  + Same size for CSS DCI 1\_0/0\_0: Huawei/HiSilicon, Ericsson, Intel, LGE (unless licensed and unlicensed operation modes are differentiated by sync raster), Apple, Qualcomm, Sharp

#### <Moderator’s Suggestion for Discussions>

Discuss further on the following proposals and issues. The proposals listed are not unanimously supported by all companies. However, more numbers of companies seem to support the proposal. Therefore, moderator suggests using the proposal as basis for further discussions (even if they may not be agreeable).

**Issue #1) Whether or not to support DBTW and number of SSB candidates**

###### Proposal 1.1-1

* Support DBTW for 120kHz, 480kHz, and 960kHz cases

###### Proposal 1.1-2

* If DBTW is supported for 480 and 960 kHz, support 128 candidate SSB positions

**Issue #2) Potential bits for required signaling for supporting DBTW in MIB**

Discuss and identify which bits are available for required signaling for supporting DBTW in MIB

* subCarrierSpacingCommon
  + Seems to be unanimous support from all companies
* controlResourceSetZero
* searchSpaceZero
* some bits of k\_SSB
* dmrs-typeA-position
* spare bit (not the Msg Extension bit)

**Issue #3) Indication of DBTW &**

###### Proposal 1.1-3

* If DBTW is supported, support implicit indication DBTW may be disabled with = 64 configuration.

###### Proposal 1.1-4

* If DBTW is supported, for values:
  + If 2 bits are available in MIB for , at least support {16, 32, 64}
  + If 1 bit is available in MIB for , support {32, 64}

**Issue #4) DCI size**

###### Proposal 1.1-5

* Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off).
* Same DCI size for DCI 0\_0 in CSS regardless of channel access mode (i.e., LBT on/off)
  + Bits will be padded, if needed, to the format with smaller DCI size between the channel access modes to match the DCI size between them.
  + Existing DCI size alignment in TS38.213 applies to DCI 1\_0 and 0\_0 in CSS.
  + FFS: DCI in USS

**Issue #5) DBTW lengths**

###### Proposal 1.1-6

* If DBTW is supported, the following DBTW length are supported for 480 and 960 kHz:
  + {2.25, 1, 0.75, 0.5, 0.25, 0.125} msec for 480 kHz.
  + {1, 0.5, 0.375, 0.25, 0.125, 0.0625} msec for 960 kHz

**Issue #6) Indication of licensed/unlicensed and LBT/no LBT in MIB**

###### Proposal 1.1-7

* Indication of licensed and unlicensed operation is not explicitly indicated in MIB content payload.
* Indication of use of LBT or no-LBT is not explicitly indicated in MIB content payload.
  + If explicit indication of DBTW disabled is supported, use of no-LBT may be inferred from DBTW disabled indication.

**Issue #7) ssb-PositionsInBurst in SIB1**

**Proposal 1.1-8**

* For ssb-PositionsInBurst in SIB1,
  + if MSB k of inOneGroup and MSB m of groupPresense are set to 1, the UE assumes that SSB(s) within DBTW with candidate SSB index(es) corresponding to SSB index equal to k-1+(m-1)×8 may be transmitted;
  + if MSB k of inOneGroup or MSB m of groupPresense are set to 0, the UE assumes that the SSB(s) are not transmitted.

#### <Outcome of 10/12 Tuesday GTW Session>

**Working Assumption**

* Support DBTW for 120kHz
  + FFS: support for 480kHz and 960kHz

#### 1st Round of Discussions

Please provide further comments on the above issues #1 ~ #7 and proposals listed. Also, if there are any other issues that require discussion, please comment them here.

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| Company | Comments |
| NTT DOCOMO | As for issue #1,   * On whether to support DBTW, while we support to confirm this and support DBTW for 480/960kHz as well, it would be ok to revisit this issue after clarifying the exact functionality of DBTW in 52.6-71GHz a bit more. * On # of candidate SSB positions, our best preference is to keep it as 64 as in FR2-1 for both 480/960kHz SCS, and to confirm WA for 120kHz SCS, since we would like to avoid a significant impact in physical layer specification to support 128 candidate SSB positions, which we think exceeds the benefit of 128 candidates. Furthermore, 128 candidate SSB positions are not possible for 120kHz SCS due to 5ms limitation. We prefer to have a unified design among 120, 480 and 960kHz SCS. On the other hand, if we need to consider 128 candidate SSB positions to support DMTW for larger SCSs, we would like to consider some other options to achieve the indication of SSB index more than 64 with minimized specification efforts, for example:   + Borrow the half frame bit in PBCH payload     - In this case, SSB burst has to be transmitted only in the first half frame or only in the last half frame   + Borrow LSB of SFN in MIB     - In this case, the frame where SSB burst is transmitted has to be limited in a certain frame   The alternatives above need to limit the exact occasions of SSB burst transmissions, while may require smaller amount of specification effort than the ones proposed already.  As for issue #2, we prefer to reuse subCarrierSpacingCommon for Q value indication in MIB.  As for issue #3, this highly depends on issue#1. We should defer the discussion.  As for issue #4, we support the Proposal 1.1-5.  As for issue #5, we do not think it is essential. Thus we propose to deprioritize the discussion.  As for issue #6, we support the Proposal 1.1-7.  As for issue #7, we think it should be discussed after determining # of candidate SSB positions. |
| OPPO | Proposal 1.1-2: support.  Proposal 1.1-3: we can accept this proposal only when 1 bit for is assumed, otherwise we think DBTW and should be configured independently, e.g., DBTW may be disabled with = 32 configuration if support {16, 32, 64}.  Proposal 1.1-4: support.  Proposal 1.1-5: not support. We think LBT on/off can be indicated in SIB, so there is no need to align the DCI sizes of LBT on/off for DCI 0\_0. We propose the following modification: *Proposal 1.1-5*  * *Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off).* * *~~Same DCI size for DCI 0\_0 in CSS regardless of channel access mode (i.e., LBT on/off)~~*   + *Bits will be padded, if needed, to the format with smaller DCI size between the channel access modes to match the DCI size between them.*   + *Existing DCI size alignment in TS38.213 applies to DCI 1\_0 and 0\_0 in CSS.*   + *FFS: DCI in USS*   Proposal 1.1-6: support.  Proposal 1.1-7: support.  Proposal 1.1-8: support. |
| Qualcomm | Issue #1 (Proposal 1.1-2): we do not support this proposal. If 480/960 kHz are agreed for DBTW, we prefer to have a common design (in terms of signaling) with SCS 120 kHz, i.e. use 64 candidate SSB, since we do not see a need to differentiate 480/960 kHz.  Issue #2:   * subCarrierSpacingCommon: yes, this is already freed since SCS of SSB = SCS of CORESET0 * controlResourceSetZero: This depends on the outcome of the CORESET0 design. We can restrict it to be only 3-bits (8 possible values) to spare one bit for Q. In the current specs, only 3 bits are used for 120 kHz SCS SSB for the valid combinations for this WI. However, this may not become available if more combinations are supported (e.g., 96 RBs).   Issue #3:   * Proposal 1.1-3: We are fine with this proposal * Proposal 1.1-4: We are fine with this proposal   Issue #4 (Proposal 1.1-5): We are fine with this proposal  Issue #5 (Proposal 1.1-6): May be good to defer this until the SSB pattern and the number of SSB candidate positions are agreed  Issue #6 (Proposal 1.1-7): We are fine with this proposal  Issue #7 (Proposal 1.1-8): We prefer to defer this until other SSB/DBTW details are agreed |
| Lenovo, Motorola Mobility | Issue #1 We do not support having 128 SSB candidates for 480/960 kHz. We agree with DOCOMO that we should avoid a significant impact in physical layer specification to support 128 candidate SSB positions and prefer a common signalling design for 120 kHz, 480 kHz, and 960 kHz.  Issue #2 subCarrierSpacingCommon bits can be used for signalling  Issue #3 We are fine with the proposal  Issue #4 support the proposal  Issue #5 This depends on the number of SSB candidates and their positions, so we can deprioritize it until that has been agreed.  Issue #6 support the proposal |
| Samsung | Proposal 1.1-2: We support the proposal. Increasing the number of candidate SSB locations to allow more transmission opportunities is the most essential feature for DBTW, and that’s not possible for 120 kHz simply due to the limited number of slots in a half frame, but such restriction is not applicable for 480 and 960 kHz. We also want to note that for Rel-16 NR-U, the number of candidate SSB locations for 15 kHz and 30 kHz are different, and SCS-specific design was supported at that time, so we didn’t see any technical issue to support more than 64 candidate SSB locations for 480 and 960 kHz only.  Proposal 1.1-3: Whether this proposal works or not depend on whether we support more than 64 candidate locations. Also, we don’t prefer an implicit method for indicating DBTW is off, since for licensed band UE, the UE needs to assume to support the feature of DBTW, and then determines Q=64 to imply DBTW is off, then why not explicitly configure the DBTW is off?  Proposal 1.1-4: We believe this is related to Proposal 1.1-3, and should be resolved together after knowing the number of candidate SSB locations.  Proposal 1.1-5: We are ok with the proposal.  Proposal 1.1-6: This is also related to the number of candidate SSB locations.  Proposal 1.1-7: We don’t have strong concern on this proposal, but it would be good to be combined with the decision on DBTW on/off indication. If a UE cannot decide whether DBTW is on/off from MIB, we cannot accept this proposal.  Proposal 1.1-8: This should be part of the RRC parameter discussion, and we believe there are obvious typos in the proposal to be resolved for clarity. |
| Interdigital | **Proposal 1.1-1**: Support DBTW for 120kHz, 480kHz, and 960kHz cases  **Proposal 1.1-2**: For the number of candidate SSB indexes, in shared spectrum if the number of candidate SSB positions is equal to maximum number of beams, i.e. 64, then the DBTW cannot function as it is supposed to. The whole support for DBTW is to enable SSB retransmissions in candidate SSB positions due to LBT failure. So, we support the candidate SSB positions to be more than 64, that is:   * For 120kHz, support at least 80 candidate SSB positions * For 480 and 960 kHz, support 128 candidate SSB positions  **Proposal 1.1-3**: We do not support implicit indication of DBTW enable/disable as it might cause ambiguity given that UE might not know the license regime.**Proposal 1.1-4**: We support the proposed values.**Proposal 1.1-5:** We support the proposal.**Proposal 1.1-6**: We support the proposal. **Proposal 1.1-7**: We do not support the proposal. We propose to indicate the license regime based on sync raster offset. |
| LG Electronics | Proposal 1.1-2: We do not support this proposal. As indicated in GTW session, we prefer a common design of DBTW for all SCSs. Thus, 64 candidate SSB positions are supported for all SCSs in FR2-2.  Issue #2: In addition to subCarrierSpacingCommon, we can consider some bits of k\_SSB (but RAN4 should be involved to confirm whether those can be re-purposed) or dmrs-typeA-position.  Proposal 1.1-3: We do not support this proposal. Particularly for 120 kHz, considering WA to support 64 candidate SSB positions, UE behavior with Q=64 assuming DBTW is disabled is exactly same as UE behavior with Q=64 assuming DBTW is enabled. Therefore, it is not necessary to let UE know whether DBTW is enabled or disabled. Instead, UE can always assume that DBTW is enabled at least for 120 kHz SSB reception.  Proposal 1.1-4: Support  Proposal 1.1-5: We think if channel access mode can be informed to UE prior to SIB reception (e.g., by using sync raster), assuming different DCI size based on channel access mode is possible. In that sense, we suggest the modification as follows (in addition, editorial in the spec reference): Proposal 1.1-5 If channel access mode (i.e., LBT on/off) is not informed to UE before SIB reception,   * Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off). * Same DCI size for DCI 0\_0 in CSS regardless of channel access mode (i.e., LBT on/off)   + Bits will be padded, if needed, to the format with smaller DCI size between the channel access modes to match the DCI size between them.   + Existing DCI size alignment in TS38.212 applies to DCI 1\_0 and 0\_0 in CSS.   + FFS: DCI in USS   Proposal 1.1-6: We can accept this proposal but can be deferred similar to other companies’ views.  Proposal 1.1-7: We prefer not to explicitly/implicitly indicate licensed/unlicensed operation and LBT on/off MIB. In this sense, we suggest the following: Proposal 1.1-7  * Indication of licensed and unlicensed operation is not indicated in MIB content payload. * Indication of use of LBT or no-LBT is not indicated in MIB content payload.   Proposal 1.1-8: It seems premature to try to converge a specific scheme for ssb-PositionsInBurst indication in SIB1. Maybe it could be a starting point to keep the size of ssb-PositionsInBurst field same as in legacy SIB1 signaling. |
| Ericsson | Issue #1  For 120 kHz, the details of the full solution must be known before the working assumption can be confirmed, e.g., how DBTW and Q are signaled.  **We do not support Proposal 1.1-2**. If 480 and 960 kHz are to be supported, then it must be a common solution for all 3 subcarrier spacings based on 64 candidate positions. We do not wish to re-open the discussion on how to signal more than 64 candidate SSB positions – the issues are no different than for 120 kHz, and the potential solutions discussed in prior meetings are all unattractive and involve changes to implementation of the MIB/PBCH processing. One solution required low level changes to the PBCH scrambling procedures. Another solution violated the Rel-15 principle that the MIB should be constant over 80 ms.  Issue #2  **In our view, the discussion should be limited to subCarrierSpacingCommon and the spare bit**. We don't agree to repurposing of controlResourceSetZero since it is not yet known if more than 8 entries in the CORESET0 configuration table are needed, i.e., there is a RAN4 dependence on channelization design. searchSpaceZero is not feasible since there are fewer than 8 reserved value, so no bit is available. We don't agree to repurposing of k\_SSB as there is a RAN4 dependence on channelization design. Furthermore, unlike Rel-16, it is unlikely that the design would result in only even or odd values of k\_SSB being needed, so no bit is available.  Issue #3  **Proposal 1.1-3 and 1.1-4 need to be merged together and discussed as a package**. We can agree to the meged proposal, **conditioned on using one or both of the ssbSubCarrierSpacingCommon and spare bits**. This is the most efficient way forward considering the RAN4 dependence discussed in Issue #2.  Issue #4  We support Proposal 1.1.5, except that we think that **the 2nd bullet may not be needed**.  In our understanding, in the Rel-16 definition of DCI 0\_0 in 38.212, padding bits are added to equalize the size of DCI 0\_0 for licensed/unlicensed. For unlicensed, 2 fewer padding bits are added.  Issue #5  **We do not support Proposal 1.1-6 (yet)**. The values of n for the SSB time domain pattern (Section 2.1.2) need to be agreed first.  Issue #6  We support the 1st two bullets of Proposal 1.1-7, but **we do not support the 3rd bullet**. Just because the DBTW is disabled, it doesn't mean that LBT is not used for other signals/channels, e.g, if the short control signaling provision is used for SSB.  Issue #7  This is a 2nd level issue, and should be deferred until DBTW design is stable. |
| ETRI | For Issue #1, we prefer common design for DBTW regardless of SCS, however also open to increase the number of candidate SSB positions if the specification impact is limited.  For Issue #2, ‘subCarrierSpacingCommon’ can be considered as the first priority, and then other bit(s) can be considered depending on the output of other issues (e.g., CORESET#0 design, sync raster, and so on)  For Issue #3, we support both Proposal 1.1-3 and Proposal 1.1-4.  For Issue #4, we support Proposal 1.1-5.  For Issue #5, we prefer to defer this issue until the details on SSB and DBTW are agreed.  For Issue #6, we support Proposal 1.1-7.  For Issue #7, we prefer to defer this issue until the details on SSB and DBTW are agreed. |
| Sharp | Issue #1  We support Proposal 1.1-2. It is reasonable to support DBTW also for 480kHz and 960kHz cases, if the principle is to have consistent design/function among SCSs. Consequently, 128 candidate SSB positions should be supported to enable effective DBTW and Q functions.  Issue #2  It becomes clear that 1 bit of *subCarrierSpacingCommon* could be repurposed. Whether 1 bit from *controlResourceSetZero* depends on the final design of CORESET#0.  Since some of the following issues depend on the outcome of Issue #1 and Issue #2, it seems better to firstly resolve Issue #1 and Issue #2.  Issue #3  We share the same view to discuss this issue after determinations on the number of candidate SSB positions and available MIB bits.  Issue #4  We are fine with Proposal 1.1-5.  Issue #5  Discuss this issue after determinations on the number of candidate SSB positions.  Issue #6  We support Proposal 1.1-7.  Issue #7  Discuss this issue after determinations on the number of candidate SSB positions. |
| Intel | Issue#1)  **Proposal 1.1-2:** Support.  We think it’s important to support DBTW for 480 kHz/960 kHz and the number of SSB candidates as 128 for these SCS values as part of DBTW operation.  Differently from SCS 120 kHz, the operation with SCS 480 kHz/960 kHz will rely heavily on highly directional beamforming to compensate the coverage shrinkage happened with the increase of SCS. Eventually, this will require a larger number of beams including those ones carrying SSBs. Therefore, a typical operation scenario for SCS 480 kHz/960 kHz is to utilize about 64 beams for SS burst transmission which is the current maximum. However, limiting the number of SSB candidates to 64 effectively means operation without DBTW in the typical usage scenario of SCS 480 kHz/960 kHz (which is with the large number of beams). At the same time, regulations of some countries require LBT operation for unlicensed spectrum from 52.6 GHz up to 71 GHz and do not define anything similar to short control signalling exemption. One example is Japan (please see or tdoc and the reference therein for details).  From those ones don’t supporting DBTW for SCS 480 kHz/960 kHz or other ones supporting only up to 64 SSB candidates, we would like to understand how to address the situation when LBT operation is mandatory and there are no short control signalling exemption rules defined.  Issue #2)  Among the bits/fields in MIB we believe the following can be repurposed in 60 GHz.  subCarrierSpacingCommon, spare bit  also if RAN4 supports fixed channel raster definitions, we believe it will be possible to take 1 bit from controlResourceSetZero, and 1bit from LSB of k\_ssb, while supporting mux pattern 1 and 3 with 24, 48 and 96 PRBs.  Issue #3)  **Proposal 1.1-3:** Fine with the proposal assuming it is for SCS 120 kHz. In the proposal’s text the clarification is needed that this is for SCS 120 kHz.  **Proposal 1.1-4:** Fine with the proposal assuming it is for SCS 120 kHz. In the proposal’s text the clarification is needed that this is for SCS 120 kHz.  Issue #4)  **Proposal 1.1-5:** Support.  Issue#5)  **Proposal 1.1-6:** Do not support.  Our preference is a single value for DBTW length (may be different for 480 kHz and for 960 kHz) that need not to be signalled. This potentially allows to reduce the amount of signalling.  Issue #6)  **Proposal 1.1-7:** Support.  Issue#7)  **Proposal 1.1-8:** Fine with the proposal assuming it is for SCS 120 kHz. In the proposal’s text the clarification is needed that this is for SCS 120 kHz. |
| vivo | 1.1-2: Support. And the potential bits can be selected from the following indication:   * subCarrierSpacingCommon * controlResourceSetZero * searchSpaceZero   1.1-3: There is no need to discuss this specific proposal. If the number of candidate SSBs is still 64 for 480K and 960K SCS, UE follows the defined behavior with Q. When Q=64, the behavior is the same as that DBTW is off and there is no need to agree this proposal again. If the number of candidate SSBs is 128 for 480K and 960K SCH, I don’t think Q=64 could imply DBTW is off. In our view, there is no need to know whether DBTW on/off in MIB. In this case, the only benefit is less PDCCH monitoring when receiving SIB.  1.1-4: Support.  1.1-5: It is better to discuss the DCI size issue after the decision of whether support the LBT on/off indication before SIB reception.  1.1-6: The design of DBTW length is highly depend on the SSB candidate number and the SSB resource pattern design. Thus it is better to postpone this discussion.  1.1-7: Support.  1.1-8: Fine to discuss this when DBTW details are agreed. |
| Huawei, HiSilicon | **Proposal 1.1-1:** Support   * We believe that DBTW is required for 480/960 kHz as short control signaling exemption cannot be used in all regions.   **Proposal 1.1-2:** Support   * 128 candidate SSB position facilitates enabling DBTW when 64 SSB indexes are used. 64 SSB for higher numerologies seems to be a more practical use case than smaller values.   **Issue #2)**   * Support using 2 bits for indicating (which may include explicit DBTW ON/OFF indication for 480/960 kHz). 2 bits are obtained from:   + *subCarrierSpacingCommon* (1 bit) for 120/480/960 kHz.   + *searchSpaceZero* (1 bit) for 120 kHz and *controlResourceSetZero* (1 bit) for 480/960 kHz   + Note 1:     - We suggest one searchSpaceZero Table for 120 kHz and one searchSpaceZero Table for 480/960 kHz. As discussed in R1-2108767, not all entries of searchspaceZero Table 13-12 for FR2-1 are required to be supported for 120 kHz in FR2-2 as, unlike FR2-1 that supports {CORESET#0, SSB}= {120, 240} kHz, FR2-2 only supports the same numerology for SSB and CORESET#0. This renders O values 2.5 and 7.5 useless for 120 kHz searchspaceZero Table for FR2-2. Therefore, 1 bit from searchSpaceZero Table for 120 kHz in FR2-2 can be saved.     - Also, based on WID which prioritizes Mux Pattern 1 for new numerologies, we do not see the need to support Mux Pattern 3 for 480/960 kHz. This facilitates saving 1 bit from controlResourceSetZero for 480/960 kHz.   + Note 2: Based on the input from some other companies, we recognize that there may be other reasonable ways to save a bit from searchSpaceZero and/or controlResourceSetZero. We are open to discuss these alternatives as well. * Support using 1 spare bit of MIB to indicate the 4th LSB of SFN when 128 candidate SSB is used in 480/960 kHz. Instead, use the 4th LSB of SFN in PBCH payload to indicate the 7th candidate SSB index.   + Note: Note that this does not violate the 80 ms MIB periodicity in Rel15/16.   **Proposal 1.1-3:** Suggest modification  We can support the proposal if this is limited to 120 kHz. Note that “implicit indication DBTW may be disabled with = 64” seems to be at odds with Proposal 1.1-2 which propose to support 128 candidate SSBs for 480/960 kHz. To our understanding, agreeing to Proposal 1.1-3 “as is” implies that max 64 candidate SSBs for 480/960 kHz are agreed. We suggest the following change  Proposal 1.1-3 (update)  For 120 kHz, if DBTW is supported, support implicit indication DBTW may be disabled with = 64 configuration  **Proposal 1.1-4:** Support  **Proposal 1.1-5:** Suggest modification  The first sub-bullet is at odds with the second sub-bullet. In Rel-15/16, the DCI 0\_0 in CSS is padded or truncated to match the size of DCI 1\_0 in CSS as mentioned in the following lines from 38.212:   |  | | --- | | Step 0:  - Determine DCI format 0\_0 monitored in a common search space according to clause 7.3.1.1.1 where  is the size of the initial UL bandwidth part.  - Determine DCI format 1\_0 monitored in a common search space according to clause 7.3.1.2.1 where  is given by  - the size of CORESET 0 if CORESET 0 is configured for the cell; and  - the size of initial DL bandwidth part if CORESET 0 is not configured for the cell.  - If DCI format 0\_0 is monitored in common search space and if the number of information bits in the DCI format 0\_0 prior to padding is less than the payload size of the DCI format 1\_0 monitored in common search space for scheduling the same serving cell, a number of zero padding bits are generated for the DCI format 0\_0 until the payload size equals that of the DCI format 1\_0.  - If DCI format 0\_0 is monitored in common search space and if the number of information bits in the DCI format 0\_0 prior to truncation is larger than the payload size of the DCI format 1\_0 monitored in common search space for scheduling the same serving cell, the bitwidth of the frequency domain resource assignment field in the DCI format 0\_0 is reduced by truncating the first few most significant bits such that the size of DCI format 0\_0 equals the size of the DCI format 1\_0. |   Therefore, we suggest the following modification: Proposal 1.1-5 (modified)  * Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off). * Same DCI size for DCI 0\_0 in CSS regardless of channel access mode (i.e., LBT on/off)   + ~~Bits will be padded, if needed, to the format with smaller DCI size between the channel access modes to match the DCI size between them.~~   + Existing DCI size alignment in ~~TS38.213~~ TS 38.212 applies to DCI 1\_0 and 0\_0 in CSS.   + FFS: DCI in USS   **Proposal 1.1-6:** Support **Proposal 1.1-7:** Suggest modification  * First, we assume that “MIB content payload” means “MIB or PBCH payload”. However, we prefer to clarify this in the proposal. * Second, we think that DBTW may be disabled but still LBT is used. Therefore, in general, an indication (implicit or explicit) of DBTW disabled cannot be used to infer no-LBT. However, this does not result in any problem during initial access. As it has been clarified already, the only reason that UE may need to know LBT on/off before reading SIB1 is to determine the size of DCI 1\_0 scrambled with SI-RNTI to avoid two blind decoding on DCI size. However, if we unify the size of DCI 1\_0 scrambled by SI-RNTI for the cases of LBT/No-LBT (as suggested in Proposal 1.1-5) UE does not need to know LBT/No-LBT Mode before reading SIB1. LBT/No-LBT mode can then be indicated in SIB1.  **Proposal 1.1-7 (modified)**  * Indication of licensed and unlicensed operation is not explicitly indicated in MIB ~~content~~ or PBCH payload. * Indication of use of LBT or no-LBT is not explicitly indicated in MIB ~~content~~ or PBCH payload.   + ~~If explicit indication of DBTW disabled is supported, use of no-LBT may be inferred from DBTW disabled indication.~~   **Proposal 1.1-8:** Support  Note that Proposal 1.1-8 on its own is the normal UE behavior in Rel-15/16. We think what is more important to agree is the following subsequent Proposal which clarifies UE behavior when Q is configured in operation with shared spectrum. We understand that the support of Q and DBTW are still under discussion, but, given the WA on the support of DBTW for 120 kHz, we think that the following proposal can also be agreed as a WA for 120 kHz.  **Proposal:**  Regardless of the value of the MSB k of inOneGroup and MSB m of groupPresense in ssb-PositionsInBurst configured in SIB1, if > , UE assumes that candidate SSB index(es) corresponding to SSB index equal to are not transmitted. |
| ZTE, Sanechips | Proposal 1.1-2: We are open to Proposal 1.1-2 as long as one bit is available to indicate candidate SSB index.  Proposal 1.1-3: We think the current Proposal 1.1-3 can only apply to 120 kHz SCS. If DBTW and 128 candidate SSBs are supported for 480/960kHz SCS, the implicit method in Proposal 1.1-3 can not work. So Proposal 1.1-3 can be modified as below.   * If DBTW is supported for 120kHz, support implicit indication DBTW may be disabled with = 64 configuration.   Proposal 1.1-4: Support.  Proposal 1.1-5: Support  Proposal 1.1-6: DBTW length for 480 and 960 kHz depends on the number of candidate SSB positions and the values of ‘n’.  Proposal 1.1-7: Support  Proposal 1.1-8: The interpretation of ssb-PositionsInBurst can be discussed later when the DBTW related is finalized. |
| Sony | For Issue #1, we support Proposal 1.1-1 and Proposal 1.1-2. However, since these proposals make an impact on MIB signalling, we can revisit it after discussion on MIB signalling is more stable.  For Issue #2, at least subCarrierSpacingCommon can be used for signalling of Q. If more bits will be required, controlResourceSetZero and searchSpaceZero could be considered, although it depends on the design of CORESET#0/search space.  For Issue #3, we support Proposal 1.1-3 and Proposal 1.1-4.  For Issue #4, we support Proposal 1.1-5.  For issue #5, Proposal 1.1-6 is related to SSB location discussion.  For Issue #6, we support Proposal 1.1-7.  For Issue #7, Proposal 1.1-8 should be discussed after SSB location is agreed. |
| Panasonic | Issue #1: For Proposal 1.1-2, we prefer 64 candidate SSB positions. We agree 128 candidate SSB positions would be useful especially for Q=64. However, even if 128 candidate SSB positions are available, SSB transmission cannot be guaranteed due to LBT failure. Considering the trade-off between the benefit and specification efforts, 64 candidate SSB positions with a common design with 120 kHz SCS would be preferable.  Issue #2: We agree that at least subCarrierSpacingCommon can be used  Issue #3: We are fine with Proposal 1.1-3 and Proposal 1.1-4.  Issue #4: We are fine with Proposal 1.1-5.  Issue #5: We prefer to defer this issue until SSB resource pattern (section 2.1.2) is concluded (although Proposal 1.1-6 is aligned our view).  Issue #6: We are fine with Proposal 1.1-7.  Issue #7: We are fine with Proposal 1.1-8 at least for 120 kHz SCS. |
| NEC | Issue#1  We support both Proposal 1.1-1 and 1.1-2. For 480/960kHz SCS, 128 SSB candidates can provide more transmission opportunity for each SSB in a term of cyclic transmission. At the same time, one more bit should be considered to indicate 128 candidate positions.  In addition, we also share the same view with InterDigital that 80 candidate SSB positions should be supported for 120kHz SCS.  Issue#2  According to the related discussion till now, subCarrierSpacingCommon could be used at least, controlResourceSetZero, searchSpaceZero and even one bit from k\_ssb also may be considered based on the pending decision about CORESET#0 and mux pattern. While for the spare bit, we think it should be kept as it is. We are open to discuss all these choices.  Issue#3 For Proposal 1.1-4, as mentioned by several companies, if this proposal is for the case of 120kHz, we support the proposal.  Issue#4 We support the Proposal 1.1-5.  Issue#5 We agree with the view from some companies to defer this discussion and determine the SSB candidate number firstly.  Issue#6 We support Proposal 1.1-7.  Issue#7 We think it also should be deferred after determining candidate SSB positions. |
| Nokia | **Issue #1)**  Like expressed we think that it is sufficient to have 64 candidate SSB positions for 480kHz and 960kHz and if DBTW is supported for 480/960kHz we can (thereby) align the design for all sub-carrier spacings. This would allow to introduce DBTW design for all sub-carrier spacings on one go. Hence,  Proposal 1.1-2: Do not support with 128 candidate, we can consider DBTW for 480kHz and 960kHz with 64 positions.  **Issue #2)** and **Issue #3)**  With max 64 candidate positions, we think that =64 could be used as implicit disabling of DBTW. To limit the number of bits needed, we think ={32,64} could be used. This way *subCarrierSpacingCommon* can be used to indicate the value (also providing the implicit disabling of DBTW). However, if 2nd bit is needed, we would prefer to use the spare bit to limit specification impact. So,  Proposal 1.1-4): We think that 1 bit would suffice, but fine with the principle. However we think that in case of 2 bits we could still consider 64 as implicit disabling, thus 4th value for could be selected.  **Issue #4)**  In my understanding UE would need only two hypotheses in the initial cell selection phase, thus there does not seem to be any complexity increase. Thus we think that this discussion can be postponed until other aspects has been addressed. Thus,  Proposal 1.1-5): we don’t support.  **Issue #5)**  As noted in our paper, for 120kHz the DBTW length is not very well aligned with the SSB burst length, thus there is no clear necessity for the change. Secondly, if we were to change the values to align with SSB burst, we need first agree the SSB slot pattern.  Proposal 1.1-6): we don’t support.  **Issue #6)**  Proposal 1.1-7): we are OK with the proposal.  **Issue #7)**  Like noted earlier, we think implicit disabling with =64 could be considered (with max 64 candidate positions, which is pending for 480/960kHz) as the UE behavior would not be affected.  Proposal 1.1-3): we would be OK with this proposal.  In my understanding current *ssb-PositionsInBurst* could be kept, event with different values, thus:  Proposal 1.1-8): we don’t support the proposal |
| Futurewei | **Issue #1)**  Proposal 1.1-1: Support DBTW for 120kHz. For 480kHz, and 960kHz cases, we do not see it necessary. Short Control Signaling can be used. We could live with it if the majority wants it.  Proposal 1.1-2: We prefer 64 candidates, if DBTW for 480kHz and 960kHz is supported.  **Issue #2) and Issue # 3)**  *subCarrierSpacingCommon* field may be used together with an additional bit to indicate a smaller set of 3 values for may be considered, so one combination can be used to disabled DBTW or LBT.  We ae OK with the proposal 1.1-4.  **Issue #4)**  We are OK with the Proposal 1.1-5  **Issue #5)**  We are OK with the Proposal 1.1.-6  **Issue #6)**  We are OK in principle with the Proposal 1.1.-7, however if DBTW is not supported for 480/960 it would require an explicit signaling for No LBT/LBT. The issue can be addressed after decision on DBTW.  **Issue #7)**  We are OK with the Proposal 1.1.-3  We prefer to wait for more discussions on candidate SSB position for the Proposal 1.1-8. For 120 kHz SCS we can support it. |
| Apple | **Issue 2:**  Proposal 1.1-3: In addition to ‘subCarrierSpacingCommon’ bit, the bit ‘controlResourceSetZero’. Given the dependency on CORESET table, we suggest deferring this discussion after CORESET#0 is settled.  **Issue 3:**  Proposal 1.1-4: We are ok with this proposal.  **Issue 4:**  Proposal 1.1-5: Yes.  On FFS, we do not realize any issue for DCI in USS as the size of fallback DCI format in USS can be different with that in CSS already since Rel-15. Also, different fallback DCI formats can be different across different UEs in legacy.  **Issue 5:**  Proposal 1.1-6: Prefer to defer discussion after SSB pattern is concluded.  **Issue 6:**  Proposal 1.1-7: Support the proposal.  **Issue 7:**  Proposal 1.1-8: We are ok with the proposal and support HW’s proposal on UE behavior.  In our view, there is no dependency with DBTW discussion as we agreed to support DBTW at least for 120kHz SCS. The signaling of Q value and DBTW size have no impact on this issue of interpretation SIB-1 SSB position signaling. Hence, we fail to see the reason to defer this after completing DBTW design. |
| Convida Wireless | **Issue #1) Whether or not to support DBTW and number of SSB candidates** Proposal 1.1-1 – we support the proposal We support DBTW for 120kHz, 480kHz, and 960kHz cases Proposal 1.1-2 – we support the proposal If DBTW is supported for 480 and 960 kHz, support 128 candidate SSB positions  **Issue #2) Potential bits for required signaling for supporting DBTW in MIB**  We prefer to use subCarrierSpacingCommon, controlResourceSetZero and spare bit. We are open for searchSpaceZero, some bits of k\_SSB, dmrs-typeA-position  **Issue #3) Indication of DBTW &** Proposal 1.1-4 – we support the proposal **Issue #4) DCI size** Proposal 1.1-5 – we are open for further discussion **Issue #5) DBTW lengths** Proposal 1.1-6 – we are ok with the proposal. **Issue #6) Indication of licensed/unlicensed and LBT/no LBT in MIB** Proposal 1.1-7 – we are open for it. **Issue #7) ssb-PositionsInBurst in SIB1** Proposal 1.1-3 – we are open for it Proposal 1.1-8 – we are open for further discussion |

#### <Summary of 1st Round of Discussions>

Issue #1)

Proposal 1.1-2) If DBTW is supported for 480 and 960 kHz, support 128 candidate SSB positions

* Support: OPPO, Samsung, Interdigital, ETRI, Sharp, Intel, vivo, Huawei/HiSilicon, ZTE/Sanechips (if 1 bit is available), Sony, NEC, Convida Wireless
  + Support of 128 was not possible in 120kHz due to exceeding half radio frame, for 480/960 there is no technical barrier to support 128
  + 480/960kHz SSB is expected to less coverage compared to 120kHz SSB. Use of 64 beams with LBT is essential for 480/960kHz (more so than 120kHz).
  + SSB with LBT operation is needed for regulatory domain without short control signal exemption (e.g. Japan)
* Not support (i.e. 64 candidates): Docomo, Qualcomm, Lenovo/Motorola Mobility, LGE, Ericsson, Panasonic, Nokia/NSB, Futurewei
  + Benefits of 128 candidates does not outweigh specific effort needed
  + Common design between 120/480/960
  + Supporting 128 may require some bits to be swapped between MIB (RRC IE) and PBCH content in L1

Issue #2)

* subCarrierSpacingCommon
  + Seems to be unanimous support from all companies
  + Docomo, Qualcomm, Lenovo/Motorola Mobility, LGE, Ericsson, ETRI, Sharp, Intel, vivo, Huawei/HiSilicon, Sony, Panasonic, NEC, Nokia/NSB, Futurewei, Apple, Convida Wireless
* controlResourceSetZero
  + Qualcomm (depends on design), Sharp (depends on design), Intel (depending on RAN4 design), vivo, Huawei/HiSilicon, Sony (depends on design), NEC, Apple, Convida Wireless
* searchSpaceZero
  + vivo, Huawei/HiSilicon (O=2.5 or 7.5 is not useful for 120kHz, mux pattern 3 is not needed for 480/960kHz), Sony (depends on design), NEC
* some bits of k\_SSB
  + LGE (need check with RAN4), Intel (depending on RAN4 design), NEC, [Convida Wireless]
* dmrs-typeA-position
  + LGE, [Convida Wireless]
* spare bit (not the Msg Extension bit)
  + Ericsson, Intel, Nokia/NSB, Convida Wireless

Issue #3)

Proposal 1.1-3

* Support: OPPO (only if 1 bit for Q), Qualcomm, Lenovo/Motorola Mobility, ETRI, Intel (for 120kHz), ZTE/Sanechips (for 120kHz), Sony, Panasonic, Nokia/NSB, Futurewei, Convida Wireless
* Not support: Samsung, Interdigital, LGE (can always assume DBTW is enabled), Huawei/HiSilicon (for 120kHz)
  + Having an explicit signaling is better
  + Should above ambiguity at the UE
* defer: Docomo, Sharp, vivo (can always assume DBTW is enabled)
* merge with 1.1-4: Ericsson

Proposal 1.1-4

* Support: OPPO, Qualcomm, Interdigital, LGE, ETRI, Intel (for 120kHz), vivo, Huawei/HiSilicon, ZTE/Sanechips, Sony, Panasonic, NEC (for 120kHz), Nokia/NSB (1bit preferred), Futurewei, Apple, Convida Wireless
* Not support:
* defer: Docomo, Samsung, Sharp
* merge with 1.1-3: Ericsson

Issue #4)

Proposal 1.1-5

* Support: Docomo, Qualcomm, Lenovo/Motorola Mobility, Samsung, Interdigital, LGE(if modified to 1.1-5A?), Ericsson (2nd bullet not needed), ETRI, Sharp, Intel, Huawei/HiSilicon (if modified to 1.1-5A?), ZTE/Sanechips, Sony, Panasonic, NEC, Futurewei, Apple
* Not support: OPPO (remove DCI 0\_0 text), Nokia/NSB
  + No need to align as LBT on/off can be indicated in SIB
* defer: vivo

Issue #5)

Proposal 1.1-6

* Support: OPPO, Interdigital, LGE, Huawei/HiSilicon, Futurewei, Convida Wireless
* Not support: Intel, Nokia/NSB
  + Since the SSB burst are short, do not need various DBTW lengths. Single length should be sufficient.
  + 120kHz the DBTW length is not very well aligned with the SSB burst length, thus there is no clear necessity for the change
* defer: Docomo, Qualcomm, Lenovo/Motorola Mobility, Samsung, LGE, Ericsson, ETRI, vivo, ZTE/Sanechips (DBTW length depends on supported values of n), Sony, Panasonic, NEC, Apple

Issue #6)

Proposal 1.1-7

* Support: Docomo, OPPO, Qualcomm, Lenovo/Motorola Mobility, ETRI, Sharp, Intel, vivo, Huawei/HiSilicon (with modification in 1.1-7A), ZTE/Sanechips, Sony, Panasonic, NEC, Nokia/NSB, Futurewei, Apple
* Not support: Samsung (can be ok if DBTW is explicitly signaled), Interdigital, LGE, Ericsson (support bullet 1 and 2, do not support bullet 3)
* Further discuss: Convida Wireless

Issue #7)

Proposal 1.1-8

* Support: OPPO, Intel (for 120kHz), Huawei/HiSilicon, Panasonic (for 120kHz), Apple
* Not support: Nokia/NSB
* defer: Docomo (after # of candidates), Qualcomm, LGE, Ericsson, vivo, ZTE/Sanechips, ETRI, Sharp, Sony, NEC, Futurewei
* should be discussed in RRC discussion: Samsung
* Further discuss: Convida Wireless

#### 2nd Round of Discussions

**Issue #1)**

Company views are split for number of candidate positions (15 company for 128 vs. 10 company for 64). Technical merits and motivation have been discussed. The following is a summary of current status.

* 128 candidate: OPPO, Samsung, Interdigital, ETRI, Sharp, Intel, vivo, Huawei/HiSilicon, ZTE/Sanechips (if 1 bit is available), Sony, NEC
  + Support of 128 was not possible in 120kHz due to exceeding half radio frame, for 480/960 there is no technical barrier to support 128
  + 480/960kHz SSB is expected to less coverage compared to 120kHz SSB. Use of 64 beams with LBT is essential for 480/960kHz (more so than 120kHz).
  + SSB with LBT operation is needed for regulatory domain without short control signal exemption (e.g. Japan)
* 64 candidates: Docomo, Qualcomm, Lenovo/Motorola Mobility, LGE, Ericsson, Panasonic, Nokia/NSB, Futurewei
  + Benefits of 128 candidates does not outweigh specific effort needed
  + Common design between 120/480/960
  + Supporting 128 may require some bits to be swapped between MIB (RRC IE) and PBCH content in L1

Moderator suggest for RAN1 to decide on either Proposal 1.1-2A or 1.1-2B. Please provide additional comments. Try to refrain from repeating the same comments. Provide comments that were not addressed before.

**Proposal 1.1-2A**

* DBTW is supported for 480 and 960 kHz and supports 64 candidate SSB positions

**Proposal 1.1-2B**

* DBTW is supported for 480 and 960 kHz and supports 128 candidate SSB positions

**Issue #2) Which bits are used for DRS operation in MIB**

subCarrierSpacingCommon field seems to be safe choice for using for DBTW operation. Several companies commented that controlResourceSetZero, searchSpaceZero, k\_SSB, and can be used conditioned that RAN4 design allows to use them. The spare-bit is another field that has zero impact to operations for NR and specifically design for this type of situations. Given that 60 GHz enhancements are not likely to be approved for release 18, use of the spare-bit could be viable option as NR system for 60GHz will not change MIB anytime soon for any enhancements, not until release 19 and even at that time, it is unclear the spare bit in MIB will be needed.

Based on the observations, moderator suggest the following proposal.

**Proposal 1.9**

* For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW
  + If only 1 bit is needed: subCarrierSpacingCommon
  + If 2 bits is needed: subCarrierSpacingCommon, and spare-bit (not the Msg Extension bit)
  + FFS: if 3 bits are required

Added proposal based on Qualcomm comments

###### Proposal 1.9A

* For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW
  + If only 1 bit is needed: subCarrierSpacingCommon
  + If 2 bits is needed: subCarrierSpacingCommon, and controlResourceSetZero (pending CORESET0 design that it allows for this bit), else, use the spare-bit (not the Msg Extension bit)
  + FFS: if 3 bits are required

**Proposal 1.9B**

* For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW
  + If only 1 bit is needed: subCarrierSpacingCommon
  + If 2 bits is needed: subCarrierSpacingCommon, and controlResourceSetZero (pending CORESET0 or search space design would ~~that it~~ allow~~s~~ for this bit), else, use the spare-bit (not the Msg Extension bit)
  + FFS: if 3 bits are required

**Issue #3) Indication of DBTW &**

Companies generally seem to be ok with Proposal 1.1-3 and 1.1-4. One company mentioned that they should be merged together. Based on comments, moderator has updated the proposal in 1.1-4A.

###### Proposal 1.1-4A

* For 120kHz SCS~~If DBTW is supported~~, for values:
  + If 2 bits are available in MIB for , at least support {16, 32, 64}
  + If 1 bit is available in MIB for , support {32, 64}
  + support implicit indication DBTW, where DBTW may be disabled with = 64 configuration.
    - When = 64 is indicated UE may assume DBTW is always used at least until successful decoding of SIB1
  + FFS: 1 bit or 2 bits used for

Added based on LG’s comments

**Proposal 1.1-4B**

* For 120kHz SCS~~If DBTW is supported~~, for values:
  + If 2 bits are available in MIB for , at least support {16, 32, 64}
  + If 1 bit is available in MIB for , support {32, 64}
  + ~~support implicit indication DBTW, where DBTW may be disabled with = 64 configuration.~~
    - When = 64 is indicated UE may assume DBTW is always used at least until successful decoding of SIB1
  + FFS: 1 bit or 2 bits used for

Added based on Samsung’s comments

**Proposal 1.1-4C**

* For 120kHz SCS~~If DBTW is supported~~, for values:
  + If 2 bits are available in MIB for , at least support {16, 32, 64}
  + If 1 bit is available in MIB for , support {32, 64}
  + ~~support implicit indication DBTW, where DBTW may be disabled with = 64 configuration.~~
    - ~~When = 64 is indicated UE may assume DBTW is always used at least until successful decoding of SIB1~~
  + For operation without shared spectrum channel access, a UE expects to be configured with = 64, which implies the DBTW is not applicable
  + FFS: 1 bit or 2 bits used for

Added based on Ericsson comments

**Proposal 1.1-4D**

* For 120kHz SCS~~If DBTW is supported~~, for values:
  + If 2 bits are available in MIB for , at least support {16, 32, 64}
  + If 1 bit is available in MIB for , support {32, 64}
  + support implicit indication DBTW, where DBTW may be disabled with = 64 configuration.
    - ~~When = 64 is indicated UE may assume DBTW is always used at least until successful decoding of SIB1~~
  + FFS: 1 bit or 2 bits used for

**Issue #4) DCI size**

While companies seem to be generally ok with Proposal 1.1-5, few companies have commented to further update the proposal. Moderator has updated the proposal in 1.1-5A.

**Proposal 1.1-5A**

* If channel access mode (i.e., LBT on/off) is not informed to UE before SIB reception,
  + Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off).
  + Same DCI size for DCI 0\_0 in CSS regardless of channel access mode (i.e., LBT on/off)
    - ~~Bits will be padded, if needed, to the format with smaller DCI size between the channel access modes to match the DCI size between them.~~
    - Existing DCI size alignment in TS38.~~213~~ 212 applies to DCI 1\_0 and 0\_0 in CSS.
    - FFS: DCI in USS

Added based on Samsung comments

**Proposal 1.1-5B**

* ~~If channel access mode (i.e., LBT on/off) is not informed to UE before SIB reception,~~
* Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off).
* Same DCI size for DCI 0\_0 in CSS regardless of channel access mode (i.e., LBT on/off)
  + ~~Bits will be padded, if needed, to the format with smaller DCI size between the channel access modes to match the DCI size between them.~~
* Existing DCI size alignment in TS38.~~213~~ 212 applies to DCI 1\_0 and 0\_0 in CSS.
* FFS: DCI in USS

**Issue #5) DBTW lengths**

Large number of companies asked to defer this discussion until number of candidates are determined. Moderator suggests revisit this issue once Issue #1 is resolved.

**Issue #6) Indication of licensed/unlicensed and LBT/no LBT in MIB**

While companies seem to be generally ok with Proposal 1.1-7, few companies have commented to further update the proposal. Moderator has updated the proposal in 1.1-7A.

###### Proposal 1.1-7A

* Indication of licensed and unlicensed operation is not ~~explicitly~~ indicated in MIB or PBCH ~~content~~ payload.
* Indication of use of LBT or no-LBT is not ~~explicitly~~ indicated in MIB or PBCH ~~content~~ payload.
  + ~~If explicit indication of DBTW disabled is supported, use of no-LBT may be inferred from DBTW disabled indication.~~

Added proposal based on Samsung comments

**Proposal 1.1-7B**

* Indication of licensed and unlicensed operation is not explicitly indicated in MIB or PBCH ~~content~~ payload.
* Indication of use of LBT or no-LBT is not explicitly indicated in MIB or PBCH ~~content~~ payload.
  + ~~If explicit indication of DBTW disabled is supported, use of no-LBT may be inferred from DBTW disabled indication.~~

**Issue #7) ssb-PositionsInBurst in SIB1**

Large number of companies asked to defer this discussion until number of candidates are determined. Moderator suggests revisit this issue once Issue #1 is resolved. However Apple pointed out the definition for ssb-PositionsInBurst doesn’t have to do much for 120kHz SCS case. Moderator thinks many companies prefer to have common design for 120kHz and 480/960kHz and therefore would like to wait for 480/960kHz DBTW support is resolved before concluding on the options.

Moderator suggests revisit this issue once Issue #1 is resolved.

Please provide comments on the proposals. Quick summary of request from moderator:

* Issue #1) provide comments on 1.1-2A and 1.1-2B. Refrain from comments that were mentioned before (e.g. we support X, or previous listed motivations for support) and try to provide comments that were not address before.
* Issue #2) provide comments on 1.1-9
* Issue #3) provide comments on 1.1-4A
* Issue #4) provide comments on 1.1-5A
* Issue# 5) revisit once issue #1 is resolved
* Issue #6) provide comments on 1.1-7A
* Issue #7) revisit once issue #1 is resolved

|  |  |
| --- | --- |
| Company | Comments |
| LG Electronics | Proposal 1.1-9: Support  Proposal 1.1-4A: As we commented before, UE doesn’t need to know whether DBTW is enabled or disabled. This is because “UE behavior for Q=64 assuming DBTW is disabled” is exactly same as “UE behavior for Q=64 assuming DBTW is enabled”. For Q<64, UE will assume DBTW is enabled. Therefore, UE can always assume that DBTW is enabled regardless of which value for is indicated. With this regard, we suggest as follow: Proposal 1.1-4A  * For 120kHz SCS~~If DBTW is supported~~, for values:   + If 2 bits are available in MIB for , at least support {16, 32, 64}   + If 1 bit is available in MIB for , support {32, 64}   + ~~support implicit indication DBTW, where DBTW may be disabled with = 64 configuration.~~     - When = 64 is indicated UE may assume DBTW is always used at least until successful decoding of SIB1   + FFS: 1 bit or 2 bits used for   Proposal 1.1-5A: Support  Proposal 1.1-7A: Support |
| vivo | Issue #1: Support 1.1-2B  Issue #2: Support 1.1-9  Issue #3: Agree with LG  Issue #4: Support 1.1-5A  Issue #6: Support 1.1-7A |
| DOCOMO | * Issue #1) We would like to clarify our current standpoint a little bit more: our priority is to support DBTW regardless of SCS in 52.6-71GHz. Although we prefer 64 in terms of the expected specification impacts (mainly), we are now open to compromise a bit more. For an essential issue to support 128, i.e. how to indicate SSB index more than 63, we prefer to minimize the specification efforts, i.e., we would like to achieve this by repurposing bits in MIB or PBCH payload which does not require much additional specification impacts. There is one bit available already, i.e. subCarrierSpacingCommon, but we would like to use it for Q indication as supported in Rel-16 NR-U. As another way, we may be able to borrow MSB of SFN in PBCH payload, but it requires to support alternative way to indicate SFN, which may require much specification impacts. Alternately, we may be able to consider restricting SSB burst transmission occasion to make e.g. LSB of SFN or HFB available. It will not require additional specification effort to indicate complete SFN or HFB, although SSB occasion is limited. Once RAN1 can find out a middle ground to support 128 candidate SSB positions, we can live with 128. * Issue #2) We are fine to support Proposal 1.1-9 * Issue #3) We are fine to support Proposal 1.1-4A * Issue #4) We are fine to support Proposal 1.1-5A * Issue# 5) Ok to revisit once issue #1 is resolved, although we do not see any strong need to do so. * Issue #6) We are fine to support Proposal 1.1-7A * Issue #7) Agree to revisit once issue #1 is resolved |
| Samsung | * Proposal 1.9: We are ok with the proposal. * Proposal 1.1-4A: We have to say if this proposal is adopted, there is no chance to discuss 128 candidate SSB locations for 480/960 kHz, so we prefer to discuss it after the number of candidate SSB locations is finalized. Also, we have concern on the third bullet, since it has uncertain UE behavior and didn’t address the case of UE in licensed band. For 64 candidate SSB locations, if Q=64, for a unlicensed band UE, it doesn’t matter DBTW is on or off, since the UE behavior is exactly the same; but for a licensed band UE, it should only expect to be indicated as Q=64 such that it can assume DBTW is off, and the assumption that DBTW is always on until reading SIB1 is not proper for licensed band. We suggest the following wording to address our comment:   + ~~support implicit indication DBTW, where DBTW may be disabled with = 64 configuration.~~     - ~~When = 64 is indicated UE may assume DBTW is always used at least until successful decoding of SIB1~~   + For operation without shared spectrum channel access, a UE expects to be configured with = 64, which implies the DBTW is not applicable * Proposal 1.1-5A: Adding the main bullet is strange: what’s the DCI size if channel access mode if informed to the UE before SIB reception? Also, if a UE can implicitly determine a channel access mode (e.g. from a Q value), does it apply to the condition in main bullet or not? We believe the original wording is more clear. * Proposal 1.1-7A: We prefer to add “explicitly” back, since it’s possible that the UE can infer information on LBT mode based on the value of Q implicitly. For example, if Q<64, then the UE knows this should be an unlicensed band and LBT is used for SSB transmission. |
| Intel | Issue #1)  Support Proposal 1.1-2B.  One of the arguments from the supporters of Proposal 1.1-2A was the unified design between SCS 120 kHz and SCS 480 kHz/960 kHz which is nice to have but technically is not justified while implying inferior functionality for SCS 480 kHz/960 kHz.  During last RAN1 meeting there were hot debates around the number of candidate SSBs for SCS 120 kHz. And we were among ones proposed larger than 64 SSB candidates. However, for the sake of compromise, we agreed on the working assumption to have max 64 SSB candidates for SCS 120 kHz. Now, as long as companies’ views has been split almost equally and for the sake of compromise, we ask to agree on 128 candidate SSBs for SCS 480 kHz/960 kHz. At least as another working assumption. To us, this would be fair.  Issue #2)  Proposal 1.9 – Support.  Issue #3)  Proposal 1.1-4A – Support.  Issue #4)  Proposal 1.1-5A – Support.  Issue #6)  Proposal 1.1-7A – Support. |
| Interdigital | **Issue #1)** We do not support Proposal 1.1-2A. We support Proposal 1.1-2B.  Considering Issue#1 and Issue#3 together, the support for only 64 candidate SSB positions undermines the whole support of the DBTW for maximum SSB beams of 64 in shared spectrum channel access. The main purpose of transmitting SSB bursts within DBTWs in to enable transmission of the missed SSB blocks due to the LBT failure in the candidate SSB positions. If only 64 candidate positions are considered and in case there are 64 SSB beams and some of them are missed, there remains no more candidate positions to transmit them.  Therefore, assuming different values for Q parameter and enable/disable of DBTW in Issiue #3 cannot make sense if the main purpose of DBTW cannot be fulfilled. In other words, the reason that many companies are providing for not supporting the 128 candidate positions in Issue#1 is the specification impact and how to signal the 7th bit. Whereas 2 bits are being discussed to be allocated to Q parameter in Issue #3 that basically makes no sense if no extra candidate positions are available within DBTW.  **Issue #2)** We support Proposal 1.1-9  **Issue #3)** We support Proposal 1.1-4A. Again, this proposal cannot be applicable if extra SSB candidate positions as discussed in Issue #1 are not considered.  **Issue #4)** We Proposal 1.1-5A  **Issue# 5)** We are OK to defer this discussion.  **Issue #6)** We do not support Proposal 1.1-7A. License regime should be indicated explicitly either through MIB or synch raster. |
| Qualcomm | Proposal 1.1-2A/ Proposal 1.1-2B: we do not support these 2 proposals as we do not support DBTW for 480/960 kHz. If BDTW is supported for 480/960 kHz, we prefer 64 candidate SSBs  Proposal 1.9: for 2-bits, instead of the spare bit, we would like to still consider controlResourceSetZero after CORESET0 design is finalized (since if we can get the bit from there if the table is not changed, which will be for free). Hence we propose changes in red:   * For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW   + If only 1 bit is needed: subCarrierSpacingCommon   + If 2 bits is needed: subCarrierSpacingCommon, and controlResourceSetZero (pending CORESET0 design that it allows for this bit), else, use the spare-bit (not the Msg Extension bit)   + FFS: if 3 bits are required   Proposal 1.1-4A: fine with this proposal  Proposal 1.1-5A: fine with this proposal  Proposal 1.1-7A: fine with this proposal |
| Lenovo, Motorola Mobility | Proposal 1.9: Support  Proposal 1.1-4A: Support  Proposal 1.1-5A: Support  Proposal 1.1-7A: Support |
| Moderator | Added the proposals based on company comments. Please provide inputs on edits being proposed by Companies as well. |
| Qualcomm | For the updated proposals:  Proposal 1.9A: fine with this proposal  Proposal 1.1-4B/C: prefer Proposal 1.1-4A wording  Proposal 1.1-5A/B: fine with both proposals  Proposal 1.1-7A/B: fine with both proposals |
| Sharp | * Issue #2: We support Proposal 1.1-9 and agree that subCarrierSpacingCommon can provide 1 bit for DRS relatated indication. For the 2 bits case, we believe it is necessary to confirm with RAN2 on using the spare bit. 3 bits seems to be very difficult due to the dependency on other topics. Might be better to constrain discussions on 1 bit or 2 bits. * Issue #3: Our discussion here is based on assuming that the 1 bit is available in MIB for DBTW and . We think even with 1 MIB bit indication, {16, 32, 64} can be supported. E.g., “0” indicates Q = 64 (equally saying DBTW is disabled). “1” indicates Q = 16 or 32 when gNB transmits SSBs. UE makes the QCL assumption considering Q = 16. If the practical Q value used by gNB is 32, the cost is increasing of PDCCH blind decoding load, but the procedure works with 1 MIB bit indication. * Issue #4: We support Proposal 1.1-5A. * Issue# 5) revisit once issue #1 is resolved: Agree with moderator’s suggestion. * Issue #6: We support Proposal 1.1-7A. * Issue #7) revisit once issue #1 is resolved: Agree with moderator’s suggestion. |
| Apple | **Proposal 1.9:** We can be ok if it is major companies’ preference.  However, it should be noted that there is only ‘1’ sparse bit in MIB and the bar using this bit is extremely high in the past RAN2 discussions.  Prefer **Proposal 1.9A.**  **Proposal 1.1-4A**: Support.  **Proposal 1.1-5A**: Support  **Proposal 1.1-7A**: Support. |
| CATT | Proposal 1.1.-2B : Support  P1.9A: support  P1.1-4A: support  P1.1-5: Don’t support. More clarification is needed here.The UE should be able to implicitly determine channel access mode from DCI\_1\_0.  Issue #7: agree to revisit after issue#1. |
| LG Electronics | Proposal 1.9A: We can accept this proposal.  Several questions/comments to Samsung:   * Proposal 1.1-4C: For the added sub-bullet (For operation without shared spectrum channel access, a UE expects to be configured with = 64, which implies the DBTW is not applicable), how can a UE know whether the cell is operated with or without shared spectrum channel access before Q is indicated to the UE? Do you assume initial access or non-initial access case? * Proposal 1.1-5B: What I intended for “If channel access mode (i.e., LBT on/off) is not informed to UE before SIB reception,” is that if UE can be aware of LBT on or off based on sync raster or explicit indication in MIB, UE can assume proper DCI size without size alignment as in Rel-16. For sure, it may depend on RAN4 sync raster design. In case RAN4 decide not to differentiate LBT on or off by using sync raster, then we can go with Proposal 1.1-5B. |
| OPPO | **Proposal 1.1-2A/2B**: Prefer proposal 1.1-2B but can accept proposal 1.1-2A.  **Proposal 1.1-4C**: Support  **Proposal 1.1-7A**: Support. |
| Ericsson | Issue #1)  Proposal 1.1-2A: Support only if it is agreed "common design for 120/480/960"  Proposal 1.1-2B: Do not support  Issue #2)  Proposal 1.9: Support  Proposal 1.9A: Do not support  Issue #3)  Proposal 1.1-4A: Support if sub-bullet "…UE may assume DBTW .." is removed. If DBTW is off (e.g., for licensed) why should the UE assume that DBTW is used?  Proposal 1.1-4B: Do not support  Proposal 1.1-4C: Do not support since DBTW can be off for unlicensed as well (however, we do agree with the last bullet about licensed spectrum)  Issue #4)  Proposal 1.1-5A: Support, but do we need the bullet for DCI 0\_0?  Proposal 1.1-5B: Okay, but do we need the bullet for DCI 0\_0?  Issue #6)  Proposal 1.1-7A: Okay.  Proposal 1.1-7B: Okay |
| Panasonic | Issue #2) Our preference is Proposal 1.9A to avoid using the spare bit as much as possible.  Issue #3) We are fine with Proposal 1.1-4C. For Proposal 1.1-4A and Proposal 1.1-4B, we share similar view with Ericsson that the need of sub-bullet “When = 64 is indicated UE may assume DBTW is always used at least until successful decoding of SIB1” would be unclear.  Issue #4) We are fine with either Proposal 1.1-5A or Proposal 1.1-5B.  Issue #6) We are fine with either Proposal 1.1-7A or Proposal 1.1-7B. |
| Huawei, HiSilicon | **Issue #1:**   * Support Proposal 1.1-2B   **Issue #2:** We prefer to use spare bit as the last resort for this (ie when 3 bits are required). So, we don’t support 1.1-9. We suggest a new Proposal based on Proposal 1.1.9A: Proposal 1.1-9B   * For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW   + If only 1 bit is needed: subCarrierSpacingCommon   + If 2 bits is needed: subCarrierSpacingCommon, and controlResourceSetZero or ‘searchSpaceZero’ (pending CORESET0 or search space design would allow for this bit), else, use the spare-bit (not the Msg Extension bit)   + FFS: if 3 bits are required   **Issue #3:**  We support “implicit indication DBTW, where DBTW may be disabled with = 64 configuration” in Proposal 1.1-4A but we don’t understand if such an indication is provided in MIB ( = 64 is set), how and why the UE would assume that “When = 64 is indicated UE may assume DBTW is always used at least until successful decoding of SIB1”. This sounds quite conflicting to us.  We suggest the following proposal based on 1.1-4A: Proposal 1.1-4D  * For 120kHz SCS~~If DBTW is supported~~, for values:   + If 2 bits are available in MIB for , at least support {16, 32, 64}   + If 1 bit is available in MIB for , support {32, 64}   + support implicit indication DBTW, where DBTW may be disabled with = 64 configuration.     - ~~When = 64 is indicated UE may assume DBTW is always used at least until successful decoding of SIB1~~   + FFS: 1 bit or 2 bits used for   **Issue #4)**  Support Proposal 1.1-5 and not support 1.1-5A. We prefer just to unify the size and avoid unnecessarily wasting a bit in MIB for LBT indication.  **Issue #6):**  Support Proposal 1.1-7A |
| ZTE, Sanechips | Issue #1: Support 1.1-2B  Issue #2: Prefer 1.1-9A  Issue #3: support 1.1-4C or 1.1-4D.  Besides, We suggest that Moderator can add a new issue, that is how to use to obtain the QCL relationship between different candidate SSBs. This is a problem that must be solved, but it was not covered in the previous discussion. For FR2-2, the UE can not derive the QCL relation between candidate SSBs if it reuses Rel-16 NR-U mechanism, i.e. according to the value of .  Issue #4: Among Proposal 1.1-5A and 1.1-5B, we support 1.1-5B  Issue #5: Support Moderator’s suggestion.  Issue #6: Among Proposal 1.1-7A and 1.1-7B, Support 1.1-7A.  Issue #7: Support Moderator’s suggestion. |

#### <Summary of 2nd Round of Discussions>

##### **Issue #1) candidate SSB in DRS and DBTW support**

Proposal 1.1-2A

* DBTW is supported for 480 and 960 kHz and supports 64 candidate SSB positions

Proposal 1.1-2B

* DBTW is supported for 480 and 960 kHz and supports 128 candidate SSB positions

Summary of support for 1.1-2A:

* Support: Docomo, Lenovo/Motorola Mobility, LGE, Panasonic, Nokia/NSB, Futurewei
* Conditional support: Ericsson (only if common design for 120/480/960)
* Not support but if had to choose can live with: Qualcomm
  + Benefits of 128 candidates does not outweigh specific effort needed
  + Common design between 120/480/960
  + Concerns on how 128 candidates signaling will be achieved as the changes are non-trivial in specification (e.g. Supporting 128 may require some bits to be swapped between MIB (RRC IE) and PBCH content in L1)

Summary of support for 1.1-2B:

* Support: OPPO, Samsung, Interdigital, ETRI, Sharp, Intel, vivo, Huawei/HiSilicon, ZTE/Sanechips (if 1 bit is available), Sony, NEC, Convida Wireless, CATT
  + Support of 128 was not possible in 120kHz due to exceeding half radio frame, for 480/960 there is no technical barrier to support 128
  + 480/960kHz SSB is expected to less coverage compared to 120kHz SSB. Use of 64 beams with LBT is essential for 480/960kHz (more so than 120kHz).
  + Only having 64 candidates undermines support of DBTW. If 64 candidates are supported, no need to optimize Q signaling in MIB.
  + SSB with LBT operation is needed for regulatory domain without short control signal exemption (e.g. Japan)
  + Unified design between 120/480/960 looks nice but not technically justified

##### **Issue #2) bits utilized in PBCH for signaling DBTW**

The following is summary of views. It looks like companies are converging on this issue. Suggest continuing discussion over email.

Proposal 1.9

* Support: LGE, vivo, NTT Docomo, Samsung, Intel, Interdigital, Lenovo/Motorola Mobility, [Sharp], [Apple]
* Not support: Huawei/HiSilicon

Proposal 1.9A

* Support: Qualcomm, Apple, CATT, LGE, Panasonic
* Do not support: Ericsson

Proposal 1.9B

* Support: Huawei/HiSilicon

##### **Issue #3) Indication of DBTW and values of Q**

Proposal 1.1-4A

* Support: vivo, Docomo, Intel, Interdigital, Qualcomm, Lenovo/Motorola Mobility
* Defer: Samsung, Apple, CATT, Panasonic

Proposal 1.1-4B

* Support: LGE (proposed 4B)
* Do not support: Ericsson, Panasonic

Proposal 1.1-4C

* Support: Samsung (proposed 4C), OPPO, Panasonic
* Do not support: Ericsson

Proposal 1.1-4D

* Support: Ericsson, Huawei/HiSilicon

##### **Issue #4) DCI size alignment**

The following is summary of views. It looks like companies are converging on this issue. Suggest continuing discussion over email.

Proposal 1.1-5A

* Support: LGE, vivo, Docomo, Intel, Interdigital, Qualcomm, Lenovo/Motorola Mobility, Sharp, Apple, [Ericsson (remove bullet for 0\_0)], Panasonic,
* Not support: CATT Huawei/HiSilicon (support 1.1-5)

Proposal 1.1-5B

* Support: Samsung (prefer 5B wording over 5A), Qualcomm, [Ericsson (remove bullet for 0\_0)], Panasonic

##### **Issue #5) DBTW lengths – discussion deferred**

##### **Issue #6) Indication of licensed/unlicensed and LBT/no LBT in MIB**

The following is summary of views. It looks like companies are converging on this issue. Suggest continuing discussion over email.

Proposal 1.1-7A

* Support: LGE, vivo, Docomo, Intel, ~~Interdigital~~, Qualcomm, Lenovo/Motorola Mobility, Sharp, OPPO, Ericsson, Apple, Huawei/HiSilicon
* Not support: Samsung (add explicit back), Interdigital

Proposal 1.1-7B

* Support: Samsung (proposed 7B), Qualcomm, Ericsson
* Not support:

##### **Issue #7) ssb-PositionsInBurst in SIB1**

Further discussion seems needed.

#### 3rd Round of Discussions

##### **Issue #1) candidate SSB in DRS and DBTW support**

###### Proposal 1.1-2A

* DBTW is supported for 480 and 960 kHz and supports 64 candidate SSB positions

###### Proposal 1.1-2B

* DBTW is supported for 480 and 960 kHz and supports 128 candidate SSB positions

Summary of support for 1.1-2A (64 candidates):

* Support: Docomo, Lenovo/Motorola Mobility, LGE, Panasonic, Nokia/NSB, Futurewei
* Conditional support: Ericsson (only if common design for 120/480/960)
* Not support but if had to choose can live with: Qualcomm
  + Benefits of 128 candidates does not outweigh specific effort needed
  + Common design between 120/480/960
  + Concerns on how 128 candidates signaling will be achieved as the changes are non-trivial in specification (e.g. Supporting 128 may require some bits to be swapped between MIB (RRC IE) and PBCH content in L1)

Summary of support for 1.1-2B (128 candidates):

* Support: OPPO, Samsung, Interdigital, ETRI, Sharp, Intel, vivo, Huawei/HiSilicon, ZTE/Sanechips (if 1 bit is available), Sony, NEC, Convida Wireless, CATT
  + Support of 128 was not possible in 120kHz due to exceeding half radio frame, for 480/960 there is no technical barrier to support 128
  + 480/960kHz SSB is expected to less coverage compared to 120kHz SSB. Use of 64 beams with LBT is essential for 480/960kHz (more so than 120kHz).
  + Only having 64 candidates undermines support of DBTW. If 64 candidates are supported, no need to optimize Q signaling in MIB.
  + SSB with LBT operation is needed for regulatory domain without short control signal exemption (e.g. Japan)
  + Unified design between 120/480/960 looks nice but not technically justified

Companies are asked to provide comments that adequately captured by the above summary, include your support for specific Proposal.

From moderator’s understanding if no agreement can be made, then DBTW will not be supported for 480/960kHz. While moderator doesn’t fully understand the implications of this in regulatory regions that require LBT and do not have short control signal exemption rules like ETSI, moderator would like to get comments from companies on whether they are ok with accepting no agreement for 480/960kHz and have RAN1 continue work further and develop specification with the understanding 480/960kHz will not support DBTW.

From the views, moderator notes there are significant number of companies are in support of DBTW, so moderator assumes that not having DBTW is an outcome that is favored by the majority. Because of this please provide comments on how you think you can compromise.

Please provide comments and ideas on how we can proceed as a group as well. Please provide comments on what companies are willing to accept as compromise, and please be trying to take the spirit of compromise seriously. Not agreeing to anything in the end only hurts the industry and impacts successful completion of the WID. This is especially more important since it is unlikely 60 GHz will have any enhancement WI for release 18. RAN1 does not have the luxury to enhance and revisit in later releases, once wrong choices have been made.

##### **Issue #2) bits utilized in PBCH for signaling DBTW**

The following is summary of views. It looks like companies are converging on this issue.

**Proposal 1.1-9**

* For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW
  + If only 1 bit is needed: subCarrierSpacingCommon
  + If 2 bits is needed: subCarrierSpacingCommon, and spare-bit (not the Msg Extension bit)
  + FFS: if 3 bits are required

###### Proposal 1.1-9B

* For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW
  + If only 1 bit is needed: subCarrierSpacingCommon
  + If 2 bits is needed: subCarrierSpacingCommon, and controlResourceSetZero (pending CORESET0 or search space design would ~~that it~~ allow~~s~~ for this bit), else, use the spare-bit (not the Msg Extension bit)
  + FFS: if 3 bits are required

Below is a summary of company positions.

Proposal 1.9

* Support: LGE, vivo, NTT Docomo, Samsung, Intel, Interdigital, Lenovo/Motorola Mobility, [Sharp], [Apple]
* Not support: Huawei/HiSilicon

Proposal 1.9B

* Support: Huawei/HiSilicon, [Qualcomm], [Apple], [CATT], [LGE], [Panasonic]
* Do not support: Ericsson

Moderator suggest to avoid dependency much as possible. Moderator realizes that time to time having agreements that have dependency was needed for progress, but still good to avoid them.

Moderator would like to note that there are two spare bits in PBCH. One is the message extension bit defined by RAN2 to use to reformat the entire MIB to a new MIB format. The other is the spare bit in the current MIB IE. Therefore, from moderator’s understanding use of the spare bit in the current MIB does not take away the possibility for MIB extension in RAN2.

As such, moderator asks companies who were not supportive of Proposal 1.9 is ok to accept 1.9 for sake of progress.

Please only comment if you have major issues with Proposal 1.9 and provide details of the concern.

The following proposal were added based on comments.

###### Proposal 1.1-9C

* (Working assumption) For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW
  + If only 1 bit is needed: subCarrierSpacingCommon
  + If 2 bits is needed: subCarrierSpacingCommon, and 1 bit from pdcch-ConfigSIB1 ~~controlResourceSetZero~~ (pending CORESET0 or search space design would ~~that it~~ allow~~s~~ for this bit), else, use the spare-bit (not the Msg Extension bit)
  + FFS: if 3 bits are required

###### Proposal 1.1-9D

* (Working assumption) For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW
  + If only 1 bit is needed: subCarrierSpacingCommon
  + If 2 bits is needed: subCarrierSpacingCommon, and 1 bit from pdcch-ConfigSIB1 ~~controlResourceSetZero~~ (pending CORESET0 or search space design would ~~that it~~ allow~~s~~ for this bit), else, use the spare-bit (not the Msg Extension bit)
    - If 2 bits are needed for both 120kHz and 480/960kHz cases, then use the same bit field combination (i.e. use pdcch-ConfigSIB1 bit for 120/480/960 kHz or spare-bit for 120/480.960 kHz)
  + FFS: if 3 bits are required

**Proposal 1.1-9E**

* (Working assumption) For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW
  + If only 1 bit is needed: subCarrierSpacingCommon
  + If 2 bits is needed: subCarrierSpacingCommon, and 1 bit from pdcch-ConfigSIB1 ~~controlResourceSetZero~~ (pending CORESET0 or search space design would ~~that it~~ allow~~s~~ for this bit), else, use the spare-bit (not the Msg Extension bit)
    - If 2 bits are needed for both 120kHz and 480/960kHz cases, then use the same bit field combination (i.e. use pdcch-ConfigSIB1 bit for 120/480/960 kHz or spare-bit for 120/480.960 kHz)
    - Note: If pdcch-ConfigSIB1 bit is used, the use of controlResourceSetZero (searchSpaceZero) for 120 kHz and searchSpaceZero (controlResourceSetZero) for 480/960 kHz is not precluded
  + FFS: if 3 bits are required

##### **Issue #3) Indication of DBTW and values of Q**

There are 3 different versions of the proposal. 1.1-4B and 1.1-4C and 1.1-4D. From moderator’s opinion, all proposals are functionally identical since there is only 64 candidates SSB positions for 120kHz.

###### Proposal 1.1-4B

* For 120kHz SCS, for values:
  + If 2 bits are available in MIB for , at least support {16, 32, 64}
  + If 1 bit is available in MIB for , support {32, 64}
  + When = 64 is indicated UE may assume DBTW is always used at least until successful decoding of SIB1
  + FFS: 1 bit or 2 bits used for

###### Proposal 1.1-4C

* For 120kHz SCS, for values:
  + If 2 bits are available in MIB for , at least support {16, 32, 64}
  + If 1 bit is available in MIB for , support {32, 64}
  + For operation without shared spectrum channel access, a UE expects to be configured with = 64, which implies the DBTW is not applicable
  + FFS: 1 bit or 2 bits used for

###### Proposal 1.1-4D

* For 120kHz SCS, for values:
  + If 2 bits are available in MIB for , at least support {16, 32, 64}
  + If 1 bit is available in MIB for , support {32, 64}
  + support implicit indication DBTW, where DBTW may be disabled with = 64 configuration.
  + FFS: 1 bit or 2 bits used for

.

Moderator suggests checking if Proposal 1.1-4E that remove the problematic bullet from the discussion. Interpretation of what Q=64 means may not need to be clarified in the specification, as the functionality whether DBTW is enable or disabled is should be identical.

###### Proposal 1.1-4E

* For 120kHz SCS, for values:
  + If 2 bits are available in MIB for , at least support {16, 32, 64}
  + If 1 bit is available in MIB for , support {32, 64}
  + FFS: 1 bit or 2 bits used for

The following proposals were added based on comments.

###### Proposal 1.1-4F

* For 120kHz SCS, for values:
  + If 2 bits are available in MIB for , ~~at least support {16, 32, 64}~~
    - Codepoint 00 indicates DBTW disabled/not supported
    - Codepoints 01, 10, 11 indicate DBTW enabled with values of = {16, 32, X} where X if FFS
  + If 1 bit is available in MIB for , ~~support {32, 64}~~
    - Codepoint 0 indicates DBTW disabled/not supported
    - Codepoint 1 indices DBTW enabled with = 32
  + FFS: 1 bit or 2 bits used for

###### Proposal 1.1-4G

* For 120kHz SCS, for values:
  + If 2 bits are available in MIB for , at least support {16, 32, 64}
  + If 1 bit is available in MIB for , at least support {32, 64}
    - FFS: methods to indicate more values, e.g., {16, 32, 64}
  + FFS: 1 bit or 2 bits used for

##### **Issue #4) DCI size alignment**

The following is summary of views. It looks like companies are converging on this issue.

###### Proposal 1.1-5A

* If channel access mode (i.e., LBT on/off) is not informed to UE before SIB reception,
  + Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off).
  + Same DCI size for DCI 0\_0 in CSS regardless of channel access mode (i.e., LBT on/off)
    - Existing DCI size alignment in TS38.212 applies to DCI 1\_0 and 0\_0 in CSS.
    - FFS: DCI in USS

###### Proposal 1.1-5B

* Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off).
* Same DCI size for DCI 0\_0 in CSS regardless of channel access mode (i.e., LBT on/off)
* Existing DCI size alignment in TS38.212 applies to DCI 1\_0 and 0\_0 in CSS.
* FFS: DCI in USS

Moderator thinks most companies have the same general understanding and goals. Therefore, suggest keeping the agreement simple as possible. This would be to remove 0\_0 and the FFS for USS. Anything not agreed can be studied further. Please note according to 212, DCI 0-0 is rate matched to 1-0. Therefore, unless companies wish to change DCI size alignment algorithm in existing specification, there is no need to mention anything about DCI 0-0.

Please only comment if you have strong concerns about 1.1-5C.

**Proposal 1.1-5C**

* ~~Same DCI size for DCI 0\_0 in CSS regardless of channel access mode (i.e., LBT on/off)~~
* Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off).
  + Existing DCI size alignment in TS38.212 applies to DCI 1\_0 and 0\_0 in CSS.
* ~~FFS: DCI in USS~~

##### **Issue #5) DBTW lengths – discussion deferred**

##### **Issue #6) Indication of licensed/unlicensed and LBT/no LBT in MIB**

The following is summary of views. It looks like companies are converging on this issue. Let’s check if Proposal 1.1-7B is ok with companies.

Please only comment if you have strong concerns about 1.1-7B.

###### Proposal 1.1-7B

* Indication of licensed and unlicensed operation is not explicitly indicated in MIB or PBCH payload.
* Indication of use of LBT or no-LBT is not explicitly indicated in MIB or PBCH payload.

The following proposals were added based on comments.

###### Proposal 1.1-7C

* Indication of licensed and unlicensed operation is not explicitly indicated in MIB or PBCH payload.
  + Note: Indication of licensed regime by different synchronization raster entries is not precluded.
* Indication of use of LBT or no-LBT is not explicitly indicated in MIB or PBCH payload.

###### Proposal 1.1-7D

* Indication of licensed and unlicensed operation is not explicitly indicated in MIB or PBCH payload.
  + ~~Note:~~ FFS: Whether or not to indicate ~~Indication of~~ licensed regime by different synchronization raster entries ~~it not precluded~~.
* Indication of use of LBT or no-LBT is not explicitly indicated in MIB or PBCH payload.

##### **Issue #7) ssb-PositionsInBurst in SIB1**

Continue discussions on Proposal 1.1-8.

###### Proposal 1.1-8

* For ssb-PositionsInBurst in SIB1,
  + if MSB k of inOneGroup and MSB m of groupPresense are set to 1, the UE assumes that SSB(s) within DBTW with candidate SSB index(es) corresponding to SSB index equal to k-1+(m-1)×8 may be transmitted;
  + if MSB k of inOneGroup or MSB m of groupPresense are set to 0, the UE assumes that the SSB(s) are not transmitted.

##### **Company comments**

Please provide comments on the proposals. Quick summary of request from moderator:

* Issue #1)
  + Provide comments/positions/preferences NOT captured in 2nd round summary.
  + Any compromises that companies can make for sake of progress.
  + Assuming not agreeing anything means not supporting DBTW for 480/960kHz, whether companies are ok and any comments on this nuclear option.
  + Please provide comments and ideas on how we can proceed as a group as well.
* Issue #2)
  + only provide comments if you have strong and serious concerns with Proposal 1.9
* Issue #3)
  + provide comments on Proposal 1.1-4E and whether you can live with this.
* Issue #4)
  + only provide comments if you have strong and serious concerns with Proposal 1.1-5C
  + Note: please read moderator comments above for explanation on Proposal 1.1-5C
* Issue# 5) revisit once issue #1 is resolved
* Issue #6)
  + Please only comment if you have strong concerns about 1.1-7B.
* Issue #7)
  + Provide comments on proposal 1.1-8.

|  |  |
| --- | --- |
| Company | comments |
| Sharp | Issue 1: Our first preference is Proposal 1.1-2B. We can live with Proposal 1.1-2A in order to at least have DBTW functionality for 480kHz/960kHz.  Issue 2: (We believe) Using of the spare bit should be confirmed with RAN2. We are fine to firstly make a working assumption based on Proposal 1. 1-9.  Issue 3: Support Proposal 1.1-4E with the following modification:   * For 120kHz SCS, for values:   + If 2 bits are available in MIB for , at least support {16, 32, 64}   + If 1 bit is available in MIB for , at least support {32, 64}   + FFS: 1 bit or 2 bits used for   Issue 7: We are fine with Proposal 1.1-8. |
| LG Electronics | Proposal 1.1-4E: Support  Proposal 1.1-8: We think another alternatives can be considered. First, if we can follow NR-U principle, **UE may expect a bit at groupPresence corresponding to a SS/PBCH block index k (>=Q) is set to 0.** For instance, if Q=32, UE expect groupPresence is set to XXXX0000 (where X=0 or 1). Alternatively, the way to construct a group can be changed depending on Q value. For instance, if Q=16, each bit of groupPresence and inOneGroup (in total 16 bits) can correspond to each of SS/PBCH block indexes 0 to 15. |
| DOCOMO | * Issue #1)   + Our preference is captured already, that is, our best preference is support DBTW regardless of SCS, with supporting 64 candidate SSB positions   + We could live with 128 candidate SSB positions, while we would like to be much careful of the required workloads. Also, in this case, we hope that 64th to 127th candidate positions are only for unlicensed band.   + We really hope to support DBTW regardless of SCS, while we also understood that the need of DBTW may be questionable from several perspectives. Thus we thought that supporting DBTW with keeping 64 candidate SSB positions could be a good middle point. That was our standpoint from several e-meetings ago. * Issue #3)   + Yes, we can live with Proposal 1.1-4E. Prefer to use subCarrierSpacingCommon only (i.e. only 1 bit) |
| Nokia | **Issue #1)**  We have a working assumption for supporting DBTW for 120kHz with 64 SSB locations. This in principle enables us to address deployments where e.g. short control signal exemption is not allowed. As noted earlier we are fine to extend the support of DBTW to 480kHz and 960kHz with the assumption that same design can be applied, i.e. we also restrict to 64 SSB candidate locations. Hence, we would be supportive of Proposal 1.1-2A if something is to be agreed.  **Issue #3)**  We would be OK with Proposal 1.1-4E.  **Issue #7)**  We think that we should further discuss how to handle the ssb-PositionsInBurst like assumed for NR-U as raised by LG once we have concluded the .  . |
| Panasonic | Issue #1) Although our preference is 64 candidate SSB positions, we are OK with 128 candidate SSB positions if PBCH bits to signal DBTW are concluded. However, as mentioned by DOCOMO, we also believe that 64 candidate SSB positions would be a good middle point for supporting DBTW.  Issue #2) We are OK with Proposal 1. 1-9 for the sake of progress. We share Sharp’s view that it would be better to be a working assumption.  Issue #3) We are OK with Proposal 1.1-4E. |
| Interdigital | **Issue #1)** We support DBTW for 480 and 960 kHz regardless of the number of candidate SSB positions.  As for the proposals, we support Proposal 1.1-2B on DBTW for 480 and 960 kHz with 128 candidate SSB positions.  To resolve the issue, we propose to consider Issue #1 along with Issue #2 and Issue #3:   * Based on Proposals 1.9 and 1.9B in Issue #2, at least 2 bits can be used in PBCH for signaling DBTW. * So, one of the bits can be used to indicate the 7th bit to support up to 128 candidate SSB positions, as discussed in Proposal 1.1-2B in Issue #1, and * The other bit can be used to indicate Q parameter with two values, as discussed in Proposal 1.1-4x for Issue #3.   **Issue #2)** We support Proposal 1.9B.  **Issue #3)** We agree with moderator’s suggestion and support Proposal 1.1-4E.  **Issue #4)** No strong view.  **Issue #6)** We do not support Proposal 1.1-7B. License regime should be indicated explicitly either through MIB or synch raster. |
| Samsung | Issue #1) We strongly support Proposal 1.1-2B. Restricting the number of candidate SSB locations to 64 make the usage of DBTW degraded remarkably. Would it be helpful to try to list the potential changes to support 128 candidate SSB locations, in order to resolve the concern from companies?  Issue #2) We are ok with Proposal 1. 1-9B, and we tend to agree that RAN1 shall try to find one bit within RAN1 first and the last choice is using the reserved bit, but we would like note that we should not abuse this as a motivation to unnecessarily remove useful configurations. If the bracket includes both CORESET#0 and Type0-PDCCH configuration, then it should be pdcch-ConfigSIB1 instead of controlResourceSetZero. It should be also clarified it’s only 1 bit from that field instead of reinterpreting the whole field.   * + If 2 bits is needed: subCarrierSpacingCommon, and 1 bit from pdcch-ConfigSIB1 ~~controlResourceSetZero~~ (pending CORESET0 or search space design would ~~that it~~ allow~~s~~ for this bit), else, use the spare-bit (not the Msg Extension bit)   Issue #3) We don’t agree with moderator’s comment on the usage of Q=64, and cannot accept Proposal 1.1-4E. In our understanding, Q is only applicable for unlicensed operation, and a device supporting licensed band only doesn’t need to support the feature of DBTW at all. Now we are designing MIB to be commonly used for both licensed and unlicensed UEs, and there is overlapping bandwidth between licensed and unlicensed bands in FR2-2. For a UE only supporting licensed operation, it can avoid further decoding of SIB1 and realize such SSB is for unlicensed band only, if it decodes Q<64, which is equivalent to “For operation without shared spectrum channel access, a UE expects to be configured with N\_SSB^QCL = 64, which implies the DBTW is not applicable”. This sentence also regulates gNB’s configuration on licensed spectrum such that UE doesn’t need to waste their energy to support DBTW in the licensed band.  Issue #4) We are ok with Proposal 1.1-5C.  Issue #6) We are ok with Proposal 1.1-7B. |
| Qualcomm | Issue #1: we still believe DBTW is not needed for 480/960 kHz. However, if the group agrees that DBTW is needed, we prefer Proposal 1.1-2A.  Issue #2: we support Proposal 1. 1-9B for the reason that (depending on the CORESET0 design) we can get a free bit out of it and no need to utilize one of the spare bits (which we can use in some later release for something else). As far as the dependency, the “else use the spare-bit” sentence should cover it (meaning we will not delay design since we have an agreed backup).  Issue #3: we are fine with FL proposal Proposal 1.1-4E  Issue #4: we are fine with FL proposal Proposal 1.1-5C  Issue #6: we are fine with FL proposal Proposal 1.1-7B |
| Intel | Issue #1) What we would like to suggest is the following:  **Working Assumption:**   * DBTW is supported for 480 and 960 kHz and supports 128 candidate SSB positions   As we compromised to have 64 SSB candidates for SCS 120 kHz last time.  In our opinion, the WA above would allow us to proceed with the rest of SSB-related aspects for SCS 480 kHz/960 kHz. And if it happened that there would be non-avoidable technical difficulties with the proposed WA, we could always roll back and reuse what we would have for SCS 120 kHz.  What is critical to support is DBTW, without this as mentioned by moderator, NR could have serious issues with operating in regulatory domain that does not have short signal exemption (e.g. Japan).  Issue #3)  Support Proposal 1.1-4E  Issue #7)  Revisit once issue #1 is resolved |
| Huawei, HiSilicon | **Issue 2:**  To companies that support 1.9 but not support 1.9B: please note that 1.9B says that **if** a bit is available from controlResourceSetZero (or SearchSpaceZero), it should be used and if it is not available, then 1.9B and 1.9 will be identical. We think that agreeing with 1.9 and not agreeing with 1.9-B only means that even if a bit is available from controlResourceSetZero (or SearchSpaceZero), it should not be used and we should directly use the spare bit. We don’t think this would be a preferred solution.  We think that if a bit from controlResourceSetZero or SearchSpaceZero is available then it should be used and if it is not then we can use the spare bit. Also, we think that since the design of neither “monitoring occasions for Type0-PDCCH CSS set” nor “CORESET for Type0-PDCCH search space set” is complete at the moment, the possibility of using one saved bit from SearchSpaceZero should not be ruled out. So, we suggest the following slight modification to 1.9B:  @To moderator: We think that Proposal 1.9B is better to be modified as below to make it aligned with the explanation inside the parentheses in the second sub-bullet).  **Proposal 1.9B (modified)**   * For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW   + If only 1 bit is needed: subCarrierSpacingCommon   + If 2 bits is needed: subCarrierSpacingCommon, and controlResourceSetZero/ searchSpaceZero (pending CORESET0 or search space design would that it allows for this bit), else, use the spare-bit (not the Msg Extension bit)   + FFS: if 3 bits are required   **Issue 3:**  Our strong preference is Proposal 1.1-4D. In fact, as the moderator pointed out, Proposal 1.1-4D and Proposal 1.1-4E are practically identical. When =64 is indicated for 120 kHz where, based on the WA , DBTW will be disabled and, to our understanding, removing the third sub-bullet from Proposal 1.1-4D would not make any difference. In any case, we can also live with Proposal 1.1-4E for the sake of progress.  **Issue 4:**  Our preference is 1.1-5B but we can also accept 1.1-5C at this point for the sake of progress.  **Issue 6:**  We think that it would be a much better progress if companies could agree with Proposal 1.1-7A (brought below) in a more general form than 1.1-7B. We don’t really see either the necessity or a realistic chance to agree on an implicit indication. However, for the sake of progress, we can agree with Proposal 1.1-7B as an intermediate step. Proposal 1.1-7A  * Indication of licensed and unlicensed operation is not ~~explicitly~~ indicated in MIB or PBCH ~~content~~ payload. * Indication of use of LBT or no-LBT is not ~~explicitly~~ indicated in MIB or PBCH ~~content~~ payload.   + ~~If explicit indication of DBTW disabled is supported, use of no-LBT may be inferred from DBTW disabled indication.~~   **Issue 7:**  Support Proposal 1.1-8. |
| Futurewei | Issue #1: We do not prefer DBTW for 480/960 kHz. However, if the majority agrees that DBTW is needed, we could live with either Proposal 1.1-2A or B.  Issue #2: we are OK with the Proposal 1.1-9B  Issue #3: we are OK with the Proposal 1.1-4E  Issue #4: we are OK with the Proposal 1.1-5B or Proposal 1.1-5C  Issue #6: we are OK with the Proposal 1.1-7B |
| CATT | **Issue 1:** We only support 1.1-2B  **Issue 2:** OK with P1.9  **Issue 3:** OK with P1.1-4E  **Issue 7:** Revisit the issue after #1 |
| Moderator | Added note to Proposal 1.1-7B (creating 1.1-7C) to address Interdigital’s concern. Hopefully, this can address the concerns.  There seems to be some concerns on Proposal 1.1-9, please comment if companies are ok to have working assumption for 1.1-9C (minor update of 1.1-9B).  Moderator suggests providing different alternatives to 1.1-8 if possible, so that further discussions (possible in next meeting) can be shortened. The different alternative will be captured in 1.1-8A.  For Issue #1, Samsung suggested that companies to provide a list of potential changes so that companies who were objective to support 128 candidates can review the potential changes in specification. Please provide further information.  Continue to provide comments. I will update the summary as companies provide more inputs. Summary below are tentative version. |
| Ericsson  (3rd round comments prior to moderator summary of 3rd round) | **Issue 1**   * We can support Proposal 1.1-2A, since it allows for common design for 120/480/960. This is a compromise for us since we don’t think that DBTW is needed for any SCS. * **Object to Proposal 1.1-2B**   Having a common design is important from an implementation POV, not just from a specification impact POV. For the solutions on the table, 128 candidate positions requires fundamental change to low layer physical processing, and there is an implementation burden from having separate MIB/PBCH processing for different SCSs. Regarding some proposals to use the HF bit from PBCH for SSB index indication, we cannot support this due to the loss in scheduling flexibility, e.g., potential incompatibility with TDD pattern on a lower band anchor in a CA configuration.  **Issue 2**   * Support Proposal 1.1-9 * We can consider Proposal 1.1-9B only under the condition that a common design for all SCSs is supported (see comment in Issue 1 above), i.e., we do not support use of spare bit for 120 and controlResourseSetZero bit for 480/960 since this would require different MIB processing for different SCSs, and there is an implementation burden from this.   **Issue 3**   * **Do not support Proposal 1.1-4E**. We do not agree to decouple the indication of DBTW on/off from indication of Q (see comments below). They should be agreed together as a package. * We support Proposal 1.1-4D * We can also support some sort of joint encoding of Q and DBTW on/off (I think Samsung suggested this). For example, if 2 bits are available the joint encoding can be codepoint 00 = means DBTW off; codepoints 01, 10, 11 mean DBTW on allowing indication of 3 different (useful) values of Q. * Hence the following alternative be discussed to see if it is agreeable to the group:   + For 120kHz SCS, for values:     - If 2 bits are available in MIB for , ~~at least support {16, 32, 64}~~       * Codepoint 00 indicates DBTW disabled/not supported       * Codepoints 01, 10, 11 indicate DBTW enabled with values of = {16, 32, X} where X if FFS     - If 1 bit is available in MIB for ~~, support {32, 64}~~       * Codepoint 0 indicates DBTW disabled/not supported       * Codepoint 1 indices DBTW enabled with = 32     - FFS: 1 bit or 2 bits used for   Regarding the other proposals:  4C it is missing a mechanism for disabling DBTW in unlicensed spectrum. This is needed since not all deployments / regions require LBT, hence a mechanism (e.g., implicit by indicating Q = 64). Moreover, the UE doesn't know it is licensed/unlicensed spectrum until SIB1 reception.  4B doesn't make sense for the same reasons – why should the UE assume DBTW is always used for licensed spectrum?  For 4E, we don't agree that the spec will be silent on what Q = 64 means. Prior to receiving SIB1, the UE doesn't know if the gNB is operating with licensed/unlicensed spectrum since the bands overlap. We think that it is necessary for the spec to say something like "Regardless of operation with/without shared spectrum channel access, if Q = 64, the UE shall assume that DBTW is not configured/supported." For licensed operation, this will allow the UE to ignore this field in MIB since DBTW is irrelevant. For unlicensed operation, since the UE knows what a DBTW is, it will know that DBTW is disabled.  **Issue 4**  Support Proposal 1.1-5C  **Issue 5**  Fine to defer discussion  **Issue 6**  Fine with Proposal 1.1-7B.  **Issue 7**  We don't support making an agreement on this issue in this meeting. This issue can be deferred until next meeting once more fundamental issues on DBTW are stabilized. |
| Moderator | Added Proposal 1.1-9D based on Ericsson’s comment.  Added Proposal 1.1-4F based on Ericsson’s comments. While note sure whether companies would be ok with 1.1-4F (based on previous comments), I’ve added the proposal so that companies can reference for discussion. |
| Sharp  (2nd comment in 3rd round) | Thank moderator for the note capturing our comments and we response with more details as follows.  We think it is commonly understood that there is limited number of MIB payload bits for Q indication (e.g., probably 1 bit at the end) and if possible indicating more Q values is preferred (e.g., {32, 64} might not be sufficient). As we commented in the second round, we propose that even with 1 MIB bit indication, {16, 32, 64} can be supported. For instance, as shown in the following table, “0” indicates Q = 64 (equally saying DBTW is disabled). “1” indicates Q = 16 or 32 when gNB transmits SSBs. UE makes the QCL assumption considering Q = 16 when UE is indicated with “1”. For Case 3 where the practical Q value used by gNB is 32 and UE assumes Q = 16, PDCCH blind decoding load is increased but the procedure works. Hence, this method could be a potential solution that enables indicating three Q values with 1 MIB bit.   |  |  |  |  | | --- | --- | --- | --- | |  | 1 bit indication for Q | used by gNB | QCL assumption at UE | | Case 1 | “0” | 64 | 64 | | Case 2 | “1” | 32 | 16 | | Case 3 | 16 | 16 |   We would like to see whether it is possible to keep the possibility of further improvement based on Proposal 1.1-4E with the following modifications (could also be applied to other proposal variants):   * For 120kHz SCS, for values:   + If 2 bits are available in MIB for , at least support {16, 32, 64}   + If 1 bit is available in MIB for , at least support {32, 64}     - FFS: methods to indicate more values, e.g., {16, 32, 64}   + FFS: 1 bit or 2 bits used for |
| DOCOMO\_v068 | Issue #3) Indication of DBTW and values of Q:  We are confused with Sharp’s update. Our understanding is that Sharp is proposing “it should be possible to have 32 SSB beams while UE assumes Q=16”. We agree it may work, but even in this case two variants of Q (i.e. {16, 64}) seem sufficient. Why do we need to further consider “methods to *indicate* more Q”? Or would Sharp be proposing {16, 64} instead of {32, 64}?  We think the actual number of SSB beams is up to implementation. If gNB sends SSB beams more than Q value, UE may consider different SSB beams as QCLed type D. If gNB sends SSB beams less than Q value, UE may consider SSB beams QCLed as different beams. Both have its pros and cons, similar impacts somehow. Thus the Q value selection should follow how much likely the number of actual SSB beams would be. We prefer 32 than 16 as 16 could be too small considering higher frequency basically requires narrower beams (i.e. more number of SSB beams).  Issue #7) ssb-PositionsInBurst in SIB1:  We agree it needs further discussions. |
| Huawei, HiSilicon | **Issue 2:** Support Proposal 1.1-9C. Can live with Proposal 1.1-9D with the following further clarification   * (Working assumption) For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW   + If only 1 bit is needed: subCarrierSpacingCommon   + If 2 bits is needed: subCarrierSpacingCommon, and 1 bit from pdcch-ConfigSIB1 ~~controlResourceSetZero~~ (pending CORESET0 or search space design would ~~that it~~ allow~~s~~ for this bit), else, use the spare-bit (not the Msg Extension bit)     - If 2 bits are needed for both 120kHz and 480/960kHz cases, then use the same bit field combination (i.e. use pdcch-ConfigSIB1 bit for 120/480/960 kHz or spare-bit for 120/480.960 kHz)       * Note: If pdcch-ConfigSIB1 bit is used, the use of controlResourceSetZero (searchSpaceZero) for 120 kHz and searchSpaceZero (controlResourceSetZero) for 480/960 kHz is not precluded   + FFS: if 3 bits are required   **Issue 3:**  Our strong preference is **Proposal 1.1-4D**.  In fact, as the moderator pointed out, Proposal 1.1-4D and Proposal 1.1-4E are practically identical. When =64 is indicated for 120 kHz where, based on the WA , DBTW would be disabled and, to our understanding, removing the third sub-bullet from Proposal 1.1-4D would not make any difference. In any case, we can also live with Proposal 1.1-4E for the sake of progress.  We don’t understand the purpose of Proposal 1.1-4F and cannot support it. According to WA, number of candidate SSBs for 120 kHz is 64 which means that . If X=64 is selected in = {16, 32, X} then it also “implicitly” indicate that DBTW is disabled. So, there is no reason to allocate another dedicated codepoint 00 for DBTW disable. Also, we don’t see the necessity of discussing the map between codepoints and values, but if it has to be discussed, codepoint 11 which indicates the maximum value of should be allocated to DBTW DISABLE.  **Issue 6:**  Still our strong preference is 1.1-7A. If it is not agreeable, we can live with 1.1-7B as long as it is the common understanding that this does not automatically mean that licensed and unlicensed or LBT/No-LBT is implicitly indicated in MIB or PBCH payload. We can also live with 1.1-7C with this change: Proposal 1.1-7C  * Indication of licensed and unlicensed operation is not explicitly indicated in MIB or PBCH payload.   + ~~Note:~~ FFS: Whether or not to indicate ~~Indication of~~ licensed regime by different synchronization raster entries ~~it not precluded~~. * Indication of use of LBT or no-LBT is not explicitly indicated in MIB or PBCH payload.   **Issue 7:**  Support Proposal 1.1-8A Alt2. |
| Apple | **Issue #1):** Given the potential use case of DBTW in region without short control signaling, we are ok with Proposal 1.1-2B considering 128 SSBs are still within 5ms DBTW window. **Issue #3):** Proposal 1.1-4E is ok for us. Indeed, with configuration = 64, UE behaviour for Type0-CSS monitoring seems identical assuming DBTW enabling/disabling as UE only monitors one Type0-CSS occasion based on the detected SSB. |
| Sharp  (3rd comment in 3rd round) | Response to Docomo:  Thank you for the questions. Firstly, we are supportive to the Q value set {32, 64} and not proposing {16, 64} only instead. Our proposal is to enabling indication Q value set {16, 32, 64}, on top of {32, 64}, with 1 MIB bit. That is, codepoint “0” indicates Q = 64 and codepoint “1” indicates Q = 16 or 32.   * For the case gNB uses Q = 16 indicating “1” and UE assumes Q = 16, UE monitors PDCCH associated to SSB with indexes *i*, *i*+16, *i*+32. * For the case gNB uses Q = 32 indicating “1” and UE assumes Q = 16, UE monitors PDCCH associated to SSB with indexes *i*, *i*+16, *i*+32 (instead of *i* and *i*+32).   For more details of the method, please refer to our previous comment.  We agree that the actual number of SSB beams is up to implementation. Thus, we believe it is better to provide more flexibility (e.g., more Q values) in specification and how to choose is left for network implementation. In our proposal enabling indication Q value set {16, 32, 64} with 1 MIB bit, gNB has more flexibility to choose from 16, 32, or 64. |
| LG Electronics | We can accept Proposal 1.1-9D.  Among the variants of 1.1-4X, we only support 1.1-4E.  As Apple pointed out, in case the corresponding UE behaviors are described in specification, what is the difference between UE with Q=64 assuming DBTW is enabled and UE with Q=64 assuming DBTW is disabled? UE doesn’t need to distinguish DBTW enabled or disabled for Q=64, and just follows legacy Rel-15 PDCCH monitoring behavior. |
| DOCOMO\_v075 | Response to Sharp:  Thanks for the follow-up.   * In your example, “UE assumes Q = 16, UE monitors PDCCH associated to SSB with indexes i, i+16, i+32” is described. In our understanding, if we follow Rel-16 NR-U, this handling is totally the same as when UE is indicated Q=16. So are you proposing to change how to interpret the exact indicated Q value? * We are still struggling to understand why “methods to *indicate* more N\_SSB^QCL values” can be FFS when only 1 MIB bit is assumed for Q indication. Are you proposing to add 1 SIB bit for Q? Isn’t it included in the intended target of the Proposal 1.1-4x?   We are ok with 1.1-4E (as described earlier). |
| Sharp | Response to Docomo:  Thank you for the follow-up questions. Please find our responses inline.  *Moderator has moved the response out of inline and copy & pasted here*   * Q) In your example, “UE assumes Q = 16, UE monitors PDCCH associated to SSB with indexes i, i+16, i+32” is described. In our understanding, if we follow Rel-16 NR-U, this handling is totally the same as when UE is indicated Q=16. So are you proposing to change how to interpret the exact indicated Q value?   [Sharp] Yes, as you estimated, it is the same handling as when UE is indicated with Q = 16. The point here is indeed to make some interpretations on the indication at the UE side, more specifically the codepoint “1”. The motivation is to enable indication of {16, 32, 64} with 1 MIB bit because additional MIB bits are difficult to repurpose.   * Q) We are still struggling to understand why “methods to *indicate* more N\_SSB^QCL values” can be FFS when only 1 MIB bit is assumed for Q indication. Are you proposing to add 1 SIB bit for Q? Isn’t it included in the intended target of the Proposal 1.1-4x?   [Sharp] Full indication can be obtained by SIB1 (either 1 bit in SIB1 indicating remaining information or 2 bits in SIB1). By saying “indicate more N\_SSB^QCL values”, the intention is to let gNB have the flexibility of choosing {16, 32, 64} rather than only {32, 64}. UE may have different assumed Q value compared to what gNB used, e.g., gNB chooses Q = 32 and UE assumes Q = 16 (Case 2 in our previous comments), but we think this works from spec point of view (the cost is additional PDCCH blind decodings). |
| Moderator | To Sharp,  Maybe I do not fully understand, I thought is a parameter used by the UE to determine which SSB index are in QCLed together. So in case of RRM measurements if the UE assumes 16, but gNB send 32 beams would this potentially lead to cases where UE tries to combine the measures of two different beams together? I am not 100% sure how this would work out.  If other companies are ok, we can add the FFS, but not sure what this actually means.  I have the same understanding as Docomo on this. I have a feeling you want to actually support {16, 64}, but have the UE also check for PDCCH candidates that would correspond to 32 candidates. This in my opinion can be considered separately from the value discussion. With that said, added Proposal 1.1-4G based on Sharp’s comments.  Added Proposal 1.1-9E based on Huawei/HiSilicon comments. However, I have a feeling the note is something that Ericsson did not want to support. With that said, please provide further comments. |
| ZTE, Sanechips | Issue #1: We think DBTW for 480/960 kHz should be supported. As a compromise, we can accept any of Proposal 1.1-2A and Proposal 1.1-2B.  Issue #2: we are OK with the Proposal 1.1-9D  Issue #3: we prefer the Proposal 1.1-4C, 1.1-4D. Proposal 1.1-4E are also fine for us.  We still suggest that Moderator can add a new issue, that is how to use to obtain the QCL relationship between different candidate SSBs. This is a problem that must be solved, but it was not covered in the previous discussion. For FR2-2, the UE can not derive the QCL relation between candidate SSBs if it reuses Rel-16 NR-U mechanism, i.e. according to the value of .  Issue #4: we are OK with the Proposal 1.1-5B or Proposal 1.1-5C  Issue #6: we are OK with the Proposal 1.1-7B  Issue #7: we think the discussion on this issue can be deferred. |
| vivo | **Issue 1:**  Our first preference is 1.1-2B and can live with 1.1-2A for sake of progress.  **Issue 2:**  We are OK with 1.1-9 and 1.1-9B  **Issue 3:**  We support 1.1-4E. Agree with Apple and LG that UE behavior is the same for Q=64+DBTW on and DBTW off when the number of candidate SSBs is 64. I think at this stage, 1.1-4E doesn’t say whether to indicate DBTW on/off is needed or not and it is still open if the number of candidate SSBs is 128. I don’t understand the concern for 1.1-4E.  **Issue 4:**  Support 1.1-5C. Better to agree together with Proposal 1.1-7B in Issue 6  **Issue 6:**  Support 1.1-7B |
| Sharp | Thank moderator for the analysis.  The purpose of the proposed method is trying to solve the problem of constrained available MIB bits for indication, during initial access procedure (before decoding SIB1). For RRM measurement, the full indication can be indicated by SIB1 and thus the QCL assumptions between gNB and UE can be aligned. For Case 2 in the following updated table, before decoding SIB1, gNB and UE assume , respectively, but both gNB and UE assume after decoding SIB1, which would not affect connected mode measurements. This is kind of two-step indication. In the first step, the MIB bit codepoint “1” indicates ”. In the second step, a SIB1 bit indicates which value between 32 and 16 is practically used by gNB.  In fact, we want to support {16, 32, 64} with 1 MIB bit indication, not only {16, 64} or only {32, 64}.   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | 1 MIB bit indication for Q | used by gNB | QCL assumption at UE (before decoding SIB1) | QCL assumption at UE (after decoding SIB1) | | Case 1 | “0” | 64 | 64 | 64 | | Case 2 | “1” | 32 | 16 | 32 | | Case 3 | 16 | 16 | 16 | |
| Lenovo, Motorola Mobility | Issue #1): We support Proposal 1.1-2A. However, for the sake of progress, we can also agree to Proposal 1.1.-2B, but we first need to discuss the possible spec impact and corresponding workload, as pointed out by DOCOMO.  Issue #3): Support Proposal 1.1-4E  Issue #7): Revisit once issue #1 is resolved |
| OPPO | We can accept Proposal 1.1-5C. |
| Nokia (3rd round) | **Issue #1)**  We have made a working assumption that DBTW (with 64) candidate locations will be supported for 120kHz. This will result some additional specification work (as evident from the other issues being discussed), and if we conclude to support DBTW also for 480/960kHz, assuming also 64 candidate locations would omit additional specification effort for support it for higher SCS. Hence we would prefer option 1.1-2A.  **Issue #2)**  Still would support 1.1-9, selecting e.g. 1.1-9E would create different motivation to modify the CORESET#0/Type0-PDCCH CSS design, which may be contradicting with the deployment flexibility (e.g. number of offsets).  **Issue #3)**  Firstly noting that in my reading, 1.1-4 did not preclude option of implicitly understanding that =64 when max 64 candidate positions have been agreed. With that said, 1.1-4D would be of course clearest, could consider 1.1-4F as well.  Is**sue #4):** This appears to be the majority view, so we can agree while not see absolute necessity for it.  **Issue #6):** OK with 1.1-7B and 1.1-7C  **Issue #7):**  While we would think that this discussion could wait for concluding the other issues, some comments and edits below.  In my reading the Alt1 and Alt2 are more or less identical, both are aligned to the principle of NR-U behavior, where the SSB indexes that fall beyond Q-1 are set to 0, and if (actually) transmitted and index<Q, set to 1.  we would propose following adjustments:  **Proposal 1.1-8A \_NOK**   * For ssb-PositionsInBurst in SIB1, consider at least the following alternatives (other alternatives are not precluded):   + ALT 1)     - UE may expect a bit at groupPresence corresponding to a SS/PBCH block index k (>=Q) is set to 0.   + ALT 2)     - if MSB k of inOneGroup and MSB m of groupPresense are set to 1, the UE assumes that SSB(s) within DBTW with candidate SSB index(es) corresponding to SSB index equal to k-1+(m-1)×8 may be transmitted;     - if MSB k of inOneGroup or MSB m of groupPresense are set to 0, the UE assumes that the SSB(s) are not transmitted.   + ALT 3)     - construct a group can be changed depending on Q value. Details FFS   Noting that other Alt4 could be added to cover the ‘other alternatives’. |
| Convida Wireless | **Issue #3)**  We are ok with Proposal 1.1-4E. |
| InterDigital | Thanks to moderator for the note reflecting our concern.  **Issue #1)** We propose following codepoints for 480 and 960kHz.  Proposal) For 480 and 960kHz, if 2 bits are available in MIB for , below table can be used to indicate DBTW enabled/disabled along with the Q parameter, while supporting up to 128 candidate SSB positions:   |  |  |  |  | | --- | --- | --- | --- | | 1st bit | 2nd bit | Codepoint | Description | | 0 | 0 | 00 | DBTW is disabled | | 0 | 1 | 01 | - DBTW is enabled and .  - 2nd bit is used to indicate the 7th bit for 128 candidate positions. | | 1 | 0 or 1 | 10 or 11 | - DBTW is enabled and .  - 2nd bit is used to indicate the 7th bit for 128 candidate positions. |   Note: The 2nd bit is also used as the 7th bit for indication of up to 128 candidate positions, i.e. 2nd bit = 0 for SSB indexes<64 and 2nd bit = 1 for SSB indexes>=64.  Example 1) If SSB candidate index = 50, obviously the 2nd bit = 0. So, the value of the 1st bit equal to 0 indicates DBTW is disabled. Otherwise if 1st bit is equal to 1, it indicates DBTW is enabled and .  Example 2) If SSB candidate index = 70, obviously the 2nd bit = 1. So, the value of the 1st bit equal to 0 indicates DBTW is enabled and . Otherwise if 1st bit is equal to 1, it indicates DBTW is enabled and .  **Issue #2)** We are OK with Proposal 1.1-9D.  **Issue #3)** We support allocating a separate codepoint to indicate DBTW enabled/disabled. Associating the with disabling DBTW may affect the future revisions with possibly more candidate positions. For example, if up to 80 candidate positions is going to be supported, the could actually have a meaning. In other words associating with DBTW disabled will prevent any further progress in increasing the number of candidate positions, for example up to 80 positions.  **Issue #6)** We support the Proposal 1.1-7C. |
| Qualcomm | Issue #1: for the sake of progress, we are fine with DBTW for 480/960 kHz as long as we have a common design with 120 kHz (i.e., Proposal 1.1-2A)  Issue #2: we support Proposal 1.1-9D to have a common design across SCSs. We do not support Proposal 1.1-9 for the reason that (depending on the CORESET0 design) we can get a free bit out of it and no need to utilize one of the spare bits (which we can use in some later release for something else).  Issue #3: we are fine with FL Proposal 1.1-4E. We do not support Proposal 1.1-4F or Proposal 1.1-4G since they waste 1 codepoint to indicate DBTW disable while Q = 64 can be used as indication to disable DBTW.  Issue #4: we are fine with FL Proposal 1.1-5C  Issue #6: we are fine with FL Proposal 1.1-7B or Proposal 1.1-7C |
| Samsung2 | Issue #1): For supporting 128 candidate SSB locations, here is our thinking.   * Indication of the extra candidate SSB index:   + If one bit in MIB is available, it can be reinterpreted for the 4th LSB of SFN, and the original 4th LSB of SFN in PHY bits can be used for indicating the new extra candidate SSB index. This would be our first preference.   + If one bit in MIB is not available, we are ok with using the half frame bit to indicate the new extra candidate SSB index, as proposed by other companies. * Impact to PBCH scrambling: yes, spec change is expected, but principle is same as in Rel-15/16, so we are basically performing a similar practice as in Rel-16 NR-U.   Issue #2): We are ok with 1.1-9C or 1.1-9D, but we didn’t get the meaning of the note in 1.1-9E (what’s the new information comparing to the main bullet?)  Issue #3): We also expressed our concern for 1.1-4E. At least some scheme to disable the DBTW (or usage of Q) for licensed band UE is needed. We are ok with 1.1.4-F.  Issue #4): We are ok with Proposal 1.1-7C, if the issue of licensed band UE’s behavior with Q is resolved. One typo in the note: “it” should be “is”. |

#### <Summary of 3rd Round of Discussions>

##### **Issue #1) candidate SSB in DRS and DBTW support**

Summary of support for 1.1-2A (64 candidates):

* Support: Docomo, Lenovo/Motorola Mobility, LGE, Panasonic, Nokia/NSB, ~~Futurewei~~
* Conditional support: Ericsson (only if common design for 120/480/960), Qualcomm (only if common design for 120/480/960)
* Ok to accept for sake of progress: Sharp, Futurewei, ZTE/Sanechips, vivo
* Not support but if had to choose can live with: Qualcomm
  + Benefits of 128 candidates does not outweigh specific effort needed
  + Common design between 120/480/960
  + Concerns on how 128 candidates signaling will be achieved as the changes are non-trivial in specification (e.g. Supporting 128 may require some bits to be swapped between MIB (RRC IE) and PBCH content in L1)

Summary of support for 1.1-2B (128 candidates):

* Support: OPPO, Samsung, Interdigital, ETRI, Sharp, Intel, vivo, Huawei/HiSilicon, ZTE/Sanechips (if 1 bit is available), Sony, NEC, Convida Wireless, CATT
* Ok to accept for sake of progress: Docomo, Sharp, Futurewei, Lenovo/Motorola Mobility
  + Support of 128 was not possible in 120kHz due to exceeding half radio frame, for 480/960 there is no technical barrier to support 128
  + 480/960kHz SSB is expected to less coverage compared to 120kHz SSB. Use of 64 beams with LBT is essential for 480/960kHz (more so than 120kHz).
  + Only having 64 candidates undermines support of DBTW. If 64 candidates are supported, no need to optimize Q signaling in MIB.
  + SSB with LBT operation is needed for regulatory domain without short control signal exemption (e.g. Japan)
  + Unified design between 120/480/960 looks nice but not technically justified

The following are some information on potential changes that may be required for supporting 128 SSB candidates. It should be noted that some similar aspects may be required for supporting 64 SSB candidates (but not all).

Potential changes, ALT 1)

|  |  |  |  |
| --- | --- | --- | --- |
| 1st bit | 2nd bit | Codepoint | Description |
| 0 | 0 | 00 | DBTW is disabled |
| 0 | 1 | 01 | - DBTW is enabled and .  - 2nd bit is used to indicate the 7th bit for 128 candidate positions. |
| 1 | 0 or 1 | 10 or 11 | - DBTW is enabled and .  - 2nd bit is used to indicate the 7th bit for 128 candidate positions. |
| Note: The 2nd bit is also used as the 7th bit for indication of up to 128 candidate positions, i.e. 2nd bit = 0 for SSB indexes<64 and 2nd bit = 1 for SSB indexes>=64.  Example 1) If SSB candidate index = 50, obviously the 2nd bit = 0. So, the value of the 1st bit equal to 0 indicates DBTW is disabled. Otherwise if 1st bit is equal to 1, it indicates DBTW is enabled and .  Example 2) If SSB candidate index = 70, obviously the 2nd bit = 1. So, the value of the 1st bit equal to 0 indicates DBTW is enabled and . Otherwise if 1st bit is equal to 1, it indicates DBTW is enabled and . | | | |

Potential changes, ALT 2)

* Indication of the extra candidate SSB index:
  + If one bit in MIB is available, it can be reinterpreted for the 4th LSB of SFN, and the original 4th LSB of SFN in PHY bits can be used for indicating the new extra candidate SSB index. This would be our first preference.
  + If one bit in MIB is not available, we are ok with using the half frame bit to indicate the new extra candidate SSB index, as proposed by other companies.
* Impact to PBCH scrambling: yes, spec change is expected, but principle is same as in Rel-15/16, so we are basically performing a similar practice as in Rel-16 NR-U.

Moderator suggest to down-select between Proposal 1.1-2A or 1.1-2B in RAN 1#106-bis-e.

##### **Issue #2) bits utilized in PBCH for signaling DBTW**

The following is summary of views.

Proposal 1.1-9

* Support: LGE, vivo, NTT Docomo, Samsung, Intel, Interdigital, Lenovo/Motorola Mobility, [Sharp], [Apple], Panasonic (as working assumption, check with RAN2), vivo, Nokia/NSB
* Not support: Huawei/HiSilicon

Proposal 1.1-9B (updated to 1.1-9C)

* Support: Huawei/HiSilicon, Sharp (spare bit requires confirmation from RAN2), Qualcomm, [Apple], [CATT], [LGE], Panasonic, Interdigital, Samsung, vivo
* Do not support: Ericsson

Proposal 1.1-9D (further update of 1.1-9C)

* Support: ZTE/Sanechips, Interdigital, Qualcomm

Proposal 1.1-9E (further update of 1.1-9D)

* Support Huawei/HiSilicon

Moderators suggest down-select between 1.1-9 (original) or 1.1-9E.

**Proposal 1.1-9**

* For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW
  + If only 1 bit is needed: subCarrierSpacingCommon
  + If 2 bits is needed: subCarrierSpacingCommon, and spare-bit (not the Msg Extension bit)
  + FFS: if 3 bits are required

**Proposal 1.1-9E**

* (Working assumption) For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW
  + If only 1 bit is needed: subCarrierSpacingCommon
  + If 2 bits is needed: subCarrierSpacingCommon, and 1 bit from pdcch-ConfigSIB1 (pending CORESET0 or search space design would allow~~s~~ for this bit), else, use the spare-bit (not the Msg Extension bit)
    - If 2 bits are needed for both 120kHz and 480/960kHz cases, then use the same bit field combination (i.e. use pdcch-ConfigSIB1 bit for 120/480/960 kHz or spare-bit for 120/480.960 kHz)
    - Note: If pdcch-ConfigSIB1 bit is used, the use of controlResourceSetZero (searchSpaceZero) for 120 kHz and searchSpaceZero (controlResourceSetZero) for 480/960 kHz is not precluded
  + FFS: if 3 bits are required

##### **Issue #3) Indication of DBTW and values of Q**

The following is summary of views.

Proposal 1.1-4G (update from 1.1-4E)

* Sharp

Objections to Proposal 1.1-4E

* Ericsson, Samsung, [Sharp]

Moderator suggest to conclude between 1.1-4F and 1.1-4G after number of SSB candidates (issue #1) is resolved.

**Proposal 1.1-4F**

* For 120kHz SCS, for values:
  + If 2 bits are available in MIB for , ~~at least support {16, 32, 64}~~
    - Codepoint 00 indicates DBTW disabled/not supported
    - Codepoints 01, 10, 11 indicate DBTW enabled with values of = {16, 32, X} where X if FFS
  + If 1 bit is available in MIB for , ~~support {32, 64}~~
    - Codepoint 0 indicates DBTW disabled/not supported
    - Codepoint 1 indices DBTW enabled with = 32
  + FFS: 1 bit or 2 bits used for

**Proposal 1.1-4G**

* For 120kHz SCS, for values:
  + If 2 bits are available in MIB for , at least support {16, 32, 64}
  + If 1 bit is available in MIB for , at least support {32, 64}
    - FFS: methods to indicate more values, e.g., {16, 32, 64}
  + FFS: 1 bit or 2 bits used for

##### **Issue #4) DCI size alignment**

The following is summary of views.

Objections to Proposal 1.1-5C

* none so far

Suggest agreeing to 1.1-5C over email.

##### **Issue #5) DBTW lengths – discussion deferred**

##### **Issue #6) Indication of licensed/unlicensed and LBT/no LBT in MIB**

The following is summary of views.

Objections to 1.1-7B

* Interdigital (licensed regime should be indicated through MIB or sync raster. Ok with 7C)

Moderator suggests concluding the following.

**Proposal 1.1-7D**

* Indication of licensed and unlicensed operation is not explicitly indicated in MIB or PBCH payload.
  + FFS: Whether or not to indicate licensed regime by different synchronization raster entries.
* Indication of use of LBT or no-LBT is not explicitly indicated in MIB or PBCH payload.

##### **Issue #7) ssb-PositionsInBurst in SIB1**

Continue discussions on Proposal 1.1-8.

Proposal 1.1-8

* Ok: Sharp
* Further discussion needed, defer: Nokia, Ericsson

Moderator suggest to provide different alternatives if possible, so that further discussions (possible in next meeting) can be shortened.

**Proposal 1.1-8A**

* For ssb-PositionsInBurst in SIB1, consider at least the following alternatives (other alternatives are not precluded):
  + ALT 1)
    - UE may expect a bit at groupPresence corresponding to a SS/PBCH block index k (>=Q) is set to 0.
  + ALT 2)
    - if MSB k of inOneGroup and MSB m of groupPresense are set to 1, the UE assumes that SSB(s) within DBTW with candidate SSB index(es) corresponding to SSB index equal to k-1+(m-1)×8 may be transmitted;
    - if MSB k of inOneGroup or MSB m of groupPresense are set to 0, the UE assumes that the SSB(s) are not transmitted.
  + ALT 3)
    - construct a group can be changed depending on Q value. Details FFS

##### **Issue #8) QCL derivation equation for DRS**

ZTE/Sanechip commented that existing equation for QCL deriviation may need to be updated once we support more than 8 SSB beams, as only reflects portion of the SSB index.

Moderator suggests to further discuss this issue once the number of SSB candidate is concluded.

#### 4th Round of Discussions

##### **Stable Issues: Issue #4 + #6**

Approve the following proposals over email. Please indicate if you have strong concerns on approving them over email.

###### Proposal 1.1-5C

* Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off).
  + Existing DCI size alignment in TS38.212 applies to DCI 1\_0 and 0\_0 in CSS.

###### Proposal 1.1-7D

* Indication of licensed and unlicensed operation is not explicitly indicated in MIB or PBCH payload.
  + FFS: Whether or not to indicate licensed regime by different synchronization raster entries.
* Indication of use of LBT or no-LBT is not explicitly indicated in MIB or PBCH payload.

**Moderator Suggestion:**

* Agree to following proposal
  + Proposal 1.1-5C
  + Proposal ~~1.1-7A~~ 1.1-7D

|  |  |
| --- | --- |
| Company | Comment (only if you have strong concerns) |
| Qualcomm | Fix typo in Moderator Suggestion: to Proposal 1.1-7D instead of Proposal 1.1-7A. |
| Moderator | Sorry, fixed typo above. |
| Huawei, HiSilicon | Agree with Proposal 1.1-5C  We can accept 1.1-7D. |
| OPPO | We are fine with Proposal 1.1-5C and 1.1-7D. |
| Ericsson | Support Proposal 1.1-5C  Support Proposal 1.1-7D |
| vivo | Support Proposal 1.1-5C and Proposal 1.1-7D |
| ZTE, Sanechips | Support Proposal 1.1-5C and Proposal 1.1-7D |
| Lenovo, Motorola Mobility | We support Proposal 1.1-5C and 1.1-7D |
| Interdigital | We support Proposal 1.1-5C and Proposal 1.1-7D. |

##### **Open Issues: Issue #1 + #2 + #3**

**Issue #1) candidate SSB in DRS and DBTW support**

Provide further comments for Proposal 1.1-2A and 1.1-2B.

###### Proposal 1.1-2A

* DBTW is supported for 480 and 960 kHz and supports 64 candidate SSB positions

###### Proposal 1.1-2B

* DBTW is supported for 480 and 960 kHz and supports 128 candidate SSB positions

Summary of support for 1.1-2A (64 candidates):

* Support: Docomo, Lenovo/Motorola Mobility, LGE, Panasonic, Nokia/NSB
* Conditional support: Ericsson (only if common design for 120/480/960), Qualcomm (only if common design for 120/480/960)
* Ok to accept for sake of progress: Sharp, Futurewei, ZTE/Sanechips, vivo
* Not support but if had to choose can live with: Qualcomm
  + Benefits of 128 candidates does not outweigh specific effort needed
  + Common design between 120/480/960
  + Concerns on how 128 candidates signaling will be achieved as the changes are non-trivial in specification (e.g. Supporting 128 may require some bits to be swapped between MIB (RRC IE) and PBCH content in L1)

Summary of support for 1.1-2B (128 candidates):

* Support: OPPO, Samsung, Interdigital, ETRI, Sharp, Intel, vivo, Huawei/HiSilicon, ZTE/Sanechips (if 1 bit is available), Sony, NEC, Convida Wireless, CATT
* Ok to accept for sake of progress: Docomo, Sharp, Futurewei, Lenovo/Motorola Mobility
  + Support of 128 was not possible in 120kHz due to exceeding half radio frame, for 480/960 there is no technical barrier to support 128
  + 480/960kHz SSB is expected to less coverage compared to 120kHz SSB. Use of 64 beams with LBT is essential for 480/960kHz (more so than 120kHz).
  + Only having 64 candidates undermines support of DBTW. If 64 candidates are supported, no need to optimize Q signaling in MIB.
  + SSB with LBT operation is needed for regulatory domain without short control signal exemption (e.g. Japan)
  + Unified design between 120/480/960 looks nice but not technically justified

Please refrain from repeating comments mentioned previously (including that I support A or B unless it is not captured in summary above). Please provide the following inputs.

* For companies not supportive of 128 candidates, please provide information that you are requesting from companies that support 64 candidates for you review the proposal (128 candidate) and possibly reconsider.
* For companies not supportive of 64 candidates, please provide information on what you would like to understand better that would allow you to review the proposal (64 candidates) and possibly reconsider.
* For companies supportive of 128 candidates, please provide information on how you think signaling aspects will be resolved, including details of the signaling bits needed.
* For companies supportive of 64 candidates, please provide information on how you think signaling aspects will be resolved, including details of the signaling bits needed

**Issue #2) bits utilized in PBCH for signaling for DBTW**

Please provide comments on Proposal 1.1-9 and 1.1-9E. At this point, moderator would like to encourage companies to provide constructive inputs to allow RAN1 to agree on some common aspects (rather than having nothing for next meeting).

###### Proposal 1.1-9

* For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW
  + If only 1 bit is needed: subCarrierSpacingCommon
  + If 2 bits is needed: subCarrierSpacingCommon, and spare-bit (not the Msg Extension bit)
  + FFS: if 3 bits are required

###### Proposal 1.1-9E

* (Working assumption) For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW
  + If only 1 bit is needed: subCarrierSpacingCommon
  + If 2 bits is needed: subCarrierSpacingCommon, and 1 bit from pdcch-ConfigSIB1 (pending CORESET0 or search space design would allow~~s~~ for this bit), else, use the spare-bit (not the Msg Extension bit)
    - If 2 bits are needed for both 120kHz and 480/960kHz cases, then use the same bit field combination (i.e. use pdcch-ConfigSIB1 bit for 120/480/960 kHz or spare-bit for 120/480.960 kHz)
    - Note: If pdcch-ConfigSIB1 bit is used, the use of controlResourceSetZero (searchSpaceZero) for 120 kHz and searchSpaceZero (controlResourceSetZero) for 480/960 kHz is not precluded
  + FFS: if 3 bits are required

Among the Proposal 1.1-9 and 1.1-9E, 1.1-9E seems to leave bit more room for discussion. Therefore, let try to converge to 1.1-9E if possible. Companies who are not supportive of 1.1-9E, please suggest methods to resolve your concerns for 1.1-9E.

Updated proposal 1.1-9E based on Qualcomm and Ericsson comments.

###### Proposal 1.1-9F

* (Working assumption) For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW
  + If only 1 bit is needed: subCarrierSpacingCommon
  + If 2 bits is needed: subCarrierSpacingCommon, and 1 bit from pdcch-ConfigSIB1 (pending CORESET0 or search space design would allow~~s~~ for this bit), else, use the spare-bit (not the Msg Extension bit)
    - The design of CORESET0 and search space shall be done without any consideration to this proposal
    - If 2 bits are needed for both 120kHz and 480/960kHz cases, then use the same bit field combination (i.e. use pdcch-ConfigSIB1 bit for 120/480/960 kHz or spare-bit for 120/480.960 kHz)
    - Note: If pdcch-ConfigSIB1 bit is used, the use of controlResourceSetZero (searchSpaceZero) for 120 kHz and searchSpaceZero (controlResourceSetZero) for 480/960 kHz is not precluded
  + FFS: if 3 bits are required
  + Note: the working assumption can be confirmed after RAN1 agrees on the number of needed SSB-CORESET0 offsets based on RAN4 channelization design

**Issue #3) Indication of DBTW and values of Q**

Please provide comments on Proposal 1.1-4F and 1.1-4G. At this point, moderator would like to encourage companies to provide constructive inputs to allow RAN1 to agree on some common aspects (rather than having nothing for next meeting).

###### Proposal 1.1-4F

* For 120kHz SCS, for values:
  + If 2 bits are available in MIB for , ~~at least support {16, 32, 64}~~
    - Codepoint 00 indicates DBTW disabled/not supported
    - Codepoints 01, 10, 11 indicate DBTW enabled with values of = {16, 32, X} where X if FFS
  + If 1 bit is available in MIB for , ~~support {32, 64}~~
    - Codepoint 0 indicates DBTW disabled/not supported
    - Codepoint 1 indices DBTW enabled with = 32
  + FFS: 1 bit or 2 bits used for

###### Proposal 1.1-4G

* For 120kHz SCS, for values:
  + If 2 bits are available in MIB for , at least support {16, 32, 64}
  + If 1 bit is available in MIB for , at least support {32, 64}
    - FFS: methods to indicate more values, e.g., {16, 32, 64}
  + FFS: 1 bit or 2 bits used for

Also please provide suggestions to merge the gap between companies who support one proposal and object to the other proposal.

On top of the inputs on Proposal 1.1-4G and 1.1-4F, please provide inputs on whether you want to have 1 or 2 bits for . Being able to narrow this down is going to be also useful.

##### **Company comments**

|  |  |
| --- | --- |
| Company | Comment for #1, #2 and #3 |
| Qualcomm | Issue #2: may be we can address Nokia’s concern for Proposal 1.1-9E by adding a disclaimer:   * (Working assumption) For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW   + If only 1 bit is needed: subCarrierSpacingCommon   + If 2 bits is needed: subCarrierSpacingCommon, and 1 bit from pdcch-ConfigSIB1 (pending CORESET0 or search space design would allow~~s~~ for this bit), else, use the spare-bit (not the Msg Extension bit)     - The design of CORESET0 and search space shall be done without any consideration to this proposal     - If 2 bits are needed for both 120kHz and 480/960kHz cases, then use the same bit field combination (i.e. use pdcch-ConfigSIB1 bit for 120/480/960 kHz or spare-bit for 120/480.960 kHz)     - Note: If pdcch-ConfigSIB1 bit is used, the use of controlResourceSetZero (searchSpaceZero) for 120 kHz and searchSpaceZero (controlResourceSetZero) for 480/960 kHz is not precluded   + FFS: if 3 bits are required   Issue #3: Having the same comment we had before, unless we are misunderstanding the proposal, but it seems like Proposal 1.1-4F requires 1 extra codepoint to convey the enable/disable of DBTW where the other proposal can do that without this extra codepoint. Hence we support Proposal 1.1-4G. |
| LG Electronics | Issue #1: We still strongly support 64 candidate SSB positions for all SCSs. To support 128 candidate SSB positions, PBCH should be designed to indicate 7-digit SSB indexes and to signal Q values based on 128 candidate positions. We have to spend more time to decide additional details, thus we don’t prefer to put our efforts into optimizing DBTW for optional SCS.  Issue #2: We prefer Proposal 1.1-9, but can accept Proposal 1.1-9E.  Issue #3: We are fine with Proposal 1.1-4G, but do not support Proposal 1.1-4F with the same reason with Qualcomm. In addition, we prefer two bits for Q indication. |
| Huawei, HiSilicon | **Issue #1)**  We support Proposal 1.1-2B.  **Issue #2)**  We support Proposal 1.1-9E. This is more flexible than Proposal 1.1-9 and we think provides a good framework at this stage where the number of bits for is not determined and CORESET0 and Search space Tables are not agreed yet. Also Proposal 1.1-9E includes Proposal 1.1-9.  **Issue #3)**  We support Proposal 1.1-4G and cannot support Proposal 1.1-4F. We think that should be indicated for 120 kHz which also serves as DBTW DISABLE. We don’t see the reason to agree on the mapping between codepoint and but if such a discussion is necessary, then codepoint 11 (and not codepoint 00) which corresponds to the maximum value of should be used as indicator to DBTW DISABLE. |
| OPPO | Issue #1)  We support Proposal 1.1-2B.  Issue #2)  We support Proposal 1.1-9.  Issue #3)  We support Proposal 1.1-4G and cannot support Proposal 1.1-4F. |
| Ericsson | **Issue #1**  Support Proposal 1.1-2A  Object to Proposal 1.1-2B. As we have stated multiple times, we have strong concerns on implementation impact from supporting different methods for 120/480/960 kHz. Support of 128 candidate positions requires signaling a 7th bit for SSB index and the solutions on the table affecting low level PBCH/MIB processing, and we do not agree to support a feature that is weakly motivated and requires such a fundamental change.  **Issue #2**  Support Proposal 1.1-9. We don't understand why it is not possible to agree to this right now – the bits are available (low hanging fruit), and there is no dependence on CORESET0 configuration design. We think it is better to decouple these issues.  We are strongly skeptical about Proposal 1.1-9E, but if we are alone in opposing it we can live with it as long as the following note is added (consistent with Proposal 1.3-1A)   * + Note: the working assumption can be confirmed after RAN1 agrees on the number of needed SSB-CORESET0 offsets based on RAN4 channelization design   **Issue #3**  Support Proposal 1.1-4F. We are confused about the comments that this requires 1 extra codepoint compared to the solution where 64 indicates DBTW disabled.  **Object to Proposal 1.1-4G unless indication of DBTW enable/disable is included**. Our objection is based on that DBTW enable/disable is not indicated. We are fine if it is indicated implicitly, e.g., by Q = 64. We don't understand why this has been removed from the "package" agreement since we have been discussing this for a long time now. For licensed operation, it is needed to support a mechanism to indicate DBTW disabled/not relevant since the UE does not know a priori if the band is licensed or unlicensed since the bands overlap. Supporting such a mechanism has been agreed previously, also for IDLE mode UEs.  We can support Proposal 1.1.-4G with the following revision   * For 120kHz SCS, for values:   + If 2 bits are available in MIB for , at least support {16, 32, 64}   + If 1 bit is available in MIB for , ~~at least~~ support {32, 64}     - ~~FFS: methods to indicate more values, e.g., {16, 32, 64}~~   + Value 64 indicates DBTW disabled/not supported   + FFS: 1 bit or 2 bits used for |
| Moderator | Updated proposal 1.1-9E to 1.1-9F based on comments from Ericsson and Qualcomm. |
| Sharp | Issue #3:  We support Proposal 1.1-4G. It is observed that consensus in this meeting is that 1 bit from subCarrierSpacingCommon can be used without any dependency. Thus, it might be better to focus the assumption of 1 bit for , which could help completing the task within limited time, although with some compromises. Otherwise, the discussion would be suspended waiting for decisions of other issues (1 bit from pdcch-ConfigSIB1) or response from RAN2 (the spare bit). |
| DOCOMO | For Issue#2, while we can accept the Proposal 1.1-9F, we prefer Proposal 1.1-9 as we would like to avoid relying this discussion on such uncertain aspects.  For Issue#3, we are open for either Proposal 1.1-4G revised by Ericsson or Proposal 1.1-4F. We strongly prefer to reduce the number of FFSs. |
| Panasonic | Issue #2: We are fine with Proposal 1.1-9F.  Issue #3: Our preference is Proposal 1.1-4G, but we are also OK with Proposal 1.1-4F. In our understanding, at least for 120 kHz SCS (64 SSB candidate positions), both proposals would behave similarly if X value is not 64 and “Codepoint 00” means that the maximum number of beams (i.e., 64 beams) can be utilized. We prefer two bits for Q indication. |
| vivo | Issue #2: We are fine with Proposal 1.1-9F  Issue #3: We support Proposal 1.1-4G. For 120KHz, UE behavior and assumption for Q=64 and DBTW disable is the same. No need to indicate DBTW disable or not. |
| Nokia (4th round) | **Issue #1)**  We would still be supportive 1.1-2A of these two alternatives. Like noted earlier, we hope that this would facilitate finalizing the DBTW design for all SCS at one go.  **Issue #2)**  I would strongly prefer proposals 1.1-9. I think it is in practice impossible to isolate the two aspects (CORESET#0/Type0-CSS design and indication) if we go with 1.1-9E. In the end, if we are only company in favor of 1.1-9, we can compromise to 1.1-9F  **Issue #3)**  We would be OK with proposal 1.1-4F or 1.1.-4G accounting the change proposal from Ericsson. |
| ZTE, Sanechips | Issue #1: We prefer Proposal 1.1-2B. but for the sake of progress. we can also accept Proposal 1.1-2A.  Issue #2: We support Proposal 1.1-9F. Indication the parameters of DBTW should not impact the design of CORESET0/Type0-PDCCH.  Issue #3: We support Proposal 1.1-4G and cannot support Proposal 1.1-4F. |
| Interdigital | **Issue #1)** We support 1.1-2B with 128 candidate positions. We have made a proposal that was mentioned in the previous round of discussions on how to include the 7th indication bit combined with the indication of DBTW disabled and the values for .  Proposal) For 480 and 960kHz, if 2 bits are available in MIB for , below table can be used to indicate DBTW enabled/disabled along with the Q parameter, while supporting up to 128 candidate SSB positions:   |  |  |  |  | | --- | --- | --- | --- | | 1st bit | 2nd bit | Codepoint | Description | | 0 | 0 | 00 | DBTW is disabled | | 0 | 1 | 01 | - DBTW is enabled and .  - 2nd bit is used to indicate the 7th bit for 128 candidate positions. | | 1 | 0 or 1 | 10 or 11 | - DBTW is enabled and .  - 2nd bit is used to indicate the 7th bit for 128 candidate positions. | | Note: The 2nd bit is also used as the 7th bit for indication of up to 128 candidate positions, i.e. 2nd bit = 0 for SSB indexes<64 and 2nd bit = 1 for SSB indexes>=64.  Example 1) If SSB candidate index = 50, obviously the 2nd bit = 0. So, the value of the 1st bit equal to 0 indicates DBTW is disabled. Otherwise if 1st bit is equal to 1, it indicates DBTW is enabled and .  Example 2) If SSB candidate index = 70, obviously the 2nd bit = 1. So, the value of the 1st bit equal to 0 indicates DBTW is enabled and . Otherwise if 1st bit is equal to 1, it indicates DBTW is enabled and . | | | |   **Issue #2)** We are ok with Proposal 1.1-9F.  **Issue #3)** We support 1.1-4F as it has a dedicated codepoint to enable/disable the DBTW, allowing future progress and increase of SSB candidate positions in SCS 120kHz. |
| Futurewei | We support Proposal 1.1-2B  We support Proposal 1.1-9F.  We support Proposal 1.1-4G |
| Qualcomm 2 | We are fine with updated: Proposal 1.1-9F and Ericsson’s updates to Proposal 1.1.-4G, i.e.:   * For 120kHz SCS, for values:   + If 2 bits are available in MIB for , at least support {16, 32, 64}   + If 1 bit is available in MIB for , ~~at least~~ support {32, 64}     - ~~FFS: methods to indicate more values, e.g., {16, 32, 64}~~   + Value 64 indicates DBTW disabled/not supported   + FFS: 1 bit or 2 bits used for |

##### **Deferred Issues: Issue #5 + #7 + #8**

Moderator suggests continuing discussion for the following issues in the next meeting.

* Issue #5) DBTW lengths for 480 and 960 kHz
* Issue #7) ssb-PositionsInBurst signaling details for 480 and 960 kHz in SIB1
* Issue #8) QCL derivation equation for DRS

**Moderator Suggestion:**

* Further discuss the following issues in RAN1 #107-e
  + Issue #5) DBTW lengths for 480 and 960 kHz
  + Issue #7) ssb-PositionsInBurst signaling details for 480 and 960 kHz in SIB1
  + Issue #8) QCL derivation equation for DRS

#### <Summary of 4th Round of Discussions>

*<Moderator to prepare summary>*

### 2.1.2 SSB Resource Pattern

* From [1] Huawei/HiSilicon:
  + Support following patterns for SSB with 480 kHz and 960 kHz SCS:
    - For operations without shared spectrum:
      * {2,9}+14n, (n=0,1,2,…,31) for both 480 kHz and 960 kHz SCS.
    - For operations with shared spectrum:
      * {2,9}+14n, (n=0,1,2,…,31,40,…,71) for 480 kHz SCS;
      * {2,9}+14n, (n=0,1,2,…,63) for 960 kHz SCS.
* From [2] Futurewei:
  + For SS/PBCH transmission at 480kHz and respectively 960kHz use “n” values that correspond to SS/PBCH transmission gaps of 8 slots and respectively 16 slots to allow low latency traffic transmissions.
* From [4] ZTE, Sanechips:
  + The following design of candidate SSBs with SCS 480/960 kHz in a half frame can be considered: First symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
    - If DBTW is not supported or DBTW is disabled
      * For 480kHz SCS, the 64 candidate SSBs are located in 32 slots, with 2 slots spacing between every 8 consecutive slots to avoid prolonged occupation, i.e. n=0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 20, 21, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 34, 35, 36, 37
      * For 960kHz SCS, the 64 candidate SSBs are located in 32 slots, with 4 slots spacing between every 16 consecutive slots to avoid prolonged occupation, i.e. n=0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35
    - If DBTW is supported and it is enabled
      * Additional 64 candidate SSB can be defined after the above original 64 candidate SSBs in the half frame
* From [5] vivo:
  + Non-LBT scenario: the value of ‘n’ for SCS 480 kHz and 960 kHz can be set as:
    - n=0,1,4,5,8,9,12,13,16,17,20,21,24,25,28,29,40,41,44,45,48,49,52,53,56,57,60,61,64,65,68,69.
  + LBT scenario: the value of ‘n’ for SCS 480 kHz and 960 kHz can be set as:
    - n=0,1,4,5,8,9,12,13,16,17,20,21,24,25,28,29,40,41,44,45,48,49,52,53,56,57,60,61,64,65,68,69, 80,81,84,85,88,89,92,93,96,97,100,101, 104,105, 108, 109,120,121,124, 125, 128, 129,132,133,136,137,140,141,144,145,148,149
* From [8] NEC:
  + Additional n values of 4, 9, 14 and 19 should be supported to indicate 80 candidate SSBs in DBTW at least for 120 kHz SCS SSB pattern.
  + The indication of additional candidate SSBs based on additional values should be investigated.
* From [9] CATT:
  + Confirming the working assumption of candidate SSB index number of 120 kHz SCS can be postponed to after the decision on maximum number of can SSB index supported for 480/960 kHz.
* From [11] Ericsson:
  + For SS/PBCH block with 120 kHz SCS, no new values of n are supported. Hence the Case D pattern from Rel-15 is supported.
  + For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame, and n = 0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 20, 21, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 34, 35, 36, 37.
* From [12] Nokia, NSB:
  + Support in for 480kHz and 960kHz SSB pattern design with slots without SSB candidate locations at every 0.25ms.
  + Define SSB slot pattern for 480kHz and 960kHz sub-carrier spacing so that 8 consecutive slots are contain SSB candidate locations, followed by 4 slots are left unoccupied (by SSBs), until all SSBs locations are accounted. Determine the slot indexes n for candidate locations as follows:
    - The slot indexes n={0,1,2,3,4,5,6,7,
    - 12,13,14,15,16,17,18,19,
    - 24,25,26,27,28,29,30,31,
    - 36,37,38,39,40,41,42,43}
* From [13] Samsung:
  + For 480 kHz and 960 kHz, the first symbols of candidate SS/PBCH block have indexes , wherein:
    - for 480 kHz SCS and operation without shared spectrum channel access;
    - for 480 kHz SCS and operation with shared spectrum channel access;
    - for 960 kHz SCS and operation without shared spectrum channel access;
    - for 960 kHz SCS and operation with shared spectrum channel access.
* From [15] Intel:
  + For SSB SCS 120 kHz, reuse Case D pattern for SSB candidate slot positions within a half-frame.
  + Consider SSB pattern in a slot with 3 SSB containing slots, each slot with 2 SSB position, followed by 1 non-SSB carrying slot for 480 kHz and 6 SSB carrying slots followed by 2 non-SSB carrying slots for 960kHz.
    - For 480kHz and 960kHz SCS based SSB, first symbols of the candidate SSB have indexes {2,9} + 14×n, where index 0 corresponds to the first symbol of the first slot in a half-frame.
    - For 480kHz, n = {0,1,2, 4,5,6, 8,9,10, 12,13,14, 16,17,18, 20,21,22, 24,25,26, 28,29,30, 32,33,34, 36,37,38, 40,41}, {42, 44,45,46, 48,49,50, 52,53,54, 56,57,58, 60,61,62, 64,65,66, 68,69,70, 72,73,74, 76,77,78, 80, 81, 82, 84}.
      * The second set of n values could be used to enable larger number of candidate SSBs, i.e.,
    - For 960kHz, n = {0,1,2,3,4,5, 8,9,10,11,12,13, 16,17,18,19,20,21, 24,25,26,27,28,29, 32,33,34,35,36,37, 40,41}, {42,43,44,45, 48,49,50,51,52,53, 56,57,58,59,60,61, 64,65,66,67,68,69, 72,73,74,75,76,77, 80,81,82,83}.
      * The second set of n values could be used to enable larger number of candidate SSBs, i.e.,
* From [16] NTT Docomo:
  + For SSB slots “n” with 480/960 kHz SCS, the following alternatives can be considered where we prefer Alt 3 the best::
    - Alt 1: Reuse “n” values defined for Case D in Rel-15/16
    - Alt 2: Define “n” values as a set of consecutive slots
    - Alt 3: Define “n” values with more number of non-SSB slots between two set of consecutive SSB slots within a SSB burst
* From [17] Panasonic:
  + For SSB slot position, Case D SSB patten is reused (i.e., n = 0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 20, 21, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 34, 35, 36, 37).
* From [19] ETRI:
  + Confirm the working assumption on the number of candidates SSBs for 120kHz as an agreement.
* From [20] Lenovo, Motorola Mobility:
  + For supporting NR from 52.6 GHz to 71 GHz in Rel. 17, for higher subcarrier spacings (numerologies) such as 960kHz for SSB, to allow the beam switching between contiguous SSBs and between SSB and CORESET, a gap (for example a symbol gap or post-fix) should be supported for beam switching at least for 960kHz
* From [21] Interdigital:
  + Support using gap slots in Case D SSB pattern in SCS 120kHz for the candidate SSB positions, wherein multiple subsets of candidate SSB indexes per gap slot are considered.
* From [22] LG Electronics:
  + For 480/960 kHz SSB, first symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame (as per agreement made in RAN1#106-e), and values of ‘n’ are consecutive integers (i.e., n = 0, 1, 2, …, 31).
* From [23] Sharp:
  + Non-contiguous values of n with 3 or 4 gap slots between SSB slots should be considered.
* From [26] Qualcomm:
  + for 480 kHz/960 kHz SSB pattern, consider the following options:
    - For 480 kHz SCS, select one of:
      * SSB slots (n) = {1, 2, 3, 4} + 6\*m, where m = 0, 1, …, 7, or
      * SSB slots (n) = {n1, n2}
        + {n1} = {1, 2, 3, 4} + 6\*m, where m = 0, 1, 2, 3
        + {n2} = {33, 34, 35, 36} + 6\*m, where m = 0, 1, 2, 3
    - For 960 kHz SCS:
      * SSB slots (n) = {2, 3, 4, 5, 6, 7, 8, 9} + 12\*m, where m = 0, 1, …, 7
    - Keep the 20 ms initial access SSB pattern period

Chart

Description automatically generated

#### Summary of Discussions

In previous RAN1 meetings the following agreement was made.

|  |
| --- |
| **Agreement:**  For SSB with 120kHz SCS for NR 52.6 GHz to 71 GHz,   * 120 kHz SCS: the first symbols of the candidate SS/PBCH blocks have indexes {4, 8,16, 20} + 28×n, where index 0 corresponds to the first symbol of the first slot in a half-frame. * For carrier frequencies within 52.6 GHz to 71GHz, support at least 𝑛 = 0, 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 15, 16, 17, 18.   + Other values of *n* (if any) are FFS, and support of additional n values are subject to support of DBTW for 120kHz SSB   **Agreement:**   * For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, X} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame.      * Alt 1: X = 8 * Alt 2: X = 9   **Agreement:**  For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame. |

* SSB pattern for 120kHz
  + Use SSB case D from Rel-15 NR
    - Ericsson, Interdigital
* SSB slot pattern for 480 kHz:
  + Continuous slots, {2,9}+14n, (n=0,1,2,…,31)
    - Huawei/HiSilicon (for licensed), Samsung (for licensed), LGE
  + 8 slot gap every 32 slots, (n=0,1,2,…,31,40,…,71)
    - Huawei/HiSilicon (for unlicensed), Samsung (for unlicensed)
  + Gap every 8 slots
    - Futurewei
  + 2 slots gap every 8 slots, n=0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 20, 21, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 34, 35, 36, 37
    - ZTE, Sanechips, Ericsson, Panasonic
  + n=0,1,4,5,8,9,12,13,16,17,20,21,24,25,28,29,40,41,44,45,48,49,52,53,56,57,60,61,64,65,68,69
    - vivo
  + 4 slot gap every 8 slots, n={0,1,2,3,4,5,6,7,12,13,14,15,16,17,18,19,24,25,26,27,28,29,30,31, 36,37,38,39,40,41,42,43}
    - Nokia/NSB
  + 1 slot gap every 3 slots, n = {0,1,2, 4,5,6, 8,9,10, 12,13,14, 16,17,18, 20,21,22, 24,25,26, 28,29,30, 32,33,34, 36,37,38, 40,41}, {42, 44,45,46, 48,49,50, 52,53,54, 56,57,58, 60,61,62, 64,65,66, 68,69,70, 72,73,74, 76,77,78, 80, 81, 82, 84}
    - Intel
  + N slot gap every M slots
    - Docomo
  + 3 or 4 slot gap every M slots
    - Sharp
  + 4 slot gap every 8 slots, n={2, 3, 4, 5, 6, 7, 8, 9} + 12\*m
    - Qualcomm
* SSB slot pattern for 960 kHz:
  + Continuous slots, {2,9}+14n, (n=0,1,2,…,31)
    - Huawei/HiSilicon (for licensed), Samsung (for licensed), LGE
  + Continuous slots, (n=0,1,2,…,63)
    - Huawei/HiSilicon (for unlicensed), Samsung (for unlicensed)
  + Gap every 16 slots
    - Futurewei
  + 4 slot gap every 8 slots, n={0,1,2,3,4,5,6,7,12,13,14,15,16,17,18,19,24,25,26,27,28,29,30,31, 36,37,38,39,40,41,42,43}
    - Nokia/NSB
  + 8 slot gap every 16, n=0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35
    - ZTE, Sanechips
  + 2 slot gap every 6 slots, {0,1,2,3,4,5, 8,9,10,11,12,13, 16,17,18,19,20,21, 24,25,26,27,28,29, 32,33,34,35,36,37, 40,41}, {42,43,44,45, 48,49,50,51,52,53, 56,57,58,59,60,61, 64,65,66,67,68,69, 72,73,74,75,76,77, 80,81,82,83}
    - Intel
  + N slot gap every M slots
    - Docomo
  + 2 slots gap every 8 slots, n=0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 20, 21, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 34, 35, 36, 37
    - Panasonic, Ericsson
  + 4 slot gap every 8 slots, n={2, 3, 4, 5, 6, 7, 8, 9} + 12\*m
    - Qualcomm

#### <Moderator’s Suggestion for Discussions>

Discuss further on the following proposals, including further aspects that should be discussed together with Proposal 1.2-1 and 1.2-2.

##### Proposal 1.2-1

* Use SSB pattern case D from Rel-15 NR for 120 kHz SSB pattern

Moderator Note: Agreement from RAN1#104-bis implies we already agreed to use case D pattern for 120kHz. As Samsung pointed out not sure if this proposal needs to be agreed again.

##### Proposal 1.2-2

* Supported value of n for 480/960kHz SSB slot pattern:
  + ALT 1) contiguous, n = 0, 1, …, Lmax
  + ALT 2) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB
    - FFS: whether same pattern will apply to 480kHz and 960kHz (i.e same N and M for 480 and 960 kHz), or scaled version pattern will apply between 480 and 960 kHz (i.e. N and M for 480kHz, 2N and 2M for 960 kHz)
    - FFS: whether n will start from 0 or N
  + Moderator’s note: If Alt 2 is selected, RAN1 should work further during RAN1 #106bis-e to settle the final slot pattern (i.e. determine values of N and M and FFS aspects)

#### 1st Round of Discussions

Please provide further comments on the above issues (Proposal 1.2-1 and 1.2-2). Especially, which alternative (ALT 1 or 2) should be selected for Proposal 1.2-2. Also, if there are any other issues that require discussion, please comment them here.

|  |  |
| --- | --- |
| Company | Comments |
| NTT DOCOMO | We agree that Proposal 1.2-1 is something agreed already.  For Proposal 1.2-2, while we are relatively open to discuss, our best preference is ALT 2. We think the benefit given by contiguous “n” would not be significant. |
| OPPO | Proposal 1.2-1: support  Proposal 1.2-2: support |
| Qualcomm | Proposal 1.2-1: ok  Proposal 1.2-2: To allow for gaps for UL/DL switching and URLLC, we support Alt 2 as one option.  However, we prefer the 2nd FFS to be “FFS: starting position of n ~~whether n will start from 0 or N~~”. The reason for this is to allow for the option to be able to align the starting position of the SSB of 480/960 with that of 120 kHz.  Also, although not very strong, but may be good to add Alt 3 at this point to allow for different patterns between 480 and 960 kHz. This is because 480 kHz have longer sweep time and there may be a need to insert a longer gap (e.g. N’ > N) somewhere in the middle. This may not be needed for 960 kHz because of shorter sweep time:  *ALT 3) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB, additional N’ slot gaps may be inserted in the middle of the pattern. N’ may be the same or different for 480kHz and 960kHz.* |
| Lenovo, Motorola Mobility | Proposal 1.2-1: support  Proposal 1.2-2: We prefer Alt 1 but are open to discuss Alt 2. |
| Samsung | Proposal 1.2-1: We believe it is already supported by combining previous agreements.  Proposal 1.2-2: We would like to explain our principle for determining the value of n: in Rel-15, for FR2, slots are reserved after every 1 ms for the purpose of potential URLLC traffic, and we follow exactly the same principle to determine the values of n for 480 kHz and 960 kHz (i.e., align the slots containing SSB with 120 kHz). So in principle, it’s aligned with Alt 2, but it may finally look like Alt 1 if M is sufficiently large (e.g. M=32). For those proposing smaller value of M, we are wondering for FR2-2, why a tighter requirement on the URLLC traffic is considered comparing to FR2-1, and 480/960 kHz SCS has a tighter requirement than 120 kHz SCS?  Moreover, there seems a typo in Alt 1, and the upper bound should be “bar{L}\_max/2-1”. |
| Interdigital | **Proposal 1.2-1**: Support the proposal.  **Proposal 1.2-2**: Support the proposal. |
| LG Electronics | Proposal 1.2-1: We don’t need to discuss about the already agreed feature again.  Proposal 1.2-2: We totally share the view with Samsung. We prefer ALT 1 since the time duration for 64 SS/PBCH blocks for 480/960 kHz is short enough (i.e., less than or equal to 1 msec) and the gap for UL control channel is not required. Also we agree with Samsung’s modification to “bar{L}\_max/2-1”. |
| Ericsson | Proposal 1.2-1: Support. Actually, the RAN1#104bis-e agreement has an FFS, so we think this agreement is still useful. It resolves the FSS to say that no other values of n are supported.  Proposal 1.2-2: We support Alt-2 since we agree that slot gaps can be used for scheduling high priority UL. We are open to discuss what value of M and N is supported; however, we prefer a common design for both 480/960 kHz. |
| ETRI | We support both Proposal 1.2-1 and Proposal 1.2-2. |
| Sharp | Proposal 1.2-1: Okay.  Proposal 1.2-2: we are fine to the solution that aligning design with Rel-15 FR2 (e.g., reserve UL slots every 1 ms). |
| Intel | Proposal 1.2-1: Support.  Proposal 1.2-2: Support.  Our preference is Alt.2  One of the aspects that need to be considered is the multiplexing of SSB and PRACH. Currently the RO slots are 3 or 7 for 480kHz and 7 and 15 for 960kHz.  If SSB are occupying 3 or 7 for 480kHz and 7 and 15 for 960kHz, then we can potentially have collision between SSB and RO. While specification puts priority for SSB and considers any collision invalid ROs, this would mean significant number of ROs are invalided for many PRACH configurations.  Therefore, we think it is important to make sure RO and SSB do not overlap as much as possible and if possible, completely avoided by design. This means we should support at least some gaps for SSB contained slots.  SSB slot pattern of 3 SSB slots followed by 1 non-SSB slot for 480kHz and 6 SSB slots followed by 2 non-SSB slots for 960kHz seems to work well with RO slot placements. Therefore, we suggest going further and try to agree to the exact pattern this meeting.  Please note this is quite different for FR1 and existing FR2 design, as some gaps at the end of the slots were possible to use by PRACH in some PRACH configurations. For 480/960kHz due the short symbol duration and slot duration, we do not expect DL and UL signals to be meaningfully multiplexed in the same slot. Therefore, slots where UL can be sent should be made available in the specifications. |
| vivo | Proposal 1.2-1: Support  Proposal 1.2-2: Prefer Alt. 3 proposed by Qualcomm and can accept Alt. 2.  If looking at 120KHz SSB design, there are two kinds of gaps: one is short gap between contiguous SSB slots which could allow transmission of short UL control information; the other is long gap (i.e. 2 slot gap every 8 SSB slots) which could allow transmission of URLLC traffic. In another word, for short gap, it occurs every 0.125ms to allow short UL control information and occurs every 1ms to allow URLLC data transmission. For 480K and 960KHz design, at least the same goal as above should be achieved. If Alt. 1 is adopted, considering UL DL switching time, short UL control information can only be sent after 1ms, which becomes even worse than 120KHz. So Alt. 1 is not acceptable to us.  To allow short control information, N=1 or 2 may be enough considering 7us UL-DL switching time. However, to allow URLLC traffic transmission, larger N’ may be needed. So Alt. 3 proposed by Qualcomm is preferred by us. Besides, to allow larger N’ in the middle could easily align the SSB position for 120KHz. One example is provided below (N=2, M=2, N’=8): |
| Huawei, HiSilicon | **Proposal 1.2-1**: support  **Proposal 1.2-2:** Suggest modification. Note that:   * If is agreed for 480/960, then the candidate SSBs for 480 kHz with DBTW ON span the duration that is approximately 4 times longer than the SSB burst for 960 kHz with DBTW OFF. So, we don’t think that exactly the same SSB pattern design should necessarily be used for both cases. * As Rx-Tx and Tx-Rx transition may be up to 7.015 usec (approximately 7 symbols in 960 kHz), a considerable portion of UL slots may be wasted in the transition time. Therefore, to reduce the percentage of transition time overhead, it is more sensible to reserve less number of set of consecutive slots for UL but, within each set, use more slots. * To this end, we prefer to use the same design principle as in 120 kHz Cased D for 480/960 kHz SSB: Reserve the slots for UL in 480/960 kHz that correspond to the reserved UL slots for Case D in 120 kHz:     As only 480 kHz SSB burst with DBTW ON spans more than equivalent of 8 slots in 120 kHz and the first slots in 120 kHz Case D that are reserved for UL are slots 9 and 10, we suggest to reserve the corresponding slots in 480 kHz with DBTW ON (slots 32 to 39) for UL as well. In all other cases, reserving UL slots are not necessary. We would like to add this option as an alternative to Proposal 1.2-2.  Also**,** in the first bullet should be changed to to be accurate ( is the maximum number of candidate SSBs and there are two SSBs per slot. Note that if DBTW is not agreed). We suggest the following: Proposal 1.2-2 (modified)  * Supported value of n for 480/960kHz SSB slot pattern:   + ALT 1) contiguous, n = 0, 1, …, ~~L~~~~max~~   + ALT 2) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB     - FFS: whether same pattern will apply to 480kHz and 960kHz (i.e same N and M for 480 and 960 kHz), or scaled version pattern will apply between 480 and 960 kHz (i.e. N and M for 480kHz, 2N and 2M for 960 kHz)     - FFS: whether n will start from 0 or N   + ALT 3) slots that do not contain SSB correspond to the slots that do not contain SSB in 120 kHz Case D.     - Note: ALT 3 means that only slots 32-39 for 480 kHz SSB pattern are reserved for UL and 960 kHz SSB pattern is contiguous. |
| ZTE, Sanechips | Proposal 1.2-1: Support  Proposal 1.2-2: We support Proposal 1.2-2, and prefer ALT 2) non-contiguous pattern to avoid prolonged occupation by SSBs and leave time gaps between SSBs for the transmission of uplink and urgent services. |
| Sony | We support Proposal 1.2-1.  We prefer Alt 2 to allow scheduling UL and URLLC traffic. We also prefer the same pattern for 480 and 960 kHz SCS. |
| Panasonic | Proposal 1.2-1: We are fine with the proposal.  Proposal 1.2-2: Our preference is ALT 2 to allow UL transmission in the gap. |
| Nokia | Proposal 1.2-1) This has been agreed already in our understanding, thus fine with the proposal (if confirmation needed)  Proposal 1.2-2) We are fine with the proposal (to down select from the two alternatives) and at this point would have a preference for Alt2 assuming that the UL gap pattern frequency is sufficiently increased from Case D. Also as expressed in our paper, we would need to reserve sufficient time allocation for UL to enable full UL slot. |
| Mediatek | Proposal 1.2-1: This topic has been agreed, the remaining issue is whether SSB slot is needed or not. Thus ok with the proposal.  Proposal 1.2-2: we support Alt 2 since UL transmission should be allowed during SSB transmission. |
| Futurewei | Proposal 2.1-1: We are OK with the Proposal.  Proposal 2.1-2: Support Alt 2 |
| Apple | Proposal 1.2-1: We shared the view that this has been agreed. Proposal 1.2-2: We support Alt.2 to allow UL transmission between consecutive SSB bursts. More specifically, a common design of M/N values is preferred. |

#### <Summary of 1st Round of Discussions>

Proposal 1.2-1

* Agree that already covered by previous agreement
  + Docomo, Samsung, LGE, Ericsson, Nokia/NSB, Mediatek, Apple
* Support: Qualcomm, OPPO, Lenovo/Motorola Mobility, Interdigital, Ericsson (to resolve the FFS from previous agreement), ETRI, Sharp, Intel, Huawei/HiSilicon, Panasonic, Futurewei
* Not support

Proposal 1.2-2

* Support: OPPO, Lenovo/Motorola Mobility, Interdigital, ETRI, Sharp (reserve UL slots every 1ms)
  + Alt 1: Lenovo/Motorola Mobility, LGE
    - Concerns: not able to support short UL control signal gap (every 0.125ms) and URLLC gap (every 1msec), large overlap with SSB and RO, Sony
  + Alt 2: Docomo, Qualcomm (FFS starting position of n), [Samsung], Ericsson, Intel, vivo (2nd preference), Sony, Pansonic, Nokia/NSB, Mediatek, Futurewei, Apple
    - Concerns: contiguous 480/960kHz SSB bursts are short enough to support URLLC gap (every 1msec)
  + Alt 3: [Qualcomm], vivo
  + Alt 4: Huawei/HiSilicon
* Not support

#### 2nd Round of Discussions

For Proposal 1.2-1, all companies agree in principal. Several companies pointed out previous agreement captures this. Some companies pointed out FFS is left open so agreement would be helpful to close the issue. Based on the comments Moderator suggest the following conclusion.

**Conclusion 1.2-3:**

* No other values of n other than agreed previously is supported for 120kHz SCS, where parameter ‘n’ is the set of values to determine the first symbols of the candidate SSB blocks for 120kHz SCS in agreement from RAN1 #104-bis-e.

**Previous Agreement (RAN1 #104-bis-e):**

For SSB with 120kHz SCS for NR 52.6 GHz to 71 GHz,

* 120 kHz SCS: the first symbols of the candidate SS/PBCH blocks have indexes {4, 8,16, 20} + 28×n, where index 0 corresponds to the first symbol of the first slot in a half-frame.
* For carrier frequencies within 52.6 GHz to 71GHz, support at least 𝑛 = 0, 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 15, 16, 17, 18.
  + Other values of *n* (if any) are FFS, and support of additional n values are subject to support of DBTW for 120kHz SSB

For proposal 1.2-2, majority of the companies seems to prefer alt 2 or alt 2 like non-consecutive SSB slot selection (15 for alt 2 or alt 2-like vs 3 for alt 1). Some companies comments that slots durations every 1msec should be reserved for UL traffic, and some companies commented that slots every few SSB slots should be reserved for short UL transmissions and possibly RO placements. While down-selecting to a specific proposal is difficult, release 17 completion date is looming and RAN1 needs to make progress. Moderator suggest to focus on Alt 2, 3, 4 or Proposal 1.2-2A.

##### Proposal 1.2-2A

* Supported value of n for 480/960kHz SSB slot pattern:
  + ~~ALT 1) contiguous, n = 0, 1, …, L~~~~max~~~~/2 - 1~~
  + ALT 2) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB
    - FFS: whether same pattern will apply to 480kHz and 960kHz (i.e same N and M for 480 and 960 kHz), or scaled version pattern will apply between 480 and 960 kHz (i.e. N and M for 480kHz, 2N and 2M for 960 kHz)
    - FFS: starting position of n~~whether n will start from 0 or N~~
  + ALT 3) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB, additional N’ slot gaps may be inserted in the middle of the pattern. N’ may be the same or different for 480kHz and 960kHz.
  + ALT 4) slots that do not contain SSB correspond to the slots that do not contain SSB in 120 kHz Case D.
    - Note: ALT 4 means that only slots 32-39 for 480 kHz SSB pattern are reserved for UL and 960 kHz SSB pattern is contiguous.

If the moderator takes comments from companies, it looks like for 480kHz slots 8k + {3,7} for 480kHz should be avoided (ROs and for short UL transmission), and slots {32 ~ 39}, {72~79} should be avoided (for urgent UL traffic), and for 960kHz slots 16k + {6,7,14,15} should be avoided (ROs and for short UL transmission), and slots {64 ~ 79} and {144~159} should be avoided (for urgent UL traffic). Proposal 1.2-2B has been made based on this observation. Please provide further comments, moderator thinks we should try to conclude on the final pattern in this meeting.

##### Proposal 1.2-2B

* Supported value of n for 480Hz SSB slot pattern:
  + If 64 SSB candidate positions are supported, n = {0,1,2, 4,5,6, 8,9,10, 12,13,14, 16,17,18, 20,21,22, 24,25,26, 28,29,30, 40,41,42, 44,45,46, 48,49}
  + If 128 SSB candidate position are supported, n = {0,1,2, 4,5,6, 8,9,10, 12,13,14, 16,17,18, 20,21,22, 24,25,26, 28,29,30, 40,41,42, 44,45,46, 48,49,50, 52,53,54, 56,57,58, 60,61,62, 64,65,66, 68,69,70, 80,81,82, 84,85,86, 88,89,90, 92,93,94, 96,97,98, 100}
* Supported value of n for 960kHz~~480Hz~~ SSB slot pattern:
  + If 64 SSB candidate positions are supported, n = {0,1,2,3,4,5, 8,9,10,11,12,13, 16,17,18,19,20,21, 24,25,26,27,28,29, 32,33,34,35,36,37, 40,41}
  + If 128 SSB candidate position are supported, n = {0,1,2,3,4,5, 8,9,10,11,12,13, 16,17,18,19,20,21, 24,25,26,27,28,29, 32,33,34,35,36,37, 40,41,42,43,44,45, 48,49,50,51,52,53, 56,57,58,59,60,61, 80,81,82,83,84,85, 88,89,90,91,92,93, 96,97,99,100}

Added proposal based on vivo’s comments

##### Proposal 1.2-2C

* Supported value of n for 480Hz SSB slot pattern:
  + If 64 SSB candidate positions are supported, n = {1,2, 5,6, 9,10, 13,14, 17,18, 21, 22, 25, 26, 29, 30, 41,42, 45, 46, 49, 50, 53, 54, 57, 58, 61, 62, 65, 66, 69, 70}
  + If 128 SSB candidate position are supported, n = {1,2,5,6,9,10,13,14,17,18, 21, 22, 25, 26, 29, 30, 41,42, 45, 46, 49, 50, 53, 54, 57, 58, 61, 62, 65, 66, 69, 70, 81,82, 85,86, 89,90, 93,94, 97,98, 101,102, 105,106, 109,110, 121,122, 125,126, 129, 130, 133,134, 137,138, 141,142, 145,146, 149,150}
* Supported value of n for 960Hz SSB slot pattern:
  + If 64 SSB candidate positions are supported, n = {2,3,4,5, 10,11,12,13, 18,19,20,21, 26,27,28,29, 34,35,36,37, 42,43,44,45, 50,51,52,53, 58,59,60,61}
  + If 128 SSB candidate position are supported, n = {2,3,4,5, 10,11,12,13, 18,19,20,21, 26,27,28,29, 34,35,36,37, 42,43,44,45, 50,51,52,53, 58,59,60,61, 82,83,84,85, 90,91,92,93, 98,99,100,101, 106,107,108,109, 114,115,116,117, 122,123,124,125, 130,131,132,133, 138,139,140,141}

Please provide comments on the proposals 1-2-3, 1.2-2A and 1.2-2B.

|  |  |
| --- | --- |
| Company | Comments |
| LG Electronics | Proposal 1.2-3: Support  Proposal 1.2-2A: If only 64 SSB candidate positions are supported, then Alt 1 and Alt 4 are eventually the same. With this understanding, we are OK with Alt 4.  Proposal 1.2-2B: We don’t understand the logic that RO location needs to be considered. First of all, we didn’t agree in which slot ROs are located, yet. Furthermore, even in Rel-15, is RACH slot considered to decide SSB pattern? From our understanding, RACH slot can be configured in any slot based on proper configuration so we don’t need to consider RACH slot to determine SSB pattern. |
| vivo | Proposal 1.2-3: Support  Proposal 1.2-2A: Support  Proposal 1.2-2B: Should the 2nd bullet for 960KHz SSB slot pattern?  Regarding the actual value of n, we think 120KHz SSB pattern should be the reference design. The design for 480K/960K can be aligned with 120K as much as possible. Based on this, our proposal would be:   * Supported value of n for 480Hz SSB slot pattern:   + If 64 SSB candidate positions are supported, n = {1,2, 5,6, 9,10, 13,14, 17,18, 21, 22, 25, 26, 29, 30, 41,42, 45, 46, 49, 50, 53, 54, 57, 58, 61, 62, 65, 66, 69, 70}   + If 128 SSB candidate position are supported, n = {1,2,5,6,9,10,13,14,17,18, 21, 22, 25, 26, 29, 30, 41,42, 45, 46, 49, 50, 53, 54, 57, 58, 61, 62, 65, 66, 69, 70, 81,82, 85,86, 89,90, 93,94, 97,98, 101,102, 105,106, 109,110, 121,122, 125,126, 129, 130, 133,134, 137,138, 141,142, 145,146, 149,150} * Supported value of n for 960Hz SSB slot pattern:   + If 64 SSB candidate positions are supported, n = {2,3,4,5, 10,11,12,13, 18,19,20,21, 26,27,28,29, 34,35,36,37, 42,43,44,45, 50,51,52,53, 58,59,60,61}   + If 128 SSB candidate position are supported, n = {2,3,4,5, 10,11,12,13, 18,19,20,21, 26,27,28,29, 34,35,36,37, 42,43,44,45, 50,51,52,53, 58,59,60,61, 82,83,84,85, 90,91,92,93, 98,99,100,101, 106,107,108,109, 114,115,116,117, 122,123,124,125, 130,131,132,133, 138,139,140,141}   One picture is shown below is candidate number of SSB is 64: |
| DOCOMO | For Conclusion 1.2-3, although we believe it is not needed because of the previous agreement, we are ok with confirming this explicitly if argued necessary.  For Proposal 1.2-2A/B:   * We are ok to remove Alt 1. * We understand that Proposal 1.2-2B is a specific example of Alt 3 of Proposal 1.2-2A (BTW, 2nd main bullet of Proposal 1.2-2B should be for 960kHz SCS)   Among three alternatives (i.e., Alt 2, Alt 3/Proposal 1.2-2B, Alt 4), we prefer Alt 2. It is important to have sufficiently large value of N, e.g. 8, to provide sufficient set of resources for DL/UL data transmission with multi-PDSCH/PUSCH scheduling or repetition, which would be typical in FR2-2, even within a half frame containing SSBs. In that sense, we can also live with Alt 3/Proposal 1.2-2B as it can also provide sufficiently large N or N’. |
| Samsung | Proposal 1.2-3: We are ok with the conclusion.  Proposal 1.2-2A: We agree with LG’s observation that Alt 1 and Alt 4 are the same if bar{L}\_max is 64. In this sense, we are ok to remove Alt 1 and we support Alt 4. The reason to support Alt 4 is trying to align the design principle as in Rel-15 FR2-1: it is clear that the gaps are aligned for 120 kHz and 240 kHz to reserve resource for URLLC traffic, with the assumption of 1ms latency requirement. Those gaps are not reserved for HARQ or RO, since HARQ can be multiplexed within the slots containing SSB and no special design is needed, while RO is not required to be considered for SSB pattern design. Also, we want to note that it’s beneficial to maintain the SSB transmission as minimum number of bursts as possible, such that the number of LBT can be minimized. In light of this, it would be the best to keep a single burst of SSB unless some resources have to reserved for essential UL transmission, such as 1 ms requirement for URLLC traffic.  Proposal 1.2-2B: We don’t such fine tuning of the slot number is needed. |
| Intel | Proposal 1.2-2A: Support.  Our preference is Alt.-2. Other alternatives seem to overcomplicate the design. At higher SCS, SS burst transmission is pretty fast. If it’s absolutely necessary (which we don’t believe in), gNB always can drop some of SSBs in favor of urgent UL transmissions.  Proposal 1.2-2B: if we have gap slots every few SSB slots, then we may not need another long gap slots every 1 msec. With this said for the sake of progress we would be ok to accept proposal 1.2-2B. We assume that the second main bullet corresponds to SCS 960 kHz (not 480 kHz). |
| Interdigital | Proposal 1.2-2A: We support Alt 4.  Proposal 1.2-2B: We do not support this proposal. The SSB pattern does not need to consider the RO placement as the PRACH slots are configurable and can be determined separate from SSB burst. |
| Qualcomm | Conclusion 1.2-3: agree  Proposal 1.2-2A: We are fine with either Alt 2 or Alt 3  Proposal 1.2-2B: Rel-15 does not support such optimization and there are rules defined for the case RO collides with SSB, hence we do not see a need to optimize for this for 480/960 kHz |
| Lenovo, Motorola Mobility | Conclusion 1.2-3: We are fine with the conclusion  Proposal 1.2-2A: We prefer Alt 4 as our main preference but are open to discuss Alt 2. |
| Moderator | Just a quick response to LGE. In last meeting RAN1 agreed to following:   |  | | --- | | Agreement:  For 480 and 960kHz PRACH,   * When a PRACH slot can contain all time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching,   + and when number of PRACH slots in a reference slot is 1,     - for 480kHz and for 960kHz PRACH   + and when the number of PRACH slots in a reference slot is 2,     - for 480kHz and for 960kHz PRACH * FFS: values, when a PRACH slot cannot contain all time domain PRACH occasions~~,~~ corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching.   FFS: whether to allow for additional values if the maximum that can be configured for the number of FD RO’s is less than 8 (due to BW limitation) |   Based on this I assumed we already know where the RO will be placed (at least for cases when we don’t have gaps). With gaps, I assumed it will be 1 more slot before the (tentatively) agreed set of values.  Just one thing about Proposal 1.2-2B, this is a proposal that no company presented. It was just my attempt on trying to consolidate comments received by companies from the 1st round. While companies should continue to express support and reasons for concerns/objections, I would appreciate if company can also provide ways that they think can provide a compromising proposal that would be acceptable by all. If all companies simply object to each other proposal and just say no, we are not going to able to finish this work.  That said, if companies can express views on which alt in Proposal 1.2-2A they prefer, it would be helpful. |
| Qualcomm | Comments on added proposal Proposal 1.2-2C: this may unnecessarily add the SSB sweep time. If beams are aligned between SCSs, it can be useful (beam direction blockage is reduced in cases of CA), but since it is not possible to align beams with Proposal 1.2-2C (we are only aligning gaps), not sure what the value is. |
| Sharp | Proposal 1.2-2A: We prefer ALT 4. |
| Apple | **Proposal 1.2-3:** Support  **Proposal 1.2-2A:** Support.  Among Alternatives, our preference is Alt.2 to reserve resource for UL transmission. The usage of ‘N’’ in Alt.3 is not clear for us at this moment. We are open to discuss it. We also share view that Alt.1 and Alt.4 are same if maximum SSB candidates is 64. The motivation to remove Alt.1 and add Alt.4 seems only progress if the maximum number SSB candidates would be increased to 128, which is FFS.  **Proposal 1.2-2B**: Not support.  We share Qualcomm’s view that SSB pattern design is unnecessary to consider the PRACH resource allocation. There are different ways to avoid collision by properly selecting RO time-domain configuration, e.g., in different radio frames, different slots of a same subframe. Given the quite shorter burst duration of SSB, this becomes easier for new SCSs compared to legacy. Even collision happens in a same slot, the collision handling rule in current specification can be reused to address it during RO validation procedure. |
| LG Electronics | @ Moderator,  Thanks for the response. Even for that agreement, the RACH slot index is with square bracket so uncertain to some extent. Anyway, the main point was we don’t need to RACH slot location to determine SSB pattern. |
| OPPO | **Proposal 1.2-3:** Support.  **Proposal 1.2-2A**: Support.  **Proposal 1.2-2B**: Not support. |
| Ericsson | Proposal 1.2-3: Support  Proposal 1.2-2A: Support  Proposal 1.2-2B: We don’t think it is necessary to align SSB gaps with ROs  Proposal 1.2-2C: We prefer a shorter SSB beam sweep. |
| Panasonic | Conclusion 1.2-3: We are fine with the conclusion.  Proposal 1.2-2A: We are fine with the proposal. Although our preference is Alt.2, we are fine with Alt.3 if the usage of N’ is clarified.  Proposal 1.2-2B: We don’t think optimization between SSB position and RO is needed as mentioned by several companies.  Proposal 1.2-2C: We share similar view with Qualcomm that the benefit to align 120 kHz SCS would be unclear. |
| ZTE, Sanechips | Conclusion 1.2-3: Support the conclusion.  Proposal 1.2-2A: We support the proposal and prefer Alt-2 as it is simple and effective.  Proposal 1.2-2B/2C: Correct some typos in the Proposal 1.2-2B. We also think the value of N slots (gap) should preferably be greater than 1 in order to facilitate multi-slot PUSCH scheduling for larger SCSs.   * Supported value of n for 480kHz SSB slot pattern:   + If 64 SSB candidate positions are supported, n = {0,1,2, 4,5,6, 8,9,10, 12,13,14, 16,17,18, 20,21,22, 24,25,26, 28,29,30, 40,41,42, 44,45,46, 48,49}   + If 128 SSB candidate positions are supported, n = {0,1,2, 4,5,6, 8,9,10, 12,13,14, 16,17,18, 20,21,22, 24,25,26, 28,29,30, 40,41,42, 44,45,46, 48,49,50, 52,53,54, 56,57,58, 60,61,62, 64,65,66, 68,69,70, 80,81,82, 84,85,86, 88,89,90, 92,93,94, 96,97,98, 100} * Supported value of n for ~~480~~960kHz SSB slot pattern:   + If 64 SSB candidate positions are supported, n = {0,1,2,3,4,5, 8,9,10,11,12,13, 16,17,18,19,20,21, 24,25,26,27,28,29, 32,33,34,35,36,37, 40,41}   If 128 SSB candidate positions are supported, n = {0,1,2,3,4,5, 8,9,10,11,12,13, 16,17,18,19,20,21, 24,25,26,27,28,29, 32,33,34,35,36,37, 40,41,42,43,44,45, 48,49,50,51,52,53, 56,57,58,59,60,61, 80,81,82,83,84,85, 88,89,90,91,92,93, 96,97,99,100} |
| CATT | Proposal 1.2-3: Support  Proposal 1.2-2A: Support  Proposal 1.2-2B: We don’t think it is necessary to align SSB gaps with ROs |

#### <Summary of 2nd Round of Discussions>

Suggest to approve the conclusion 1.2-3 over email approval.

Conclusion 1.2-3

* Support: LGE, vivo, Docomo (Ok to agree though not needed), Lenovo/Motorola Mobility, Apple, OPPO, Ericsson, Panasonic, CATT

Companies seem to be generally ok with Proposal 1.2-2A. Further down-selection between 2, 3, and 4 is needed. Details of Alt 4 seems to be complete. Suggest companies that support Alt 2 and 3 to provide concrete details so that companies can review and down-select.

Proposal 1.2-2A

* Support: vivo, Docomo, Intel, Interdigital, Qualcomm, Sharp, Apple, OPPO, Ericsson, Panasonic, CATT
* Alt 2: Docomo, Intel, Qualcomm, [Lenovo/Motorola Mobility], Apple, Panasonic
* Alt 3: Qualcomm, Panasonic(if usage of N’ is clarified)
* Alt 4: LGE, Samsung (if Lmax = 64), Interdigital, Lenovo/Motorola Mobility, Sharp

Proposal 1.2-2B

* Support:
* Willing to accept: Docomo, Intel
* Not support: LGE, Samsung, Qualcomm, Apple, OPPO, Ericsson, Panasonic

Proposal 1.2-2C

* Support: vivo
* Not support: Qualcomm, Ericsson, Panasonic

#### 3rd Round of Discussions

Moderator assumes conclusion 1.2-3 will be treated for email approval and no further discussion is needed.

Please provide preferences on support of Alt 2, 3, and 4 for Proposal 1.2-2A.

Also from moderator understanding Alt 4 is the following Proposal 1.2-2D. Can companies confirm this is the correct understanding?

Can companies in favor of Alt 2 and Alt 3 provide detailed values of n? If companies are split on how Alt 2 and 3 should look like, maybe that could be reasons to try to converge to other alternative that has more support.

ALT 4) slots that do not contain SSB correspond to the slots that do not contain SSB in 120 kHz Case D.

* Case D - 120 kHz SCS: the first symbols of the candidate SS/PBCH blocks have indexes {4, 8,16, 20}+ 28\**n*.
* For carrier frequencies within FR2, 𝑛 = {0,1,2,3}, {5,6,7,8}, {10,11,12,13}, {15,16,17,18}.

###### Proposal 1.2-2D (alt 4)

* Supported value of n for 480Hz SSB slot pattern:
  + If 64 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, *(gap)* 20,21,22,23, 24,25,26,27, 28,29,30,31, 32,33,34,35}
  + If 128 SSB candidate position are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, *(gap)* 20,21,22,23, 24,25,26,27, 28,29,30,31, 32,33,34,35, *(gap)* 40,41,42,43, 44,45,46,47, 48,49,50,51, 52,53,54,55, *(gap here)* 60,61,62,63, 64,65,66,67, 68,69,70,71, 72,73,74,75}
* Supported value of n for 960kHzSSB slot pattern:
  + If 64 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31}
  + If 128 SSB candidate position are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31, *(gap)* 40,41,42,43, 44,45,46,47, 48,49,50,51, 52,53,54,55, 56,57,58,59, 60,61,62,63, 64,65,66,67, 68,69,70,71}

###### Proposal 1.2-3 (alt 4 revised correction)

* Supported value of n for 480Hz SSB slot pattern:
  + If 64 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, *~~(gap)~~* 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31~~, 32,33,34,35~~} (no gap slot)
  + If 128 SSB candidate position are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, *~~(gap)~~* 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31, ~~32,33,34,35,~~ *(gap)* 40,41,42,43, 44,45,46,47, 48,49,50,51, 52,53,54,55, 56,57,58,59 *~~(gap here)~~* 60,61,62,63, 64,65,66,67, 68,69,70,71, 72,73,74,75} (a gap of size 8 slots starting from slot 32)
* Supported value of n for 960kHzSSB slot pattern:
  + If 64 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31} (no gap slot)
  + If 128 SSB candidate position are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31, 32,33,34,35, 36,37,38,39 *~~(gap)~~* 40,41,42,43, 44,45,46,47, 48,49,50,51, 52,53,54,55, 56,57,58,59, 60,61,~~62,63, 64,65,66,67, 68,69,70,71~~} (no gap slot)

**Proposal 1.2-3A (alt 4 revised correction)**

* Supported value of n for 480Hz SSB slot pattern:
  + If 64 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, *~~(gap)~~* 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31~~, 32,33,34,35~~} (no gap slot)
  + If 128 SSB candidate position are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, *~~(gap)~~* 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31, ~~32,33,34,35,~~ *(gap)* 40,41,42,43, 44,45,46,47, 48,49,50,51, 52,53,54,55, 56,57,58,59 *~~(gap here)~~* 60,61,62,63, 64,65,66,67, 68,69,70,71, ~~72,73,74,75~~} (a gap of size 8 slots starting from slot 32)
* Supported value of n for 960kHzSSB slot pattern:
  + If 64 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31} (no gap slot)
  + If 128 SSB candidate position are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31, 32,33,34,35, 36,37,38,39 *~~(gap)~~* 40,41,42,43, 44,45,46,47, 48,49,50,51, 52,53,54,55, 56,57,58,59, 60,61,62,63, ~~64,65,66,67, 68,69,70,71~~} (no gap slot)

**Proposal 1.2-4 (alt 2 N=2, M=8)**

* Supported value of n for 480/960 kHz SSB slot pattern:
  + If 64 SSB candidate positions are supported, n = 0,1,2,3,4,5,6,7, 10,11,12,13,14,15,16,17, 20,21,22,23,24,25,26,27, 30,31,32,33,34,35,36,37
  + If 128 SSB candidate positions are supported, n = 0,1,2,3, 4,5,6,7, 10,11,12,13, 14,15,16,17, 20,21,22,23, 24,25,26,27, (gap) 30,31,32,33, 34,35,36,37, 40,41,42,43, 44,45,46,47, 50,51,52,53, 54,55,56,57, 60,61,62,63, 64,65,66,67, 70,71,72,73, 74,75,76,77

###### Proposal 1.2-4A (alt 2 N=4, M=8)

* Supported value of n for 480/960 kHz SSB slot pattern:
  + (Lmax/2 – 1) entries from pattern {1, 2, 3, 4, 5, 6, 7} + 12\*m, where m = 0, 1, …

###### Proposal 1.2-4B (alt 2 N=2, M=4 for 480kHz, N=4, M=8 for 960kHz)

* Supported value of n for 480/960 kHz SSB slot pattern:
  + For 480kHz: (Lmax/2 – 1) entries from pattern {1, 2, 3, 4} + 6\*m, where m = 0, 1, …
  + For 960kHz: (Lmax/2 – 1) entries from pattern {2, 3, 4, 5, 6, 7, 8, 9} + 12\*m, where m = 0, 1, …

###### Proposal 1.2-4C (alt 2 N=1, M=3 for 480kHz, N=2, M=6 for 960kHz)

* Supported value of n for 480/960 kHz SSB slot pattern:
  + For 480kHz: (Lmax/2 – 1) entries from pattern {0, 1, 2} + 4\*m, where m = 0, 1, …,
  + For 960kHz: (Lmax/2 – 1) entries from pattern {0, 1, 2, 3, 4, 5} + 8\*m, where m = 0, 1, …

**Proposal 1.2-4D (alt 2 N=2, M=8 for 480kHz, N=4, M=16 for 960kHz)**

* Supported value of n for 480 kHz SSB slot pattern:
  + If 64 SSB candidate positions are supported, n = 0,1,2,3,4,5,6,7, 10,11,12,13,14,15,16,17, 20,21,22,23,24,25,26,27, 30,31,32,33,34,35,36,37
  + If 128 SSB candidate positions are supported, n = 0,1,2,3,4,5,6,7, 10,11,12,13,14,15,16,17, 20,21,22,23,24,25,26,27, 30,31,32,33,34,35,36,37, 40,41,42,43,44,45,46,47, 50,51,52,53,54,55,56,57, 60,61,62,63,64,65,66,67, 70,71,72,73,74,75,76,77
* Supported value of n for 960 kHz SSB slot pattern:
  + If 64 SSB candidate positions are supported, n = 0,1,2,3,4,5,6,7,8,9, 10,11,12,13,14,15, 20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35
  + If 128 SSB candidate positions are supported, n = 0,1,2,3,4,5,6,7,8,9, 10,11,12,13,14,15, 20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35, 40,41,42,43,44,45,46,47,48,49,50,51,52,53,54,55, 60,61,62,63,64,65,66,67,68,69,70,71,72,73,74,75

##### **Company comments**

|  |  |
| --- | --- |
| Company | comments |
| Sharp | We support Proposal 1.2-2D. |
| LG Electronics | As a proponent of Alt 4, we suggest the following modification. Proposal 1.2-2D (alt 4)  * Supported value of n for 480Hz SSB slot pattern:   + If 64 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31}   + If 128 SSB candidate position are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31, *(gap)* 40,41,42,43, 44,45,46,47, 48,49,50,51, 52,53,54,55, 56,57,58,59, 60,61,62,63, 64,65,66,67, 68,69,70,71} * Supported value of n for 960kHzSSB slot pattern:   + If 64 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31}   + If 128 SSB candidate position are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31, 32,33,34,35, 36,37,38,39, 40,41,42,43, 44,45,46,47, 48,49,50,51, 52,53,54,55, 56,57,58,59, 60,61,62,63} |
| DOCOMO | We generally believe that larger number of consecutive non-SSB slots would be needed to accommodate UL repetitions and/or multi-PDSCH/PUSCH scheduling, e.g. N=8 in Alt 2 or Alt 3. Alt 3 differentiate N and N’ so that they can be different lengths assuming different usages, which could also be acceptable for us if either N or N’ could be sufficiently large. We are open for M value. In this sense, Proposal 1.2-2D is not our preference due to the length of consecutive non-SSB slots. |
| Nokia | (Just a note that we are also OK with Conclusion 1.2-3)  Apologizes if I miss something, but the wording for Alt4 seems to suggest that the intention is to leave same slots empty as with 120kHz? With 120kHz we have SSBs in 8 consecutive slots (flowed by gap of 2 slots). This would result 32 slots for e.g. 480kHz to be aligned.  In respective of Alt3/4 we had following proposal in our paper:  n={0,1,2,3,4,5,6,7,(gap),12,13,14,15,16,17,18,19,(gap),24,25,26,27,28,29,30,31,(gap)36,37,38,39,40,41,42,43}  I.e. M=8 with N=4. We assumed this to be identical to both scs (for simplicity), but it would be also possible option have different. |
| Panasonic | As a proponent of Alt 2, our preference for n values are as follows (N=2, M=8). It is based on Case D SSB pattern.   * Supported value of n for 480/960 kHz SSB slot pattern:   + If 64 SSB candidate positions are supported, n = 0,1,2,3,4,5,6,7, 10,11,12,13,14,15,16,17, 20,21,22,23,24,25,26,27, 30,31,32,33,34,35,36,37   + If 128 SSB candidate positions are supported, n = 0,1,2,3,4,5,6,7, 10,11,12,13,14,15,16,17, 20,21,22,23,24,25,26,27, 30,31,32,33,34,35,36,37, 40,41,42,43,44,45,46,47, 50,51,52,53,54,55,56,57, 60,61,62,63,64,65,66,67, 70,71,72,73,74,75,76,77 |
| Inerdigital | We support the proposal revision by LG.   * For 480kHz: No gap is required for 64 SSB candidate positions and only gap is required for extension to 128 SSB candidate positions. * For 960kHz: No gap is required, neither for 64 nor 128 SSB candidate positions. |
| Samsung | We support LG’s proposal, and we believe those are aligned with the intention of Alt 4. |
| Qualcomm | We support Alt 2 (slightly preferred over Alt 3). We do not support Alt 4.  For Alt 2, in our paper we proposed (*option B in the figure*):   * 480 kHz (M=4, N=2): SSB slots (n) = {1, 2, 3, 4} + 6\*m, where m = 0, 1, …, 7 * 960 kHz (M=8, N=4): SSB slots (n) = {2, 3, 4, 5, 6, 7, 8, 9} + 12\*m, where m = 0, 1, …, 7   Chart  Description automatically generated |
| Intel | We support Proposal 1.2-2A with Alt-2.  Regarding particular values of n for SCS 480 kHz/960 kHz, our preference is 3 SSB slots followed by 1 gap slot (3 SSB slots + 1 gap slot) for SCS 480 kHz and (6 SSB slots + 2 gap slots) for 960 kHz.  Among the Alt 2 pattern, we didn’t think there was a huge difference for transmission of SSB. Therefore, everything else being equal we preferred a pattern that would align with RO transmission during the gap slots. This would allow more PRACH configuration to be vallid  In particular:   * Supported value of n for 480Hz SSB slot pattern:   + If 64 SSB candidate positions are supported, n = {0,1,2, 4,5,6, 8,9,10, 12,13,14, 16,17,18, 20,21,22, 24,25,26, 28,29,30, 32,33,34, 36,37,38, 40,41}   + If 128 SSB candidate position are supported, n = {0,1,2, 4,5,6, 8,9,10, 12,13,14, 16,17,18, 20,21,22, 24,25,26, 28,29,30, 32,33,34, 36,37,38, 40,41,42, 44,45,46, 48,49,50, 52,53,54, 56,57,58, 60,61,62, 64,65,66, 68,69,70, 72,73,74, 76,77,78, 80,81,82, 84} * Supported value of n for 960kHz SSB slot pattern:   + If 64 SSB candidate positions are supported, n = {0,1,2,3,4,5, 8,9,10,11,12,13, 16,17,18,19,20,21, 24,25,26,27,28,29, 32,33,34,35,36,37, 40,41}   + If 128 SSB candidate position are supported, n = {0,1,2,3,4,5, 8,9,10,11,12,13, 16,17,18,19,20,21, 24,25,26,27,28,29, 32,33,34,35,36,37, 40,41,42,43,44,45, 48,49,50,51,52,53, 56,57,58,59,60,61, 64,65,66,67,68,69, 72,73,74,75,76,77, 80,81,82,83}   However, we understand concerns from some companies wanted to have a faster SSB sweeping. To address them, we could propose a longer continuous transmissions of SSBs with a smaller total number of gap slots. Something like (4 SSB slots + 1 gap slot) for SCS 480 kHz and (8 SSB slots + 2 gap slots) for 960 kHz.  If we support SSB slots pattern such as (8 SSB slots + 2 gap slots), it is not clear if additional larger gap would be needed as suggested in Alt 3, as urgent data transmission can be support in this fashion. |
| Huawei, HiSilicon | We support ALT 4 in Proposal 1.2-2A. However, we don’t think that ALT4 in Proposal 1.2-2A is the same as the new Proposal 1.2-2D (we do not support Proposal 1.2-2D).  Please note that, ALT4 in Proposal 1.2-2A states that   * + ALT 4) slots that do not contain SSB correspond to the slots that do not contain SSB in 120 kHz Case D.     - Note: ALT 4 means that only slots 32-39 for 480 kHz SSB pattern are reserved for UL and 960 kHz SSB pattern is contiguous.   The correctness of the note is probably clearer from the following figure (more details in our t-doc R1-2108767). In the following Figure, the first line represents Case D for 120 kHz:    The mistake in translating ALT 4 in Proposal 1.2-2A to Proposal 1.2-2D probably stems from the fact that each n in Case D represents two consecutive slots (Case D: ) while in the agreement in RAN1 106-e regarding 480/960 kHz SSB pattern n represent only one slot (For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, X} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame.)  It is easy to see from Case D in 38.213 that slots {8-9, 18-19, 28-29, 38-39} in 120 kHz Case D are gap slots. These correspond to slots {32-39, 72-79, 112-119, 152-159} in 480 kHz and {64-79, 144-159, 224-239,304-319} in 960 kHz. Therefore, we think proposal 1.2-2D should be changed to the following Proposal 1.2-2D (alt 4) (modified)  * Supported value of n for 480Hz SSB slot pattern:   + If 64 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, *~~(gap)~~* 16, 17, 18, 19, 20,21,22,23, 24,25,26,27, 28,29,30,31~~, 32,33,34,35~~} (no gap slot)   + If 128 SSB candidate position are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, *~~(gap)~~* 16, 17, 18, 19, 20,21,22,23, 24,25,26,27, 28,29,30,31, ~~32,33,34,35,~~ *(gap)* 40,41,42,43, 44,45,46,47, 48,49,50,51, 52,53,54,55, 56, 57, 58, 59 *~~(gap here)~~* 60,61,62,63, 64,65,66,67, 68,69,70,71, 72,73,74,75} (a gap of size 8 slots starting from slot 32) * Supported value of n for 960kHzSSB slot pattern:   + If 64 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31} (no gap slot)   + If 128 SSB candidate position are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31, 32, 33, 34, 35, 36, 37, 38, 39 *~~(gap)~~* 40,41,42,43, 44,45,46,47, 48,49,50,51, 52,53,54,55, 56,57,58,59, 60,61,~~62,63, 64,65,66,67, 68,69,70,71~~} (no gap slot) |
| Moderator | Thanks for spotting my error. Revised Alt 4 (1.2-2D to 1.2-2E) with correct values of n.  Added other options based on comments received so far.  Also companies who prefer Alt 2 or 3, please provide inputs on whether which options you would be ok with.  Continue to provide comments. I will update the summary as companies provide more inputs. Summary below are tentative version. |
| Ericsson  (3rd round comments prior to noderator summary of 3rd round) | **We support LG's revision of Proposal 1.2-2D**, since the design principle is that gaps are not needed more often than every 1 ms (same principle from Rel-15). Furthermore, the SSB sweep time is minimized. Clearly, for 64 candidate positions, no gap is needed for either 480 or 960 kHz. We don't support 128 candidate positions; however, since that is being discussed separately, it's okay to leave it in this proposal as "if supported."  We could also support Alt-2 with M = 8, N = 2, i.e., M and N scaled by 2x compared to Case D pattern for 120 kHz. This would allow UL every 250 ms (still probably more often than needed), while keeping the SSB beam sweep still quite short (1.1875 ms).  We don't think further fine tuning of the gaps is needed since the beam sweep time is short to start with for 480/960 kHz. |
| Apple | **We support** Proposal 1.2-4 (N=2, M=8).  This pattern allows fast UL transmission e.g., at least HARQ-ACK over PUCCH to improve the URLLC latency by leveraging the short slot duration with new SCSs. |
| LG Electronics | **To Moderator,**  Alt 4 needs to be modified, as follows: Proposal 1.2-3 (alt 4 revised correction)  * Supported value of n for 480Hz SSB slot pattern:   + If 64 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, *~~(gap)~~* 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31~~, 32,33,34,35~~} (no gap slot)   + If 128 SSB candidate position are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, *~~(gap)~~* 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31, ~~32,33,34,35,~~ *(gap)* 40,41,42,43, 44,45,46,47, 48,49,50,51, 52,53,54,55, 56,57,58,59 *~~(gap here)~~* 60,61,62,63, 64,65,66,67, 68,69,70,71} (a gap of size 8 slots starting from slot 32) * Supported value of n for 960kHzSSB slot pattern:   + If 64 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31} (no gap slot)   + If 128 SSB candidate position are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31, 32,33,34,35, 36,37,38,39 *~~(gap)~~* 40,41,42,43, 44,45,46,47, 48,49,50,51, 52,53,54,55, 56,57,58,59, 60,61,62,63~~62,63, 64,65,66,67, 68,69,70,71~~} (no gap slot)   Regarding an argument point of latency requirement, which requirements are additionally needed compared to Rel-15 URLLC? Since Alt 4 provides the same level of gaps for UL with 120 kHz SCS in Rel-15, we cannot see any problem from latency requirement perspective. |
| Moderator | Fixed the error with Proposal 1.2-3 in 1.2-3A. |
| ZTE, Sanechips | As a proponent, we prefer Proposal 1.2-4 (alt 2 N=2, M=8) |
| vivo | Our first preference is Alt. 3 and can accept Alt. 2. Among the alternatives for Alt. 2, we support proposal 1.2-4B.  If looking at 120KHz SSB pattern, there are 4 or 8 symbol gap between consecutive SSBs, e.g. 4 symbol gap between SSB#1 and SSB#2, 8 symbol gap between SSB#3 and SSB#4. This allows short PUCCH transmission in the last symbol in each 120KHz slot by considering UL-DL/DL-UL switching time is 7us. In short, for any SSB slot for 120KHz (i.e. 0.125ms), a short PUCCH could be transmitted in the last symbol.  For Alt. 4, there are at most 4 symbol gap between consecutive SSBs, e.g. 4 symbol gap between SSB#1 and SSB#2. There is no enough time for DL-UL switching if we want to transmit short PUCCH in the last symbol of any SSB slot since 1 symbol length for 480K and 960KHz is much smaller than DL-UL switching time. This means short PUCCH can only be sent every 1ms, which has larger latency compared to 120KHz SSB resource pattern. So we don’t support Alt. 4. |
| Lenovo, Motorola Mobility | We support the updated version of Alt 4. |
| OPPO | We support Alt 2. For 480kHz SSB slot pattern, we think N=2, M=8 is reasonable. For 960kHz SSB pattern, our preference is to have aligned SSB slots, i.e., N=4, M=16.  Hence, we would like to have the following proposal: Proposal 1.2-4D (alt 2 N=2, M=8 for 480kHz, N=4, M=16 for 960kHz)  * Supported value of n for 480 kHz SSB slot pattern:   + If 64 SSB candidate positions are supported, n = 0,1,2,3,4,5,6,7, 10,11,12,13,14,15,16,17, 20,21,22,23,24,25,26,27, 30,31,32,33,34,35,36,37   + If 128 SSB candidate positions are supported, n = 0,1,2,3,4,5,6,7, 10,11,12,13,14,15,16,17, 20,21,22,23,24,25,26,27, 30,31,32,33,34,35,36,37, 40,41,42,43,44,45,46,47, 50,51,52,53,54,55,56,57, 60,61,62,63,64,65,66,67, 70,71,72,73,74,75,76,77 * Supported value of n for 960 kHz SSB slot pattern:   + If 64 SSB candidate positions are supported, n = 0,1,2,3,4,5,6,7,8,9, 10,11,12,13,14,15, 20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35   + If 128 SSB candidate positions are supported, n = 0,1,2,3,4,5,6,7,8,9, 10,11,12,13,14,15, 20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35, 40,41,42,43,44,45,46,47,48,49,50,51,52,53,54,55, 60,61,62,63,64,65,66,67,68,69,70,71,72,73,74,75 |
| Nokia (3rd round) | Just few notes from us, while the majority seems to be for Case D.  For Case D (@120kHz), we have two full slots (every 1ms) for UL data operation, in addition to two or four symbols every slot e.g. for UL control**.** For 480kHz and 960kHz, there are not enough symbols at end of SSB slots. Thus, by aligning with the Case D pattern the all UL control and data needs to follow the 1ms, which is a differentiation from Rel-15 assumption.  For the other patterns, in the case we have UL gaps in between the SSBs, if also in the UL more spatially selective reception is used, if might be good to enable transmission/reception from different spatial directions e.g. by having multiple slots in the gap. |
| CATT | We support proposal 1.2-4 (Alt 2 N=2, M=8) |

#### <Summary of 3rd Round of Discussions>

Objection to Proposal 1.2-2A (list of options)

* none so far

The following is views from companies.

Proposal 1.2-3 (Alt 4)

* Support: LGE, Interdigital, Samsung, Huawei/HiSilicon, Ericsson, Lenovo/Motorola Mobility
* No support: Docomo

Proposal 1.2-4 (Alt 2 N=2, M=8)

* Support: Panasonic, [Intel ?], Ericsson, Apple, ZTE/Sanechips, OPPO (for 480kHz), CATT

Proposal 1.2-4A (alt 2 N=4, M=8)

* Support: Nokia

Proposal 1.2-4B (alt 2 N=2, M=4 for 480kHz, N=4, M=8 for 960kHz)

* Support: Qualcomm, vivo

Proposal 1.2-4C (alt 2 N=1 M=3 for 480kHz, N=2, M=6 for 960kHz)

* Support: Intel

Alt 2 or Alt 3 if N=8

* Docomo

Given the temperature of the companies views, moderator suggest to simply down-select between Proposal 1.2-3 (Alt 4) or Proposal 1.2-4A (Alt 2 with N=2, M=8). While I understand, the two proposal are not most preferred, but moderator doesn’t think other options have any realistic chance for adoption.

Nokia provided comment that having slots without SSB every 1msec for 480/960kHz while allows UL data transmissions, do not account for ability to transmit short UL signals more frequently. This does seems to be something different compared to FR2-1 and supporting 1.2-4 does seem to be taking away something that was supported before. Based on this could companies compromise to Proposal 1.2-4A (Alt 2 with N=2, M=8)?

Check first on whether companies can live with Proposal 1.2-4A (Alt 2 with N=2, M=8) for sake of progress? If not check on Proposal 1.2-4.

If both proposals cannot be agreed, agree to Proposal 1.2-2A, or further down-selection of Proposal 1.2-2A.

#### 4th Round of Discussions

##### **Stable Issues**

Approve the following proposals over email. Please indicate if you have strong concerns on approving them over email.

###### Conclusion 1.2-3:

* No other values of n other than agreed previously is supported for 120kHz SCS, where parameter ‘n’ is the set of values to determine the first symbols of the candidate SSB blocks for 120kHz SCS in agreement from RAN1 #104-bis-e.

**Moderator Suggestion:**

* Conclude to following proposal
  + Conclusion 1.2-3

|  |  |
| --- | --- |
| Company | Comment (only if you have strong concerns) |
| Ericsson | Support Conclusion 1.2-3 |
| DOCOMO | Ok with Conclusion 1.2-3 if there’s a company arguing its necessity. |

##### **Open Issues**

Moderator has narrow down potential SSB slot patterns for further discussion.

###### Proposal 1.2-5

* Supported value of n for 480/960kHz SSB slot pattern:
  + ALT A) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB
    - same pattern will apply to 480kHz and 960kHz (i.e same N and M for 480 and 960 kHz)
    - N = 2, M = 8
    - FFS: starting position of n
  + ALT B) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB
    - scaled version pattern will apply between 480 and 960 kHz (i.e. N and M for 480kHz, 2N and 2M for 960 kHz)
    - N = 2, M = 8
    - FFS: starting position of n
  + ALT C) slots that do not contain SSB correspond to the slots that do not contain SSB in 120 kHz Case D.
    - Note: ALT 4 means that only slots 32-39 for 480 kHz SSB pattern are reserved for UL and 960 kHz SSB pattern is contiguous.

###### Proposal 1.2-4 (alt A with N=2, M=8)

* Supported value of n for 480/960 kHz SSB slot pattern:
  + If 64 SSB candidate positions are supported, n = {0,1,2,3,4,5,6,7, (gap) 10,11,12,13,14,15,16,17, (gap) 20,21,22,23,24,25,26,27, (gap) 30,31,32,33,34,35,36,37}
  + If 128 SSB candidate positions are supported, n = 0,1,2,3, 4,5,6,7, (gap) 10,11,12,13, 14,15,16,17, (gap) 20,21,22,23, 24,25,26,27, (gap) 30,31,32,33, 34,35,36,37, (gap) 40,41,42,43, 44,45,46,47, (gap) 50,51,52,53, 54,55,56,57, (gap) 60,61,62,63, 64,65,66,67, (gap) 70,71,72,73, 74,75,76,77}

###### Proposal 1.2-4D (alt B with N=2, M=8)

* Supported value of n for 480 kHz SSB slot pattern:
  + If 64 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, (gap) 10,11,12,13, 14,15,16,17, (gap) 20,21,22,23, 24,25,26,27, (gap) 30,31,32,33, 34,35,36,37
  + If 128 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, (gap) 10,11,12,13, 14,15,16,17, (gap) 20,21,22,23, 24,25,26,27, (gap) 30,31,32,33, 34,35,36,37, (gap) 40,41,42,43 ,44,45,46,47, 50,51,52,53, 54,55,56,57, (gap) 60,61,62,63, 64,65,66,67, (gap) 70,71,72,73, 74,75,76,77}
* Supported value of n for 960 kHz SSB slot pattern:
  + If 64 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, (gap) 20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35}
  + If 128 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, (gap) 20,21,22,23, 24,25,26,27, 28,29,30,31, 32,33,34,35, (gap) 40,41,42,43, 44,45,46,47, 48,49,50,51, 52,53,54,55, (gap) 60,61,62,63, 64,65,66,67, 68,69,70,71, 72,73,74,75}

###### Proposal 1.2-3A (Alt C)

* Supported value of n for 480Hz SSB slot pattern:
  + If 64 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31} (no gap slot)
  + If 128 SSB candidate position are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31, (gap) 40,41,42,43, 44,45,46,47, 48,49,50,51, 52,53,54,55, 56,57,58,59 60,61,62,63, 64,65,66,67, 68,69,70,71}
* Supported value of n for 960kHzSSB slot pattern:
  + If 64 SSB candidate positions are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31} (no gap slot)
  + If 128 SSB candidate position are supported, n = {0,1,2,3, 4,5,6,7, 8,9,10,11, 12,13,14,15, 16,17,18,19, 20,21,22,23, 24,25,26,27, 28,29,30,31, 32,33,34,35, 36,37,38,39, 40,41,42,43, 44,45,46,47, 48,49,50,51, 52,53,54,55, 56,57,58,59, 60,61,62,63} (no gap slot)

Proposal 1.2-4D scaling N and M for 960kHz, might give something between Proposal 1.2-4 and Proposal 1.2-3A.

First of all, can companies live with Proposal 1.2-4D? I have a feeling we are not going to able to agree to either Proposal 1.2-3A nor Proposal 1.2-4. Moderator thinks its time for companies to put on their compromise hats and try to conclude. Not sure if pushing this to next meeting is going to bring more fruitful discussion.

If Proposal 1.2-4D is not acceptable, moderator suggests trying to agree to Proposal 1.2-5 which simply list the three options. If companies to down-select even further between Alt A, B that would be great as well. Companies that prefer A, please indicate if you are ok to live with either Proposal B or C. If ok, moderator will remove ALT A from the list, so that we can down-select between B and C in the next meeting.

##### **Company comments**

|  |  |
| --- | --- |
| Company | Comments |
| Qualcomm | We are fine with FL suggestion to agree to Proposal 1.2-4D. If not agreed, we are also ok with Proposal 1.2-5 (we are also ok dropping ALT A). |
| LG Electronics | We do not support Proposal 1.2-4D, but we are fine with Proposal 1.2-5 (also fine with Alt A removed). |
| Huawei, HiSilicon | We are not ready to accept with Proposal 1.2-4D. We think that agreeing on Proposal 1.2-5 might be the best we could do at this time. We are OK to remove ALT A of this proposal and narrow down between ALT B and ALT C. |
| OPPO | We support Proposal 1.2-4D and can accept Proposal 1.2-5. |
| Ericsson | Our first preference is Alt-C of Proposal 1.2-5, but we can live with Alt-B.  Summary:  Support 1.2-5 with Alt-A removed  We can live with Proposal 1.2-4D. |
| Sharp | Our first preference is Alt C and second preference is Alt B. If consensus cannot be achieved, we are fine with Proposal 1.2-5 to make some progress. |
| DOCOMO | Fine with Proposal 1.2-4D, and also ok with Proposal 1.2-5 (prefer to remove Alt-A). |
| Panasonic | We are fine with 1.2-4D. If not agreed, we are also OK with Proposal 1.2-5 (also fine with removing ALT A). |
| vivo | We support Proposal 1.2-4D. If not agreed, we are also ok with proposal 1.2-5 (fine with dropping Alt. A) |
| Nokia (4th round) | Like noted, Alt-A seems more or less equal to Alt-C for 960kHz (i.e. UL is in practice after the SSB burst). Downside of both Alt B and C is that the slot index pattern for different numerologies is different (hence the reason why we proposed N=4, M=8 for both in our paper).  That being said, among the options listed, we would have slight preference for Alt B (or 1.2-4D), but can also accept Alt C (or 1.2-3A). Also fine taking 1.2-5 without Alt-A to conclude in next meeting. |
| ZTE, Sanechips | We support Alt-B of Proposal 1.2-5, and support the pattern in Proposal 1.2-4D. |
| Lenovo, Motorola Mobility | We support Proposal 1.2-5 and are also fine to remove Alt A. |
| Interdigital | Our preference is Proposal 1.2-3A (Alt. C).  We are ok with Proposal 1.2-5 with Alt. A removed. |
| Futurewei | We are OK with the Proposal 1.2-4D and OK with the Proposal 1.2-5 |

#### <Summary of 4th Round of Discussions>

*<Moderator to prepare summary>*

### 2.1.3 CORESET#0 Configuration

* From [1] Huawei/HiSilicon:
  + For CORESET for Type0-PDCCH in 52.6GHz to 71GHz spectrum, support the following:
    - For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {120, 120} kHz, support multiplexing pattern 1 and multiplexing pattern 3 as per Agreement in RAN1 104-e.
    - For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {480, 480} kHz, support multiplexing pattern 1 only.
    - For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {960, 960} kHz, support multiplexing pattern 1 only.
  + For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {120, 120} kHz, in addition to the supported values of (, ) from Rel-15, support = 96 with ={1,2} for multiplexing pattern 1.
  + Support the following CORESET#0 RB offsets values for {SSB, CORESET#0} SCS={120, 120} kHz:
    - For CORESET#0 with 24 RBs and 48 RBs: the same as supported values in Table 13-8 of 38.213.
    - For CORESET#0 with 48 RBs: additional RB offsets values of 0 and 28 RBs can be considered for multiplexing pattern 1.
    - For CORESET#0 with 96 RBs: RB offsets values of 0 and 76 RBs can be considered for multiplexing pattern 1.
    - Note: All above RB offsets are nominal and may need to be modified after finalizing synch raster and channel raster design in FR2-2.
  + Support the following CORESET#0 RB offsets values for {SSB, CORESET#0} SCS={480, 480} kHz and {960, 960} kHz:
    - For CORESET#0 with 24 RBs: the same as supported values in Table 13-8 of 38.213.
    - For CORESET#0 with 48 RBs: In addition to the offset of 14 RBs already supported in Rel-16, additional values of 0 and28 RBs can be considered for multiplexing pattern 1.
  + The parameters for PDCCH monitoring occasions for Type0-PDCCH CSS set - SS/PBCH block and CORESET multiplexing pattern 1 listed in Table [1]-4 and Table [1]-5 should be supported. For 480kHz and 960 kHz SCS, the scaling factor X in Table 5 is when DBTW is OFF and when DBTW is ON.
    - Note: DBTW OFF is indicated in MIB using a value of

Table 4 Parameters for PDCCH monitoring occasions for Type0-PDCCH CSS set - SS/PBCH block and CORESET multiplexing pattern 1 and FR2-2 when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Index |  | Number of search space sets per slot |  | **First symbol index** |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 5 | 1 | 1 | 0 |
| 2 | 0 | 2 | 1/2 | {0, if is even}, {7, if is odd} |
| 3 | 5 | 2 | 1/2 | {0, if is even}, {7, if is odd} |
| 4 | 0 | 2 | 1/2 | {0, if is even}, {, if is odd} |
| 5 | 5 | 2 | 1/2 | {0, if is even}, {, if is odd} |
| 6 | 0 | 1 | 2 | 0 |
| 7 | 5 | 1 | 2 | 0 |

Table 5 Parameters for PDCCH monitoring occasions for Type0-PDCCH CSS set - SS/PBCH block and CORESET multiplexing pattern 1 and FR2-2 when {SS/PBCH block, PDCCH} SCS is {480, 480} kHz or {960, 960} kHz

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Index |  | Number of search space sets per slot |  | **First symbol index** |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 2 | 1/2 | {0, if is even}, {7, if is odd} |
| 2 | 5X | 1 | 1 | 0 |
| 3 | 5X | 2 | 1/2 | {0, if is even}, {7, if is odd} |
| 4 | 5 | 1 | 1 | 0 |
| 5 | 5 | 2 | 1/2 | {0, if is even}, {7, if is odd} |
| 6 | 5+5X | 1 | 1 | 0 |
| 7 | 5+5X | 2 | 1/2 | {0, if is even}, {7, if is odd} |
| 8 | 0 | 1 | 2 | 0 |
| 9 | 5 | 1 | 2 | 0 |
| 10-15 | Reserved | | | |

* + To find the offset between an off-synch raster SSB and the corresponding CORESET#0 in 60GHz unlicensed spectrum, RAN1 should uniquely determine the hypothetical on-synch raster SSB that serves as the reference for the offset to the off-synch raster SSB in case more than one synch rasters are included in a channel bandwidth.
* From [2] Futurewei:
  + Rel 17 FR2-2 the SS/PBCH and CORESET#0 for Type0-PDCCH should have only the same SCS.
  + Use O from the set {0, 5, 2.5, 5+2.5} for 120 kHz, {0, 5, 2.5/X, 5+2.5/X} for 480 kHz, and {0, 5, 2.5/(2\*X), 5 + 2.5/(2\*X)} for 960 kHz, with X values TBD.
* From [4] ZTE, Sanechips:
  + In addition to multiplexing pattern 1, multiplexing pattern 3 for three approved SCS combinations of SSB and Type0-PDCCH can also be considered in FR2-2.
    - (SSB, Type0-PDCCH): SCS (120 kHz, 120 kHz)
    - (SSB, Type0-PDCCH): SCS (480 kHz, 480 kHz)
    - (SSB, Type0-PDCCH): SCS (960 kHz, 960 kHz)
  + For {SSB, CORESET# for Type0-PDCCH} SCS = {120, 120} kHz, even though RAN4 has agreed the minimum CBW is increased to 100 MHz, at least SSB and CORESET#0 multiplexing patterns, number of RBs for CORESET#0, number of symbols (duration of CORESET#0) that are supported in Rel-15/16 should still be supported.
* From [5] vivo:
  + Support Multiplexing pattern 1 and 3 for SCS 120 kHz, and support Multiplexing pattern 3 for SCS 480 kHz and 960 kHz when operation in FR2-2.
  + Support 96 RB for SCS 120kHz and 480 kHz. Do not support 96 RB for SCS 960kHz.
  + If the sync raster/ channel raster is designed with FR 2-1, the existing RB offset design can be reused for SCS 480 kHz and 960 kHz. Otherwise, the RB offset should be re-designed.
  + For {SSB, PDCCH} SCS {120, 120} kHz, {480, 480} kHz and {960, 960} kHz, the tables for PDCCH monitoring occasions for type0-PDCCH CSS set configuration defined for FR2-1 in Rel-15 can be reused with little adjustment.
* From [9] CATT:
  + The subCarrierSpacingCommon field in MIB can be saved and repurposed.
  + Multiplexing pattern 2 or 3 can be used for further multiplexing SSB/CORSET#0 with periodic CSI-RS/paging PDCCH&PDSCH in frequency.
  + For SSB and CORESET#0/Type0-PDCCH with 120 KHz SCS, support the following combinations of SSB/CORESET multiplexing pattern, number of RB and symbols for CORESET.
    - {mux pattern 1, 48 PRB CORESET, 1 symbol CORESET}
    - {mux pattern 1, 48 PRB CORESET, 2 symbol CORESET}
    - {mux pattern 3, 48 PRB CORESET, 2 symbol CORESET}
  + The configuration of {0, if *i* is even}, {, if *i* is odd} can be supported, considering for SCS=120 KHz use case, the gNB could use implementation to avoid beam switching gap issue if it choose to.
  + The default TDRA table for pattern 1 in TS 38.214 can be enhanced, e,g at least {S=6 ,L=7}, {S=2，L=11} is supported.
* From [10] Xiaomi:
  + Detail parameters modification for controlResourceSetZero configuration should be based on channel and sync raster design in RAN4.
* From [11] Ericsson:
  + RAN1 should strive to design a common CORESET0 configuration table for use for all 3 supported SCS combinations (120,120), (480,480), and (960, 960).
  + If RAN4 defines a floating channelization with a sync raster granularity in line with the design, add offset values 2 and 26 for the option of 48 RB CORESET0 and make Table 13-8 in 38.213 applicable also for operation with 480 and 960 kHz SCS.
  + Reuse existing Table 13-12 in 38.213 for operation with 480 and 960 kHz SCS. For subcarrier spacings 480 and 960 kHz, select Alternative 1 to define offset values.
* From [12] Nokia, NSB:
  + For CORESET#0 with 120kHz sub-carrier spacing, consider supporting also ={96} for multiplexing pattern 1.
  + For SSB and CORESET#0 with 480kHz sub-carrier spacing with SSB and CORESET#0 multiplexing pattern 3, following configuration options could be considered:
    - ={2}
    - ={24, 48}.
  + Support the following ’O’ values for both 480 and 960 kHz sub-carrier options: {0, 1.5, 5, 6.5} ms.
  + Support values {1,2} for the number of search space sets per slot, and values {1, 1/2} for the shift M. Additionally, given room in table also M={2} could be supported.
  + Support first symbol index configuration options 0 and {0, if  is even}, {7, if  is odd}
  + Support Type0-PDCCH CSS configuration presented in Table [12]-7 for multiplexing pattern 1.

|  |  |  |  |
| --- | --- | --- | --- |
| **O** | **Number of search space sets per slot** |  | **First symbol index** |
| 0 | 1 | 1 | 0 |
| 0 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 1.5 | 1 | 1 | 0 |
| 1.5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 5 | 1 | 1 | 0 |
| 5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 6.5 | 1 | 1 | 0 |
| 6.5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 0 | 1 | 2 | 0 |
| 5 | 1 | 2 | 0 |

* + Consider also SSB and CORESET#0 multiplexing pattern 3 for 120kHz SSB.
  + Pending on the UE minimum BW capability, consider also SSB and CORESET#0 multiplexing pattern 3 for 480kHz SSB.
* From [13] Samsung:
  + For CORESET#0 configuration with 120 kHz SCS,
    - additional CORESET#0 RB offsets are needed;
    - support 96 RB as the number of RBs for CORESET#0.
  + For CORESET#0 configuration with 480 kHz and 960 kHz SCS,
    - support multiplexing pattern 3;
    - support 96 RB as the number of RBs for CORESET#0;
    - further study the RB offset based on RAN4 design of channel and synchronization rasters.
  + Type0-PDCCH configuration, support all configurations from Rel-15 table except for the changes to O values:
    - For 120 kHz, ;
    - For 480 kHz, ;
    - For 960 kHz, .
  + For 480 kHz and 960 kHz SCS, a UE only monitors one slot for Type0-PDCCH:
    - Alt 1: the one slot is slot for all cases;
    - Alt 2: the one slot is slot for and , and configured from slot and for
* From [14] Mediatek:
  + Support adjusting the time-domain offset between SSB and CORESET #0 for 480/960 kHZ SCS.
* From [15] Intel:
  + Support 96 PRB CORESET for {SS/PBCH, PDCCH} equal to {120,120}, {480,480} and {960,960} kHz with = {1, 2}.
  + Support the following CORESET#0 RB offset values for {120, 120} kHz, {480, 480}, {960, 960} kHz for multiplexing patterns 1 and 3:
    - For CORESET#0 with 24 RBs: [0] for multiplexing pattern 1 and –20 if kssb =0 (-21 if kssb > 0) for multiplexing pattern 3.
    - For CORESET#0 with 48 RBs: [0], for multiplexing pattern 1 and –20 if kssb =0 (-21 if kssb > 0) for multiplexing pattern 3.
      * FFS: inclusion of RB offset of [1]
    - For CORESET#0 with 96 RBs: [0] for multiplexing pattern 1 and –20 if kssb =0 (-21 if kssb > 0) for multiplexing pattern 3.
    - Modify Table 13.8 in TS 38.213 to support the proposed RB offset when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz
    - Support addition of a new table in 38.213 for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {480, 480} kHz or {960, 960} kHz.
  + For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
    - Support O = {0, 2.75, 5, 7.75} for 480kHz (in case Lmax = 128)
    - Support O = {0, 1.5, 5, 6.5} for 960kHz {in case Lmax = 128)
  + The equation for determining the slot number for PDCCH monitoring is modified to account for the non-contiguous numbering of the SSB slot pattern for {SSB, Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz.
    - Support the following modified equation:
    - For 480 kHz: where and
    - For 960 kHz: where and
* From [16] NTT Docomo:
  + If time allows, support the following for 480/960 kHz SCS, considering the support of two sets of SSB-CORESET#0 multiplexing within a slot:
    - More number of RBs for CORESET#0 PDCCH
    - Enhance Default PDSCH TDRA Table A
  + If time allows, support smaller ‘O’ value especially for 960 kHz SCS
* From [17] Pansonic:
  + 96 PRB CORESET for 120 kHz SCS is supported.
* From [21] Interdigital:
  + Introduce the enhancements on SS/PBCH block transmission patterns to deliberately include the CORESET#0 and SIB1 in fixed time locations along with the corresponding SS/PBCH block to ensure the channel occupancy as much as possible, in the initial access operations with 120kHz SCS for unlicensed spectrum in beyond 52.6GHz.
* From [22] LG Electronics:
  + Reuse Table 13-12 in TS 38.213 specification for type0-PDCCH CSS set configuration with 120/480/960 kHz, except for O values for 480/960 kHz.
* From [23] Sharp:
  + For Type0-PDCCH CSS set configuration rows where the first symbol index is given by {0, if i is even}, {, if i is odd}, the configuration rows should be modified such that gap symbols between different beams can be supported.
  + ‘O’ is from the set {0, 5, X5, 5+ X5} for 480 kHz, and {0, 5, X6, 5 + X6} for 960 kHz, where X5 and X6 stand for durations that count for consecutive transmission of SSB burst of 480kHz SCS and 960kHz SCS, respectively.
* From [24] Apple:
  + In addition to 24 and 48 PRBs, 96 PRBs can be considered for CORESET#0 BW with 120kHz SCS.
  + For Type0-PDCCH Mos determination, the offset values are defined as for 480kHz and 960kHz SCS respectively, where .
* From [26] Qualcomm:
  + for FR2-2, CORESET0 SCS = SSB SCS for all SCSs
  + consider minimizing the overhead of beam switching gaps by supporting multiplexing pattern 3
  + for ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, the following set of parameters are supported for SS/PBCH block and CORESET multiplexing pattern 1:

|  |  |  |
| --- | --- | --- |
| Number of search space sets per slot | M | First symbol index |
| 1 | 1 | 0 |
| 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | 1/2 | {0, if  is even}, {+ 1, if  is odd} |
| 1 | 2 | 0 |

* + - Note: the number of entries corresponding the same {number of SS per slot, M, first symbol index} tuple (listed above) will depend on supported ‘O’ for each tuple
    - For 960 kHz, re-interpret the offsets of O = {0, 2.5, 5, 7.5} from Table 13-12 as O = {0, 1.25, 5, 6.25}

#### Summary of Discussions

In RAN1 #104e and #105e the following agreement was made.

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Agreement:**  For CORESET#0 and Type0-PDCCH search space configured in MIB:   * Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {120, 120} kHz   + Support at least SSB and CORESET#0 multiplexing patterns, number of RBs for CORESET#0, number of symbols (duration of CORESET#0) that are supported in Rel-15/16 for {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS = {120, 120} kHz.     - FFS: Supporting additional values   + FFS: Supported values for SSB to CORESET#0 offset RBs * If 480kHz SSB SCS that configures CORESET#0 and Type0-PDCCH CSS in MIB is agreed to be supported,   + Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {480, 480} kHz * If 960 kHz SSB SCS that configures CORESET#0 and Type0-PDCCH CSS in MIB is agreed to be supported,   + Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {960, 960} kHz * If 240 kHz SSB SCS is agreed to be supported,   + Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {240, 120} kHz * FFS: any other combinations between one of SSB SCS (120, 240, 480, 960) and one of CORESET#0 SCS (120, 480, 960)   + FFS: initial timing resolution based on low SCS (120 kHz) and its impact on the performance of higher SCS (480/960 kHz)   **Agreement:**  For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,   * Support the following set of parameters.  |  |  |  | | --- | --- | --- | | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | | 1 | 24 | 2 | | 1 | 48 | 1 | | 1 | 48 | 2 |  * + Note: the number of entries corresponding the same {mux pattern, number of RB, number of symbol} tuple (listed above) will depend on required RB offsets that needs to be supported based on channel and sync raster design. * FFS: addition other set of parameters |

The following are a summary of company views on CORESET#0 configuration aspects.

* For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz
  + controlResourceSetZero
    - Addition of 96 PRB CORESET#0 with {1,2} symbols
      * Support: Huawei/HiSilicon, vivo, Nokia/NSB, Samsung, Intel, Panasonic, Apple
      * Do not support: LGE
    - Addition of mux pattern 3
      * Support: Huawei/HiSilicon (according to RAN1#104-e agreement), ZTE/Sanechips, vivo, [CATT], Nokia/NSB, Intel, LGE
      * Do not support:
    - RB offset values for Mux 1
      * 24 RB
        + 0, 4 : Huawei/HiSilicon
        + 0: Intel
      * 48 RB
        + 0, 28: Huawei/HiSilicon
        + 2, 14, 26: Ericsson
        + 0, 1: Intel
      * 96 RB
        + 0, 76: Huawei/HiSilicon
        + 0: Intel
  + searchSpaceZero
    - Use Table 13-12 (originally intended for {120,120} kHz)
      * Samsung, Intel, LGE
    - Use Table 13-12 (originally intended for {120,120} kHz) except O values (2.5 and 7.5)
      * Huawei/HiSilicon
* For {SSB, CORESET#0/Type0-PDCCH} = {480, 480} and {960, 960} kHz
  + controlResourceSetZero
    - Addition of 96 PRB CORESET#0
      * Support: vivo (for 480kHz), Intel
      * Do not support: vivo (for 960kHz), LGE
    - Addition of mux pattern 3
      * Support: ZTE/Sanechips, [CATT], Nokia/NSB (for 480kHz), Samsung, Intel, Qualcomm, LGE
      * Do not support: Huawei/HiSilicon
    - RB offset values for Mux 1
      * 24 RB
        + 0, 4 : Huawei/HiSilicon, Ericsson (for 960kHz)
        + 0: Intel
      * 48 RB
        + 0, 14, 28: Huawei/HiSilicon
        + 2, 14, 26: Ericsson
        + 0: Intel
      * 96 RB
        + 0: Intel
    - RB offset values for Mux 3
      * -20/-21 depend on k\_ssb
      * N, where N is number of RBs for CORESET
  + searchSpaceZero
    - Use Table 13-12 (originally intended for {120,120} kHz) except O values
      * Nokia/NSB, Intel, LGE
    - Based on Table 13-12 (originally intended for {120,120} kHz) except O values and remove the rows with First symbol index {N\_symb^CORESET, if i is odd}
      * Huawei/HiSilicon
    - O values
      * {0, 5/X, 5, 5 + 5/X} with X = 2^(µ-3) for DBTW OFF, X = 2^(µ-4) for DBTW ON
        + Huawei/HiSilicon
      * {0, 5, 2.5/X, 5+2.5/X} for 480 kHz and {0, 5, 2.5/(2X), 5+2.5/(2X)} for 960 kHz
        + Futurewei
      * {0, 1.5, 5, 6.5}
        + Nokia/NSB
      * {0, 1.25, 5, 6.25} for 480 kHz and {0, 0.625, 5, 5.625} for 960 kHz
        + Samsung, Apple
      * {0, 2.75, 5, 7.75} for 480 kHz and {0, 1.5, 6, 6.5 } for 960 kHz
        + Intel
      * {0, 5, X, 5 +X} for 480kHz and {0, 5, Y, 5+Y} for 960kHz, X and Y are slot duration number that correspond to SSB burst
        + Sharp
      * {0, 2.5, 5, 7.5} for 480 kHz and {0, 1.25, 5, 6.25} for 960 kHz
        + Qualcomm
* Other proposals
  + Common CORESET and SS table for all SCS
    - Ericsson
  + For 480 kHz and 960 kHz, whether to monitor Type0-PDCCH in n0 only or in {n0, n0+1}
    - Samsung
  + Update PDCCH monitoring equation to account to non-contiguous numbering of SSB slots pattern for 480/960kHz
    - Intel
  + Enhancement of default PDSCH TDRA Table A
    - NTT Docomo, CATT

#### <Moderator’s Suggestion for Discussions>

Discussion and decisions are needed for the following issues:

* For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz
  + Whether or not to include 96 PRB CORESET
    - 9 company support, no objections so far
  + Whether or not to support mux pattern 3 – RAN1 seemed to have agreed to this in RAN1 #104-e
  + searchspaceZero - Use Table 13-12 as is or with modifications (e.g. O values, removal of entries, etc)
  + RB offset values for 24, 48, [96] PRB CORESET: FFS
* For {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and = {960, 960} kHz
  + Whether or not to include 96 PRB CORESET
  + Whether or not to support mux pattern 3
    - 7 companies support, 2 companies do not support
  + searchspaceZero - Use Table 13-12 with modification of O values
    - whether or not to use different O value depending on whether DBTW is ON/OFF
    - {0, 5, X, 5 +X} for 480kHz and {0, 5, Y, 5+Y} for 960kHz, values of X and Y FFS
  + RB offset values for 24, 48, [96] PRB CORESET: FFS
* Other proposals that require discussions
  + Common CORESET and SS table for all SCS
  + For 480 kHz and 960 kHz, whether to monitor Type0-PDCCH in n0 only or in {n0, n0+1}
  + Update PDCCH monitoring equation to account to non-contiguous numbering of SSB slots pattern for 480/960kHz
  + Enhancement of default PDSCH TDRA Table A
    - Discuss in Section 2.1.5

Moderator would like to encourage companies to initiate some discussion on RB offset values for CORESET. RAN1 has 1 more meeting left (in November) before completion of release 17 for RAN1. RAN4 does not have a meeting until November, and if RAN4 does not complete the raster design by November, then RAN1 may not be able complete the specification. Therefore, moderator suggests companies to investigate into RB offset values needed based on currently available raster proposals in RAN4. RAN1 can potentially make tentative proposals for few potential raster scenarios (being considered in RAN4). This way RAN1 at least has some idea on how many entries will be used for CORESET#0 and is able to pick out a final set as soon as RAN4 concludes on the raster design.

**Issue #1)**

**Proposal 1.3-1**

* For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz, support multiplexing pattern 1 with 96 PRB CORESET#0, and {1, 2} symbol durations

**Issue #2)**

##### Proposal 1.3-2

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz,
  + use Table 13-12 in TS38.213 for multiplexing pattern 1,
  + use Table 13-15 in TS38.213 for multiplexing pattern 3.

Moderator note: As pointed out by few companies, RAN1 agreement from #104 implies multiplexing pattern 3 is agreed to be supported.

**Issue #3)**

##### Proposal 1.3-3

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 1:
  + FFS: The value of X (≥ 0)
  + FFS: whether or not to use different X value depending on whether DBTW is ON/OFF
  + FFS: whether or not to use same or different X value for 480 and 960 kHz

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Index |  | Number of search space sets per slot |  | **First symbol index** |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | ~~2.5~~ X | 1 | 1 | 0 |
| 3 | ~~2.5~~ X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 4 | 5 | 1 | 1 | 0 |
| 5 | 5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 6 | 0 | 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 7 | ~~2.5~~ X | 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 8 | 5 | 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 9 | ~~7.5~~ 5 + X | 1 | 1 | 0 |
| 10 | ~~7.5~~ 5 + X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 11 | ~~7.5~~ 5 + X | 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 12 | 0 | 1 | 2 | 0 |
| 13 | 5 | 1 | 2 | 0 |
| 14 | Reserved | | | |
| 15 | Reserved | | | |

**Proposal 1.3-4**

* If supported, for ‘searchSpaceZero’ configuration for {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 3:

|  |  |  |
| --- | --- | --- |
| Index | PDCCH monitoring occasions (SFN and slot number) | **First symbol index**  **(*k* = 0, 1, … 31)** |
| 0 |  | 2, 9 in |
| 1 ~ 15 | Reserved | |

**Issue #4)**

Discuss further on the following issue:

* For 480 kHz and 960 kHz, whether to monitor Type0-PDCCH in n0 only or in {n0, n0+1}

**Issue #5)**

Discuss further on the following issue:

* Update PDCCH monitoring equation to account to non-contiguous numbering of SSB slots pattern for 480/960kHz

**Issue #6) RB offset values**

Moderator would like to encourage companies provide companies views on the required RB offsets, even if they are speculative (based on specific assumptions in raster design in RAN4). If possible, please share details of how required RB offset were computed (similar to how [11] from Ericsson provided information on the assumptions).

#### 1st Round of Discussions

Please provide further comments on the above issues #1 ~ #6. Also, if there are any other issues that require discussion, please comment them here.

|  |  |
| --- | --- |
| Company | Comments |
| NTT DOCOMO | For issue #1, we support the proposal 1.3-1, while we can also live with deferring this decision.  For issue #2, we support the proposal 1.3-2.  For issue #3, we support the proposal 1.3-3 and 1.3-4.  For issue #4, it depends on the design of multi-slot PDCCH monitoring capability.  For issue #5, we do not understand the motivation of such updates. Could someone clarify? |
| OPPO | Proposal 1.3-1: support  Proposal 1.3-2: support  Proposal 1.3-3: not support. We prefer to change O from {0, 2.5, 5, 7.5} to {0, X, Y, Z} and FFS the values of X, Y, Z at current stage.  Proposal 1.3-4: support  Regarding issue #4, two PDCCH monitoring occasions as legacy should be supported. For the monitoring span, UE capability (e.g., slot-group based) could be considered. |
| Qualcomm | Issue #1 (Proposal 1.3-1): no strong view  Issue #2 (Proposal 1.3-2): we are fine with this proposal  Issue #3   * Proposal 1.3-3:   + We are fine with the ‘O’ portion of the proposal   + For the “First symbol index” we think that back-to-back SS0 is not possible if beam switching gaps are needed. Hence, we prefer {0, if  is even}, {+ 1, if  is odd} * Proposal 1.3-4: we are fine with this proposal   Issue #4: This can be discussed in agenda 8.2.2 |
| Lenovo, Motorola Mobility | Issue #1 (Proposal 1.3-1): support  Issue #2 (Proposal 1.3-2): support  Issue #3 (Proposal 1.3-3 and Proposal 1.3-4): We are fine with both proposals  Issue #4 we agree with Qualcomm that it can be discussed in 8.2.2. |
| Samsung | Proposal 1.3-1: We support the proposal.  Proposal 1.3-2: We support the proposal. Just one typo in the main bullet, and one clarification on moderator’s note.   * For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} SCS = {120, 120} kHz,   + use Table 13-12 in TS38.213 for multiplexing pattern 1,   + use Table 13-15 in TS38.213 for multiplexing pattern 3.   Moderator note: As pointed out by few companies, RAN1 agreement from #104 implies multiplexing pattern 3 is agreed to be supported for {SSB, CORESET#0/Type0-PDCCH} SCS = {120, 120} kHz.  Proposal 1.3-3: We support the proposal. There is a bracket on X>=0 - although we believe X cannot be 0, but it’s ok to leave it there.  Proposal 1.3-4: We support the proposal. Maybe the following rewording is more clear.   * If multiplexing pattern 3 is supported for {SSB, CORESET#0/Type0-PDCCH} SCS = {480, 480} kHz and {960, 960} kHz, ‘searchSpaceZero’ configuration uses the following table:   Issue 4: We support only monitoring one slot for Type0-PDCCH for 480 kHz and 960 kHz, to avoid back-to-back slot monitoring for such higher SCSs. The slot can be fixed as n0 or configurable between n0 and n1 (using reserved rows in searchSpaceZero)  Issue 5: It’s not preferable to have non-contiguous burst of RMSI, which cases many LBT operation for unlicensed band. |
| Interdigital | **Proposal 1.3-1**: Do not support 96 RBs as it is not necessary.  **Proposal 1.3-2**: Support the proposal.  **Proposal 1.3-3**: Support the proposal.  **Proposal 1.3-4**: Support the proposal. |
| LG Electronics | Proposal 1.3-1: We do not support introducing 96 PRBs since it is not essential.  Proposal 1.3-2: OK also with Samsung’s modifications.  Proposal 1.3-3: Support  Proposal 1.3-4: Support  Issue #4: We agree with Qualcomm that it can be discussed in 8.2.2.  Issue #5: This is tightly related with Proposal 1.2-2. If alt 1 (contiguous slot pattern) is adopted, we don’t need discuss any more on this proposal.  Issue #6: One way could be to keep the same RB offset values as in Rel-15 and inform it RAN4 to check whether it would be problematic or not when sync/channel rasters are designed. |
| Ericsson | Issue #1  **We do not support Proposal 1.3-1 (yet)**. As we stated before, we think this is a not essential optimization. However, we can be open to discuss this later after it is known how many entries of the CORESET0 configuration table are available, e.g., after RAN4 completes its channelization design and the RB offsets are known at least =for 48 and 24 RB CORESET0. Hence, for now this should be deferred.  Issue #2  We support Proposal 1.3-2 with the typo correction from Samsung.  Issue #3  **We support Proposal 1.3-3**. Agree with Samsung that the (≥0) can be removed from the first FFS. My mistake in the comments I made previously – it should have been X > 0.  **We do not support Proposal 1.3-4 (yet)**. This should be deferred, and if there is time left at the end of the WI to have a full design for multiplexing pattern 3 (including CORESET0 configuration and offsets), we can treat it then. We note the following from the WID:   * + - Prioritize support SSB-CORESET#0 multiplexing pattern 1. Other patterns discussed on a best effort basis.   Issue #4  We prefer a common design for all 3 SCSs.  We don't agree that this is an issue to be discussed.  Issue #5  We don't understand the rationale behind this proposal. What does "non-contignous number of SSB slots pattern" mean? This seems like a deviation from Rel-15 design, and we don’t see the point. Moreover, we prefer a common design for all 3 SCSs.  Issue #6  In our contribution on channelization design (R1-2109441), we investigate the needed SSB-CORESET0 offsets and find that they depend on (1) the sync raster granularity, and (2) the spectral utilization, i.e., # of RBs in a given nominal channel bandwidth (e.g., 66 RBs in 100 MHz BW in Rel-15). We found that if RAN4 follows the design paradigm from Rel-15 to have a regularly spaced channel and sync raster for the 57–71 GHz band, where the latter is more coarse than the former (Option 1-C being discussed in RAN4), the the following offsets are needed:   * 48 RB CORESET0: {2 14 26} RBs (assuming 86.4% spectral utilization) or {0 14 28} RBs (assuming > 90% spectral utilization) * 24 RB CORESET0: {0 4} RBs   Of course the final values will depend on what RAN4 decides, our view is that for multiplexing pattern 1 with both 1 and 2 symbol CORESET0, RAN1 should keep a placeholder for up to 3 offsets for 48 RB CORESET0 and up to 2 offsets for 24 RB CORESET0. |
| ETRI | For Issue #1, we support Proposal 1.3-1.  For Issue #2, we support Proposal 1.3-2.  For Issue #3, we support Proposal 1.3-3 and Proposal 1.3-4  For Issue #4, we agree with Qualcomm |
| Sharp | Issue #1: we are fine with Proposal 1.3-1.  Issue #2: we are fine with Proposal 1.3-2.  Issue #3: we generally support Proposal 1.3-3 and share the same view from Qualcomm on “first symbol index”. In addition, we think that the back-to-back Type0-PDCCH problem could be solved by shifting the first symbol index for the O > 0 cases. While for O = 0, {0, if  is even}, {, if  is odd} should be reused.  We are fine with Proposal 1.3-4.  Issue #4: Agree this issue should be handled in AI8.2.2. |
| Intel | Issue #1: Proposal 1.3-1 Support  Issue #2: Proposal 1.3-2 Support  Issue #3: Proposal 1.3-3 Support  Proposal 1.3-4 Support  For SCS 480 kHz and 960 kHz, we support X values of 2.75 and 1.5 respectively. Values smaller than this may potentially lead to overlapped placement of Type0-PDCCH in case of 128 SSB candidates. Existing values may not allow co-location of Type-0 PDDCH in the same slot as the SSB.  Issue #4: while our preference is to keep the monitoring behavior for Type0-PDCCH the same (i.e. two slots n0 and n0+1) but we are open for discussion. We would like to ask proponents of single slot monitoring, what kind of UE complexity benefit they think could be achieved given that Type0-PDCCH monitoring only happens every 20msec and only when system information needs to be decoded, which is very seldom event.  Issue #5: We propose modifying the PDCCH monitoring equation to account for non-contiguous slot numbering in case of 480 kHz and 960 kHz SCS. FR1 SSB slot pattern was consecutive since empty symbols in each slot could be utilized for uplink transmission. For 480 kHz and 960 kHz since the symbol and slot duration is smaller, the gNB will need to utilize empty slots after the SSB slots for uplink. The existing equation does not account for the non-contiguous numbering of the slot pattern. In the figure below (M=0.5), Type0-PDCCH for SSB#6 and SSB#7 will be monitored in slot 3, which in this example is a non-SSB carrying slot and collocation of Type0-PDCCH and SSB in the same slot will not be possible.    Issue #6: We propose RB offset values [0, 1] for multiplexing pattern 1 and [-20/-21] for multiplexing pattern 3 for 24, 48, 96 PRB CORESET. Based on our study, these values would be sufficient for spectrum utilization of 89% or higher. Some analysis is described in our Tdoc R1-2109598. |
| vivo | Proposal 1.3-1: Support.  Proposal 1.3-2: Support.  Proposal 1.3-3: We think the value of ‘X’ is also depended on the duration of candidate SSBs. It is preferable to determine the SSB resource pattern first.  Proposal 1.3-4: Support. |
| Huawei, HiSilicon | **Proposal 1.3-1:** Support  **Proposal 1.3-2:**  We cannot agree with the first sub-bullet of this proposal. We think that O values 2.5 and 7.5 are not justifiable for 120kHz FR2-2. These values are included in Table 13-12 of 38.213 to accommodate 120 kHz Type0-PDCCH allocation right after the 240 kHz SSB burst set. This is a non-existent scenario in FR2-2 and we don’t see why they need to be supported. We suggest the following modification Proposal 1.3-2 (modified)  * For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz,   + use Table 13-12 in TS38.213 for multiplexing pattern 1 excluding the rows corresponding to O=2.5 and O=7.5,   + use Table 13-15 in TS38.213 for multiplexing pattern 3.   **Proposal 1.3-3:** We can agree with the proposal if rows 6,7,8, 11 are removed (corresponding to {, if  is odd})  We are OK with the O values.We still have serious concern about the“First symbol index” values of {, if  is odd} and we think they should be removed due to the beam switching gap requirement. While Qualcomm’s proposal ({+ 1, if  is odd}) may address the beam switching gap requirement, considering that even index SSBs are located at symbol 2, the only way that CORESET0 of odd SSBs do not collide with the even SSBs is to configure CORESET0 set after the SSB burst set. In such a case, considering that SSB burst set length is at least 32 slots, we don’t see any real advantage of using {+ 1, if  is odd} compared to {7, if  is odd} for CORESET#0 location in terms of initial access latency reduction: If CORESET0 set has to be configured after at least 32 slots SSB burst set, configuring the odd CORESET0 4 or 5 symbols (7-(+1)) earlier within the same slot does not really contribute in initial access latency reduction.  More important, ({0, if  is even}, {7, if  is odd}) has another advantage compared to ({0, if  is even}, {, if  is odd}): It facilitates configuring PDSCH associated with Type0-PDCCH right after the corresponding Type0-PDCCH at symbol if i is even and 7+ if i is odd. This further relieves UE from beam switching for the whole half of the slot.  **Proposal 1.3-4:**  RAN1 has not agreed to support Multiplexing pattern 3 for {CORESET0, SSB} = {480, 480} kHz or {960, 960} kHz. Therefore, discussing the corresponding ‘searchSpaceZero’ Table for {480, 480} kHz or {960, 960} kHz seems to be premature. Also a minor note: k may go larger than 31 if DBTW is agreed for 480/960 kHz.  **Issue #6) RB offset values**  For us, the first priority regarding RB offset is that, for MUX1 and for any supported CORESET#0 #RBs and #Symbols, at least one of the lowest RB or the highest RB of CORESET#0 and SSB should be aligned (assuming synch/channel raster design does not impose any restriction against such a design). This facilitates allocating larger number of contiguous RBs on top or bottom of SSB for PDSCH associated with Type0-PDCCH. |
| ZTE, Sanechips | Proposal 1.3-1: It can be introduced only when there is a strong demand.  Proposal 1.3-2: Support  Proposal 1.3-3: Support  Proposal 1.3-4: Support  Issue #4: We think the number of Type0-PDCCH monitoring slots can keep unchanged, but we agree with Qualcomm that 8.2.2 is the best place to discuss this issue.  Issue #5: We don't quite understand this issue and it may need more clarification. |
| Sony | For Issue #1, we support Proposal 1.3-1.  For Issue #2, we support Proposal 1.3-2.  For Issue #3, we support Proposal 1-3-3 and Proposal 1.3-4.  For Issue #4, we agree with Qualcomm that this issue should be discussed on AI 8.2.2 |
| Nokia | **Issue #1)**  Proposal 1.3-1) We are OK with this.  **Issue #2)**  Proposal 1.3-2) We are OK with this proposal  **Issue #3)**  Proposal 1.3-3) We are fine with the proposal, though do not see cases with first symbol index as ({0, if  is even}, {, if  is odd}) essential.  Proposal 1.3-4) we are OK with this proposal.  **Issue #4)**  We don’t see a need to change the assumptions for this part. This was introduced for NW scheduling flexibility.  **Issue #5)**  As an afterthought (and as noted few meetings back) it would have been probably most beneficial if we would have modified pattern2 (with single numerology) to 480kHz and 960kHz. This could be something we would be willing to consider if other companies are interested. This would of course depend on the final SSB pattern for 480kHz/960kHz. |
| Futurewei | Proposal 1.3-1: support  Proposal 1.3-2: support  Proposal 1.3-3: support  Proposal 1.3-4: ok |
| Apple | **Issue #1)**  Proposal 1.3-1): Support the proposal.  **Issue #2)**  Proposal 1.3-2) : Support  **Issue #3)**  Proposal 1.3-3): Support.  On the row with ‘’, we do not see clear use case for FR2-2. We are open to keep it as current or removing the row. We do not see the need to enhance it by adding gap symbol due to lack of use case.  Proposal 1.3-4): Support.  **Issue #4):** We agree this can be continuously handled in AI 8.2.2.  **Issue #5):** Pending discussion after conclusion on SSB pattern. |

#### <Summary of 1st Round of Discussions>

Issue #1)

Proposal 1.3-1

* Support: Docomo, OPPO, Lenovo/Motorola Mobility, Samsung, ETRI, Sharp, Intel, vivo, Huawei/HiSilicon, Sony, Nokia/NSB, Futurewei, Apple
* Not Support: Interdigital, LGE
  + 96 PRB not needed
* Ok if strong demand: ZTE/Sanechips
* Defer: Docomo, Ericsson

Issue #2)

Proposal 1.3-2

* Support: Docomo, OPPO, Qualcomm, Lenovo/Motorola Mobility, Samsung, Interdigital, LGE, Ericsson, ETRI, Sharp, Intel, vivo, ZTE/Sanechips, Sony, Nokia/NSB, Futurewei, Apple
* Not Support: Huawei/HiSilicon (remove O=2.5 and 7.5)
* Defer:

Issue #3)

Proposal 1.3-3

* Support: Docomo, Lenovo/Motorola Mobility, Samsung, Interdigital, LGE, Ericsson, ETRI, Intel, ZTE/Sanechips, Sony, Nokia/NSB ({0, N\_symb} starting symbol entries not essential), Futuerwei, Apple (({0, N\_symb} starting symbol entries not essential)
* Not Support: OPPO (update O values), Qualcomm (O value are ok, update for beam switching gap), Sharp(O value are ok, update for beam switching gap), Huawei/HiSilicon (O values are ok, remove entry with {0, N\_symb} starting symbol)
  + Change O from {0, 2.5, 5, 7.5} to {0, X, Y, Z}
  + Change start symbol from {0, N\_symb} to {0, N\_symb+1}
  + Remove entries with {0, N\_symb} starting symbol
* Defer: vivo

Proposal 1.3-4

* Support: Docomo, OPPO, Qualcomm, Lenovo/Motorola Mobility, Samsung, Qualcomm, Interdigital, LGE, ETRI, Sharp, Intel, vivo, ZTE/Sanechips, Sony, Futurewei, Apple
* Not Support:
* Defer: Ericsson, Huawei/HiSilicon
  + WID states “Prioritize support SSB-CORESET#0 multiplexing pattern 1. Other patterns discussed on a best effort basis”
  + Wait to agree to mux pattern 3

**Proposal 1.3-4A**

* If multiplexing pattern 3 is supported for {SSB, CORESET#0/Type0-PDCCH} SCS = {480, 480} kHz and {960, 960} kHz, ‘searchSpaceZero’ configuration uses the following table~~:If supported, for ‘searchSpaceZero’ configuration for {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 3:~~

|  |  |  |
| --- | --- | --- |
| Index | PDCCH monitoring occasions (SFN and slot number) | **First symbol index**  **(*k* = 0, 1, … 31)** |
| 0 |  | 2, 9 in |
| 1 ~ 15 | Reserved | |

Issue #4)

* Two slot monitoring {n0, n0+1} (current spec): OPPO, Ericsson, Intel, Nokia/NSB
* One slot monitoring {n0 or n1}: Samsung
* FFS: Docomo (depends on multi-slot PDCCH monitoring capability) , Intel (open to discuss)
* Discuss in PDCCH agenda: LGE, Qualcomm, Lenovo/Motorola Mobility, ETRI, Sharp, ZTE/Sanechips, Sony, Apple

Issue #5)

Update PDCCH monitoring equation to account to non-contiguous numbering of SSB slots pattern for 480/960kHz

* Support: Intel, Nokia/NSB (depends on SSB pattern)
* Do not support: Samsung, Ericsson
  + Common design for 120, 480, and 960kHz
* FFS: Apple (depends on SSB pattern)

Issue #6)

RB offset values:

* Ask RAN4 if existing RB offset values can be kept
  + LGE
* 48 RB CORESET0: {2 14 26} RBs (assuming 86.4% spectral utilization) or {0 14 28} RBs (assuming > 90% spectral utilization)
  + Ericsson
* 24 RB CORESET0: {0 4} RBs
  + Ericsson
* 24 RB CORESET: 0 RB; 48 RB CORESTE: 0, 1 RB; 96 RB CORESET: 0 RB; all assuming 89% spectrum utilization or higher
  + Intel
* for MUX1 and for any supported CORESET#0 #RBs and #Symbols, at least one of the lowest RB or the highest RB of CORESET#0 and SSB should be aligned (assuming synch/channel raster design does not impose any restriction against such a design)
  + Huawei/HiSilicon

#### 2nd Round of Discussions

**Issue #1) 120kHz CORESET 96 PRB**

Based comments significant number of companies are ok or favor supporting 96PRB (16 for vs. 2 against). There were at least two companies who wanted to defer the decision. Moderator suggest to agree to proposal 1.3-1 as working assumption over email 2nd week of the meeting. This way the decision can be deferred to near end of the meeting.

##### Proposal 1.3-1

* For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz, support multiplexing pattern 1 with 96 PRB CORESET#0, and {1, 2} symbol durations

**Issue #2) 120kHz CORESET/SS aspects**

Based comments significant number of companies are ok or favor supporting Proposal 1.3-2 (20 for vs. 1 against). One company pointed out O=2.5 and 7.5 are not needed and should be removed from mux pattern 1. Moderator suggests companies to provide comments on Proposal 1.3-2A (editorial correction) and 1.3-2B.

##### Proposal 1.3-2A

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} SCS = {120, 120} kHz,
  + use Table 13-12 in TS38.213 for multiplexing pattern 1,
  + use Table 13-15 in TS38.213 for multiplexing pattern 3.

##### Proposal 1.3-2B

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} SCS = {120, 120} kHz,
  + use Table 13-12 in TS38.213 for multiplexing pattern 1 excluding the rows corresponding to O=2.5 and O=7.5,
  + use Table 13-15 in TS38.213 for multiplexing pattern 3.

**Issue #3) SS for 480/960kHz**

Large number of companies supported 1.3-3 (16 ok vs 5 not ok). The concerns seems to be focus on {0, N\_symb} starting positions and ability to beam switch quickly at the gNB. While some companies commented beam switch can be absorbed by CP, it is true RAN4 has not completed the beam switch gap and information for inter-panel beam switching for gNB is missing from RAN4.

I’ve updated the proposal to see if we can accommodate the views in Proposal 1.3-3A. This doesn’t resolve the problem completely, but at least the agreement is taking the group bit further. If possible, moderator would like to resolve all the FFS for 1.3-3A during RAN1 #106-bis-e meeting. Please provide further comments on Proposal 1.3-3A.

**Proposal 1.3-3A**

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 1:
  + FFS: The value of X (>~~≥~~ 0)
  + FFS: whether or not to use different X value depending on whether DBTW is ON/OFF
  + FFS: whether or not to use same or different X value for 480 and 960 kHz
  + FFS: whether Y = , or Y=, or whether to remove entries with Y

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Index |  | Number of search space sets per slot |  | **First symbol index** |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | ~~2.5~~ X | 1 | 1 | 0 |
| 3 | ~~2.5~~ X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 4 | 5 | 1 | 1 | 0 |
| 5 | 5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 6 | 0 | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 7 | ~~2.5~~ X | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 8 | 5 | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 9 | ~~7.5~~ 5 + X | 1 | 1 | 0 |
| 10 | ~~7.5~~ 5 + X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 11 | ~~7.5~~ 5 + X | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 12 | 0 | 1 | 2 | 0 |
| 13 | 5 | 1 | 2 | 0 |
| 14 | Reserved | | | |
| 15 | Reserved | | | |

##### Proposal 1.3-3B

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 1:
  + FFS: The value of X (>~~≥~~ 0)
  + FFS: whether or not to use different X value depending on whether DBTW is ON/OFF
  + FFS: whether or not to use same or different X value for 480 and 960 kHz
  + FFS: whether Y = , or Y=, ~~or whether to remove entries with Y~~

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Index |  | Number of search space sets per slot |  | **First symbol index** |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | ~~2.5~~ X | 1 | 1 | 0 |
| 3 | ~~2.5~~ X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 4 | 5 | 1 | 1 | 0 |
| 5 | 5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 6 | 0 | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 7 | ~~2.5~~ X | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 8 | 5 | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 9 | ~~7.5~~ 5 + X | 1 | 1 | 0 |
| 10 | ~~7.5~~ 5 + X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 11 | ~~7.5~~ 5 + X | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 12 | 0 | 1 | 2 | 0 |
| 13 | 5 | 1 | 2 | 0 |
| 14 | Reserved | | | |
| 15 | Reserved | | | |

For proposal 1.3-4, there are 18 companies that are supportive, no company against, and 3 companies that think decision should be deferred as multiplexing pattern 3 is de-prioritized by the WID. Therefore, moderator suggests to take email approval of the proposal in 2nd week of the meeting and check whether we can make agreement in 2nd week. This way it will provide companies to further assess and allow other issues to be resolved first.

##### Proposal 1.3-4

* If supported, for ‘searchSpaceZero’ configuration for {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 3:

|  |  |  |
| --- | --- | --- |
| Index | PDCCH monitoring occasions (SFN and slot number) | **First symbol index**  **(*k* = 0, 1, … 31)** |
| 0 |  | 2, 9 in |
| 1 ~ 15 | Reserved | |

**Proposal 1.3-4A**

* If multiplexing pattern 3 is supported~~,~~ for ‘searchSpaceZero’ configuration for {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 3:

|  |  |  |
| --- | --- | --- |
| Index | PDCCH monitoring occasions (SFN and slot number) | **First symbol index**  **(*k* = 0, 1, … 31)** |
| 0 |  | 2, 9 in |
| 1 ~ 15 | Reserved | |

**Issue #4) Type0-PDCCH monitoring**

Several companies comments that this should be treated in PDCCH agenda.

Conclusion:

Moderator suggests proponent companies to bring up the issues and provide comments to [106bis-e-R17-52-71GHz-02] email discussion thread.

**Issue #5) Type0-PDCCH monitoring slot equation update**

Further discussion on the issue seems needed. Intel has provided some further explanation that some companies requested, please review Intel comments.

**Issue #6) CORESET RB offset**

Further discussion on the issue seems needed.

Please provide comments on the above issues and proposals.

Quick summary of request from moderator:

* Issue #1) check for approval in 2nd week of meeting, please provide comments later (next week approval)
* Issue #2) provide comments on Proposal 1.3-2A and 1.3-2B
* Issue #3) comment on Proposal 1.3-3A, please provide comments later for 1.3-4 (next week approval)
* Issue #4) discuss in 8.2.2 agenda – no further comments in this agenda
* Issue# 5) continue to provide further comments on updating PDCCH monitoring equation to account for gap in SSB slots
* Issue #6) continue to provide information and inputs on RB offset for further discussion

|  |  |
| --- | --- |
| Company | Comments |
| LG Electronics | Proposal 1.3-2A and Proposal 1.3-2B: Support Proposal 1.3-2A and do not support Proposal 1.3-2B. O=2.5 or 7.5 could be useful in licensed carrier especially when gNB uses not more than 32 SSB indexes. Basically, we should keep the entry introduced in Rel-15.  Proposal 1.3-3A: Even though we prefer Y = , we can accept the proposal for the sake of progress.  Proposal 1.3-4: Support |
| vivo | Issue#1: support Proposal 1.3-1 Issue#2: no strong view and slightly prefer Proposal 1.3-2A  Issue#3: Support 1.3-3A  Issue#4: Support 1.3-4 |
| DOCOMO | * Issue #1) ok to defer * Issue #2) open to discuss, while prefer Proposal 1.3-2A. What is the issue on O=2.5 and 7.5 with 120kHz SCS? We think they anyway work, thus no need of enhancements. * Issue #3) We support Proposal 1.3-3A * Issue #4) agree to discuss in 8.2.2 agenda * Issue# 5) we think it depends on the definition of SSB slots. Prefer to defer. * Issue #6) we’re open to discuss. |
| Samsung | * Proposal 1.3-2A & Proposal 1.3-2B: We tend to agree that O=2.5 and 7.5 are not designed for 120 kHz in FR2-1 but for 240 kHz, but didn’t see harm to keep them there. We still prefer Proposal 1.3-2A, but ok with Proposal 1.3-2B if that’s the only way to get consensus. * Proposal 1.3-3A: We are ok with the proposal. Just want to comment that if Y=, the second search space collides with the first SSB in the slot, so we don’t think this is a technical solid alternative (e.g. either keeping Y= or delete the rows), but we are ok to keep it in the FFS. * For Issue #4, actually we proposed it regardless of the selection of alternative for multi-slot PDCCH monitoring. We just try to avoid back-to-back slot monitoring for 480 and 960 kHz in a general sense. If all companies want to discuss in 8.2.2, we are ok. |
| Intel | Issue #1:  Proposal 1.3-1 Support  Issue #2:  Proposal 1.3-2B Support  O values 2.5 and 7.5 may be unnecessary since 64 SSB candidates for {120, 120} kHz are contained in 4.75 msec and could potentially lead to overlapped placement of Type0- PDCCH.  For the sake of progress, we are also ok to accept Proposal 1.3-2A.  Issue#3:  Proposal 1.3-3A and Proposal 1.3-4 Support  For 480 kHz and 960 kHz, we support X values of 2.75 and 1.5 due to co-location and overlapped placement of Type-0 PDCCH.  Issue#4:  We prefer two-slot monitoring, but are open to further discussion on why back-to-back slot monitoring could be beneficial.  Issue#5:  For proposal 1.2-2, majority of the companies seem to prefer non-contiguous SSB slot selection (Alt 2 or variants of Alt 2). The existing equation will not work accurately for non-contiguous SSB slot pattern as explained in our previous comments. We encourage other companies to consider this issue. Our suggestion is to have a working assumption as follows:  Proposal 1.3-5  If non-contiguous SSB slot pattern is supported, modify the PDCCH monitoring equation to account for gaps in SSB slots.  For 480 kHz and 960 kHz since the symbol and slot duration is smaller, the gNB will need to utilize empty slots after the SSB slots for uplink. The existing equation does not account for the non-contiguous numbering of the slot pattern. In the figure below (M=0.5), Type0-PDCCH for SSB#6 and SSB#7 will be monitored in slot 3, which in this example is a non-SSB carrying slot and collocation of Type0-PDCCH and SSB in the same slot will not be possible.    The issue was not critical in FR1, since SSB slots were always consecutive.  In FR2-1 (previous FR2), as Huawei pointed out, SSB pattern never really supported multiplexing of two PDCCH monitoring occasions, {0, }, when using multiplexing pattern 1. This is because the second PDCCH monitoring position within the slot overlaps with SSB and they are not compatible. The obvious choice for supporting same slot multiplexing was using multiplexing pattern 3 for FR2-1. So this is unique issue for FR2-2. WID basically down-scoped multiplexing pattern 3 for FR2-2. The SSB pattern was supported as {2,9}+14n because companies wanted to possibility to support same slot multiplexing. Therefore, we suggest to consider modifying PDCCH monitoring equation to account for this.  Issue #6:  In our contribution R1-2109598, we have provided our analysis on a channelization design which allows flexibility between maximum spectrum utilization and maximum coexistence with 802.11 ad/ay systems. Based on our study we propose RB offset values [0] for multiplexing pattern 1 and [-20/-21] for multiplexing pattern 3 for 24, 48, 96 PRB CORESET assuming 95% spectrum utilization. |
| Interdigital | **Issue #1)** We are OK to defer.  **Issue #2)** We support Proposal 1.3-2A. As LG mentioned, the O=2.5 or 7.5 might be used in case of lower SSB indexes.  **Issue #3)** No strong view and we support proposal 1.3-3A for the purpose of progress.  We support Proposal 1.3-4. |
| Qualcomm | Proposal 1.3-1: no strong view  Proposal 1.3-2A/B: slightly prefer 1.3-2A for minimal spec changes  Proposal 1.3-3A: support  Proposal 1.3-4: support |
| Lenovo, Motorola Mobility | Proposal 1.3-2A and 1.3-2B: fine with either of the proposal  Proposal 1.3-3A: support  Proposal 1.3-4: support |
| Sharp | Issue #2: We support Proposal 1.3-2A for minor specification effort, even though O = 2.5 does not represent the tight offset for 120kHz SSB burst. Otherwise, it might be better to introduce a tight offset value counting for 120kHz SSB burst (but this requires specification effort).  Issue #3: We agree with Samsung’s comment “if Y=, the second search space collides with the first SSB in the slot” but this should be only for O = 0. For O > 0, there might be no SSB in the same slot where the search space set is configured. Thus, our preference is to keep the row unchanged for O = 0 and Y= in rows where O > 0. |
| Apple | **Proposal 1.3-1:** Support.  **Proposal 1.3-2A/B:** Slightly prefer 1.3-2A to minimize the specification change and potentially used when number of SSB beams is smaller on licensed band (as LG commented)  **Proposal 1.3-3A**: Ok.  **Proposal 1.3-4**: Support. |
| OPPO | **Proposal 1.3-1:** Support.  **Proposal 1.3-2A:** Support.  **Proposal 1.3-3A**: Support.  **Proposal 1.3-4**: Support. |
| Ericsson | Proposal 1.3-1: We can support this at the end of the WI if it is known that there are enough table entries left over after 48 and 24 RB CORESET are specified with the SSB-CORESET0 offsets according to RAN4 channelization design  Proposal 1.3-2A: Support  Proposal 1.3-2B: Object. We don't agree to remove O = 2.5 and 7.5. This would mean that RMSI beam sweep cannot be in the same half frame as SSB beam sweep.  Proposal 1.3-3A: Support as long as "…whether to remove entries with Y" is removed  Proposal 1.3-4: Support, but reword to say "If multiplexing pattern 3 is supported …" |
| ZTE, Sanechips | Issue #1: Support Proposal 1.3-1 as a working assumption Issue #2: Prefer Proposal 1.3-2A (O=2.5 and 7.5 can be used when the configured <= 32 and the DBTW length <3ms in unlicensed spectrum)  Issue #3: Support 1.3-3A and support 1.3-4 Issue #4: Support the conclusion Issue #5: We still don't quite understand this issue. If it is related to 480/960 kHz SCS SSB design as commented by Intel, the discussion could be postponed until the value of ’n’ for 480/960 kHz SCS SSB has been determined. |
| CATT | Issue #1: defer this Issue #2: Support proposal 1.3-2A  Issue #3: Support 1.3-3A and support 1.3-4 Issue #4: Support the conclusion |

#### <Summary of 2nd Round of Discussions>

##### **Issue #1) 120kHz CORESET 96 PRB**

Check for approval in 2nd week of meeting, please provide comments later (next week approval). The following is recap of summary from 1st round discussion.

Proposal 1.3-1

* Support: Docomo, OPPO, Lenovo/Motorola Mobility, Samsung, ETRI, Sharp, Intel, vivo, Huawei/HiSilicon, Sony, Nokia/NSB, Futurewei, Apple
* Not Support: Interdigital, LGE
  + 96 PRB not needed
* Ok if strong demand: ZTE/Sanechips
* Defer: Docomo, Ericsson (until end of WI),CATT
* WA: ZTE/Sanechips

##### **Issue #2) 120kHz CORESET/SS aspects**

While many companies are ok with both 1.3-2A and 1.3-2B, among the two proposals, 1.3-2A seems to be have bit more support. Moderator suggest to try to see if 1.3-2A is acceptable for email approval for all.

Proposal 1.3-2A

* Support: LGE, vivo (2nd preference), Docomo, Samsung (1st preference), Intel (2nd preference), Interdigital, Qualcomm (1st preference), Lenovo/Motorola Mobility, Sharp, Apple (1st preference) , OPPO, Ericsson, ZTE/Sanechips,CATT

Proposal 1.3-2B

* Support: vivo (1st preference), Samsung (2nd preference), Intel (1st preference), Qualcomm (2nd preference), Lenovo/Motorola Mobility, Apple (2nd preference)
* Not support: LGE, Ericsson

##### **Issue #3) SS for 480/960 kHz**

The following is summary of views. It looks like companies are converging on this issue. Suggest continuing discussion over email.

Proposal 1.3-3A

* Support: LGE(ok to accept), vivo, Docomo, Samsung, Intel, Interdigital, Qualcomm, Lenovo/Motorola Mobility, [Sharp?], Apple, OPPO, ZTE/Sanechips
* Not support: Ericsson (removing entries is not ok)

Proposal 1.3-3B

* Support: Ericsson

Proposal 1.3-4A seem quite stable. Suggest asking the proposal for email approval.

Proposal 1.3-4A

* Support: LGE, vivo, Intel, Interdigital, Qualcomm, Lenovo/Motorola Mobility, Apple, OPPO, Ericsson, ZTE/Sanechips
* Moderator note: companies express support for 1.3-4 but assume 1.3-4A is minor editorial change that companies are ok with.

##### **Issue #4) Type0-PDCCH monitoring – move to 8.2.2**

No discussion.

##### **Issue# 5) Type0-PDCCH monitoring occasion update**

The following is proposed by Intel. However, further discussion is likely required.

**Proposal 1.3-5**

* If non-contiguous SSB slot pattern is supported, modify the PDCCH monitoring equation to account for gaps in SSB slots.

##### **Issue #6) CORESET RB offsets**

Continuation of discussion is needed.

#### 3rd Round of Discussions

##### **Issue #1) 120kHz CORESET 96 PRB**

Suggest seeking for email approval for Proposal 1.3-1 at the end of the meeting. Please comment if you have strong concerns.

##### **Issue #2) 120kHz CORESET/SS aspects**

While many companies are ok with both 1.3-2A and 1.3-2B, among the two proposals, 1.3-2A seems to be have bit more support. Moderator suggests trying to see if 1.3-2A is acceptable for email approval. Please comment only if you have strong concerns for 1.3-2A.

##### **Issue #3) SS for 480/960 kHz**

The following is summary of views. It looks like companies are converging on this issue. Please comment on whether companies are ok with 1.3-3B. Since 1.3-3A is a superset of 1.3-3B, if 1.3-3B is not agreeable at this point, suggest agreeing to 1.3-3A.

**Proposal 1.3-3A**

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 1:
  + FFS: The value of X (> 0)
  + FFS: whether or not to use different X value depending on whether DBTW is ON/OFF
  + FFS: whether or not to use same or different X value for 480 and 960 kHz
  + FFS: whether Y = , or Y=, or whether to remove entries with Y

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Index | O | Number of search space sets per slot | M | **First symbol index** |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 2 | 1/2 | {0, if *i* is even}, {7, if *i* is odd} |
| 2 | ~~2.5~~ X | 1 | 1 | 0 |
| 3 | ~~2.5~~ X | 2 | 1/2 | {0, if *i* is even}, {7, if *i* is odd} |
| 4 | 5 | 1 | 1 | 0 |
| 5 | 5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 6 | 0 | 2 | 1/2 | {0, if *i* is even}, {Y, if  is odd} |
| 7 | ~~2.5~~ X | 2 | 1/2 | {0, if *i* is even}, {Y, if  is odd} |
| 8 | 5 | 2 | 1/2 | {0, if *i* is even}, {Y, if  is odd} |
| 9 | ~~7.5~~ 5 + X | 1 | 1 | 0 |
| 10 | ~~7.5~~ 5 + X | 2 | 1/2 | {0, if  is even}, {7, if *i* is odd} |
| 11 | ~~7.5~~ 5 + X | 2 | 1/2 | {0, if *i* is even}, {Y, if *i* is odd} |
| 12 | 0 | 1 | 2 | 0 |
| 13 | 5 | 1 | 2 | 0 |
| 14 | Reserved | | | |
| 15 | Reserved | | | |

###### Proposal 1.3-3B

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 1:
  + FFS: The value of X (> 0)
  + FFS: whether or not to use different X value depending on whether DBTW is ON/OFF
  + FFS: whether or not to use same or different X value for 480 and 960 kHz
  + FFS: whether Y = , or Y=

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Index | O | Number of search space sets per slot | M | **First symbol index** |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 2 | 1/2 | {0, if *i* is even}, {7, if *i* is odd} |
| 2 | ~~2.5~~ X | 1 | 1 | 0 |
| 3 | ~~2.5~~ X | 2 | 1/2 | {0, if *i* is even}, {7, if *i* is odd} |
| 4 | 5 | 1 | 1 | 0 |
| 5 | 5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 6 | 0 | 2 | 1/2 | {0, if *i* is even}, {Y, if  is odd} |
| 7 | ~~2.5~~ X | 2 | 1/2 | {0, if *i* is even}, {Y, if  is odd} |
| 8 | 5 | 2 | 1/2 | {0, if *i* is even}, {Y, if  is odd} |
| 9 | ~~7.5~~ 5 + X | 1 | 1 | 0 |
| 10 | ~~7.5~~ 5 + X | 2 | 1/2 | {0, if  is even}, {7, if *i* is odd} |
| 11 | ~~7.5~~ 5 + X | 2 | 1/2 | {0, if *i* is even}, {Y, if *i* is odd} |
| 12 | 0 | 1 | 2 | 0 |
| 13 | 5 | 1 | 2 | 0 |
| 14 | Reserved | | | |
| 15 | Reserved | | | |

Proposal 1.3-4A seem quite stable. Suggest asking the proposal for email approval. Please comment only if you have strong concerns for 1.3-4A.

##### **Issue# 5) Type0-PDCCH monitoring occasion update**

The following is proposed by Intel. However, further discussion is likely required. Moderator has a feeling that this discussion may need to be deferred until the SSB candidate is resolved. With that said, please provide further comments.

###### Proposal 1.3-5

* If non-contiguous SSB slot pattern is supported, modify the PDCCH monitoring equation to account for gaps in SSB slots.

##### **Issue #6) CORESET RB offsets**

Continuation of discussion is needed.

##### **Company comments**

Please provide comments on the proposals. Quick summary of request from moderator:

* Issue #1) only provide comments if you have strong and serious concerns with Proposal 1.3-1. If no concerns, moderator will ask for email approval at end of meeting.
* Issue #2)
  + only provide comments if you have strong and serious concerns with Proposal 1.3-2A. If no concerns, moderator will ask for email approval at end of meeting
* Issue #3)
  + Please comment if companies are ok with 1.3-3B, if not ok, moderator suggest companies to comment if they can accept 1.3-3A for sake of progress (given that 1.3-3A is a superset of 1.3-3B).
* Issue #4) no discussion
* Issue# 5) comment further on Proposal 1.3-5.
* Issue #6) continue discussions

|  |  |
| --- | --- |
| Company | comments |
| Sharp | Issue 3: Okay with Proposal 1.3-3B. |
| LG Electronics | Proposal 1.3-1: Do not support.  Proposal 1.3-3A or Proposal 1.3-3B: Is the different between them only “or whether to remove entries with Y”? If this is the case, we prefer Proposal 1.3-3B.  Proposal 1.3-5: Since we support contiguous SSB slot pattern, we don’t see the issue.  Issue #6: As we commented earlier, one way could be to keep the same RB offset values as in Rel-15 and inform it RAN4 to check whether it would be problematic or not when sync/channel rasters are designed. |
| DOCOMO | * Issue #3)   + The only difference between 1.3-3A and 1.3-3B seems whether to explicitly capture the removal of rows with Y (i.e. 1.3-3A) or not (i.e. 1.3-3B) in the last FFS, correct? If so, while we can live with 1.3-3A, we prefer 1.3-3B. We believe minimizing the FFSs would be important now. * Issue# 5) Given that less views from companies are available now, we think it should be discussed further. We are open to discuss. |
| Nokia | Issue #3)  We would be fine with proposal 1.3-3A.  Issue #5)  Like noted this is modifying multiplexing pattern 1 to achieve same as multiplexing pattern 2 but with same sub-carrier spacing for SSB and CORESET#0. We think that this type of multiplexing option could have some merits, but not sure if we should completely revise multiplexing pattern 1 to achieve it. |
| Interdigital | No strong view. We are OK with proposal 1.3-3A. |
| Samsung | Issue #3)  We are ok with Proposal 1.3-3A, and don’t prefer 1.3-3B. As mentioned in the previous round, Y= is not a valid configuration actually, since the symbol location of Y collides with the first SSB location in the slot. If there is an issue with processing time, we would rather remove that configuration, so we want to keep the possibility to delete those rows, although our first preference is still Y=.  Issue #5)  We don’t think we should modify the PDCCH monitoring equation to accommodate non-contiguous SSB pattern. Non-contiguous SSB pattern already exists Rel-15 FR2-1, and we didn’t make any special treatment for PDCCH monitoring equation to accommodate the non-contiguous SSB pattern. |
| Qualcomm | Issue #3: we are fine with either 1.3-3A or 1.3-3B |
| Intel | Issue#3: We support Proposal 1.3-3B, but we are also ok with Proposal 1.3-3A.  Issue #5: Proposal 1.3-5 Support  Even though the discussion for ‘n’ values is still ongoing, we suggest that companies (especially those who support Proposal 1.2-2A) initiate discussion whether the existing PDCCH monitoring equation will work for non-contiguous SSB slot pattern (which is the most favored in Section 2.1.2).  In our opinion, it will not work as desired for any set of ‘n’ if the SSB slot pattern is non-contiguous. We support potential modification to PDCCH monitoring equation in case of non-contiguous ‘n’ values, so that we can further discuss the options for said modification in the next meeting.  For example, if the SSB resource pattern uses n = {0,1,2, 4,5,6, 8,9, 10,…} with M=0.5. Type0-PDCCH for SSB#1 to SSB#5 will be monitored in slots 0-2, collocated with the SSB as expected. Type0-PDCCH for SSB#6 and SSB#7 will be monitored in slot 3, while the SSB#6 and SSB#7 will be located in slot 4 as shown in the figure below.    Issue #6: In our contribution R1-2109598, we have provided our analysis on a channelization design which allows flexibility between maximum spectrum utilization and maximum coexistence with 802.11 ad/ay systems and minimizes the raster entries to reduce cell search complexity. Based on our study, the proposed minimum required RB offsets for 24, 48, 96 PRB CORESET are as follows:  SU 95%: [0] for mux-1, [-20/-21] for mux-3  SU 89%: [0, 2] for mux-1, [-20/-21] for mux-3  SU 86.4%: [0, 3] for mux-1, [-20/-21] for mux-3 |
| Huawei, HiSilicon | **Issue#2:**  We have serious concerns regarding 1.3-2A. As discussed in our t-doc (R1-2108767) and in the first round of comments, for 120 kHz SCS in FR2-2, the O values of {2.5, 7.5} are not useful at all because they are only used in FR2-1 for mix numerology configuration to facilitate CORESET0 set allocation in 120 kHz SCS right after the SSB burst set of 240 kHz. Note that the SSB burst set of 240 kHz length is approximately 2.5 ms (and that is why O ={2.5, 7,5} is required in FR2-1). In FR2-2, SSB burst set last 5 ms and supporting values of O ={2.5, 7,5} has little technical justification in our view.  We support Proposal 1.3-2B.  **Issue#3:**  We cannot support Proposal 1.3-3B at this time. We can only support Proposal 1.3-3A which seems to have only one objection and also includes Proposal 1.3-3B if it will not finally be agreed to remove the rows with {, if  is odd}.  As discussed in the first round of comments We still have serious concern about the“First symbol index” values of {, if  is odd} and we think they should be removed due to the beam switching gap requirement. While Qualcomm’s proposal ({+ 1, if  is odd}) may address the beam switching gap requirement, considering that even index SSBs are located at symbol 2, the only way that CORESET0 of odd SSBs do not collide with the even SSBs is to configure CORESET0 set after the SSB burst set. In such a case, considering that SSB burst set length is at least 32 slots, we don’t see any real advantage of using {+ 1, if  is odd} compared to {7, if  is odd} for CORESET#0 location in terms of initial access latency reduction: If CORESET0 set has to be configured after at least 32 slots SSB burst set, configuring the odd CORESET0 4 or 5 symbols (7-(+1)) earlier within the same slot does not really contribute in initial access latency reduction. More important, ({0, if  is even}, {7, if  is odd}) has another advantage compared to ({0, if  is even}, {, if  is odd}): It facilitates configuring PDSCH associated with Type0-PDCCH right after the corresponding Type0-PDCCH at symbol if i is even and 7+ if i is odd. This further relieves UE from beam switching for the whole half of the slot. |
| CATT |  |
| Moderator | CATT comments seem to be missing.  Added 1.3-2C as an alternative to 1.3-2A. However, not sure if companies are supportive of 1.3-2C based on previous comments. I’ve added it for the time being so that companies can reference it in discussions.  To LGE: while you mentioned 96 PRB is not essential to support (previously), give that there is large number of companies supporting it, can you provide some technical reasons why supporting would be bad? If the issue is simply not needing the option, then moderator would like to strongly urge to just agree to 1.3-1 or maybe agree as working assumption, so that we can move on finalizing the type0-PDCCH configurations.  Continue to provide comments. I will update the summary as companies provide more inputs. Summary below are tentative version. |
| Ericsson  (3rd round comments prior to moderator summary of 3rd round) | **Issue 1**   * **We do not support Proposal 1.3-1 as written**. We understand we are in the minority; hence we we can compromise and support the following.   Working assumption:   * For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz, support multiplexing pattern 1 with 96 PRB CORESET#0, and {1, 2} symbol durations. * Note: the working assumption can be confirmed once RAN1 agrees on the number of needed SSB-CORESET0 offsets for 24 and 48 RB CORESET0 based on RAN4 channelization design   **Issue 2**   * Support Proposal 1.3-2A * We do not support Proposal 1.3-2B since removal of O = 2.5/7.5 would not allow RMSI beem sweep in the same half frame as the SSB beam sweep when a moderate number of SSBs is used.   **Issue 3**   * We support Proposal 1.3-3B * We can live with Proposal 1.3-3A; however, we don't see why there should be discussion on removing the rows with Y.   **Issue 4**  Fine to remove discussion  **Issue 5**  Prefer to defer discussion  **Issue 6**  Discussion can continue in the next meeting when we may know more about RAN4 channelization design. |
| Moderator | Added 1.3-1A based on Ericsson’s comments |
|  |  |
| Huawei, Hisilicon | **Issue#2:**  We support 1.3-2B and can accept 1.3-2C.  Still we have serious concern regarding 1.3-2A as we think O=2.5 and 7.5 have little practical relevance in FR2-2. O=2.5 and 7.5 are supported in FR2-1 to beam sweep 120 kHz RMSI after 240 kHz SSB burst. We don’t have such a use case in FR2-2.  **To Ericsson:** RMSI and SSB can beamsweep on the same subframe with O=0 and 5 for any number of transmitted SSBs. If I am not mistaken, you are referring to beamsweep of RMSI “burst” after ending the SSB burst when there are only 32 SSB transmitted (approximately 2.5 ms). But if we are concerned about such cases, then we probably should also support O=1.25 and 6.25 for the case that only 16 SSBs are transmitted and 3.75 and 8.75 when 48 SSBs are transmitted? We are not sure such scenarios should a concern when designing CORESET zero table. If we want to optimize for such cases, we would probably need more than four bits for coresetzero indication in MIB.  **Issue #3:**  Still support Proposal 1.3-3A and have strong concern about Proposal 1.3-3B  We don’t think 1.3-4A has a lot of practical value as Mux 3 is not agreed for 480/960 kHz yet and if agreed, agreeing on the MO table should not be very difficult (not much choices in designing Mux MO table). In any case, if we want to agree on this, we think that k should go from 0 to and not from 0 to 31. |
| LG Electronics | **To Moderator,**  Once we agree on introducing 96 RB CORESET#0, we may need to further discuss proper RB offset value(s) for 96 RB CORESET#0 and whether to support 96 RB CORESET#0 for SCSs other than 120 kHz SCS, even though we think it is not essential. Certainly, it can take some time to decide all of details but we have still other essential topics to be decided. With this regard, we still have a concern on Proposal 1.3-1, but we can accept Proposal 1.3-1A with the following modification. Proposal 1.3-1A  * Working assumption:   + For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz, support multiplexing pattern 1 with 96 PRB CORESET#0, and {1, 2} symbol durations   + Note: the working assumption can be confirmed once the number of needed SSB-CORESET0 offsets for 24 and 48 RB CORESET0 based on RAN4 channelization design is decided no later than RAN1#107-e. |
| Moderator | To LGE:  Would you be ok with Proposal 1.3-1A. It does seem bit odd to place a requirement on RAN4, especially when RAN1 design needs to be completed by RAN1 #107-e. Any work that is needed beyond RAN1 #107-e will require a formal exception sheet to be approved by RAN Plenary.  I think we should avoid text that seem like there could be something beyond RAN1#107-e. In my opinion RAN1 will need to finish design by RAN1#107-e regardless of RAN4 status. If any exceptions are needed that should be discussed in RAN Plenary. |
| ZTE, Sanechips | Issue #1: Support Proposal 1.3-1A as a working assumption Issue #2: Prefer Proposal 1.3-2A. we can also accept Proposal 1.3-2C as a compromise.  Issue #3: Support 1.3-3A. Issue #4: Support the suggestion Issue #5: The discussion on this issue can be deferred until the SSB pattern for 480/960kHz in a half frame is determined. |
| LG Electronics | **To Moderator,** Thanks a lot for the response. With that explanation, we are OK with Proposal 1.3-1A. |
| Vivo | We are OK with either 1.3-3A or 1.3-3B |
| Lenovo, Motorola Mobility | We prefer Proposal 1.3-3A, but are also fine with Proposal 1.3-3B |
| OPPO | Issue 3: We are fine with Proposal 1.3-3B. |
| Nokia (3rd round) | **Issue #1):** Ok with taking proposal 1.3-1 as working assumption.  **Issue #2)** we would prefer to maintain the option to concatenate the broadcast sweep in time (e.g. when moderate number of SSBs are used), thus still see some benefit to have time offset values 2.5ms and 7.5ms.  **Issue #3)**  (Still) Fine with proposal Proposal 1.3-3A. As the affirmative number for ‘Y’ cases cannot be probably made until RAN4 concludes it’s discussion, we would be fine removing these rows. It is also good to note that we have alternatives (i.e. {0, 7}) that cover two SS per slot. |

#### <Summary of 3rd Round of Discussions>

##### **Issue #1) 120kHz CORESET 96 PRB**

Objections to 1.3-1

* LGE
  + Not essential

**Proposal 1.3-1A**

* Working assumption:
  + For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz, support multiplexing pattern 1 with 96 PRB CORESET#0, and {1, 2} symbol durations
  + Note: the working assumption can be confirmed once RAN1 agrees on the number of needed SSB-CORESET0 offsets for 24 and 48 RB CORESET0 based on RAN4 channelization design

Moderator suggest agreeing to Proposal 1.3-1A as working assumption.

##### **Issue #2) 120kHz CORESET/SS aspects**

The following is summary of views.

Objections 1.3-2A

* Huawei/HiSilicon (support 1.3-2B)

**Proposal 1.3-2C**

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} SCS = {120, 120} kHz,
  + use Table 13-12 in TS38.213 for multiplexing pattern 1 excluding the rows corresponding to O=2.5 and O=7.5,
    - FFS: whether to support rows corresponding to O=2.5 and O=7.5
  + use Table 13-15 in TS38.213 for multiplexing pattern 3.

Check to see if companies are ok with Proposal 1.3-2C.

##### **Issue #3) SS for 480/960 kHz**

The following is summary of views.

Proposal 1.3-3A

* Ok: Nokia/NSB, Intergital, Samsung, Qualcomm, Intel, Huawei/HiSilicon, ZTE/Sanechips, vivo, Lenovo/Motorola Mobility

Proposal 1.3-3B

* Ok: LGE, Sharp, Docomo (can accept 2A), Qualcomm, Intel, Ericsson, vivoc, Lenovo/Motorola Mobility, OPPO
* Not ok: Samsung, Huawei/HiSilicon,

Objections to 1.3-4A

* <none received so far – moderator will further update>

Moderator suggest agreeing to Proposal 1.3-4A and 1.3-3A.

**Proposal 1.3-3A**

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 1:
  + FFS: The value of X (>~~≥~~ 0)
  + FFS: whether or not to use different X value depending on whether DBTW is ON/OFF
  + FFS: whether or not to use same or different X value for 480 and 960 kHz
  + FFS: whether Y = , or Y=, or whether to remove entries with Y

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Index |  | Number of search space sets per slot |  | **First symbol index** |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | ~~2.5~~ X | 1 | 1 | 0 |
| 3 | ~~2.5~~ X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 4 | 5 | 1 | 1 | 0 |
| 5 | 5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 6 | 0 | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 7 | ~~2.5~~ X | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 8 | 5 | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 9 | ~~7.5~~ 5 + X | 1 | 1 | 0 |
| 10 | ~~7.5~~ 5 + X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 11 | ~~7.5~~ 5 + X | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 12 | 0 | 1 | 2 | 0 |
| 13 | 5 | 1 | 2 | 0 |
| 14 | Reserved | | | |
| 15 | Reserved | | | |

**Proposal 1.3-4A**

* If multiplexing pattern 3 is supported~~,~~ for ‘searchSpaceZero’ configuration for {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 3:

|  |  |  |
| --- | --- | --- |
| Index | PDCCH monitoring occasions (SFN and slot number) | **First symbol index**  **(*k* = 0, 1, … 31)** |
| 0 |  | 2, 9 in |
| 1 ~ 15 | Reserved | |

##### **Issue# 5) Type0-PDCCH monitoring occasion update**

Further discussion may be needed. It was noted that if gaps slots are not supported for SSB slot pattern, there is no need to consider the issue.

##### **Issue #6) CORESET RB offsets**

Continuation of discussion is needed.

#### 4th Round of Discussions

##### **Stable Issues: Issue #1 + (part of) #3**

Approve the following proposals over email. Please indicate if you have strong concerns on approving them over email.

###### Proposal 1.3-1A

* Working assumption:
  + For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz, support multiplexing pattern 1 with 96 PRB CORESET#0, and {1, 2} symbol durations
  + Note: the working assumption can be confirmed once RAN1 agrees on the number of needed SSB-CORESET0 offsets for 24 and 48 RB CORESET0 based on RAN4 channelization design

###### Proposal 1.3-4A

* If multiplexing pattern 3 is supported~~,~~ for ‘searchSpaceZero’ configuration for {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 3:

|  |  |  |
| --- | --- | --- |
| Index | PDCCH monitoring occasions (SFN and slot number) | **First symbol index**  **(*k* = 0, 1, … 31)** |
| 0 |  | 2, 9 in |
| 1 ~ 15 | Reserved | |

Update to fix the indexing issue for Proposal 1.3-4A

###### Proposal 1.3-4B

* If multiplexing pattern 3 is supported~~,~~ for ‘searchSpaceZero’ configuration for {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 3:

|  |  |  |
| --- | --- | --- |
| Index | PDCCH monitoring occasions (SFN and slot number) | **First symbol index**  **(*k* = 0, 1, … ~~31~~Lmax/2 - 1)** |
| 0 |  | 2, 9 in |
| 1 ~ 15 | Reserved | |

**Moderator Suggestion:**

* Agree to following proposal
  + Proposal 1.3-1A
  + Proposal 1.3-4A ~~1.3-4B~~

|  |  |
| --- | --- |
| Company | Comment (only if you have strong concerns) |
| Huawei, HiSilicon | We don’t see any necessity to include the note in Proposal 1.3-1A but, if all companies agree to keep the note, we will not object and can accept Proposal 1.3-1A as is.  We don’t see any value in agreeing in Proposal 1.3-4A. If Mux 3 is agreed, to our understanding, there is no other way to configure searchSpaceZero. So, this proposal would not be a step forward in any way. Also, we think that k should go from 0 to and not from 0 to 31. If the number of candidate SSBs is =128, then k=0,1,…, 63. |
| Ericsson | Support Proposal 1.3-1A only if the note is preserved |
| Moderator | Fixed the indexing issue in Proposal 1.3-4A and updated to Proposal 1.3-4B. Sorry for the error. |
| ZTE, Sanechips | We support Proposal 1.3-1A and Proposal 1.3-4B). We don't understand why Moderator changed Proposal 1.3-4B to Proposal 1.3-4A in his suggestion. |

##### **Open Issues: Issue #2 + #3**

**Issue #2) 120kHz CORESET/SS aspects**

Check to see if companies are ok with Proposal 1.3-2C.

###### Proposal 1.3-2C

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} SCS = {120, 120} kHz,
  + use Table 13-12 in TS38.213 for multiplexing pattern 1 excluding the rows corresponding to O=2.5 and O=7.5,
    - FFS: whether to support rows corresponding to O=2.5 and O=7.5
  + use Table 13-15 in TS38.213 for multiplexing pattern 3.

Updated proposal based on LG’s comments.

###### Proposal 1.3-2D

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} SCS = {120, 120} kHz,
  + use Table 13-12 in TS38.213 for multiplexing pattern 1 ~~excluding the rows corresponding to O=2.5 and O=7.5~~,
    - FFS: whether to keep or ~~support~~ remove rows corresponding to O=2.5 and O=7.5
  + use Table 13-15 in TS38.213 for multiplexing pattern 3.

**Issue #3) SS for 480/960 kHz**

Check to see if companies are ok with Proposal 1.3-3A.

###### Proposal 1.3-3A

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 1:
  + FFS: The value of X (>~~≥~~ 0)
  + FFS: whether or not to use different X value depending on whether DBTW is ON/OFF
  + FFS: whether or not to use same or different X value for 480 and 960 kHz
  + FFS: whether Y = , or Y=, or whether to remove entries with Y

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Index |  | Number of search space sets per slot |  | **First symbol index** |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | ~~2.5~~ X | 1 | 1 | 0 |
| 3 | ~~2.5~~ X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 4 | 5 | 1 | 1 | 0 |
| 5 | 5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 6 | 0 | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 7 | ~~2.5~~ X | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 8 | 5 | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 9 | ~~7.5~~ 5 + X | 1 | 1 | 0 |
| 10 | ~~7.5~~ 5 + X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 11 | ~~7.5~~ 5 + X | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 12 | 0 | 1 | 2 | 0 |
| 13 | 5 | 1 | 2 | 0 |
| 14 | Reserved | | | |
| 15 | Reserved | | | |

##### **Company comments**

Companies are asked to see if they can live with Proposal 1.3-2C and 1.3-3A for sake of progress. We had further discussion to trying narrow down options, but it is clear that effort was not successful. Proposal 1.3-2C and 1.3-3A seem to be superset of proposals that most companies are ok with.

Please comment if Proposal 1.3-2C and 1.3-3A are not acceptable. If so which proposal you are ok with or please suggest way to resolve your concern in a constructive way so that RAN1 can get some agreement to use basis for next meeting.

|  |  |
| --- | --- |
| Company | Comment |
| Qualcomm | We are fine with FL proposals 1.3-2C and 1.3-3A. |
| LG Electronics | Whether to remove the legacy entries or not is already captured in FFS for each proposal. So, we suggest to delete “excluding the rows corresponding to O=2.5 and O=7.5” in Proposal 1.3-2C, which seems consistent to two proposals. We can accept Proposal 1.3-3A. Proposal 1.3-2C  * For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} SCS = {120, 120} kHz,   + use Table 13-12 in TS38.213 for multiplexing pattern 1 ~~excluding the rows corresponding to O=2.5 and O=7.5~~,     - FFS: whether to ~~support~~ remove rows corresponding to O=2.5 and O=7.5   + use Table 13-15 in TS38.213 for multiplexing pattern 3. |
| Moderator | Added Proposal update based on LGE’s comments. |
| Huawei, HiSilicon | We support Proposal 1.3-2C. We don’t think Proposal 1.3-2D is the way to go which includes all rows and then discuss whether or not some rows should be excluded. We think it is better to agree on the common denominator and then discuss if other rows should also be included (as in Proposal 1.3-2C).  Proposal 1.3-3A: OK |
| OPPO | We are fine with Proposals 1.3-2D and 1.3-3A. |
| Ericsson | Object to Proposal 1.3-2C since we have very strong concerns to removing O = 2.5 and 7.5. We do not want to lose the scheduling flexibility of having RMSI beam sweep following SSB beam sweep and both contained in the same half frame (assuming a moderate number of SSBs used). Why is key Rel-15 functionality being thrown away?  We can agree to Proposal 1.3-2D with the FFS bullet removed.  We can live with Proposal 1.3-3A. |
| Sharp | We are fine with Proposal 1.3-3A. |
| DOCOMO | For Issue#2, we can accept Proposal 1.3-2D but prefer to remove its FFS.  For Issue#3, ok with Proposal 1.3-3A. |
| vivo | We are fine with Proposals 1.3-2D and 1.3-3A. |
| Nokia (4th round) | We can accept proposal 1.3-2D (with or without the FFS point).  We are OK with 1.3-3A |
| ZTE, Sanechips | We can live with FL proposals 1.3-2D (the FFS can be deleted) and fine with 1.3-3A. |
| Lenovo, Motorola Mobility | We are fine with Proposals 1.3-2D and 1.3-3A. |
| Futurewei | We are OK with Proposal 1.3-2D and 1.3-3A |
| Qualcomm 2 | We are ok with updated Proposal 1.3-2D |

##### **Deferred Issues: Issue #4 + #5 + #6**

Moderator suggests continuing discussion for the following issues in the next meeting.

* Issue #5) Type0-PDCCH monitoring occasion update
* Issue #6) CORESET RB offsets

**Moderator Suggestion:**

* Further discuss the following issues in RAN1 #107-e
  + Issue #5) Type0-PDCCH monitoring occasion update
  + Issue #6) CORESET RB offsets

#### <Summary of 4th Round of Discussions>

*<Moderator to prepare summary>*

### 2.14 ANR/CGI Reporting Aspects

* From [3] Spreadtrum:
  + The mechanism of two offsets in MIB defined for NR-U, i.e. Alt 2), can be reused for UE to determine CORESET#0/Type0-PDCCH.
* From [7] OPPO:
  + For ANR design, RAN1 considers one of the two options
    - Option 1: RAN1 holds ANR discussion until RAN4 concludes the channelization, LBT bandwidth and sync raster relationship.
    - Option 2: RAN1 does not follow R16 baseline solution and redesign ANR.
* From [9] CATT:
  + There is no need to study additional method(s) to enable support to obtain neighbor cell SIB1 contents related to CGI reporting in Rel-17.
* From [13] Samsung:
  + No need to support extra method for providing the CORESET#0/Type0-PDCCH configuration for ANR purpose.
* From [26] Qualcomm:
  + for ANR, do not consider additional methods (compared to current NR) to signal the NCGI

#### Summary of Discussions

3 Companies expressed that there is no need to consider additional methods to support neighbor cell SIB1 reading. 2 Companies mentioned the possibility of supporting offset based neighbor cell CORESET#0 determination, similar to what was defined for Rel-16 NR-U.

#### <Moderator’s Suggestion for Discussions>

From moderator’s understanding whether offset based neighbor cell determination is possible may depend on raster design in RAN4. Therefore, based on limited discussion from companies, and potential dependency on RAN4 decision, moderator suggest de-prioritize discussion in this meeting.

#### 1st Round of Discussions

Please provide further comments on moderator’s suggestion above. If there are any other issues that require discussion on ANR and CGI reporting, please comment them here.

|  |  |
| --- | --- |
| Company | Comments |
| OPPO | As discussed in our contribution, ANR issue should be revisited after RAN4 concludes the channelization, LBT bandwidth and sync raster relationship. |
| LG Electronics | We agree with the Moderator’s suggestion, we can deprioritize the discussion on ANR issue in this meeting. |
| Ericsson | We agree that there is no need to support extra method for providing the CORESET#0/Type0-PDCCH configuration for ANR purpose.  Regarding the Rel-16 mechanism introcued for NR-U we don't think it will work for the 57 – 71 GHz band. However, we can reassess when more details are known on the channelization design. |
| Intel | Agree with Moderator’s suggestion. |
| vivo | Agree with the moderator’s suggestion. |
| ZTE, Sanechips | We agree that channelization and sync raster defined for FR2-2 may have some impact on the current supported ANR method (i.e. using MIB configuration). RAN1 can discuss if some enhancements are needed after RAN4’s work on channelization and sync raster is completed. So we support Moderator’s suggestion. |
| Nokia | Agree. |
| Apple | Agree. |

#### <Summary of 1st Round of Discussions>

Tentative Conclusion:

De-prioritize the discussions for RAN1 #106-bis-e. Proponent companies to provide further information if needed in the comment section below.

|  |  |
| --- | --- |
| Company | Further information on ANR/CGI reporting related proposal |
| DOCOMO | We agree with the tentative conclusion. |
| Intel | Agree with this Conclusion |
| ZTE, Sanechips | Agree with the tentative conclusion. |

*Further updated:*

Given the lack of time for discussion in RAN1 #106-bis-e and consensus to deprioritize the discussion for ANR/CGI reporting, suggest closing the discussion for RAN1 #106-bis-e, and continue discussion in next meeting.

**Moderator Suggestion:**

* Further discuss the following issues in RAN1 #107-e
  + potential enhancements for ANR/CGI reporting

#### == Discussion Closed for #106-bis-e ==

### 2.1.5 Various other aspects on SSB Design

* From [3] Spreadtrum:
  + SSB with 240kHz SCS can be down-prioritized.
  + Supporting initial cell selection with 480kHz SSB should be an optional UE capability separately from supporting other processing with 480/960kHz SCS.
  + The SSB-based TRS/CSI-RS validation can be supported.
* From [7] OPPO:
  + The raster step size for 120kHz and 480kHz are 3\*17.28MHz and 15\*17.28MHz, respectively, leading to a total number of raster entries 428.
* From [9] CATT:
  + Symbol #6 and symbol #13 can be reserved for beam switching. Neither PDCCH nor PDSCH can be transmitted on the reserved symbols.
  + The default TDRA table for pattern 1 in TS 38.214 can be enhanced, e,g at least {S=6 ,L=7}, {S=2，L=11} is supported.
* From [12] Nokia, NSB:
  + It is possible to apply SCSe to one part of actually transmitted SSBs and LBT procedure for other/rest of the SSBs.
  + Consider semi-static or predetermined mechanism to determine which SSBs are under SCSe and which under LBT in certain time windows.
* From [13] Samsung:
  + RAN1 clarifies that the configurable SCS for initial BWP configured by SIB1 can be 120 kHz, 480 kHz, and 960 kHz.
  + For 480 and 960 kHz, support the following 4 configurations for NR carrier RSSI measurement:
    - Configuration #0: {0, 1};
    - Configuration #1: {0, 1, …, 5};
    - Configuration #2: {0, 1, …, 8};
    - Configuration #3: {0, 1, …, 12}.



* From [20] Lenovo, Motorola Mobility:
  + For supporting NR from 52.6 GHz to 71 GHz in Rel. 17, with higher subcarrier spacings (numerologies), coverage enhancement of channels and signals used for initial access should be considered for NR beyond 52.6 GHz
  + For initial access in NR unlicensed bands between 52.6 GHz and 71 GHz, with directional LBT based channel access mechanism, indication of sensing beams can be considered during the initial access
* From [25] Convida Wireless:
  + SSB coverage enhancement should be studied for higher SCS.

#### Summary of Discussions

* Companies have provided the following issues
  + Raster design
  + Capability aspect for initial access
  + Support of SSB based TRS/CSI-RS validiation
  + TDRA table update
  + Short control signal exemption applicability to signals
  + RSSI symbol update due to new SSB design
  + Coverage enhancement
  + Sensing beam indication

#### <Moderator’s Suggestion for Discussions>

For the following issues, moderator has provided comments on whether to further discuss during this meeting.

* Raster design
  + Should be discussed in RAN4
* Capability aspect for initial access
  + Should be discussed in 8.17.2
* Support of SSB based TRS/CSI-RS validiation
  + Moderator asks the proponent company to provide further information on what needs to be considered and specified in RAN1.
* TDRA table update
  + Moderator suggest to discuss further this meeting
* Short control signal exemption applicability to signals
  + Should be discussed in 8.2.6 channel access agenda
* RSSI symbol update due to new SSB design
  + Moderator suggest to discuss further this meeting
* Coverage enhancement
  + Moderator suggest to de-prioritize this discussion as coverage enhancement was explicitly de-scoped from the WID
* Sensing beam indication
  + Moderator thinks 8.2.6 channel access agenda might be a better suited agenda for discussion

Further discuss on the following proposals.

**Issue #1)** TDRA table update

Currently, Type0-PDCCH uses default TDRA A and C for CORESET multiplexing pattern 1 and 3, respectively. Please provide further comments on whether TDRA table should be updated and if so how it should be updated.

**Issue #2)** RSSI symbol update due to new SSB design for 480 and 960 kHz

##### Proposal 1.5-1

* For 480 and 960 kHz, support the following 4 configurations for NR carrier RSSI measurement:
  + Configuration #0: {0, 1};
  + Configuration #1: {0, 1, …, 5};
  + Configuration #2: {0, 1, …, 8};
  + Configuration #3: {0, 1, …, 12}.



#### 1st Round of Discussions

Please provide further comments on the above issue #1 and #2. If there are any other issues that require discussion, please comment them here.

|  |  |
| --- | --- |
| Company | Comments |
| Qualcomm | Issue #1: For TDRA C, since the SSBs start on symbols 2 and 9, for CORESET0 of 2 symbols, we may need to account for TDRA C “S = 11” and “L = 2” values. |
| Samsung | Issue #1:   * If pattern 3 is supported for 480/960 kHz, there is expected enhancement to the TDRA C table due to different SSB locations in a slot. * For TDRA A table, we are open to the discussion on enhancement if there is a need.   Issue #2: we support Proposal 1.5-1 as the proposing company. |
| LG Electronics | Issue #1: We agree with Qualcomm and Samsung that adjustment of TDRA C can be considered to be aligned with new SSB symbol-level pattern for 480/960 kHz.  Issue #2: We do not support Proposal 1.5-1. In NR-U/LAA, the symbol location to measure RSSI irrespective of synchronization signals. To be specific, the measurement duration can be configured among 1/14/28/42/70 symbols and those values can be reused also for FR2-2. Anyway, the relevant discussion can be discussed under 8.2.6. |
| Ericsson | Issue #1  We don't think we should spend time on optimizing the TDRA table – this was a very long discussion in Rel-16.  Issue #2  We don't see the need for optimizations of RSSI measurement configuration for the 57 – 71 GHz band. |
| Intel | We are fine with Proposal 1.5-1 |
| ZTE, Sanechips | Issue #1: The motivation for enhancing TDRA A in [9] is to reserve some symbols (e.g. symbol #6 and #13) for beam switching. Since RAN4 has not reached a final conclusion for beam switching time, it is too early to say that beam switching must be realized by reserving symbols. In addition, some existing configurations (e.g. S=2, L=10) in TDRA A can support above purpose. For TDRA C, we share same views as Qualcomm.  Issue #2: We are a little confused about Proposal 1.5-1 as the discussion on Rel-16 NR-U RSSI measurement did not involve the SSB pattern. |
| Nokia | **Issue #1)**  In TDRA table A, we have rows 6 (with DMRS position 2) and 14 which would seem to align with the SSB’s at least. For TDRA table C, we think that to meet the intended purpose some update maybe needed.  **Issue #2)**  Could be down prioritized and returned later. |

#### <Summary of 1st Round of Discussions>

Issue #1) TDRA enhancements

* Enhancements to TDRA A for multiplexing pattern 1
  + Open for discussion
    - Samsung, ZTE/Sanechips (depends on beam switching time)
  + No enhancement
    - Ericsson, Nokia/NSB
* Enhancements to TDRA C for multiplexing pattern 3
  + needed for 480/960kHz SSB pattern, if supported
    - Qualcomm, Samsung, LGE, Nokia/NSB
  + No enhancement
    - Ericsson

Issue #2) RSSI symbol update

Proposal 1.5-1

* Supported: Samsung, Intel
* Not supported: LGE, [ZTE/Sanechips?]
  + RSSI for unlicensed may not need to related to SSB symbols
* Defer: Nokia/NSB

#### 2nd Round of Discussions

Further discussion on Issue #1 and #2 seems to be needed. Continue to provide comments and inputs for Issue #1 and #2 (Proposal 1.5-1).

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | We want to clarify our proposal better, since we find companies taking an opposite position misunderstand this with RSSI measurement, and has nothing related to unlicensed band operation.  What we proposed is for “NR carrier RSSI measurement”, which is a component to calculate SS-RSRQ as specified in section 5.1.3 of TS 38.215. There is a table 5.1.3-1 defining the symbols contributes to the NR carrier RSSI measurement calculation, but those symbols are determined based on the SSB starting symbol location as {2, 8} in a slot. Since we have agreed a new SSB pattern for 480 and 960 kHz in FR2, the measured symbols for NR carrier RSSI measurement should be changed accordingly. We copied the table below for information, and our proposal is to revise the ending symbol for row “1” and “3”, to be aligned with the new SSB pattern.  Table 5.1.3-1: NR Carrier RSSI measurement symbols   |  |  | | --- | --- | | **OFDM signal indication *endSymbol*** | **Symbol indexes** | | | 0 | {0,1} | | 1 | {0,1,2,..,10,11} | | 2 | {0,1,2,…, 5} | | 3 | {0,1,2,…, 7} | |
| Intel | **Issue #1)**  We are open for discussion on both TDRA A for mux pattern 1 and TDRA C for mux pattern 3. However, due to remaining initial access-related aspects of more importance, we propose to defer this discussion.  **Issue #2)**  We are fine with Proposal 1.5-1. However, if companies want to defer this discussion to have more time to think about, we are also fine. |
| ZTE, Sanechips | Except for TDRA C for multiplexing pattern 3 with SCS 480/960 kHz, we don't think other issues need to be enhanced/optimized. But TDRA C enhancements could be discussed only after RAN1 decides to support multiplexing pattern 3 with SCS 480/960 kHz, which is being discussed in section 2.1.3. |

#### <Summary of 2nd Round of Discussions>

Continue discussion on Proposal 1.5-1 and TDRA enhancements.

#### 3rd Round of Discussions

Samsung has provide further information on Proposal 1.5-1. Please comment whether is acceptable with the explanation.

Please provide further comments on TDRA enhancements that has not been made so far.

|  |  |
| --- | --- |
| Company | comments |
| Nokia | **Issue #1)**  To clarify, we think that for TDRA table C there might a need to do some adjustment for 480kHz and 960kHz to meet the intended purpose. |
| Ericsson | We think Proposal 1.5-1 is an optimization and we should focus on other higher priority topics  Discussion on TDRA enhancements should be deferred |
| ZTE, Sanechips | TDRA C enhancements can be discussed after RAN1 decides to support multiplexing pattern 3 with SCS 480/960 kHz. We think other issues do not need to be enhanced/optimized.  For RSSI measurement in Samsung’s comments, we do not find any relationship between Table 5.1.3-1 and SSB pattern for 120/240kHz SCS, so why it should be enhanced only for 480/960kHz SCS? |

#### <Summary of 3rd Round of Discussions>

Moderator suggests further discussion on the two issues.

*Further updated:*

Given the lack of time for discussion in RAN1 #106-bis-e and need for further discussions for the issues identified, moderator suggest closing this topic for discussion in RAN1 #106-bis-e.

**Moderator Suggestion:**

* Further discuss the following issues in RAN1 #107-e
  + Potential changes to symbols for RSSI measurement for 480 and 960kHz
  + Potential TDRA allocation A and C enhancements to account for supported SSB/CORESET#0/SS#0 patterns for 480/960 kHz

#### == Discussion Closed for #106-bis-e ==

## 2.2 PRACH Aspects

### 2.2.1 PRACH Sequence and Format

* From [1] Huawei/HiSilicon:
  + Additionally support L=571 for 480 kHz PRACH.
* From [2] Futurewei:
  + Do not support PRACH length L=571 for 480kHz PRACH.
* From [4] ZTE, Sanechips:
  + Support sequence length 571 for 480KHz PRACH SCS for 52.6 to 71 GHz.
* From [5] vivo:
  + Support 120KHz and 480KHz as candidate SCS of initial UL BWP.
  + Support 480KHz and 960KHz SCS in addition to 120KHz SCS for PRACH.
* From [11] Ericsson:
  + We are open to further discuss whether or not L = 571 is supported for 480 kHz.
* From [12] Nokia, NSB:
  + Support L=571 for PRACH with 480kHz.
* From [13] Mediatek:
  + Support only sequence length L=139 when PRACH SCS=480 kHz.
* From [15] Intel:
  + Support PRACH formats A1~A3, B1~B4, C0, C2 for with SCS 480 kHz, i.e., .
* From [22] LG Electronics:
  + The 120 kHz PRACH SCS with sequence lengths L=571 and L=1151 are not required for the licensed spectrum where the regulatory requirements are not defined on PSD limit.
  + PRACH with sequence length L=571 can be supported for the 480 kHz SCS in addition to L=139 for initial/non-initial access and 960 kHz SCS PRACH with L=139 is only supported for non-initial access.
* From [23] Sharp:
  + Only support L = 139 for PRACH with 480kHz and 960 kHz SSB SCS.
* From [24] Apple:
  + Support PRACH length L=571 for 480 kHz PRACH.

#### Summary of Discussions

The following are previous agreements on PRACH sequence and formats.

|  |
| --- |
| **Agreement:**   * For initial access and non-initial access use cases, support 120kHz PRACH SCS with sequence length L=571, 1151 (in addition to L=139) for PRACH Formats A1~A3, B1~B4, C0, and C2. * For non-initial access use cases,   + if 480kHz and/or 960 kHz SSB SCS is agreed to be supported, support 480 and/or 960 kHz PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively.     - FFS: support of sequence length L = 571, 1151 * FFS: Support of 480 and/or 960 kHz PRACH SCS for initial access use cases, if 480 and/or 960 kHz SSB SCS is agreed to be supported for initial access   Agreement:  Do not support PRACH length L=571, 1151 for 960kHz PRACH and at least L =1151 for 480kHz PRACH. |

* Supported sequence lengths
  + PRACH length L=571 for 480kHz
    - Support: Huawei/HiSilicon, ZTE/Sanechips, Nokia/NSB, Intel, LGE, Apple, Sharp
    - Do not support: Futurewei
* Supported subcarrier spacing for initial UL BWP
  + 120 kHz, 480 kHz: vivo

#### <Moderator’s Suggestion for Discussions>

Further discussion on following proposals.

**Proposal 2.1-1**

* Additionally support PRACH length L=571 for 480kHz

##### Proposal 2.1-2

* Support 120 kHz and 480 kHz subcarrier spacing for initial UL BWP

#### 1st Round of Discussions

Please provide further comments on the above issues (Proposal 2.1-1 and 2.1-2). Also, if there are any other issues that require discussion on PRACH sequences and formats, please comment them here.

|  |  |
| --- | --- |
| Company | Comments |
| LG Electronics | We support both Proposal 2.1-1 and Proposal 2.1-2.  Meanwhile, we would like to clarify whether proposal 2.1-2 means that 960 kHz subcarrier spacing is not supported for initial UL BWP. |
| NTT DOCOMO | We are fine with both proposals, 2.1-1 and 2.1-2. |
| OPPO | Proposal 2.1-1: not support.  Proposal 2.1-2: support. |
| Qualcomm | Proposal 2.1-2: support |
| Lenovo, Motorola Mobility | Proposal 2.1-1: support.  Proposal 2.1-2: support. |
| Interdigital | **Proposal 2.1-1**: Support the proposal.  **Proposal 2.1-2**: Support the proposal. |
| Ericsson | Proposal 2.1-1: We don't think this is strictly needed, but we okay to support it if the majority wants it.  Proposal 2.1-2: An initial UL BWP is configured on an SCell too (according to 38.331), so is 960 kHz SCS precluded on an SCell? Perhaps it should be clarified that the proposal is for PCell. |
| ETRI | We support both Proposal 2.1-1 and Proposal 2.1-2.  We also agree with LG’s comment regarding whether to support 960kHz for initial UL BWP. |
| Sharp | We are fine with both proposals. |
| Intel | Proposal 2.1-1: Support.  Proposal 2.1-2: Support.  As mentioned numerous times, our motivation for supporting Proposal 2.1-1 is to achieve at least 100 MHz for PRACH such that no transmission power penalty is applied by US regulations. |
| vivo | **Proposal 2.1-1**: Support.  **Proposal 2.1-2**: Support. |
| Huawei, HiSilicon | Proposal 2.1-1: Support  Proposal 2.1-2: Support |
| ZTE, Sanechips | Proposal 2.1-1: Support  Proposal 2.1-2: Support |
| Sony | Proposal 2.1-1: Support  Proposal 2.1-2: Support |
| Nokia | Proposal 2.1-1) We are OK with the proposal.  Proposal 2.1-2) Like noted by Ericsson, it is not clear if the intention is to preclude 960kHz configuration from PSCell and/or SCell (which should not be the case). |
| Futurewei | Proposal 2.1-1: Support  Proposal 2.1-2: Support |
| Apple | Proposal 2.1-1: Ok for us.  Proposal 2.1-2: Support. |

#### <Summary of 1st Round of Discussions>

Proposal 2.1-1

* Support: LGE, Docomo, Lenovo/Motorola Mobility, Interdigital, ETRI, Sharp, Intel, vivo, Huawei/HiSilicon, ZTE/Sanechips, Sony, Nokia/NSB, Futurewei, Apple
* Ok: Ericsson
* Not Support

Proposal 2.1-2

* Support: LGE, Docomo, Qualcomm, Lenovo/Motorola Mobility, Interdigital, Ericsson (clarify this is for PCell), ETRI, Sharp, Intel, vivo, Huawei/HiSilicon, ZTE/Sanechips, Sony, Nokia/NSB (clarify this is for PCell), Futurewei, Apple
* Not Support

#### 2nd Round of Discussions

Based on company feedback, I think we can try to agree to Proposal 2.1-1 and 2.1-2A.

##### Proposal 2.1-1

* Additionally support PRACH length L=571 for 480kHz

##### Proposal 2.1-2A

* Support 120 kHz and 480 kHz subcarrier spacing for initial UL BWP for PCell

Assuming the proposal is stable, moderator will ask for email approval of this proposal. **Please only comment if you have serious concerns of the proposal**.

|  |  |
| --- | --- |
| Company | Comments |
| Ericsson | Proposal 2.1-1: If the majority supports, we are okay with it  Proposal 2.1-2: Support |
| ZTE, Sanechips | Proposal 2.1-1: Support.  Proposal 2.1-2A: Is the 960KHz supported in SCell? We don’t think this is needed. but we okay to support it if the majority wants it. |

#### <Summary of 2nd Round of Discussions>

Moderator suggest asking for email approval for the following proposals

* Proposal 2.1-1 and 2.1.2-A.

With the above being approved and no further comments, discussion on this topic will be closed.

**Moderator Suggestion:**

* Agree to following proposal
  + Proposal 2.1-1
  + Proposal 2.1.2-A

#### == Discussion Closed for #106-bis-e ==

### 2.2.2 RACH Occasion Resources

* From [1] Huawei/HiSilicon:
  + For 480 kHz and 960 kHz PRACH, support one gap symbol between consecutive ROs in time domain at least for Formats A1, B1, and A1/B1.
  + For PRACH format A1, B1 and A1/B1, the first symbols for each RO in a reference slot can be derived using equation (2) if a gap symbol between consecutive ROs is introduced. The same triples of in Table 6.3.3.2-4 of 38.211 are reused.
    - Note: Equation (2) guarantees that no RO straddles between slots and .

(2)

* From [2] Futurewei:
  + If when the LBT is required prior to RACH transmissions there is no necessary to add extra gaps between successive RO in the same PRACH slot.
  + For 480kHz and 960 kHz SCS reuse Table 6.3.3.2-4: Random access configurations for FR2 and unpaired spectrum, where the slot index is scaled up by 4 and respectively by 8 as per prior agreement. For 120 kHz SCS use the Table 6.3.3.2-4 as is.
  + Update the table 8.1-2 to indicate the necessary Ngap for higher SCS.
* From [4] ZTE, Sanechips:
  + For 480kHz and 960kHz, it is unnecessary to introduce gap between ROs for LBT and/or beam switching.
  + For 480kHz and 960kHz, it is unnecessary to allow for additional values if the maximum that can be configured for the number of FD ROs is less than 8.
* From [5] vivo:
  + The gaps between the consecutive ROs should be supported for LBT and/or beam switching.
  + The ROs for a given PRACH configuration spanned more than one PRACH slot should not be supported.
* From [6] Fujitsu:
  + Gaps between time-domain ROs in a slot are needed not only for LBT/beam switching, but also to avoid strong inter-RO interference due to power ramping up and rolling down.
  + For FR2-2, support gaps between time-domain ROs in a slot. The gaps can be enabled and configured by RRC signaling.
* From [9] CATT:
  + The reference slot duration corresponds to 60 kHz SCS. PRACH slot index corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.
  + For 480/960 kHz PRACH slots configuration, higher PRACH slot density or higher RO density in time domain can be supported to compensate the impact from MSGS –FDM decreasing and LBT/beam switching GAP.
    - For 480KHz SCS, PRACH slot density can be 2 or 4 times comparing to than 120KHz SCS
    - For 960KHz SCS, PRACH slot density can be 4 times comparing to 120KHz SCS
  + If gap for LBT or beam switching is needed before UE transmit a msg-1, one RO can be disabled by RRC in a 60 KHz reference slot, and UE can perform LBT or beam switching on the disable RO.
* From [10] Xiaomi:
  + Inconsecutive RO time domain configuration should be supported at least for 480 and 960 kHz case.
* From [11] Ericsson:
  + Do not support additional values if the maximum number of configured FD ROs is less than 8.
  + Do not specify gaps between consecutive PRACH occasions. If needed, gaps to account for gNB receive beam switching time can be created purely by gNB implementation based on the gNB's own knowledge of the switching time.
  + There is no need to further consider additional values for the case when a PRACH slot cannot contain all time domain PRACH occasions
  + Support the following values of
    - When number of PRACH slots in a reference slot is 1,
      * for 480kHz and for 960kHz PRACH
    - When the number of PRACH slots in a reference slot is 2,
      * for 480kHz and for 960kHz PRACH
* From [12] Nokia, NSB:
  + Do not introduce LBT gap between consecutive ROs.
  + Re-use the FR2-1 PRACH configuration for 120kHz sub-carrier spacing.
* From [13] Samsung:
  + Support non-consecutive RO configuration to alleviate the RACH LBT failure.
  + Postpone the decision of additional values until the gap generation method has been determined.
* From [14] Mediatek:
  + RAN 1 to discuss the value of for NR operation to 52.6-71 GHz.
* From [15] Intel:
  + If gaps between consecutive ROs are necessary, gNB is able to configure PRACH with a large number of repetitions where some extra repetitions may be skipped and, thus, serve as gaps between ROs.
* From [16] NTT Docomo:
  + For RO configuration for PRACH with 480/960 kHz SCS, no need to consider either LBT or beam switching gap for RO design in 52.6 – 71 GHz
* From [21] Interdigital:
  + Do not support gap insertion between consecutive ROs in time domain as it causes inefficiency and application ambiguity.
  + Consider the enhancements to RO configuration without inserting gaps in between consecutive ROs.
  + For 52.6 – 71 GHz with 120kHz, 480kHz, and 960kHz PRACH, inserting gaps to achieve non-consecutive RACH occasions is not supported.
  + For 52.6 – 71 GHz, support sharing and extending the COT for LBT-free PRACH transmission in the consecutive ROs.
* From [22] LG Electronics:
  + When LBT is used to transmit the PRACH preamble, consider to insert CCA gap between adjacent RACH occasions in time domain (e.g. X usec or Y symbol) to avoid inter-UE LBT blocking due to the propagation delay of PRACH transmitted in an earlier RO.
  + The starting PRACH slot index for 480/960 kHz is given by:
    - when the number of PRACH slots in a reference slot is 1,
      * for 480 kHz and for 960 kHz PRACH
    - when the number of PRACH slots in a reference slot is 2,
      * for 480 kHz and for 960 kHz PRACH
    - where X is the number of additional slots to provide a gap between all of consecutive RACH occasions corresponding to a PRACH configuration index in Table 6.3.3.2-4 of TS 38.211, based on the configured number of symbols for the gap required for LBT and/or beam switching.
      * Note: If a PRACH slot cannot contain all time domain PRACH occasions corresponding to a PRACH configuration index in Table 6.3.3.2-4 of TS 38.211 including gap(s) between consecutive PRACH occasions to account for LBT and/or beam switching, then X=0.
* From [23] Sharp:
  + Gaps between consecutive ROs should be supported at least for LBT purposes.
  + A starting symbol index of a PRACH occasion is given by If non-zero duration gaps are configured between consecutive ROs and the ROs would span multiple PRACH slots, for 480 and 960 kHz SCS, respectively. Otherwise, for 480 and 960 kHz SCS, respectively.
* From [24] Apple:
  + Maximum 4 PRACH ROs can be configured for 120kHz SCS with .
  + Maximum 2 PRACH ROs can be configured for 120kHz SCS with .
  + If a gap between consecutive PRACH occasions is not configured or not supported,
    - When number of PRACH slots in a reference slot is 1, for 480kHz and for 960kHz PRACH.
    - When number of PRACH slots in a reference slot is 2, for 480kHz and for 960kHz PRACH.
  + Pending confirmation from RAN4 on 59ns beam switching time, a SIB1-configurable gap between time-domain ROs cand be considered.
  + Keep the same values if the maximum that can be configured for the number of FD RO’s is less than 8
* From [26] Qualcomm:
  + a maximum of 4 and 2 FD multiplexed ROs for SCS = 120 kHz and sequence length = 571 and 1151, respectively
  + for SCS = 120 kHz, if the maximum number of FD ROs are reduced, consider ways to increase the TD ROs (to maintain the same capacity) with minimal specification impact
  + for higher RACH SCS (480 and 960 kHz), consider including a gap between ROs which can be symbol-level (for gNB beam switching delay) or RO-level (for LBT)
  + for 480 kHz and 960 kHz PRACH:
    - ROs for a given PRACH configuration may need extra PRACH slot if gaps between consecutive ROs are supported for LBT and/or beam switching purposes
      * Option A: TDM "RO + gap" until all required number of ROs are satisfied (even if they extend to an extra slot)
      * Option B: split the number of ROs as evenly as possible among multiple slots such that the pattern is the same for all slots (distribute the "RO + gap" among slots)
    - For the extra slots (if needed) consider the following 2 alternatives:
      * Alt1: the extra slots are added such that the distribution of the slots is even within the RACH reference slot
      * Alt2: the extra slots are added next to the original slots

Table

Description automatically generated

#### Summary of Discussions

The following are previous agreements on PRACH sequence and formats.

|  |
| --- |
| Agreement:  For 480 and 960kHz PRACH:   * At least the same RO density in time domain (i.e. number of specified RO per reference slot according the PRACH configuration index) as for 120kHz PRACH in FR2 is supported   + FFS: Support gap between consecutive ROs in time domain and the details to derive the gap   Agreement:  For 480 and 960kHz PRACH,   * When a PRACH slot can contain all time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching,   + and when number of PRACH slots in a reference slot is 1,     - for 480kHz and for 960kHz PRACH   + and when the number of PRACH slots in a reference slot is 2,     - for 480kHz and for 960kHz PRACH * FFS: values, when a PRACH slot cannot contain all time domain PRACH occasions~~,~~ corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching. * FFS: whether to allow for additional values if the maximum that can be configured for the number of FD RO’s is less than 8 (due to BW limitation) |

The following is a summary of company views.

* Gap between consecutive ROs
  + Support: Huawei/HiSilicon (only for Formats A1, B1, A1/B1), vivo, Fujitsu, [CATT], [Xiaomi], Samsung, LGE, Sharp, Qualcomm
  + Do not support: ZTE/Sanechips, [Futurewei], Ericsson, Intel, Nokia/NSB, NTT Docomo, Interdigital
* Do not support ROs that span more than one PRACH slot
  + vivo
* RO disabling RRC configuration to provide gap for LBT or beam switching
  + CATT
* Maximum 4 PRACH ROs can be configured for 120kHz SCS with . Maximum 2 PRACH ROs can be configured for 120kHz SCS with .
  + Apple, Qualcomm
* Do not support additional values if the maximum number of configured FD ROs is less than 8.
  + Ericsson, ZTE/Sanechips, Apple
* values
  + If number of PRACH slots per reference slot is 1,
    - Confirm WA, for 480kHz and for 960kHz PRACH
      * Ericsson, Apple
    - for 480 kHz and for 960 kHz PRACH
      * LGE
    - If gap between RO is configured, for 480kHz and for 960kHz PRACH
      * Sharp
  + If number of PRACH slots per reference slot is 2,
    - Confirm WA, for 480kHz and for 960kHz PRACH
      * Ericsson, Apple
    - for 480 kHz and for 960 kHz PRACH
      * LGE

#### <Moderator’s Suggestion for Discussions>

Whether or not gap is supported between consecutive RO is the most controversial and critical issue that seems to impact other discussion for RO design. Suggest discussing and conclude on this aspect first. Please further discuss on the following proposal.

##### Proposal 2.2-1

* Support gap between consecutive ROs for 480kHz and 960kHz
  + FFS: whether supporting gaps is fixed in specification or RRC configured by gNB

##### Proposal 2.2-1B (previously as 2.2-2)

* Do not support gap between consecutive ROs for 480kHz and 960kHz

#### 1st Round of Discussions

Please provide further comments on the above issues (Proposal 2.1-1 or 2.1-2). Also, if there are any other issues that require discussion on PRACH ROs, please comment them here.

|  |  |
| --- | --- |
| Company | Comments |
| LG Electronics | We support Proposal 2.1-1 and the LBT gap is needed between the consecutive ROs to avoid inter-UE LBT blocking due to the propagation delay of PRACH transmitted in an earlier RO. The supporting gaps can be RRC configured by gNB since the required gap length may vary depending on whether the gap between ROs is for beam switching or LBT, and two or more 480/960 kHz PRACH slots may be required to maintain the same RO density for the gap for LBT. |
| NTT DOCOMO | As captured by FL, we support Proposal 2.1-2. We still think the necessity of gap between Ros would be questionable. |
| OPPO | We support gap between consecutive ROs for 480kHz and 960kHz. |
| Qualcomm | We support Proposal 2.1-1 |
| Lenovo, Motorola Mobility | We support Proposal 2.1-1. |
| Interdigital | **Proposal 2.1-2**: Support the proposal. As such, no gap is required between consecutive ROs. |
| Ericsson | Proposal 2.1-1: **We do not support gaps between consecutive ROs**.  For LBT, this was not needed in Rel-16, and it is even less motivated in the 57 – 71 GHz band where potential LBT blocking would be a virtually non-existent event considering that extensive system simulations have shown that LBT failure is rare. Moreover, in most regions LBT is not neede for PRACH.  For gNB Rx beam switching, if the gNB wants to create a gap due to it's own (known) beam switch time it can do so purely by gNB implementation as we discuss in our contribution. The gNB can simply drop several samples at the beginning of the PRACH reception during the time that it switches its beam.  Proposal 2.1-2. We support. |
| ETRI | We support Proposal 2.1-1. |
| Sharp | We support Proposal 2.1-1. |
| Intel | Proposal 2.1-1: Do not support  Proposal 2.1-2: Support  In both proposals there is no differentiation between types of the gaps. Therefore, we assume that both LBT and beam switching gaps are discussed.  We don’t see strong need in LBT gaps in PRACH as UE chooses one RO for RACH preamble transmission.  The beam switching gaps may be needed. However, it happens that gNB is able to configure a RACH preamble format with a large number of repetitions and use some of the extra repetitions for beam switching. This would effectively serve as a gap. |
| vivo | We support Proposal 2.1-1 to have LBT gap to avoid inter-UE blocking as mentioned by LG. |
| Huawei, HiSilicon | We think gap is required to accommodate beam switching latency especially for PRACH formats with smaller CP, that is A1, B1, A1/B1. We support Proposal 2.1-1 with the following modification: Proposal 2.1-1 – alternative to 2.1-2 (Modified)  * Support gap for between consecutive ROs for 480kHz and 960kHz   + FFS: whether supporting gaps is fixed in specification or RRC configured by gNB   + FFS: Whether gaps are supported for all PRACH formats or only for formats with smaller CP (eg, A1, B1, A1/B1) |
| Fujitsu | Besides for LBT/beam switching, we think the gaps are also to avoid strong inter-RO interference due to power ramping up and rolling down. The inter-RO interference issue is as shown in the example below. Since the duration of power ramping/rolling down is 5us while the symbol length for 960kHz is nearly 1us, the PRACH transmission using RO2 would be severely interfered by the power rolling down and power ramping up for PRACH transmissions using RO1 and RO3 respectively.    And considering different gap length needed for different purpose, the gaps should be configurable. |
| ZTE, Sanechips | We support Proposal 2.1-2.LBT Gap has been discussed in Rel-16 NR-U to resolve resource collision issue but no consensus. wherein, omni-directional beam is used for sensing/transmission in Rel-16 NR-U and operation frequency band is below 7GHz. But in Rel-17 above 52.6GHz, directional narrow beam is used for transmission and reception, this beam characteristic naturally helps to alleviate the issue of the resource collision. Therefore, there is no strong need to introduce the LBT gap for 480KHz and 960KHz.For beam switching gap, the potential issue is gNB RX beam switching only. TR 38.817-02 has also captured simulation results that to prevent degradation of system performance, switching time must be less than 80% of the CP length. For 960 kHz SCS NCP, this results in approximately 59 ns time window. Additionally, as shown in the Table 6.3.3.1-2 of TS 38.211, the PRACH CP is at least 1.5 times longer than the NCP. So it is also unnecessary to introduce the beam switching time between ROs. |
| Nokia | We don’t support gaps between ROs thus we would support Proposal 2.1-2) |
| Mediatek | We support Proposal 2.1-2 since gaps between consecutive ROs are not necessary. |
| Futurewei | Support Proposal 2.1-2 – alternative to 2.1-1, we do not think that gaps are needed |

#### <Summary of 1st Round of Discussions>

Proposal 2.1-1

* LGE (configurable), OPPO, Qualcomm, Lenovo/Motorola Mobility, ETRI, Sharp, vivo, Huawei/HiSilicon (for some formats), Fujitsu
  + PRACH transmit power ramp up and ramp down can effect LBT of other UEs
  + Gap needed to absorb inter-UE block from differences in propagation delay

Proposal 2.1-2

* Docomo, Interdigital, Ericsson, Intel, ZTE/Sanechips, Nokia/NSB, Mediatek, Futurewei
  + Beam switching gap can be created by the gNB side (in specification transparent manner) with more PRACH repetitions
  + Likelihood of LBT failure is low for simulated deployment scenarios

#### 2nd Round of Discussions

Companies view are split on this (11 vs 10). One camp of companies who think gap is needed, and other camp of companies do not think it is necessary.

We do need conclude and finalize this issue in this meeting. For this issue, moderator would like to suggest the group to focus on supporting the gap (with possibility of configuring no gap) unless there are major technical problems of having a gap defined. From the comments, while beam switching gap could be absorbed by configuring larger repetition formats, empty gaps are needed to combat LBT issues. At least one companies commented that they do not think LBT failure is a likely event to occur (at least based on the simulated deployment cases), but other companies think it is something that the specifications should provision for. If we allow support for no gap, at least this allows companies who do not think gap is needed for gNBs to operate without an gap. For the UEs, there should not be a big difference whether gap exist or not, as long as symbol and slots are well defined.

As such please provide further comments on the following proposal.

##### Proposal 2.2-1A

* Support gap between consecutive ROs for 480kHz and 960kHz
  + ~~FFS: whether supporting gaps is fixed in specification or RRC configured by gNB~~
  + gNB may configure the gap between ROs, including no gap configuration
  + FFS: Whether gaps are supported for all PRACH formats or only for formats with smaller CP (eg, A1, B1, A1/B1)

Based on proposals made, I’ve put together proposal for determining the slot and symbol locations for the ROs. Please check if this is acceptable (if Proposal 2.1-1A is ok).

##### Proposal 2.2-2

* If gap is supported between consecutive ROs for 480kHz and 960kHz,
  + Gap can be configured by gNB
  + The first symbols for each RO in a reference slot can be derived using following equation if a gap symbol between consecutive ROs is introduced. The same triples of in Table 6.3.3.2-4 of 38.211 are reused.
  + starting PRACH slot index for 480/960 kHz is given by:
    - when the number of PRACH slots in a reference slot is 1,
      * for 480 kHz and for 960 kHz PRACH
    - when the number of PRACH slots in a reference slot is 2,
      * for 480 kHz and for 960 kHz PRACH
    - where X is smallest integer value that satisfies
    - is set to configure no gap between ROs
  + FFS: supported value(s) of (other than 0)
  + FFS: Whether gaps are supported for all PRACH formats or only for formats with smaller CP (eg, A1, B1, A1/B1)

Added based on Qualcomm comments

##### Proposal 2.2-2A

* If gap is supported between consecutive ROs for 480kHz and 960kHz,
  + Gap can be configured by gNB
  + The first symbols for each RO in a reference slot can be derived using following equation if a gap symbol between consecutive ROs is introduced. The same triples of in Table 6.3.3.2-4 of 38.211 are reused.

    - *(for example)*
  + starting PRACH slot index for 480/960 kHz is given by:
    - when the number of PRACH slots in a reference slot is 1,
      * for 480 kHz and for 960 kHz PRACH
    - when the number of PRACH slots in a reference slot is 2,
      * for 480 kHz and for 960 kHz PRACH
    - where X is smallest integer value that satisfies
    - is set to configure no gap between ROs
  + FFS: supported value(s) of (other than 0)
  + FFS: Whether gaps are supported for all PRACH formats or only for formats with smaller CP (eg, A1, B1, A1/B1)

##### Proposal 2.2-2B

* Support gap between consecutive ROs for 480kHz and 960kHz
  + ~~FFS: whether supporting gaps is fixed in specification or RRC configured by gNB~~
  + gNB may configure the gap between ROs, including no gap configuration, the detailed configuration method is down select from following:
    - explicit indication, e.g., by explicit bit field or parameter to configure gap value;
    - implicit indication, e.g., by indication of RO to be used, like odd, even number of RO as similar in PRACH mask indication.
  + FFS: Whether gaps are supported for all PRACH formats or only for formats with smaller CP (eg, A1, B1, A1/B1)

Added by LG comments

##### Proposal 2.2-2C

* If gap is supported between consecutive ROs for 480kHz and 960kHz,
  + Gap can be configured by gNB
  + The first symbols for each RO in a reference slot can be derived using following equation if a gap symbol between consecutive ROs is introduced. The same triples of in Table 6.3.3.2-4 of 38.211 are reused.

    - *~~(for example)~~*
  + starting PRACH slot index for 480/960 kHz is given by:
    - when the number of PRACH slots in a reference slot is 1,
      * for 480 kHz and for 960 kHz PRACH
    - when the number of PRACH slots in a reference slot is 2,
      * for 480 kHz and for 960 kHz PRACH
    - ~~where X is smallest integer value that satisfies~~
    - is set to configure no gap between ROs
  + FFS: supported value(s) of (other than 0)
  + FFS: Whether gaps are supported for all PRACH formats or only for formats with smaller CP (eg, A1, B1, A1/B1)

Please provide comments on the proposals.

|  |  |
| --- | --- |
| Company | Comments |
| vivo | Proposal 2.2-1A: Support  Proposal 2.2-2: We agree the principle here but the details need more discussion. However, if following such way, RO may span multiple PRACH slots, which should be avoided. |
| DOCOMO | For Proposal 2.2-1A, we still do not support the introduction of gap between Ros. Why something not supported in Rel-16 NR-U (while extensively discussed) needs to be supported in NR-U in 52.6-71GHz is not clear, especially assuming beam-based operation in this FR. Furthermore, if we consider such gap, gap length should be equal to (or longer than) LBT duration. Are the proponents assuming quite small duration of cat-2 LBT will be introduced? Otherwise, we have to define more number of PRACH slots for larger SCSs to keep the same RO density, which causes large specification impacts. |
| Intel | Do not support neither Proposal 2.2-1A nor Proposal 2.2-2.  Another issue with gaps between consecutive ROs is that the starting PRACH slot changes in case of gaps introduced. For example, instead of for 480 kHz and for 960 kHz PRACH, the starting slots would be for 480 kHz and for 960 kHz PRACH. This may cause overlapping with slots carrying SSBs as according to current proposals, non-consecutive SSB slots are introduced assuming only the original starting PRACH slots (i.e., for 480 kHz and for 960 kHz PRACH) to avoid overlapping. |
| Interdigital | **Proposal 2.2-1A and Proposal 2.2-2.** We do not support the proposals. No gap is required between the consecutive ROs. As for the switching delay, the PRACH allocations could be grouped based on the SSB beams, so that the PRACH corresponding to one of the SSB beams group could be transmitted while the beam switching corresponding to the other SSB beams group is taking place. As for the LBT, the MCOT could be extended to enable LBT-free PRACH transmission in consecutive ROs within the PRACH slot. |
| Qualcomm | Proposal 2.2-1A: fine with the proposal  Proposal 2.2-2: fine with the principle, but details may be discussed. For example, the current formulation yields ROs not starting from the beginning of the previous slot (the 1st RO starting symbol is not aligned to the slot boundary). *This may yield un-necessary larger number of slots to be needed*. An alternative example (which guarantees slot alignment for the starting of the 1st symbol):   * (for example)   Example for    This design accounts for the extra slot in the immediate previous symbols.  To allow for PRACH load balancing within a reference slot, we can consider another design option where the extra slots are distributed within the reference slot. |
| Lenovo, Motorola Mobility | We support Proposal 2.2-1A and agree with vivo and Qualcomm that Proposal 2.2-2 needs further discussion |
| Moderator | Added proposal based on comments from Qualcomm.  Please continue to provide inputs and comments. |
| Sharp | Proposal 2.2-1: Support.  Proposal 2.2-2: Support in general and open to discussions on details. |
| Samsung | Some concerns for the gap is that the RO after introducing the gap will span over 2 slots. This can be avoided by having the gap indication, e.g., gNB can configure only a certain number of RO, the odd or even number RO are used, the not used RO is used as gap. Thus, the gap is configured and no RO postpone is needed so no RO will span over slot anyway.  We support first proposal by modification:   * Support gap between consecutive ROs for 480kHz and 960kHz   + ~~FFS: whether supporting gaps is fixed in specification or RRC configured by gNB~~   + gNB may configure the gap between ROs, including no gap configuration, the detailed configuration method is down select from following:     - explicit indication, e.g., by explicit bit field or parameter to configure gap value;     - implicit indication, e.g., by indication of RO to be used, like odd, even number of RO as similar in PRACH mask indication.   + FFS: Whether gaps are supported for all PRACH formats or only for formats with smaller CP (eg, A1, B1, A1/B1)   The second proposal could be on hold. Because if implicit one is used, the determination of the gap is quite simple and no need UE to further calculation. |
| Ericsson | Do not support neither Proposal 2.2-1A nor Proposal 2.2-2.  Regarding potential gap for LBT  Gaps were extensively discussed in Rel-16 for 5/6 GHz where LBT is actually useful, and such gaps were not specified. The arguments were that occasional LBT blocking is not catastrophic to system operation. The worst that can happen is that the UE tries again with another preamble transmission. The chances of being blocked repeatedly are low since the gNB will hear the preamble from a blocking user, thus removing the blocker.  In contrast, for beam based operation in 60 GHz, LBT failure is a much more rare (and often non-existent) event. Hence optimizing for LBT failure is even less motivated than Rel-16.  Agree with DOCOMO's comments about specification impact regarding duration of gap with respect to LBT duration  Regarding gaps for gNB Rx beam switching  As discussed in our contribution, if the motivation for gaps is for gNBs with longer Rx beam switching times, it is not needed to specify gaps. They can be created simply by gNB implementation in a spec-transparent way. The UE can simply omit Rx samples during its (known) Rx beam switching duration. Since all PRACH formats contain repetitions and one repetition serves as the CP for the next, dropping samples is not problematic    In summary, gaps are not motivated for LBT, and they are not needed for gNB Rx beam switching. We do not believe the specification impact and potentially long discussion time is worth it for a weakly motivated feature. |
| ZTE, Sanechips | As the moderator said, we do need conclude and finalize this issue in this meeting. If this issue can not conclude in the meeting, we do not have time to consider the related issue, e.g.:RA-RNTI calculation.  It is unnecessary to introduce both LBT gap and beam switching gap in above 52.GHz for 480KHz and 960KHz as we explained in the above discussion..  If the gap is added, discussing how to configure gap is quite time-consuming.As shown in proposal 2.2-2, the different company has different opinions, and it quiet diverse. |
| CATT | We don’t support introduction of gap therefore not supporting both proposals |

#### <Summary of 2nd Round of Discussions>

##### Issue #1) Gap or no Gap between ROs

**Proposal 2.2-1**

* Support gap between consecutive ROs for 480kHz and 960kHz
  + FFS: whether supporting gaps is fixed in specification or RRC configured by gNB

**Proposal 2.2-1A**

* Support gap between consecutive ROs for 480kHz and 960kHz
  + ~~FFS: whether supporting gaps is fixed in specification or RRC configured by gNB~~
  + gNB may configure the gap between ROs, including no gap configuration
  + FFS: Whether gaps are supported for all PRACH formats or only for formats with smaller CP (eg, A1, B1, A1/B1)

**Proposal 2.2-2**

* Do not support gap between consecutive ROs for 480kHz and 960kHz

Recap of summary of from 1st round discussion.

Proposal 2.1-1 (introduce gap)

* LGE (configurable), OPPO, Qualcomm, Lenovo/Motorola Mobility, ETRI, Sharp, vivo, Huawei/HiSilicon (for some formats), Fujitsu
  + PRACH transmit power ramp up and ramp down can effect LBT of other UEs
  + Gap needed to absorb inter-UE block from differences in propagation delay

Proposal 2.1-2 (no gap)

* Docomo, Interdigital, Ericsson, Intel, ZTE/Sanechips, Nokia/NSB, Mediatek, Futurewei,CATT
  + Beam switching gap can be created by the gNB side (in specification transparent manner) with more PRACH repetitions
  + Likelihood of LBT failure is low for simulated deployment scenarios due to use of narrow beams
  + In case LBT fails, UE may try transmit at later time, therefore occasional LBT blocking is not catastrophic

Proposal 2.2-1A (introduce gap with configurability)

* Support: vivo, Qualcomm, Lenovo/Motorola Mobility, Sharp
* Not support: Docomo, Intel, Interdigital, Ericsson

##### Issue #2) If gap supported, details of supporting gap

Proposal 2.2-2 (details of supporting gap)

* Support
* Agree in principle further discussion needed: vivo, Qualcomm, Lenovo/Motorola Mobility, Sharp
* Not support: Intel, Interdigital, Ericsson

Proposal 2.2-2A (details of supporting gap)

* Support: Qualcomm

Proposal 2.2-2B (details of supporting gap)

* Support: Samsung

#### 3rd Round of Discussions

Please provide comments on Proposals on RO gaps. As suggested by Chairman, moderator will assume with the lack of agreement RAN1 will continue to develop specification such that RO without any gap need to be complete.

Also provide comments if Proposal 2.2-2, 2.2-A, or 2.2-2B can resolve some of the concerns on supporting gap between RO.

Other alternatives could be restricting the support of gaps for small repetition PRACH formats, and/or restricting the support of gaps for PRACH format with lower overall RO density (for example, PRACH configuration 0, where RO is mapped every 160msec). Please provide comments on what companies are willing to accept as compromise, and please be trying to take the spirit of compromise seriously. Not agreeing to anything in the end only hurts the industry and impacts successful completion of the WID. This is especially more important since it is unlikely 60 GHz will have any enhancement WI for release 18. RAN1 does not have the luxury to enhance and revisit in later releases, once wrong choices have been made.

|  |  |
| --- | --- |
| Company | comments |
| DOCOMO | We still do not think having gap is justified enough. If it is only for the limited PRACH formats and/or RO configuration with lower RO density and/or etc, why don’t we use the other PRACH formats and/or RO configurations instead of specifying gap? NW operation can avoid all the issues raised by the proponents basically. |
| Interdigital | We believe no gap is required between consecutive ROs and other means can be adopted to resolve the possible issues. |
| Qualcomm | We are fine with the FL proposal of restricting the support of gaps for PRACH format with lower overall RO density |
| Intel | Issue #1)  We are still not convinced that the gaps are absolutely needed between the consecutive ROs.  Regarding LBT gaps, the necessity was not acknowledged even in Rel-16.  Regarding beam switching gaps or UL blocking issue, etc., the current PRACH configuration table, which is reused for 480 kHz/960 kHz, is flexible enough to address all the mentioned issues.  Issue #2)  For the sake of compromise, we could agree only on configurable *beam switching* gaps (e.g., at most 1 symbol between the consecutive ROs) if most of the companies agree to have such gaps. But this should be applicable only to PRACH slots containing *all* configured ROs together *with* the gaps between the ROs, e.g., there is no spill over the PRACH slot boundary. |
| Huawei, HiSilicon | **Issue 1:**  We support gap for shorter repetition formats A1, B1, A1/B1. However, at this stage, we think that the decision should be between A) Gap is supported for at least some Formats and by specification or configuration; and B) No Gap is supported under any condition.  As such, we suggest to merge back Proposals 2.2-1 and 2.2-1A to the following:  **Proposal 2.2-1B:**   * Support gap between consecutive ROs for 480kHz and 960kHz   + FFS: whether supporting gaps is fixed in specification or RRC configured by gNB   + FFS: Whether gaps are supported for all PRACH formats or only for formats with smaller CP (eg, A1, B1, A1/B1)   In any case, we cannot support Proposal 2.2-2 (no Gap).  **Issue 2:**  Regarding Proposal 2.2-2, we think that it is mathematically accurate and, in that sense, we are supportive of it. However, if X=1, it seems that UE may not be able to derive this only from RAR and some indication (1 bit in DCI) may be required. These details can be sort out in the next meeting. |
| Moderator | Added Proposal 2.2-1C based on Huawei/HiSilicon’s proposal.  Again, I urge companies to provide some suggestions on how potential compromise can be made among companies.  Continue to provide comments. I will update the summary as companies provide more inputs. Summary below are tentative version. |
| Ericsson | **Issue #1**  We still do not support gaps as they are completely unjustified. As we commented previously, gaps for gNB beam switching can be created completely by gNB implementation. Gaps for LBT are not needed at all in the 60 GHz band – they are even less motivated than in the 5/6 GHz band where the motivation was weak to start with. The worst that can happen on the (extremely rare) occurrence that LBT blocking happens is that the UE will transmit a preamble again. We should not be optimizing for such rare scenarios.  We don't think Proposal 2.2-1C is needed. The CP duration is irrelevant. Since all PRACH formats are based on multiple repetitions, one repetition (the whole repetition) creates a CP for the previous one.  Agree with moderator that if no gaps are agreed, we have a working system and there is nothing stopping us moving ahead to specification with the existing agreements.  **Issue #2**  As we commented above, the gNB can create a gap simply by implementation by dropping Rx samples during the beam switching time (if needed). |
| LG Electronics | For Issue #1, we support Proposal 2.2-1 and 2.2-1A to provide a gap to account for the beam switching and/or LBT. It is noted that no gap configuration can be configured at any time when the gap between ROs is not necessary since it is always managed by gNB control. If it is not acceptable to the opposition companies, we can compromise to only one symbol gap between ROs. We are also fine with Proposal 2.2-2C which is proposed by Huawei.  For Issue #2, Proposal 2.2-2A is preferred to avoid unnecessarily larger number of slots to be needed. In addition, the formula to calculate the value of X should be modified as .  Therefore, we suggest to delete the yellow highlights part in Proposal 2.2-A as below:  Proposal 2.2-2A   * If gap is supported between consecutive ROs for 480kHz and 960kHz,   + Gap can be configured by gNB   + The first symbols for each RO in a reference slot can be derived using following equation if a gap symbol between consecutive ROs is introduced. The same triples of in Table 6.3.3.2-4 of 38.211 are reused.      - *~~(for example)~~*   + starting PRACH slot index for 480/960 kHz is given by:     - when the number of PRACH slots in a reference slot is 1,       * for 480 kHz and for 960 kHz PRACH     - when the number of PRACH slots in a reference slot is 2,       * for 480 kHz and for 960 kHz PRACH     - ~~where X is smallest integer value that satisfies~~     - is set to configure no gap between ROs   + FFS: supported value(s) of (other than 0)   FFS: Whether gaps are supported for all PRACH formats or only for formats with smaller CP (eg, A1, B1, A1/B1) |
| Huawei, HiSilicon | We think there is some mistake in numbering the proposals. There are two very different proposals with the same number 2.2-2 and it may have created some confusion: Proposal 2.2-2  * If gap is supported between consecutive ROs for 480kHz and 960kHz,   + Gap can be configured by gNB   + The first symbols for each RO in a reference slot can be derived using following equation if a gap symbol between consecutive ROs is introduced. The same triples of in Table 6.3.3.2-4 of 38.211 are reused.   + starting PRACH slot index for 480/960 kHz is given by:     - when the number of PRACH slots in a reference slot is 1,       * for 480 kHz and for 960 kHz PRACH     - when the number of PRACH slots in a reference slot is 2,       * for 480 kHz and for 960 kHz PRACH     - where X is smallest integer value that satisfies     - is set to configure no gap between ROs   + FFS: supported value(s) of (other than 0)   + FFS: Whether gaps are supported for all PRACH formats or only for formats with smaller CP (eg, A1, B1, A1/B1)   **Proposal 2.2-2**   * Do not support gap between consecutive ROs for 480kHz and 960kHz   We support the first Proposal 2.2-2 on the details of ROs when gap is support ed and do not the second Proposal 2.2-2.  Also, our compromise proposal is as follows (has two FFSs): Proposal 2.2-1C  * Support gap between consecutive ROs for 480kHz and 960kHz   + ~~FFS: whether supporting gaps is fixed in specification or RRC configured by gNB~~   + FFS: gNB may configure the gap between ROs, including no gap configuration   + FFS: Whether gaps are supported for all PRACH formats or only for formats with smaller CP (eg, A1, B1, A1/B1) |
| Moderator | Apologizes for the duplicate proposal numbering. I’ve changed the first 2.2-2 regarding gap to 2.2-1B. Proposal 2.2-2 will be about the details of supporting gap (slot, symbol equations and such).  Added Proposal 2.2-1D based on updated Huawei’s comments.  Added Proposal 2.2-2C based on LGE’s comments. |
| ZTE, Sanechips | For **Issue #1**:  Agree with moderator that if no gap introduced, there is no additional spec impact and the discussion can be ended in the meeting as the moderator’s expectation.  For the beam switching time, we have the same view as Ericsson.  For **Issue #2**:  We have the same view as Ericsson. |
| Nokia (3rd round) | **Issue #1:**We still don’t see the support of gaps necessary.  **Issue #2:** As pointed by Ericsson, it should be possible for gNB, to omit samples of the gap from received preamble. |
| Mediatek | **Issue #1:** We don’t see the necessity of the gaps for consecutive ROs  **Issue #2:** As gaps can be generated by implementation, we don’t need to explicitly specify the gaps. |

#### <Summary of 3rd Round of Discussions>

##### Issue #1) Gap or no Gap between Ros – Need Down-select

Recap of summary of from 1st round discussion.

Proposal 2.1-1 (introduce gap)

* LGE (configurable), OPPO, Qualcomm, Lenovo/Motorola Mobility, ETRI, Sharp, vivo, Huawei/HiSilicon (for some formats), Fujitsu
  + PRACH transmit power ramp up and ramp down can effect LBT of other UEs
  + Gap needed to absorb inter-UE block from differences in propagation delay

Proposal 2.2-1A (introduce gap with configurability)

* Support: vivo, Qualcomm, Lenovo/Motorola Mobility, Sharp
* Not support: Docomo, Intel, Interdigital, Ericsson

Proposal 2.1-2 (no gap)

* Docomo, Interdigital, Ericsson, Intel, ZTE/Sanechips, Nokia/NSB, Mediatek, Futurewei,CATT
  + Beam switching gap can be created by the gNB side (in specification transparent manner) with more PRACH repetitions
  + Likelihood of LBT failure is low for simulated deployment scenarios due to use of narrow beams
  + In case LBT fails, UE may try transmit at later time, therefore occasional LBT blocking is not catastrophic

Added proposal by Huawei/HiSilicon

###### Proposal 2.2-1C

* Support gap between consecutive ROs for 480kHz and 960kHz
  + ~~FFS: whether supporting gaps is fixed in specification or RRC configured by gNB~~
  + gNB may configure the gap between ROs, including no gap configuration
  + FFS: Whether gaps are supported for all PRACH formats or only for formats with smaller CP (eg, A1, B1, A1/B1)

###### Proposal 2.2-1D

* Support gap between consecutive ROs for 480kHz and 960kHz
  + ~~FFS: whether supporting gaps is fixed in specification or RRC configured by gNB~~
  + FFS: gNB may configure the gap between ROs, including no gap configuration
  + FFS: Whether gaps are supported for all PRACH formats or only for formats with smaller CP (eg, A1, B1, A1/B1)

Potential compromise for supporting gap

* Gap to be configurable + at most 1 symbol for gap between consecutive RO + PRACH slot contain all configured RO with gaps
  + Intel

From the discussions, the group is no where near consensus. Suggest to check quickly if any of Proposal 202-1, 2.2-1C or 2.2-2D can be agreeable. If not, the only outcome, that the moderator thinks we can take, is not agree to anything or conclude on Proposal 2.2-1B:

##### Proposal 2.2-1B (previously as 2.2-2)

* Conclusion:
  + Do not support gap between consecutive ROs for 480kHz and 960kHz

##### Issue #2) If gap supported, details of supporting gap

Proposal 2.2-2 (details of supporting gap)

* Support: Huawei/HiSilicon
* Agree in principle further discussion needed: vivo, Qualcomm, Lenovo/Motorola Mobility, Sharp
* Not support: Intel, Interdigital, Ericsson

Proposal 2.2-2A (details of supporting gap)

* Support: Qualcomm

Proposal 2.2-2B (details of supporting gap)

* Support: Samsung

This issue only needs to be discussed if gap is supported.

#### <Outcome GTW 10/18>

Conclusion:

* Do not support gap between consecutive ROs for 480kHz and 960kHz

Given the conclusion above, and lack of time for discussion in RAN1 #106-bis-e, moderator suggest closing this topic for discussion in RAN1 #106-bis-e.

#### == Discussion Closed for #106-bis-e ==

### 2.2.3 RAR Window & RA Preamble ID

* From [1] Huawei/HiSilicon:
  + For the same RO density per reference slot as 120 KHz PRACH, the RA-RNTI corresponding to 480 kHz and 960 kHz ROs can be generated according to equation (5) by compressing the t\_id to .
    - When some ROs are backward shifted to the immediately preceding slot of the specified slot due to the use of a gap symbol between consecutive ROs, support a 1 bit indication field in the DCI scheduling RAR/MsgB to resolve the PRACH slot ambiguity.
    - RA-RNTI = 1+s\_id+14×floor(t\_id⁄2^(μ-3) )+14×80×f\_id+14×80×8×ul\_carrier\_id (5)
  + Support maximum of 40 ms for ra-ResponseWindow for operation with shared spectrum and msgB-ResponseWindow for both operations with and without shared spectrum. Support indicating two LSBs of SFN at which gNB has received msg1 (MsgA) in DCI format 1\_0 with CRC scrambled by RA-RNTI (MsgB-RNTI).
* From [2] Futurewei:
  + For 480kHz and 960kHz use the following formula for RA-RNTI
    - RA-RNTI = 1 + s\_id + 14 × t\_id + 14 × 160 × f\_Id + 14 × 160 × 8 × ul\_carrier\_Id
    - and divide the RAR window in N segments where each segment is 160 slots, and signal the segment index in the DCI that schedules the MSG2/B.
* From [4] ZTE, Sanechips:
  + For higher PRACH SCS (480 and/or 960 kHz), consider the following options for further down-selection of RA-RNTI enhancements: option 2, 3, or 7
* From [5] vivo:
  + For larger PRACH SCS (480KHz/960KHz), the following options can be considered for RA-RNTI calculation:
    - Alt.1: Modify the RA-RNTI formula as following and introduce some contention resolution mechanism to resolve the conflict.
    - RA-RNTI = (1+s\_id+14×t\_id+14×X×f\_id +14×X×8×ul\_carrier\_id) mod A
    - Alt.2: Reuse the current RA-RNTI formula while introducing additional indicator field to indicate the time-frequency resource together with RA-RNTI.
    - Alt.3: Depending on the RO configuration pattern, reuse/modify the RA-RNTI formula and express the slot indexes t\_id based on a new specific subcarrier spacing.
* From [6] Fujitsu:
  + When calculating RA-RNTI for 480kHz and 960kHz PRACH, the following should be considered to uniquely identify a RO:
    - t\_id is determined in a way that more than one slot can have the same t\_id; and
    - DCI scheduling RAR indicates the local index among the slots having the same t\_id.
* From [9] CATT:
  + For supporting Msg1 transmission with 480 KHz/960 KHz SCS, RA-RNTI is divided into two parts. One part of RA-RNTI is carried by DCI, and the remaining 16-bit of RA-RNTI could be used to scramble CRC of the DCI1. Two possible options are:
    - Option A:
      * RA-RNTI = (1 + s\_id + 14 × t\_id + 14 ×× f\_id + 14 × × 8 × ul\_carrier\_id) mod
      * inDCI\_bit = floor ((1 + s\_id + 14 × t\_id + 14 ×× f\_id + 14 × × 8 × ul\_carrier\_id) /)
      * s\_id is the index of the first OFDM symbol of the PRACH occasion (0 ≤ s\_id < 14)
      * t\_id is the index of the first slot of the PRACH occasion in a system frame (0 ≤ t\_id < 640)
    - Option B:
      * RA-RNTI = 1 + s\_id + 14 ×(t\_id mod 80) + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id
      * inDCI\_bit =
      * s\_id is the index of the first OFDM symbol of the PRACH occasion (0 ≤ s\_id < 14)
      * t\_id is the index of the first slot of the PRACH occasion in a system frame (0 ≤ t\_id < 640)
* From [10] Xiaomi:
  + Confirm the working assumption that for 120 kHz SSB, the number of candidates SSBs in a half frame is 64.
  + For 480/960 kHz SSB, candidates SSB index can be up to 128.
  + Whether DBTW or Q is needed can be decoded together with Q value.
* From [11] Ericsson:
  + For 480/960 kHz PRACH, reuse the RA-RNTI expressions from Rel-15/16, with the additional statement that for 480/960 kHz PRACH, t\_id should be determined based on a subcarrier spacing of 120 kHz.
  + Postpone further discussions of RA-RNTI design until the PRACH configuration design is completed.
* From [12] Nokia, NSB:
  + Reuse RA-RNTI formula defined for 120 kHz SCS also for the cases PRACH is configured with 480 or 960 kHz SCS where
    - assumes 480/960 kHz SCS
    - assumes 120 kHz SCS
* From [15] Intel:
  + RA-RNTI computation equation should be adjusted to avoid overflow in case of PRACH SCS 480 kHz and 960 kHz;
    - Support the following modified equation for RA-RNTI computation:
      * ,
      * where t\_id is based on the value of specified in clause 5.3.2 of TS 38.211.
* From [19] ETRI:
  + Propose to reuse the current equation with minor modifications for RA preamble ID calculation.
    - RA-RNTI = 1 + s\_id + 14 × t\_id + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id
      * *t\_id is the index of 120kHz slot that contains RO in a system frame*
      * s\_id is the index of the first OFDM symbol of RO based on the value of specified in clause 5.3.2 of TS 38.211
      * If additional PRACH slots are configured, the index(s) of the first OFDM symbol of ROs may be configure not to overlap each other between two PRACH slots within a 120kHz slot.
* From [22] LG Electronics:
  + Since the same RO density in time domain as for 120 kHz PRACH in FR2 is maintained regardless of whether there is a gap between ROs, RA-RNTI/MSGB-RNTI associated with the PRACH occasion for 480 and 960 kHz SCS using the existing RA-RNTI equation, the following options can be considered:
    - In the case of mapping RA-RNTI to hypothetical 480/960 kHz PRACH slot assuming that the gap between RACH occasions is zero,
      * Option 1: Reuse the existing RA-RNTI/MSGB-RNTI equation by reinterpreting the slot indexes t\_id based on a new specific subcarrier spacing as the slot indexes of 120 kHz SCS (e.g., floor(t\_id/n) where n=4 for 480 kHz SCS and n=8 for 960 kHz).
    - In the case of mapping RA-RNTI to actual 480/960 kHz PRACH slot,
      * Option 2: Divide the RAR window for RA-RNTI (or msg2 window for MSGB-RNTI) into N sub-periods (where each sub-period is 80 slots using the used SCS) + signal the sub-period index using the DCI that schedules the MSG2/MSGB.
* From [23] Sharp:
  + Assuming RO density per reference slot is unchanged, without modifying the formula and definition of s\_id. Modify the definition of t\_id as the slot index referring to 120kHz SCS.
* From [24] Apple:
  + modifying the existing calculation equation or redefine t\_id based on 120kHz SCS to solve the RA-RNTI overflowing problem:
* From [26] Qualcomm:
  + for higher RACH SCS (480 and 960 kHz), consider the following options for the RA-RNTI:
    - Case 1: no extra RACH slots needed/configured
      * Same RA-RNTI equation as Rel-15/16
      * t\_id is the index of the first slot (based on 120 kHz numerology) of the PRACH occasion in a system frame (0 ≤ t\_id < 80)
    - Case 2: extra RACH slots needed/configured (but with the same number of ROs per reference slot)
      * Same RA-RNTI equation as Rel-15/16
      * s\_id is the index of the first OFDM symbol of the PRACH occasion within the one or more slots spanned by the ROs excluding any gaps (0 ≤ s\_id < 14)
      * t\_id is the index of the first slot (based on 120 kHz numerology) of the PRACH occasion in a system frame (0 ≤ t\_id < 80)
    - Case 3: extra RACH slots needed/configured (with more number of ROs per reference slot)
      * Option A: Extend s\_id to more than 14:
        + RA-RNTI = (1 + s\_id + S × t\_id + S × 80 × f\_id + S × 80 × 8 × ul\_carrier\_id) mod 216
        + s\_id is the index of the first OFDM symbol of the PRACH occasion within the one or more slots spanned by the ROs excluding any gaps (0 ≤ s\_id < S), S can take value > 14
        + t\_id is the index of the first slot (based on 120 kHz numerology) of the PRACH occasion in a system frame (0 ≤ t\_id < 80)
      * Option B:
        + Same RA-RNTI equation as Rel-15/16
        + t\_id is the index of the first slot (based on 120 kHz numerology) of the PRACH occasion in a system frame (0 ≤ t\_id < 80)
        + And signaling in the DL DCI that schedules the MSG2/MSGB the 480/960 kHz slot index within the 120 kHz slot

#### Summary of Discussions

The following list of options are from last meetings discussion.

|  |
| --- |
| * + **Plain Modulus Category**     - Option 1)   + **PRACH Sub-segmentation Method Category**     - Option 2)       * The same PRACH slot location in each 120kHz slot duration     - Option 3)       * Segment the PRACH into N segments       * is the index of the PRACH slot that contains the PRACH occasion in a segment.       * In DCI: RA-indication = Segment index     - Option 4)       * Segment the PRACH into N segments       * In DCI:     - Option 5)       * Segment the PRACH into N segments       * In DCI:     - Option 6)       * In DCI:   + **Compressing some indices Category (may require a matching RO configuration to work properly)**     - Option 7)       * is the index of the first 120kHz slot that contains the PRACH occasion in a system frame.       * is the index of the first OFDM symbol of the PRACH occasion based on the value of specified in clause 5.3.2 of TS 38.211.     - Option 8)       * RA-RNTI = 1 + s\_id + 14 × floor(t\_id / ) + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id,       * t\_id is based on the value of specified in clause 5.3.2 of TS 38.211. |

The following is summary of company views.

* Alt 1) Plain Modulus Category, some example in option 1
  + vivo
* Alt 2) PRACH Sub-segmentation Method Category, some examples in option 2 ~ 6
  + Futurewei, ZTE/Sanechips, vivo, Fujitsu, CATT, LGE, Qualcomm
* Alt 3) Compressing some indices Category (may require a matching RO configuration to work properly), some examples in option 7 ~ 8
  + ZTE/Sanechips, Ericsson, Intel, vivo, Fujitsu, Nokia/NSB, ETRI, LGE, Sharp, Apple, Qualcomm, Huawei/HiSilicon

#### <Moderator’s Suggestion for Discussions>

RO design needs to be further progressed in order to assess which scheme is most suitable for fixing the RA-RNTI overflow issues. Suggest discussing this further once RO gap issue has been resolved and are determined.

#### 1st Round of Discussions

Please provide further comments on the moderator’s suggestion. Also, if there are any other issues that require discussion on RAR window and RA preamble ID, please comment them here.

|  |  |
| --- | --- |
| Company | Comments |
| LG Electronics | We are fine with Moderator’s Suggestion. However, we can consider the method of calculating RA-RNTI (regardless of configured RO gap) by mapping RA-RNTI to hypothetical 480/960 kHz PRACH slot assuming that the gap between RACH occasions is zero (corresponding to Option 1 in our contribution). |
| Ericsson | Fine with moderator's suggestion. |
| Intel | We are fine with Moderator’s suggestion. |
| vivo | Fine with moderator's suggestion. |
| ZTE, Sanechips | We are fine with Moderator’s suggestion. |
| Nokia | Agree. |
| Apple | Agree with Moderator to complete the RO design first. |

#### <Summary of 1st Round of Discussions>

Tentative Conclusion:

Discuss further on this issue once RO design proposals are more stable.

**Moderator will re-initiate discussion on this topic once issues in Section 2.2.2 has been mostly resolved.**

*Further updated:*

Given the lack of time for discussion, moderator suggests continuing discussion in the next RAN1 meeting based on the conclusion that we do not support gap between consecutive RO for 480/960kHz.

**Moderator Suggestion:**

* Further discuss the following issues in RAN1 #107-e
  + RA-RNTI calculation & RAR Window determination for 480 and 960 kHz

#### == Discussion Closed for #106-bis-e ==

### 2.2.4 Other aspects on PRACH

* From [2] Futurewei:
  + Support short control signaling LBT exception for RACH transmissions.

#### Summary of Discussions

One company provided inputs on applicability of short control signal exemption for PRACH transmission.

#### <Moderator’s Suggestion for Discussions>

Moderator suggest discussing short control signal exemption aspects under 8.2.6 channel access agenda.

#### 1st Round of Discussions

Please provide further comments on moderator’s suggestion above. Also, if there are any other issues that require discussion other aspects of PRACH, please comment them here.

|  |  |
| --- | --- |
| Company | Comments |
| LG Electronics | We support the Moderator’s suggestion that discussing short control exemption aspects under 8.2.6. |
| Ericsson | SCS exemption has already been agreed in channel access AI. |
| Intel | This was agreed in RAN1#105-e:  Agreement:   * Contention Exempt Short Control Signaling rules apply to the transmission of msg1 for the 4 step RACH and MsgA for the 2-step RACH for all supported SCS.   + Note restriction for short control signalling transmissions apply (10% over any 100ms intervals)   + Alt 1: The 10% over any 100ms interval restriction is applicable to all available msg1/msgA resources configured (not limited to the resources actually used) in a cell   + Alt 2: The 10% over any 100ms interval restriction is applicable to the msg1/msgA transmission from one UE perspective * FFS: Other UL signals/channels can be transmitted with Contention Exempt Short Control Signaling rule, such as msg3, SRS, PUCCH, PUSCH without user plain data, etc |
| ZTE, Sanechips | We agree with the Moderator’s suggestion that discussing short control exemption aspects under 8.2.6. |
| Nokia | Not sure if Channel Access agenda item will address the case when sub-set of SSBs/ROs fall under SCSe and whether it would need some additional handling (from UE perspective) or whether it can be left fully for network implementation. But with that note, we can follow the moderator proposal. |

#### <Summary of 1st Round of Discussions>

Conclusion:

Proponent companies with short control signal exemption related issues to bring up the issues and provide comments to [106bis-e-R17-52-71GHz-07] email discussion thread.

Moderator will assume this agenda is closed

#### == Discussion Closed for #106-bis-e ==

## 2.3 Others Aspects

* From [1] ZTE, Sanechips:
  + The existing parameter subCarrierSpacingCommon in MIB should be captured into Rel-17 RRC parameter table, as it will no longer be used to indicate the SCS of CORESET#0 in FR2-2.

#### Summary of Discussions

One company provided inputs on RRC parameters needed for initial access.

#### <Moderator’s Suggestion for Discussions>

Moderator suggest discussing the RRC parameters related issues under 8.2 RRC parameter discussion thread, “[106bis-e-R17-RRC-60GHz] Email discussion on Rel-17 RRC parameters for supporting NR from 52.6 GHz to 71 GHz – Jing (Qualcomm).”

#### 1st Round of Discussions

Please provide further comments on moderator’s suggestion above. Also, if there are any other issues that require discussion on issues not discussed in this summary document, please comment them here.

|  |  |
| --- | --- |
| Company | Comments |
| Ericsson | Agree to discuss in RRC thread |
| Intel | We agree with Moderator’s suggestion |
| ZTE, Sanechips | We agree with Moderator’s suggestion. |
| Convida Wireless | We are ok with Moderator’s suggestion to discuss in RRC thread. |

#### <Summary of 1st Round of Discussions>

Conclusion:

Proponent companies with RRC related issues to bring up the issues and provide comments to [106bis-e-R17-RRC-60GHz] email discussion thread.

Moderator will assume this agenda is closed

#### == Discussion Closed for #106-bis-e ==

# Summary of Proposals for Discussion/Approval

Suggested proposals for agreement.

###### Proposal 1.1-5C

* Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off).
  + Existing DCI size alignment in TS38.212 applies to DCI 1\_0 and 0\_0 in CSS.

###### Proposal 1.1-7D

* Indication of licensed and unlicensed operation is not explicitly indicated in MIB or PBCH payload.
  + FFS: Whether or not to indicate licensed regime by different synchronization raster entries.
* Indication of use of LBT or no-LBT is not explicitly indicated in MIB or PBCH payload.

###### Conclusion 1.2-3:

* No other values of n other than agreed previously is supported for 120kHz SCS, where parameter ‘n’ is the set of values to determine the first symbols of the candidate SSB blocks for 120kHz SCS in agreement from RAN1 #104-bis-e.

###### Proposal 1.3-1A

* Working assumption:
  + For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz, support multiplexing pattern 1 with 96 PRB CORESET#0, and {1, 2} symbol durations
  + Note: the working assumption can be confirmed once RAN1 agrees on the number of needed SSB-CORESET0 offsets for 24 and 48 RB CORESET0 based on RAN4 channelization design

###### Proposal 1.3-4B

* If multiplexing pattern 3 is supported~~,~~ for ‘searchSpaceZero’ configuration for {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 3:

|  |  |  |
| --- | --- | --- |
| Index | PDCCH monitoring occasions (SFN and slot number) | **First symbol index**  **(*k* = 0, 1, … ~~31~~Lmax/2 - 1)** |
| 0 |  | 2, 9 in |
| 1 ~ 15 | Reserved | |

###### Proposal 2.1-1

* Additionally support PRACH length L=571 for 480kHz

###### Proposal 2.1-2A

* Support 120 kHz and 480 kHz subcarrier spacing for initial UL BWP for PCell

# Summary of Agreements made in RAN1 #106-bis-e

Outcome of 10/12 Tuesday GTW Session

**Working Assumption**

* Support DBTW for 120kHz
  + FFS: support for 480kHz and 960kHz

Outcome of 10/18 Monday GTW Session

Conclusion:

* Do not support gap between consecutive ROs for 480kHz and 960kHz

# Reference

1. R1-2108767, “Initial access signals and channels for 52-71GHz spectrum,” Huawei, HiSilicon
2. R1-2108782, “Initial access for Beyond 52.6GHz,” FUTUREWEI
3. R1-2108902, “Discussion on initial access aspects for NR for 60GHz,” Spreadtrum Communications
4. R1-2108934, “Discussion on the initial access aspects for 52.6 to 71GHz,” ZTE, Sanechips
5. R1-2108959, “Discussions on initial access aspects for NR operation from 52.6GHz to 71GHz,” vivo
6. R1-2109032, “Considerations on initial access for NR from 52.6GHz to 71 GHz,” Fujitsu
7. R1-2109070, “Discusson on initial access aspects,” OPPO
8. R1-2109120, “Discussion on initial access aspects supporting NR from 52.6 to 71 GHz,” NEC
9. R1-2109208, “Initial access aspects for up to 71GHz operation,” CATT
10. R1-2109401, “On initial access aspects for NR from 52.6-71 GHz,” Xiaomi
11. R1-2109433, “Initial Access Aspects,” Ericsson
12. R1-2109442, “Initial access aspects,” Nokia, Nokia Shanghai Bell
13. R1-2109476, “Initial access aspects for NR from 52.6 GHz to 71 GHz,” Samsung
14. R1-2109557, “Remaining issues on initial access of 52.6-71 GHz NR operation,” MediaTek Inc.
15. R1-2109598, “Discussion on initial access aspects for extending NR up to 71 GHz,” Intel Corporation
16. R1-2109665, “Initial access aspects for NR from 52.6 to 71 GHz,” NTT DOCOMO, INC.
17. R1-2109741, “Initial access aspects for NR from 52.6 GHz to 71 GHz,” Panasonic Corporation
18. R1-2109777, “Considerations on initial access aspects for NR from 52.6 GHz to 71 GHz,” Sony
19. R1-2109808, “Discussion on initial access aspects for NR from 52.6 to 71GHz,” ETRI
20. R1-2109897, “Initial access aspects for NR from 52.6 GHz to 71GHz,” Lenovo, Motorola Mobility
21. R1-2109903, “Discussion on initial access channels and signals for operation in 52.6-71GHz,” InterDigital, Inc.
22. R1-2109961, “Initial access aspects to support NR above 52.6 GHz,” LG Electronics
23. R1-2109992, “Initial access aspects,” Sharp
24. R1-2110021, “Initial access signals and channels,” Apple
25. R1-2110109, “NR SSB design consideration for 52.6 GHz to 71 GHz,” Convida Wireless
26. R1-2110172, “Initial access aspects for NR in 52.6 to 71GHz band,” Qualcomm Incorporated
27. R1-2110320, “Discussion on initial access aspects for NR beyond 52.6GHz,” WILUS Inc.