**3GPP TSG RAN WG1 Meeting #106-e R1-210xxxx**

**e-Meeting, August 16 – 27, 2021**

**Source: Moderator (Intel Corporation)**

**Title: Summary #4 of email discussion on initial access aspect of NR extension up to 71 GHz**

**Agenda item: 8.2.1**

**Document for: Discussion**

# Introduction

In this contribution, we summarize discussion on aspects related to initial access for extending NR up to 71 GHz for RAN1 #106-e.

# Summary of issues

## 2.1 SSB Aspects

### 2.1.1 DRS Related Aspects (and other MIB design other than CORESET#0/Type0-PDCCH)

* From [1] Huawei/HiSilicon:
  + For operation with shared spectrum and for 480 kHz and 960 kHz SSBs, indicate the 7th bit of the candidate SSB index by borrowing the 4th LSB of SFN in the PBCH payload. Indicate the 4th LSB of SFB in MIB payload.
  + Support discovery burst transmission window for all numerologies in shared spectrum in 52.6GHz to 71GHz.
  + If LBT on/off indication is deemed required to determine the size of DCI 1\_0 whose CRC scrambled with SI-RNTI, such an indication may be performed using one of the following methods:
    - Using one bit in MIB
    - Implicitly using the synch raster entry of the associated SSB used for initial access
  + Similar to Rel-16 NR-U, use the following method to implicitly indicate in SIB1 that DBTW is enabled/disabled:
    - If DBTW length is equal to or smaller than the time duration from the beginning of the half frame to the end of the slot containing the candidate SSB index N\_SSB^QCL-1, DBTW is disabled.
    - If DBTW length is larger than the time duration from the beginning of the half frame to the end of the slot containing the candidate SSB index N\_SSB^QCL -1, DBTW is enabled.
    - Note 1: DBTW is configured in SIB1 and N\_SSB^QCL is acquired from the MIB payload.
    - Note 2: Prior to reading SIB1, UE assumes that DBTW includes all candidate SSB positions in a half frame.
  + Values {8, 16, 32, 64} should be supported for N\_{SSB}^{QCL}\ in operation with shared spectrum above 52.6GHz.
  + Configure DBTW length in SIB1 for operation with shared spectrum in 52.6GHz to 71GHz with the following values:
    - 120 kHz SCS: {40, 32, 24, 16, 8, 4} slots = {5, 4, 3, 2, 1} ms
    - 480 kHz SCS: {72, 32, 24, 16, 8, 4} slots = {2.25, 1, 0.75, 0.5, 0.25, 0.125} ms
    - 960 kHz SCS: {64, 32, 24, 16, 8, 4} slots = {1, 0.5, 0.375, 0.25, 0.125, 0.0625} ms
  + In operation with shared spectrum in 60 GHz, for MSB k, k≥1, of inOneGroup and MSB m, m≥1, of groupPresense of ssb-PositionsInBurst:
    - if MSB k of inOneGroup and MSB m of groupPresense are set to 1, the UE assumes that SSB(s) within DBTW with candidate SSB index(es) corresponding to SSB index equal to k-1+(m-1)×8 may be transmitted;
    - if MSB k of inOneGroup or MSB m of groupPresense are set to 0, the UE assumes that the SSB(s) are not transmitted.
  + Regardless of the value of the MSB k of inOneGroup and MSB m of groupPresense in ssb-PositionsInBurst configured in SIB1, if , UE assumes that candidate SSB index(es) corresponding to SSB index equal to are not transmitted.
* From [2] vivo:
  + The following fields could be considered to indicate the value of Q in PBCH:
    - subCarrierSpacingCommon
    - LSB of ssb-SubcarrierOffset
    - Coreset#0 and Type#0 PDCCH indication
  + When DBTW is enabled with indicated value of Q, how to interpret the meaning of ssbPositionsInBurst should be studied.
  + More number of candidate SSBs should be specified for LBT case to alleviate LBT failure than non-LBT case.
  + Support DBTW in un-licensed band/LBT case from 52.6 GHz to 71 GHz for SSB with all supported SCSs.
  + The following methods could be considered to determine whether there is DBTW:
    - Alt. 1: GSCN (licensed or un-licensed);
    - Alt. 2: The indicator in PBCH;
  + Supported DBTW length as the same in NR-U, which is 0.5, 1, 2, 3, 4, 5 msec.
  + The number of candidate SSB positions for SCS 120 kHz and SCS 480 kHz should be 64 and 128 respectively.
  + LBT on/off is not indicated in MIB.
* From [3] Spreadtrum:
  + Confirm that DBTW is supported at least for 120kHz SCS.
* From [4] Interdigital:
  + Enhance the initial access operation to support Discovery Burst (DB) and Discovery Burst Transmission Window (DBTW) in unlicensed spectrum operations that require LBT in beyond 52.6GHz spectrum.
  + Consider indicating enable/disable of DBTW in initial access operations based on a sync raster offset used by SS/PBCH block.
  + Consider the enhancements to indicate the mode of operation regarding the enable/disable of the DBTW, on/off of the LBT, and the license regime based on the combination of Sync. raster offset and MSB of controlResourceSetZero.
  + Support enhancements on the reference tables in indication of Q parameter for up to 64 SSB beams in initial access operations for unlicensed spectrum in beyond 52.6GHz, e.g., subsamples of the Q parameter.
    - Support Alt A, for the total number of options for the Q parameter to not exceed 4.
* From [5] Sony:
  + Discovery Burst Transmission Window should be supported.
  + Enabling/disabling DBTW and should be signalled in MIB
    - Indication of disabling DBTW should be jointly coded with
      * Parameter to signal disabling DBTW and indicates {16, 32, 64, or disabling DBTW} if the number of candidate SSB position is more than 64
      * Parameter to signal disabling DBTW and indicates {8, 16, 32, or disabling DBTW} if the number of candidate SSB position is 64
  + Candidate SSB positions should be extended when DBTW is enabled.
    - For 120 kHz SCS,
      * The number of candidate SSB positions should be 80
      * additional n values (4, 9, 14, 19) should be supported when DBTW is enabled
    - For 480/960 kHz SCS,
      * The number of candidate SSB positions should be 128
      * First symbols of the candidate SSB have index {4, 8, 16,20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
      * n = {0, 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 15, 16, 17, 18} when DBTW is disabled.
      * n = 0 - 31 when DBTW is enabled
  + For indication of candidate SSB indices, QCL relation, and disabling DBTW, subCarrierSpacingCommon and reserved state of pdcchConfig-SIB1 should be used.
* From [6] Lenovo/Motorola Mobility
  + For NR operation in unlicensed bands between 52.6 GHz and 71 GHz, potential enhancements related to periodic transmission of DRS such as SSB/PBCH/CORESET#0 are needed including:
    - performing directional LBT prior to the transmission of SSB according to the ssb-PositionsInBurst
    - directional LBT on multiple beams at the same time at the beginning of the DRS window
    - Cat 2 LBT (depending on the gap) before actual transmission
* From [7] Samsung:
  + For 480 kHz and 960 kHz,
    - Support the same SS/PBCH block pattern in a slot, and the same pattern is given by Case A/C (i.e., Alt 1 with X=2 and Y=8).
    - Support larger number of slots including candidate SS/PBCH block, when DBTW is enabled.
  + Support discovery burst transmission window for all SCSs on the 60 GHz unlicensed spectrum.
    - The indication of Q can be in MIB for a best effort, and if not possible, in SIB1;
    - The indication of DBTW disabling can be joint coded with the indication of Q, if Q is indicated in MIB; and the indication can use 1 bit in MIB, if Q is not indicated in MIB;
    - The case of an unlicensed operation with DBTW disabled can be supported implicitly, by comparing the Q value and the DBTW window size;
    - Support more than 64 candidate SS/PBCH block locations within a half frame;
      * Current PBCH payload can support timing indication of up to 128 candidate SS/PBCH block candidate locations;
      * Use one PHY bit to indicate the extra candidate SS/PBCH block index (e.g. 7th LSB);
    - For initial access, different synchronization raster entries are applied for licensed and unlicensed operations; for non-initial access, support an explicit indication of licensed or licensed operation when configuring a cell.
* From [8] CATT:
  + The subCarrierSpacingCommon field in MIB can be saved and repurposed.
  + More than 64 SSB transmission opportunities shall be defined within a 5ms SSB burst set to support up to 64 beams for SSB beam sweeping in case of LBT failure. The issue of supporting additional bit(s) for the indicating SSB candidate index needs further study.
  + For no-LBT operation or licensed spectrum operation, value “n” can keep the same value as for the 120KHz SCS case.
  + Additional n value such as #4, #9, #14, and #19 can be used for new SSB candidates if LBT/DBTW is needed for SSB transmission.
  + For up to 71GHz operation and at least for NO-LBT operation, some values of ‘n’ can be reserved for uplink grant scheduling.
  + For NR operation in 60 GHz unlicensed spectrum, the discovery burst transmission window (DBTW) shall be supported for 120 KHz SSB at least when gNB configures more than 56 SSB transmissions.
  + DBTW is not needed for SSB with 480 KHz/960 KHz SCS since the duty cycle is less than 10% over the 100 ms observation window for the short control signaling transmissions.
  + For supporting DBTW of 120KHz SCS SSB, more than 64 SSB (up to a total of 80 ) positions are needed. A total of 7 bits of information is needed to indicate more than 64 SSB candidate locations.
  + For indication of （if needed at for 120kHz SSB）， legacy mechanism can be reused.
  + Considering Contention Exempt Short Control Signalling rules can be applicable to the transmission of SS/PBCH for most cases , only 5ms duration for DBTW operation is supported .
  + For 120 kHz SSB, signaling in MIB can indicate enable/disable of DBTW.
  + If LBT ON/OFF state is indicated in MIB/PBCH, joint coding can be used for indication of LBT ON/OFF, DBTW enabling/disabling and one bit information for candidate SSB index.
  + If LBT ON/OFF state is not indicated in MIB/PBCH, it can be indicated in DCI 1\_0 scrambled by SI-RNTI.
* From [9] ZTE/Sanechips:
  + Discovery burst transmission window (DBTW) should be supported for 120 kHz SSB SCS and other SSB SCSs.
  + In order to reduce the impact of standardization caused by indicating candidate SSB indices, the maximum number of candidate SSB defined in the half-frame can be kept unchanged (maintain 64) or limited to 128 for 480/960 kHz SSB SCS.
  + Four candidate values {8,16,32,64} for are preferred.
  + For 120 kHz SSB, enable/disable of DBTW can be indicated by comparing the value of  in MIB and DBTW length, and explicit signaling is not needed for this purpose.
* From [11] Ericsson:
  + Before RAN1 can agree that DBTW is supported, the following two aspects need to be jointly decided:
    - If and how additional candidate SSB positions are to be supported, and
    - How to signal the following: Q and DBTW on/off
  + Conclude that a DBTW is not supported for the 52.6 – 71 GHz band and that the size of DCI 1\_0 is the same regardless of channel access mode (Option 1). LBT on/off is signaled in SIB1.
* From [12] Futurewei:
  + For 480/960 kHz SS/PBCH DBTW should not be supported.
  + Support enabling and disabling LBT for channel access in shared spectrum, with LBT mode default enabled. Signal LBT disabled in the MIB.
  + For 480/960 kHz SS/PBCH SCS use the field subCarrierSpacingCommon to indicate LBT disabled.
  + For 120 kHz SS/PBCH SCS use the field subCarrierSpacingCommon and the LSB of ssb-SubcarrierOffset to indicate the N\_SSB^QCL, where one of the values indicates LBT disabled.



* + Use the following DBTW lengths values 0.5, 1, 2, 3, 4, 5 msec.
  + For 120 kHz SS/PBCH SCS use DBTW zero length in SIB1 to indicate that DBTW is disabled.
  + For 120kHz SSB the maximum number of candidate positions is 64.
  + Consider using CSI-RS presence in the discovery burst for possible ways to implement beam refinement during the initial channel access.
* From [13] Nokia/NSB:
  + Support operation with and without DBTW for 120 kHz.
  + Support DBTW also for 480/960 kHz SSB.
  + Provide LBT on/off indication in SIB1.
  + Support Option 2: enable/disable of DBTW is indicated by distinct GSCN used by the SSB.
  + Support Alt B) Explicit indication of SSB index and/or SSB candidate location.
  + Support 80 candidate positions for SSB when DBTW is enabled with 120 kHz.
  + Support also 80 candidate positions for SSB when DBTW is enabled with 480/960 kHz (if DBTW is supported for 480/960 kHz).
  + Group additional SSB locations and associate each group to set of regular SSB positions, e.g. after each block of 16 regular SSB positions there is associated group of up to four additional positions that can be used to retransmit any of the associated actual SSBs.
  + Use subCarrierSpacingCommon to indicate whether or not the SSB is in additional SSB position. Use kSSB bits in the SSB located in the additional position (based on subCarrierSpacingCommon) together with SSB index (PBCH DMRS and MSBs in PBCH payload) to provide UE information about the slot timing and actual SSB index transmitted.
  + Supported values for discoveryBurstWindowLength are same as used for Rel-16 NR-U
    - 0.5, 1, 2, 3, 4, 5 ms
  + It is possible to apply SCSe to one part of actually transmitted SSBs and LBT procedure for other/rest of the SSBs.
  + Consider semi-static or predetermined mechanism to determine which SSBs are under SCSe and which under LBT in certain time windows.
  + For 120kHz SSB pattern, introduce additional candidate locations for SSB transmission support for 𝑛 = 4, 9, 14, 19, where n is the slot index in half-frame.
    - The first symbols of the additional candidate SS/PBCH blocks have indexes {4, 8,16, 20} + 28×n.
  + For 480kHz and 960kHz SSB pattern, introduce additional candidate locations for SSB transmission support for 𝑛 = [{8, 9, 10, 11} ,{32,33,34,35}], where n is the slot index in half-frame.
* From [14] Charter:
  + DBTW is not introduced for 120 kHz, 480 kHz, and 960 kHz SCS SSB, including the non-initial access case.
  + If DBTW is introduced, supported DBTW lengths follow Alt 1) 0.5, 1, 2, 3, 4, 5 msec. Number of candidate positions when DBTW is enabled is 64.
* From [15] NEC:
  + DBTW should be supported for SSB transmission with 120 kHz and 480/960 kHz SCS.
  + The long term sensing could be considered as an approach to enabling/disabling DBTW.
  + DBTW indication for SSB transmission could be indicated per SSB/beam.
  + When LBT is used on unlicensed spectrum, enabling/disabling DBTW and LBT on/off indication could be jointly indicated in MIB.
  + At least for 120 kHz SCS SSB, the candidate SSB indication in NR-U should be reused with enhancement to indicate DBTW enabling/disabling and Q value jointly in MIB.
  + Additional discovery burst transmission window in the adjacent frame could be considered as a method of cycling SSB transmission.
  + With concurrent spatial multiplexing DBTWs, all SSBs could be transmitted in a cycling transmission fashion.
  + Additional n values of 4, 9, 14 and 19 should be supported to indicate 80 candidate SSBs in DBTW at least for 120 kHz SCS SSB pattern.
  + The indication of additional candidate SSBs based on additional n values should be investigated.
  + If DBTW is additionally supported for 480/960kHz SCS SSB transmission, 128 SSB candidates should be supported.
* From [16] Panasonic:
  + DBTW is supported regardless of SCS.
  + The number of candidate SSB positions is 64.
  + For enabling/disabling DBTW, Option 1-1 (disabling DBTW is jointly coded with ) with SIB indication of no-LBT mode is supported.
* From [18] Qualcomm:
  + do not support discovery burst transmission window (DBTW) for SSB for SCS 480 and 960 kHz
  + for an unlicensed band that requires LBT, if DBTW for SSB is adopted for 120 kHz SSB:
    - MIB signaling to support indication of for 120 kHz SSB
    - Minimize the number of bits needed to signal (1 or 2 bits) and thus the values (2 or 4 values)
    - Enabling/disabling DBTW can be implicit in the value
    - Consider getting the bits needed from one or more of the following: controlResourceSetZero, searchSpaceZero, ssb-SubcarrierOffset, subCarrierSpacingCommon
    - Number of candidate positions when DBTW is enabled = 64 for 120 kHz SSB
    - Consider having a subset of the SSBs (< 64) transmitted under the short control signal assumption while another subset can be best effort or have multiple positions per beam (have a within the subset)
  + consider increasing the size of the DCI 0\_0 and 1\_0 for NR licensed, by adding a field, to align with the size of the corresponding DCIs for the NR-U
* From [19] LG Electronics:
  + Adopt the following methods to indicate enabled/disabled DBTW for idle and/or connected mode UEs.
    - Separate two sets of GSCN values where one set corresponds to the case of disabled DBTW while the other set corresponds to the case of enabled DBTW
    - Signalling via system information (e.g., measObject)
    - UE-specific RRC signaling (e.g., for SCell addition)
  + Consider all or some of the following bits to indicate candidate values.
    - subCarrierSpacingCommon
    - LSB(s) of ssb-SubcarrierOffset
    - dmrs-TypeA-Position
  + Do not indicate LBT on/off in PBCH. DCI format 1\_0 size should be aligned regardless of LBT on or off.
  + Support of additional n values for the time domain pattern of SS/PBCH block with 120 kHz SCS can be considered to increase SS/PBCH block’s transmission opportunities, only if PBCH payload is sufficient to indicate the increased number of candidate SS/PBCH block indexes.
  + For 480/960 kHz SSB, first symbols of the candidate SSB have index are {4, 8, 16, 20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame (i.e., Alt 2 in previous agreement), and values of ‘n’ are consecutive integers (i.e., n = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15).
* From [20] ETRI:
  + Propose to support DBTW for all SSB SCSs and the same DBTW lengths with Rel-16 NR-U.
  + Propose to support joint coding for LBT, DBTW, and , and study which bits can be used for reinterpretation for the joint coding.
* From [22] Intel:
  + Support DBTW for SSB with SCS 120 kHz
    - The max number of candidate SSB is
    - Support additional values of , such as 4, 9, 14, 19, in the equation defining the first symbols of candidate SS/PBCH blocks
    - Additional candidate SSBs (i.e., with index greater or equal to 64) are indexed in non-ascending order in time
      * An example relationship between candidate SSB index and SSB slot parameter can be specified in a closed form as follows:
  + Support DBTW for SSB with SCS 480 kHz/960 kHz
    - The max number of candidate SSB is
    - All candidate SSBs are indexed in ascending order in time
  + DBTW length is 5 ms.
  + For QCL relationship indication across SSBs, reuse Rel-16 NR-U mechanism by introducing parameter.
  + Explicitly indicate candidate SSB index for and in MIB.
    - No changes to MIB payload size. Further discuss and consider reinterpreting bits from some bit fields within MIB to extend candidate SSB index and provide information
    - FFS:
      * Two or four values of , e.g., or ;
      * Whether the set of values depends on SSB SCS, e.g., for SCS 120 kHz and for SCS 480 kHz/960 kHz.
  + Distinguishing between channel access cases is not needed during reception of DRS based on SS burst.
  + No need to indicate DBTW enabling. The network can configure parameter value to operate as if no DBTW is used.
  + For unlicensed operation, LBT on/off indication is within DCI scheduling SIB1.
  + Indication of licensed vs. unlicensed operation could be done based on SSB raster position. If this is not possible due to future compatibility issues, indicate licensed vs. unlicensed operation in DCI scheduling SIB1
    - To avoid DCI size ambiguity issue for licensed case, apply bit padding to DCI scheduling SIB, i.e., increase the number of reserved bits for DCI 1\_0 scrambled with SI-RNTI.
* From [23] Apple:
  + If DBTW is introduced, for above 52.6GHz frequency band, consider the following:
    - Re-purposing the 1-bit 'subCarrierSpacingCommon'
    - If more than one bit is needed, re-purposing 1-bit MSB of controlResourceSetZero in MIB or providing one more bit information by selecting one sequence from two candidates to scramble CRC bits of PBCH payload.
    - Support joint encoding Q value and licensed/unlicensed band indication.
      * If joint encoding is not possible, licensed/unlicensed band can be signaled in SIB1 and UE monitors the DCI 1\_0 for SIB1 scheduling assuming two different sizes.
* From [24] Sharp:
  + Adopt DBTW for SSB with 120 kHz SCS in above 52.6GHz.
* From [25] NTT Docomo:
  + With 120 kHz SCS, ‘n’ value(s) which can be added on top of the ones agreed already are limited, i.e., ‘n’ = {4, 9, 14, 19} only
  + With 120 kHz SCS, no significant need to support additional ‘n’ values on top of the ones agreed already
  + With 480/960 kHz SCS, not support more than 64 candidate SSB positions
  + DBTW should be supported irrespective of SCS.
    - In a certain region, e.g., Japan, sensing needs to be performed for initiating any transmission by any device in 60 GHz.
  + For DBTW to be supported in Rel-17 NR 52.6 – 71 GHz, similar to DBTW in Rel-16 NR-U, subCarrierSpacingCommon field in MIB should indicate QCL parameter, which is up to 64.
    - Following information can be implicitly indicated via subCarrierSpacingCommon
    - Enabling/disabling of DBTW
    - Licensed/unlicensed band
    - LBT on/off
* From [26] Xiaomi:
  + Alt1 (same as Rel-16 FR1 NR-U) is supported.
  + The number of candidate positions when DBTW is enabled is 64.
* From [27] Convida:
  + Increasing the number of SSB candidate positions to above 64 to increase transmission opportunities to cope with LBT failure should be considered.
  + The number of values for ‘n’ should be dependent on LBT operation and the actual values of ‘n’ for each SCS 480 GHz/960 GHz can be further studied.
* From [28] WILUS:
  + We propose to support discovery burst transmission window (DBTW) for at least 120kHz SCS which makes it possible to define candidate SSB positions within the DBTW with support of DB which was already agreed.
  + It should be further considered that the additional candidate SS/PBCH block locations within a DBTW can be set to the closest slot locations after LBT failure at candidate SS/PBCH blocks locations as defined in FR2.

#### Summary of Contribution Discussions

The following are previous agreements on DRS aspects.

|  |
| --- |
| **Agreement:**  For an unlicensed band that requires LBT, further study whether/how to support discovery burst (DB) and discovery burst transmission window (DBTW) at least for 120 kHz SSB SCS   * If DB supported   + FFS: What signals/channels are included in DB other than SS/PBCH block * If DBTW is supported   + Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs     - FFS: how to support UEs performing initial access that do not have any prior information on DBTW.   + PBCH payload size is no greater than that for FR2   + Duration of DBTW is no greater than 5 ms   + Number of PBCH DMRS sequences is the same as for FR2 * The following points are additionally FFS:   + How to indicate candidate SSB indices and QCL relation without exceeding limit on PBCH payload size   + Details of the mechanism for enabling/disabling DBTW considering LBT exempt operation and overlapping licensed/unlicensed bands * Whether or not to support DBTW for SSB SCS(s) other than 120 kHz if other SSB SCS(s) are supported   **Agreement:**   * For operation with shared spectrum channel access of NR 52.6 – 71 GHz, support discovery burst (DB) and define the DB same as in Rel-16 37.213 Section 4.0 * FFS: Support discovery burst transmission window (DBTW) at least for SSB with 120 kHz SCS with the following requirements   + PBCH payload size is no greater than that for FR2   + Duration of DBTW is no greater than 5 ms   + Number of PBCH DMRS sequences is the same as for FR2   + FFS: applicability of DBTW design for 120kHz to SSB with 480kHz and 960kHz SCS   + Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs     - FFS: how to support UEs performing initial access that do not have any prior information on DBTW.     - FFS: details of the mechanism for enabling/disabling DBTW considering LBT exempt operation and overlapping licensed/unlicensed bands     - FFS: details of how to inform UEs of the configuration of DBTW   **Agreement:**  FFS: Support DBTW at least for 120kHz   * FFS whether DBTW will be applicable for 480/960 kHz SSB SCS   + If DBTW is supported for 480/960kHz SSB:     - For the case agreed in RAN1 #104bis-e where 480/960 kHz SSB location and SCS are explicitly provided to the UE (non-initial access), indication of DBTW configuration (e.g. enable/disable of DBTW,  , and DBTW length) are supported by dedicated signaling.  * For 120kHz SSB, support mechanism to distinguish at least the following scenarios:   + Case 1) (Unlicensed with LBT off) + DBTW disabled   + Case 2) (Unlicensed with LBT on) + DBTW enabled   + Case 3) (Unlicensed with LBT on) + DBTW disabled   + Case 4) (Licensed) + DBTW disabled   + FFS: Whether/how LBT on/off is indicated in MIB     - If not indicated in MIB, then FFS whether/how the UE determines different sizes of DCI 1\_0 with CRC scrambled by SI-RNTI   + FFS: whether any case(s) can be combined for DBTW signaling design and how to handle implications to DCI 1\_0 size ambiguity if is not distinguished in signaling   + FFS: whether all above cases need an explicit indication   + FFS: Whether a single indication can be used for combination of more than one cases * For 120 kHz SSB, enable/disable of DBTW is indicated by one or more of the following methods:   + Option 1) signaling in MIB     - Option 1-1) disabling DBTW is jointly coded with  * + - Option 1-2) indicated by other bit fields in MIB     - FFS: among options 1-1 and 1-2   + Option 2) distinct GSCN used by the SSB   + Option 3) By comparing the value of  in MIB and DBTW length after UE reads SIB1 or by comparing the value of  in MIB and default DBTW length of 5 ms before UE reads SIB1.  * + FFS: whether to support option 1, 2, 3, or any combination of the options.   + Note: enable/disable signaling of DBTW by MIB or GSCN does not preclude other signaling methods   **Agreement:**  If DBTW is supported,   * Working assumption: MIB signaling to support   + Alt A) indication of at least for 120kHz SSB  * + - In this case, the total number of values of to not exceed 4  * + Alt B) Explicit indication of SSB index and/or SSB candidate location     - FFS on the details of signaling   + FFS betweenAlt A, or B, or supporting both * Supported DBTW lengths   + Alt 1) 0.5, 1, 2, 3, 4, 5 msec     - Note: same as Rel-16 FR1 NR-U   + Alt 2) maximum 5 msec     - FFS other values   + FFS between Alt 1 and 2 * Number of candidate positions when DBTW is enabled   + For 120kHz SSB     - FFS between 64 or 80   + If DBTW is additionally supported for 480/960kHz SSB     - FFS between 64 or 128 |

The following is a summary of company position of various aspects of DRS.

* Supporting DBTW
  + Support: Huawei/HiSilicon, vivo, Spreadtrum (for 120kHz), Interdigital, Sony, Samsung, CATT(if more than 56 SSB with 120kHz), ZTE/Sanechips, Futurewei (for 120kHz), Nokia, NEC, Panasonic, ETRI, Intel, Sharp (for 120kHz), NTT Docomo, WILUS (for 120kHz), OPPO, LGE, Xiaomi, Lenovo/Motorola Mobility
  + Do not support: Ericsson, CATT (for 480/960kHz) Futurewei (for 480/960kHz), Charter, Qualcomm (for 480/960kHz)
* Indication of licensed and unlicensed operation:
  + Raster: Samsung, OPPO, Interdigital
  + No distinction: Intel, Qualcomm, ZTE/Sanechips, Ericsson, Huawei/HiSilicon
* Indication of LBT
  + MIB: Huawei/HiSilicon, Interdigital, CATT, Futurewei, OPPO, Xiaomi
  + Other than MIB (e.g. SIB1): vivo, CATT, Ericsson, Nokia/NSB, Intel, Qualcomm, MTK, LGE, Lenovo/Motorola Mobility, Huawei/HiSilicon (Raster)
* Indication of DBTW (for initial access)
  + Implicit:
    - MIB: ~~Huawei/HiSilicon~~, vivo, Interdigital, Samsung, Intel, ZTE/Sanechips, NEC, Qualcomm, NTT Docomo, Panasonic, Lenovo/Motorola Mobility
    - raster: Interdigital, vivo, Nokia/NSB, LGE
    - NR-U solution: Huawei/HiSilicon
      * Comparison of Q in MIB and DBTW length in SIB1. Assume DBTW enabled before reading SIB1.
  + Explicit:
    - Sony (jointly coded with ), Futuerwei, Samsung (jointly coded with ), Ericsson (if DBTW supported, then DBTW on/off jointly coded with )
* Supporting means of conveying candidate SSB location & SSB beams
  + Supported values:
    - 2 values: Qualcomm, NTT Docomo (64 and smaller), OPPO, Xiaomi, Ericsson (if DBTW supported)
    - {8,64}: Intel
    - 4 values: Huawei/HiSilicon, Interdigital, Sony, Qualcomm, Intel, Xiaomi, Futurewei
    - {4,8,16,64}: Intel
    - {8,16,32,64}: Huawei/HiSilicon, ZTE/Sanechips, LGE, Lenovo/Motorola Mobility, Sony (if indication of DBTW is not jointly coded with )
    - {16, 32,64,reserved}: Sony (if indication of DBTW is jointly coded with and number of candidate is >64)
    - {8, 16,32,reserved}: Sony (if indication of DBTW is jointly coded with and number of candidate is 64)
  + Support explicit indication of SSB index and/or SSB candidate location
    - Nokia
* Supported DBTW lengths
  + {0.5, 1, 2, 3, 4, 5}msec for all SCS (as in NR-U)
    - vivo, Futurewei, Nokia, Charter (if DBTW is supported), Xiaomi, Qualcomm (120 kHz), NTT Docomo, ZTE/Sanechips, LGE, NEC, Lenovo/Motorola Mobility, Ericsson (if DBTW supported), Sony
  + 5 msec
    - Intel, CATT
  + 120 kHz SCS: {40, 32, 24, 16, 8, 4} slots = {5, 4, 3, 2, 1} ms
    - Huawei/HiSilicon
  + 480 kHz SCS: {72, 32, 24, 16, 8, 4} slots = {2.25, 1, 0.75, 0.5, 0.25, 0.125} ms
    - Huawei/HiSilicon
  + 960 kHz SCS: {64, 32, 24, 16, 8, 4} slots = {1, 0.5, 0.375, 0.25, 0.125, 0.0625} ms
    - Huawei/HiSilicon
* Number of SSB candidates for DBTW
  + For 120kHz:
    - 64: vivo, CATT(for no LBT/no DBTW cases), Futurewei. Charter (if DBTW is supported), NTT Docomo, Xiaomi, Qualcomm, Panasonic, MTK, LGE, Ericsson (if DBTW supported), Huawei/HiSilicon
    - > 64: Convida
    - 80: Intel, Sony, CATT (for LBT/DBTW cases), Nokia, NEC, ZTE/Sanechips, OPPO
  + For 480kHz:
    - 64: Charter (if DBTW is supported), NTT Docomo, Xiaomi, Qualcomm, Panasonic, MTK, LGE, Lenovo/Motorola Mobility, Futurewei
    - > 64: Convida
    - 80: Nokia
    - 128: vivo, Intel, Sony, Samsung, ZTE/Sanechips, Nokia, NEC, Huawei/HiSilicon
  + For 960kHz:
    - 64: LGE
    - 80: Nokia
    - 128: Nokia, NEC, Lenovo/Motorola Mobility, Huawei/HiSilicon
* DCI sizes between licensed and unlicensed
  + Same size for DCI 1\_0: Ericsson, Qualcomm, LGE, Intel (for SI-RNTI)
  + Same size for DCI 0\_0: Qualcomm
  + Different size for DCI 1\_0: Apple (if joint encoding of Q and licensed/unlicensed band indication is not possible)

#### **1st Round Discussion:**

Please provide comments on the above summary (including aspects that are missing, aspects captured incorrectly, etc). Moderator will provide a suggested proposal once the summary captures all company opinion correctly.

If the above summary is directly edited (please use a color to highlight changes, e.g. RED) and mention the changes/additions in the comment below.

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | * For the number of candidate SSBs, we have a question on the motivation to support at most 64 candidate SSBs when DBTW is on. In our understanding, for FR2-2, there is no strong motivation to support a small number of SSB beams, and very likely in implementation, the number of SSB beams will be larger than 32, then the utilization of DBTW with only 64 candidate SSB locations is indeed limited, and that’s the reason we support more than 64 candidate SSB locations when DBTW is on. * For the SCS applicable to DBTW, we want to address that short control signaling is not globally applicable to all the regions, and there are regions requiring LBT as mandatory procedure for channel access, so the application of DBTW should be for all supported SCSs. Also, some companies mentioned the duty cycle of SSB when using 480/960 is small than the requirement of short control signaling, but it’s not a correct observation. The 20 ms periodicity of SSB is only for initial access and from the UE perspective, but the calculation of duty cycle should be from the cell perspective (i.e., channel utilization). In this sense, if gNB configures a 5 ms periodicity for SSB, there are lots of scenarios for 480/960 kHz SCS cannot satisfy the short control signaling duty cycle. * For the indication of Q, we are not sure whether current MIB can have sufficient number of bits that can be re-interpreted for this purpose. I believe we can utilize similar approach as NR-U: using MIB as the best effort, otherwise use SIB1. * For the DCI 1\_0 size issue, one way is aligning the DCI 1\_0 size for operation with/without shared spectrum channel access, and another way could be indicating operation with/without shared spectrum channel access in MIB (no need to know the value of Q). * We also want a clarification on the proposal of using sync raster to indicate DBTW on/off. In our understanding, DBTW on/off is a semi-static configuration, but sync raster is fixed, so we are not sure how to utilize sync raster to indicate DBTW on/off. Our proposal is to use sync raster to indicate licensed/unlicensed, since it’s a fixed information. |
| Qualcomm | Please see our added support above using “Qualcomm” |
| Panasonic | Please see our added support above using “Panasonic” |
| Mediatek | Please see our added support above using “MTK” |
| Docomo | * For # of candidate SSB positions, the reason why we propose up to 64, which is same as FR2, is because we see remaining MIB fields and PBCH payload are quite limited. We do not strongly prefer to have a significant change on the interpretation of these fields either. On the other hand, we can understand Samsung’s first point. Since DBTW functionality is important from our perspective, we are relatively open to whether 64 or more about # of candidate SSB positions. We would like to hear more views from companies. * We would like to echo Samsung’s 2nd point regarding DBTW per SCS. Since short control signaling is not global rule, “treated as short control signaling” would not justify not to support DBTW. * For Q value indication, of course more variety gives us more flexibility on operation, while we doubt the feasibility in terms of the remaining MIB/PBCH payload available. *subCarrierSpacingCommon* can clearly repurposed for Q as well as Rel-16 NR-U since same SCS is assumed between SSB and CORESET#0. Otherwise use SIB for Q is fine for us. * For the indication of licensed/unlicensed and LBT on/off, our preference is to combine them with Q value single all of them are associated with same aspect and Q value is something already supported in NR. |
| ZTE/Sanechips | Please see our added support above using “ZTE/Sanechips” |
| Nokia | As there are regions where LBT is required, and short control signaling may not be applied (either by rule or due to limitations e.g. in case of 120kHz). Hence DBTW support would seem preferable. If DBTW is supported, our concern is that especially with 120 kHz SCS, there is limited number of available additional candidate location for all SSBs when more than 32 SSBs are used (i.e. =80). It’s expected that at the frequency range of interest the system should be designed to have 64 SSBs. Thus, limiting the DBTW operation only to low number of beams seems counter-intuitive. Hence, if, based on majority view, the based approach is selected, we would like to see also =64 supported.  For the number of candidate locations, we updated the FL summary above to account also the 960kHz case. In terms of total number of SSB candidate locations, we would be fine to assume 128 for 480kHz and 960kHz, but if we want to align with 120kHz sub-carrier spacings, also 80 could be considered.  For the DCI size, we were considering that as the double hypothesis applies only in cell selection phase, assuming two different sizes only in the initial phase would not be overly complex. |
| OPPO | Please see our added support above using “OPPO” |
| LG Electronics | Our views are added above.  Regarding DBTW enabling/disabling, we’d like to clarify how it can be implicitly indicated by using MIB. Does it mean that if MIB indicates Q less than 64, DBTW is enabled, otherwise DBTW is disabled?  Our main concern for more than 64 SSB candidate positions is whether PBCH payload can indicate 7 digits for more than 64 SSB candidate positions. If it will be resolved, we can consider more than 64 SSB candidate positions. |
| NEC | Please see our added support above using “NEC” |
| Xiaomi | Please see our added support above using “Xiaomi” |
| Lenovo, Motorola Mobility | Please see our added support above using “Lenovo/Motorola Mobility” |
| Futurewei | Please see our added support above using “Futurewei” |
| Ericsson | Please see our added support above using "Ericsson"  Our strong view is that we cannot agree to support DBTW for any SCS unless a conclusion is reached on the following two aspects since they directly affect the number of bits in MIB that can be repurposed. So far we have not seen a complete solution, and we are skeptical that enough bits can be found. We have trouble agreeing until a complete solution is on the table (including resolved dependencies to other working groups, e.g., RAN4):   1. If and how additional candidate SSB positions (>64) are to be supported, and 2. How to signal the following: Q and DBTW on/off   Our view on the above two aspects is:   * 64 candidate SSB positions in order to reuse the FR2-based signaling of SSB index * DBTW on/off needs to be provided in MIB which is aligned with previous agreement saying the following:   + If DBTW is supported     - Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs * LBT on/off can be signaled in SIB1 * DCI 1\_0 size is the same for both licensed and unlicensed. Alternatively, if it is desired to maintain different DCI 1\_0 sizes (as in Rel-16 NR-U) and it is acceptable for the UE to perform two blind decodes on DCI 1\_0 with CRC scrambled by SI-RNTI, that is okay too. * Any MIB bits that are repurposed for signaling of Q and DBTW on/off must be unused for both licensed and unlicensed operation in order for the UE to correctly determine the MIB for both licensed or unlicensed   + One such bit that can be repurposed for sure is *subCarrierSpacingCommon* since only (120,120), (480,480), and (960,960) combinations are supported |
| CATT | Please see our added support above using “CATT” |
| InterDigital | Please see our added support above using “Interdigital”.  For the indication of licensed/unlicensed, DBTW enable/disable, and LBT on/off, we propose to jointly indicate the mode of operation based on the combination of sync. raster offset and MSB of controlResourceSetZero. |
| Sony | Please see our added support above using “Sony”  As for values, it should depend on whether indication of DBTW is jointly or not jointly coded with . Although our 1st preference is that indication of DBTW is jointly coded with , we added our 2nd preference in the case that indication of DBTW is not jointly coded with . |
| Huawei/HiSilicon | * Regarding the issues addressed in the above summary: We have made some addition/modifications using “Huawei/HiSilicon”   + **Supporting DBTW:** We would like to echo the views of some other companies that short control signaling exemption is not supported in all regions and may not be used to justify that DBTW is not required for 480/960 kHz. Also, as Samsung has mentioned above, assuming that 480/960 kHz SSB burst satisfies the max 10% channel occupation every 100 ms is not accurate. 10% channel occupation should be satisfied from the transmitting equipment perspective (gNB) and is not based on the receiving equipment assumption (UE).   + **Indication of licensed and unlicensed operation:** We would like to have some clarification as to why such an indication is important during initial access. In our view, what may be important for the UE during initial access is to know whether LBT is on or off to resolve the ambiguity in the size of DCI 1\_0 scrambled with SI-RNTI. If LBT on/off is indicated to the UE or the ambiguity in DCI 1\_0 size is resolved by other means, we do not see why UE further need to know if it is operating in shared or unshared spectrum during initial access.   + **Indication of LBT:** During initial access, it is required for resolving the ambiguity in the size of DCI 1\_0 scrambled with SI-RNTI. We suggest indication using synch raster. If ambiguity in the size of DCI 1\_0 scrambled with SI-RNTI is resolved using above solution or any other means, we do not see a strong motivation to indicate LBT/no-LBT to UE before UE reads SIB1.   + **Indication of DBTW:** DBTW enabled/disabled is never explicitly indicated to the UE in Rel-16 NR-U. In Rel-16, UE can infer whether DBTW is enabled/disabled only after reading SIB1 by comparing the maximum number of transmitted SSB indexes (acquired from MIB payload) with the DBTW length (*DiscoveryBurst-WindowLength* provided in SIB1). If DBTW length that is configured in SIB1 is such that DBTW can include more than candidate SSB indexes, UE can infer that DBTW is enabled. In turn, if DBTW length that is configured in SIB1 is such that DBTW cannot include more than candidate SSB indexes, UE can infer that DBTW is disabled. Before reading SIB1, UE assumes that DBTW length is a half frame (includes all candidate SSB positions), and, as such, DBTW is enabled.   It is unclear for us why above mechanism is not also usable in 60 GHz. As such, we added the option of using NR-U solution in above summary.   * + **Supported DBTW lengths:** As discussed above, supported DBTW lengths should be such that, when compared to the values of , UE can infer whether it is enabled or disabled. As we explained in our tdoc in details, since the time interval containing SSB indexes are different in 120, 480, 960 kHz, it is preferable to support different sets of DBTW for different SCSs.   + **Number of SSB candidates for DBTW:** For 120 kHz, we prefer not to change Case D SSB pattern. DBTW is still useful if the number of transmitted SSB indexes is less than 64. For 480 and 960 kHz, up to 128 candidate SSB indexes can be supported by indicating the 7th bit of the candidate SSB index by borrowing the 4th LSB of SFN in the PBCH payload and indicating the 4th LSB of SFN in MIB payload. Note that this does not reduce the periodicity of MIB payload below the current 80 ms. * In addition, we find it important that the following two issues to be discussed in this meeting:   + How to indicate additional Candidate SSB indexes if   How to interpret ssb-PositionsInBurst configured in SIB1 in relation to the indicated value of . |

#### **1st Round Discussion Summary:**

**Issue 1)** On the support of DBTW, there is clear majority for at least 120kHz cases (see below). Suggest discussing further on Proposal 1.1-1 and if possible, agree to it or some modification of it.

|  |
| --- |
| * Supporting DBTW   + Support: Huawei/HiSilicon, vivo, Spreadtrum (for 120kHz), Interdigital, Sony, Samsung, CATT(if more than 56 SSB with 120kHz), ZTE/Sanechips, Futurewei (for 120kHz), Nokia, NEC, Panasonic, ETRI, Intel, Sharp (for 120kHz), NTT Docomo, WILUS (for 120kHz), OPPO, LGE, Xiaomi, Lenovo/Motorola Mobility   + Do not support: Ericsson, CATT (for 480/960kHz) Futurewei (for 480/960kHz), Charter, Qualcomm (for 480/960kHz) |

**Proposal 1.1-1)**

* Support DBTW at least for 120kHz
  + FFS whether DBTW will be applicable for 480/960 kHz SSB SCS

**Issue 2)** For indication of licensed/unlicensed, LBT/no LBT, and DBTW/no DBTW cases. Companies are somewhat split, but there are certain options that have greater support. The DCI size handling for licensed and unlicensed seems to related to the same issue as well. Suggest discussing further on Proposal 1.1-2 and if possible, agree to it or some modification of it.

|  |
| --- |
| * Indication of licensed and unlicensed operation:   + Raster: Samsung, OPPO, Interdigital   + No distinction: Intel, Qualcomm, ZTE/Sanechips, Ericsson, Huawei/HiSilicon * Indication of LBT   + MIB: Huawei/HiSilicon, Interdigital, CATT, Futurewei, OPPO, Xiaomi   + Other than MIB (e.g. SIB1): vivo, CATT, Ericsson, Nokia/NSB, Intel, Qualcomm, MTK, LGE, Lenovo/Motorola Mobility, Huawei/HiSilicon (Raster) * Indication of DBTW (for initial access)   + Implicit:     - MIB: ~~Huawei/HiSilicon~~, vivo, Interdigital, Samsung, Intel, ZTE/Sanechips, NEC, Qualcomm, NTT Docomo, Panasonic, Lenovo/Motorola Mobility     - raster: Interdigital, vivo, Nokia/NSB, LGE     - NR-U solution: Huawei/HiSilicon       * Comparison of Q in MIB and DBTW length in SIB1. Assume DBTW enabled before reading SIB1.   + Explicit:     - Sony (jointly coded with ), Futuerwei, Samsung (jointly coded with ), Ericsson (if DBTW supported, then DBTW on/off jointly coded with ) * DCI sizes between licensed and unlicensed   + Same size for DCI 1\_0: Ericsson, Qualcomm, LGE, Intel (for SI-RNTI)   + Same size for DCI 0\_0: Qualcomm   + Different size for DCI 1\_0: Apple (if joint encoding of Q and licensed/unlicensed band indication is not possible) |

**Proposal 1.1-2)**

* No indication for licensed and unlicensed operation will be performed in SSB (including MIB)
* Use of LBT by the cell and UEs connected to the cell is not indicated MIB.
  + FFS where and how this is indicated, e.g. SIB1
* For supported SCS cases of DBTW, the indication of use or no use of DBTW will be implicitly indicated (deriving that DBTW is used or not used via configuration of MIB (and SIB1) parameter(s) in certain combinations) in MIB.
  + FFS details of implicit indication in MIB (and in SIB1)
* For both licensed or unlicensed operation and with or without LBT, support the same DCI size for:
  + DCI format 1\_0 scrambled with SI-RNTI
  + FFS for DCI format 1\_0 scrambled with other RNTI, and other DCI formats

**Issue 3)** For means of conveying candidate SSB location & SSB beams, majority of the companies seem to prefer NR-U based approach. Suggest discussing further on Proposal 1.1-3 and if possible, agree to it or some modification of it.

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| --- |
| * Supporting means of conveying candidate SSB location & SSB beams   + Supported values:     - 2 values: Qualcomm, NTT Docomo (64 and smaller), OPPO, Xiaomi, Ericsson (if DBTW supported)     - {8,64}: Intel     - 4 values: Huawei/HiSilicon, Interdigital, Sony, Qualcomm, Intel, Xiaomi, Futurewei     - {4,8,16,64}: Intel     - {8,16,32,64}: Huawei/HiSilicon, ZTE/Sanechips, LGE, Lenovo/Motorola Mobility, Sony (if indication of DBTW is not jointly coded with )     - {16, 32,64,reserved}: Sony (if indication of DBTW is jointly coded with and number of candidate is >64)     - {8, 16,32,reserved}: Sony (if indication of DBTW is jointly coded with and number of candidate is 64)   + Support explicit indication of SSB index and/or SSB candidate location     - Nokia |

**Proposal 1.1-3)**

* For supported SCS cases of DBTW, support configuration of in MIB, with following {8,16,32,64} values

**Issue 4)** For Supported DBTW lengths clear majority supports the same lengths as in NR-U. Suggest discussing further on Proposal 1.1-4 and if possible, agree to it or some modification of it.

**Proposal 1.1-4)**

* For supported SCS cases of DBTW, support DBTW lengths {0.5, 1, 2, 3, 4, 5} msec
  + Note: this should be the same as Rel-16 NR-U DBTW lengths.

**Issue 5)** For number of SSB candidates for DBTW, support of DBTW for 480/960kHz is pending, but we could further discuss for the 120kHz case. There is larger support for 64 candidates for 120kHz, compared to 80 candidates (10 companies vs 7 companies). Moderator thinks some further discussion would be helpful. Maybe companies can elaborate bit further the concerning aspect of the proposal not supported (so that we get better understanding where the core issues lie). Suggest discussing further on Proposal 1.1-5 and if possible, down-select between alt 1 and 2.

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| * Number of SSB candidates for DBTW   + For 120kHz:     - 64: vivo, CATT(for no LBT/no DBTW cases), Futurewei. Charter (if DBTW is supported), NTT Docomo, Xiaomi, Qualcomm, Panasonic, MTK, LGE, Ericsson (if DBTW supported), Huawei/HiSilicon     - > 64: Convida     - 80: Intel, Sony, CATT (for LBT/DBTW cases), Nokia, NEC, ZTE/Sanechips, OPPO   + For 480kHz:     - 64: Charter (if DBTW is supported), NTT Docomo, Xiaomi, Qualcomm, Panasonic, MTK, LGE, Lenovo/Motorola Mobility, Futurewei     - > 64: Convida     - 80: Nokia     - 128: vivo, Intel, Sony, Samsung, ZTE/Sanechips, Nokia, NEC, Huawei/HiSilicon   + For 960kHz:     - 64: LGE     - 80: Nokia     - 128: Nokia, NEC, Lenovo/Motorola Mobility, Huawei/HiSilicon |

**Proposal 1.1-5)**

* For 120kHz SSB, the number of candidates for DBTW is:
  + Alt 1) 64
  + Alt 2) 80

#### **2nd Round Discussion:**

Please provide comments for Proposals 1.1-1 ~ 1.5 (copied below for convenience).

##### **Proposal 1.1-1)**

* Support DBTW at least for 120kHz
  + FFS whether DBTW will be applicable for 480/960 kHz SSB SCS

##### **Proposal 1.1-2)**

* No indication for licensed and unlicensed operation will be performed in SSB (including MIB)
* Use of LBT by the cell and UEs connected to the cell is not indicated MIB.
  + FFS where and how this is indicated, e.g. SIB1
* For supported SCS cases of DBTW, the indication of use or no use of DBTW will be implicitly indicated (deriving that DBTW is used or not used via configuration of MIB (and SIB1) parameter(s) in certain combinations) in MIB.
  + FFS details of implicit indication in MIB (and in SIB1)
* For both licensed or unlicensed operation and with or without LBT, support the same DCI size for:
  + DCI format 1\_0 scrambled with SI-RNTI
  + FFS for DCI format 1\_0 scrambled with other RNTI, and other DCI formats

##### **Proposal 1.1-3)**

* For supported SCS cases of DBTW, support configuration of in MIB, with following {8,16,32,64} values

##### **Proposal 1.1-4)**

* For supported SCS cases of DBTW, support DBTW lengths {0.5, 1, 2, 3, 4, 5} msec
  + Note: this should be the same as Rel-16 NR-U DBTW lengths.

##### **Proposal 1.1-5)**

* For 120kHz SSB, the number of candidates for DBTW is:
  + Alt 1) 64
  + Alt 2) 80

|  |  |
| --- | --- |
| Company | Comments |
| vivo | **Proposal 1.1-1**: Support. As mentioned by several companies, short control signaling is not available in all regions. We prefer to support DBTW for all SCSs.  **Proposal 1.1-2**: Partially support  On licensed/unlicensed indication, we think it is too early to conclude this since it is unknown that we could achieve a totally common design for licensed and unlicensed operation;  On LBT indication, we support the proposal;  On DBTW on/off indication, we support the proposal;  On DCI 1\_0 size, whether to have the same size for licensed and unlicensed depends on whether to have licensed/unlicensed indication in SSB, which is preferred to be determined later. We support the same DCI 1\_0 size for unlicensed operation with or without LBT. One more comment is that DCI 1\_0 size is not bundled with RNTI but CSS or USS. So we suggest to change “DCI format 1\_0 scrambled with SI-RNTI” to “DCI format 0\_0 monitored in a common search space”.  **Proposal 1.1-3:** Support  **Proposal 1.1-4:** Support  **Proposal 1.1-5:** Support |
| DOCOMO | **Proposal 1.1-1**: ok to support for 120k SCS at first. We also prefer to support DBTW for all SCSs.  **Proposal 1.1-2**:  On licensed/unlicensed indication, we are fine with not indicating in MIB;  On LBT indication, we are open since it may be implicitly indicated in a certain MIB field;  On DBTW on/off indication, we support the proposal;  On DCI 1\_0 size, open to further discuss  **Proposal 1.1-3:** Support  **Proposal 1.1-4:** Support  **Proposal 1.1-5:** Support Alt 1. |
| Spreadtrum | * + 1. Support     2. FFS. It is related to in MIB, since we don’t know whether there is a bit reserved for the indication of disable/enable DBTW or LBT     3. Support configuration of in MIB. FFS the values.     4. Support multiple candidates of DBTW length. FFS the values.   Support 64 |
| Nokia | Proposal 1.1-1: We would be fine with this proposal.  Proposal 1.1-2: (Assuming that this proposal would be packet with 1.1-1). Regarding the DCI format 1\_0, we don’t see it necessary to align the sizes. The dual hypothesis exists only for the first SIB1 reception. Beyond that we can take this proposal to progress the work.  Proposal 1.1-3: This is evidently majority view, but we would prefer to take this as a working assumption as we need to further consider how the method can be made to operate if Alt 2 of Proposal 1.1-5 is adopted.  Proposal 1.1-4: OK.  Proposal 1.1-5: Our preference would be alt 2. As expressed earlier, as the short control signal exemption cannot always be used and does not cover all SSBs in case of 120kHz, thus supporting DBTW in case of higher number of beams would be preferred. |
| LG Electronics | Proposal 1.1-1) Support but prefer to introduce DBTW for 480/960 kHz SCS as well  Proposal 1.1-2) We still fail to understand how DBTW enabling/disabling can be implicitly indicated by MIB. According to explanation from Huawei, we could understand how UE can infer whether DBTW is enabled/disabled by using SIB1 configuration. However, implicit mechanism by using MIB should be clarified first.  Proposal 1.1-3) Support  Proposal 1.1-4) Support  Proposal 1.1-5) Prefer Alt 1, considering additional 1 bit is need to indicated increased SSB candidate positions |
| ZTE, Sanechips | **Proposal 1.1-1**: Support. We prefer to support DBTW for 480/960 kHz as well.  **Proposal 1.1-2**: Support.  **Proposal 1.1-3:** Support  **Proposal 1.1-4:** Support  **Proposal 1.1-5:** Support. Further, we prefer Alt 2. |
| Samsung | Proposal 1.1-1) We are ok with the proposal, and we support it for 480/960 kHz SCS as well.  Proposal 1.1-2)   * For unlicensed/licensed indication, we are ok with no using MIB to indicate such information, but RAN1 shall not add any intention to prevent RAN4 on the sync raster design. So the wording can be changed to “No indication for licensed and unlicensed operation ~~will be performed in SSB (including MIB)~~ in MIB” * For the indication of LBT, we are ok with the proposal. * For the indication of DBTW, we don’t agree with the proposal. The key issue is, a UE should be able to know whether DBTW is on or off before monitoring Type0-PDCCH, since the monitoring behavior is not the same (e.g. whether to apply Q). Any approach needing the information from SIB1 cannot achieve the purpose. Q is only applicable when DBTW is on, so we don’t understand why we need to indicate Q in MIB even without knowing whether the DBTW is on or off. We still support the proposal of joint coding DBTW off and Q values. * For DCI size, we are ok.   Proposal 1.1-3) As mentioned in the comment in Proposal 1.1-2), Q value is only applicable when DBTW is on, so we don’t think Proposal 1.1-3) is compatible with Proposal 1.1-2). Also, the value of Q depends on the decision of the number of candidate SSB locations, e.g. if the max is 64, and Q doesn’t need to take a value of 64.  Proposal 1.1-4) We are ok with the proposal.  Proposal 1.1-5) We are ok with the proposal, but we wonder what’s the different from the FFS in the last meeting’s agreement “FFS between 64 and 80”? Also this new proposal didn’t include proposal for 480 and 960, then it seems weaker than the agreement of last meeting.  Other than above, we also want to address companies’ concern on supporting larger than 64 number of candidate locations. TTI of MIB is 80 ms, so the 4th LSB of SFN can be re-interpreted for indicating the extra MSB of candidate SSB index and use a MIB bit to indicate the 4th LSB of SFN. This doesn’t impact other indication of timing in PBCH payload and using DMRS of PBCH. |
| Intel | **Proposal 1.1-1)** - agree  **Proposal 1.1-2)** - agree  **Proposal 1.1-3)** – don’t agree. Our first preference is the set of 2 values for as its indication in MIB would require only 1 bit.  The set of 2 values for would assume a small number of beams and a large number of beams. All cases in between could be configured by SSB presence pattern. It’s straightforward to put the large number for equal to the max, i.e., 64 for all SSB SCS. Regarding the small value, we think it should depend on the SCS. For example, in case of SSB SCS 480 kHz/960 kHz, there are no strong reasons to operate with a number of beams 8 (the current max for NR-U Rel-16). Therefore, we propose for SSB SCS 480 kHz/960 kHz. For SSB SCS 120 kHz, the smaller value could be lowered, i.e., .  **Proposal 1.1-4)** – don’t agree. In our understanding, the support of multiple DBTW lengths would require some kind of indication of exact value of DBTW length from the set. This what we try to avoid by proposing a single fixed DBTW length equal to 5 ms.  **Proposal 1.1-5)** – agree. Our preference is Alt.2.  As we showed in our tdoc, it is possible to provide additional SSB candidates for SSB SCS 120 kHz (i.e., with indices 64~79) without affecting the ordering of legacy SSB candidates (i.e., with indices 0~63). One additional bit would be required in the MIB to indicate an index of the larger number of candidate SSBs. This could be done via repurposing the *subCarrierSpacingCommon* bit as SCS for SSB and CORESET#0 has been agreed to always the same for NR in FR2-2. |
| NEC | Proposal 1.1-1) Support, and prefer to support DBTW for all SCSs  Proposal 1.1-2) Support except the indication of DBTW. We share the similar views on joint coding DBTW indication and Q values.  Proposal 1.1-3) Support and FFS the values of Q.  Proposal 1.1-4) Support.  Proposal 1.1-5) Support and prefer Alt 2. |
| Apple | **Proposal 1.1-1: Ok for us.**  **Proposal 1.1-2:** We shared the concern raised by LGe. Our recommendation is to discuss implicit indication solution together with explicit indication directly, instead of agreeing with it and keep FFS on how it works.  **Proposal 1.1-3:** Support. Meanwhile, our understanding is that this proposal has impact on Proposal 1.1-2. Proposal 1.1-2 is reasonable if we conclude to not support explicit indication of DBTW window present using joint coding approach.  **Proposal 1.1-4:** Support.  **Proposal 1.1-5:** Our preference is Alt.1, 64. |
| Convida Wireless | Proposal 1.1-1: We are ok with the proposal.  Proposal 1.1-2: We are ok with the proposal.  Proposal 1.1-3: We are ok with the proposal.  Proposal 1.1-4: We are ok with the proposal.  Proposal 1.1-5: We are ok with the proposal. Our preference is Alt.2, 80. |
| Qualcomm | Proposal 1.1-1: fine for sake of progress  Proposal 1.1-2: generally fine with the proposal, however, implicit DBTW ON/OFF may make sense for MIB but may need further considerations for SIB1, hence we prefer the following:   * *For supported SCS cases of DBTW, the indication of use or no use of DBTW will be implicitly indicated (deriving that DBTW is used or not used via configuration of MIB ~~(and SIB1)~~ parameter(s) in certain combinations) in MIB.*   + *FFS for SIB1*   Proposal 1.1-3: since Proposal 1.1-2 assumes DBTW enable disable may be implicit in MIB (Q value), the maximum need to be similar to the number of candidate SSB locations (to disable) which depends on status of Proposal 1.1-5. Suggest we treat this proposal after we treat Proposal 1.1-2 and Proposal 1.1-5. In addition, we may need to conclude on the number of available MIB signaling bits first, since we may only have 1 bit and that leave 2 values only.  Proposal 1.1-4: fine with the proposal  Proposal 1.1-5: We still need gaps for UL/DL switching and other URLLC data. Hence prefer Alt 1. |
| Futurewei | **Proposal 1.1-1**: Support. On DCI 1\_0 size, open to further discuss  **Proposal 1.1-2**: Support.  **Proposal 1.1-3:** Support  **Proposal 1.1-4:** Support  **Proposal 1.1-5:** Support. We prefer Alt 1 (64). |
| Ericsson | **Proposal 1.1-1**  As we commented in the 1st round, we object to supporting DBTW for any SCS until a full solution is available, including exactly which MIB bits are repurposed and/or resolution of potential dependencies to RAN4  The solution must include:   1. If and how additional candidate SSB positions (>64) are to be supported, and 2. How to signal the following: Q and DBTW on/off   We are certainly open to continuing the discussion on the solution for 1 and 2, but until there is convergence, we cannot agree to support DBTW  **Proposal 1.1-2**  We support the proposal (wiht, except for the following:   * ~~For supported SCS cases of DBTW, the indication of use or no use of DBTW will be implicitly indicated (deriving that DBTW is used or not used via configuration of MIB (and SIB1) parameter(s) in certain combinations) in MIB.~~   + ~~FFS details of implicit indication in MIB (and in SIB1)~~   As we commented in the first round, this reverts the following part of the agreement from RAN#104, and the reason for this agreement is that even for unlicensed operation, it allows the DBTW to be disabled for deployments that don't need it.   * If DBTW is supported   + Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs     - FFS: how to support UEs performing initial access that do not have any prior information on DBTW.   During initial access, IDLE mode UEs have not yet read SIB1, so the above solution does not work. In our view, the preferred solution is to indicate DBTW on/off using a MIB bit. Some companies have suggested using a different sync raster positions for indicating DBTW on/off, but clearly there is a RAN4 dependency, and we cannot assume that RAN4 follows that design.  Furthermore, we think there is a different understanding amongst companies of what "implicit" means. Some companies refer to implicit as using a particular value of Q to indicate DBTW off, e.g., Q = 64. We support such a mechanism.  **Proposal 1.1-3**  We cannot agree to this proposal until it is identified which bits in MIB can be repurposed . For signaling 4 values of Q, 2 bits needed. So far, we have only seen that there is 1 bit available, namely *subCarrierSpacingCommon*  **Proposal 1.1-4**  We support this proposal with the following modification:  For supported SCS cases of DBTW (if supported), support DBTW lengths {0.5, 1, 2, 3, 4, 5} msec  **Proposal 1.1-5**  This proposal has already been agreed in the prior meeting |
| Huawei, HiSilicon | **Proposal 1.1-1:** Support. Although we believe that DBTW should be supported for all numerologies.  **Proposal 1.1-2:**   * First bullet: We can support this with the clarification that indication of licensed/unlicensed and indication of LBT/No-LBT are two different issues as a system in unlicensed spectrum may or may not use LBT. Therefore, we propose the following clarification:   + No indication for licensed and unlicensed operation will be performed in SSB (including MIB)     - Whether and/or how LBT/No-LBT is indicated is separately discussed. * Second bullet: Support * Third bullet: Support with the following change:   + For supported SCS cases of DBTW, the indication of use or no use of DBTW will be implicitly indicated (~~deriving that~~ DBTW is used or not used is derived via configuration of MIB (and SIB1) parameter(s) in certain combinations) ~~in MIB~~.     - UE assumes DBTW is used prior to deriving implicit indication (Rel-16 NR-U behavior)     - FFS details of implicit indication in MIB (and in SIB1) * Fourth bullet: We can support it for the sake of progress.   **Proposal 1.1-3:** Support  **Proposal 1.1-4:** We cannot support it.  We believe that a similar method as in Rel-16 NR-U should be used to implicitly indicate whether DBTW is enabled or disabled and, if DBTW lengths {0.5, 1, 2, 3, 4, 5} msec is used for all SCSs, such implicit indication would be completely dysfunctional.  Rel-16 NR-U behavior: As explained before in the first round, DBTW enabled/disabled is never explicitly indicated to the UE in Rel-16 NR-U. In Rel-16, UE can infer whether DBTW is enabled/disabled only after reading SIB1 by comparing the maximum number of transmitted SSB indexes (acquired from MIB payload) with the DBTW length (*DiscoveryBurst-WindowLength* provided in SIB1). If DBTW length that is configured in SIB1 is such that DBTW can include more than candidate SSB indexes, UE can infer that DBTW is enabled. In turn, if DBTW length that is configured in SIB1 is such that DBTW cannot include more than candidate SSB indexes, UE can infer that DBTW is disabled. Before reading SIB1, UE assumes that DBTW length is a half frame (includes all candidate SSB positions), and, as such, DBTW is enabled.  Now, assume that DBTW is supported for 960 kHz and = {8,16,32,64} are supported as in Proposal 1.1-3. This means that the first (=8,16,32,64) can be mapped to the first (4, 8, 16, 32) slots where, for the sake of simplicity of the discussion, we assumed that no UL slots are reserved in the first 32 slots. (4, 8, 16, 32) slots in 960 kHz are (*0.0625, 0.125, 0.25, 0.5) ms.*This simply shows that if DBTW lengths {0.5, 1, 2, 3, 4, 5} msec are supported as in Rel-16, since the smallest supported DBTW value is 0.5 ms, UE assumes that DBTW is always enabled if is configured to be any value less than 64.  Other than above, there is also another major problem with supporting {0.5, 1, 2, 3, 4, 5} msec DBTW lengths especially for higher SCSs. Imagine (four slots of SSB) is configured for 960 kHz SCS. Do companies believe that a DBTW length as large as 5 msec is a viable choice for in 960 kHz? We don’t think so. DBTW = 5 msec for in 960 kHz means that UE assumes the pattern of 8 SSBs repeats 80 times!  **Proposal 1.1-5:** Support Alt 1.  A note to **Samsung** and **Qualcomm** regarding implicit indication of DBTW in MIB and SIB1 in Proposal 1.1-2, to our understanding, this is exactly Rel-16 NR-U behavior (please see our above explanation Rel-16 NR-U behavior). We don’t see why such behavior should change in 60 GHz. Please note that, similar to Rel-16 NR-U, UE should assume DBTW is used prior to deriving implicit indication. We suggested adding this UE assumption to the third bullet of Proposal 1.1.-2. |

#### **2nd Round Discussion Summary:**

From the comments companies Proposal 1.1-1 and 1.1-4 seem generally acceptable. Proposal 1.1-2, 1.1-3, and 1.1-5 seem connected in sense that depending on how many SSB candidates are supported, companies have slight different preferences on how to handle the implicit indication for DBTW enable/disable (including whether this is at all needed).

Moderator suggests to first tackle Proposal 1.1-1 and 1.1-4. Next discuss on the actual number of candidates Proposal 1.1-5, then further discuss how to narrow down the proposal even further based on Proposal 1.1-2 and 1.1-3.

**Proposal 1.1-1)**

* Support DBTW at least for 120kHz
  + FFS whether DBTW will be applicable for 480/960 kHz SSB SCS
* Ok: vivo, Docomo (apply to all SCS ), Spreadtrum, Nokia, LGE (apply to all SCS), ZTE/Sanechips (apply to all SCS), Samsung, Intel, NEC, Convida, Qualcomm, Futurewei, Huawei/HiSilicon (apply to all SCS)
* Not ok: Ericsson (information on exact bit composition in order to make proposal work is needed)

**Proposal 1.1-4A)**

* For supported SCS cases of DBTW (if supported), support DBTW lengths {0.5, 1, 2, 3, 4, 5} msec
  + Note: this should be the same as Rel-16 NR-U DBTW lengths.
* Ok: vivo, Spreadtrum, Nokia, LGE, ZTE, Samsung, NEC, Convida, Qualcomm, Futurewei, Ericsson
* Not ok: Intel (only support 5msec), Huawei/HiSilicon (need to scale with SCS)

Down-Select among Alt 1 and Alt 2 during GTW (if possible)

**Proposal 1.1-5)**

* For 120kHz SSB, the number of candidates for DBTW is:
  + Alt 1) 64
  + Alt 2) 80
* Alt 1: Docomo, Spreadtrum, LGE, NEC, Convida, Qualcomm, Futurewei, Huawei/HiSilicon
* Alt 2: Nokia, ZTE/Sanechips, Intel

Based on comments received Proposal 1.1-2 and 1.1-3 were updated to 1.1-2A and 1.1-3A.

**Proposal 1.1-2A)**

* No indication for licensed and unlicensed operation in MIB ~~will be performed in SSB (including MIB)~~
  + Whether and/or how LBT/No-LBT is indicated is separately discussed
* Use of LBT by the cell and UEs connected to the cell is not indicated MIB.
  + FFS where and how this is indicated, e.g. SIB1
* For supported SCS cases of DBTW, the indication of use or no use of DBTW will be implicitly indicated (~~deriving that~~ DBTW is used or not used is derived via configuration of MIB ~~(and SIB1)~~ parameter(s) in certain combinations) in MIB.
  + UE assumes DBTW is used prior to deriving implicit indication (Rel-16 NR-U behavior)
  + FFS details of implicit indication in MIB ~~(and in SIB1)~~
  + FFS whether information in SIB1 can be utilized to determine whether DBTW is enabled or disabled
* For both licensed or unlicensed operation and with or without LBT, support the same DCI size for:
  + ~~DCI format 1\_0 scrambled with SI-RNTI~~
  + DCI format 0\_0 monitored in a common search space
  + FFS for DCI format 1\_0 scrambled with other RNTI, and other DCI formats

Below are company preferences based on original proposal.

* Ok: vivo, ZTE/Sanechips, Intel, Convida, Qualcomm, Futurewei, Huawei/HiSilicon
* Maybe: Spreadtrum
* Not ok: NEC, Nokia (concern on DCI size aspect), LGE (concern on DBTW enable/disable), Samsung (concern on DBTW enable/disable), NEC (concern on DBTW enable/disable), Ericsson (DBTW enable/disable, need to clarify what implicit means)

**Proposal 1.1-3A)**

* For supported SCS cases of DBTW, support configuration of in MIB, with at least {16, 64}~~following~~ ~~{8,16,32,64}~~ values
  + FFS whether 64 can be replaced with disable of DBTW indication
  + No more than 4 states of value are to be supported.

Below are company preferences based on original proposal.

* Ok: vivo, Spreadtrum, Nokia (for alt 2 of proposal 5), LGE, ZTE/Sanechips, NEC, Convida, Futurewei, Huawei/HiSilicon
* Not ok: Samsung (only applicable with DBTW enabled), Intel (support only 2 values), Qualcomm (need to jointly assess proposal 1.1-2 and 1.1-3), Ericsson (information on exact bit composition in order to make proposal work is needed)

#### **Conclusion from GTW (Week 1 - Thursday):**

**Conclusion:**

RAN1 will continue discussion to develop solutions for supporting DBTW.

#### **3rd Round Discussion:**

Please provide comments for Proposals 1.1-4A, 1.1-5, 1.1-2A, and 1.1-3A (copied below for convenience).

For proposal 1.1-5, moderator’s goal is not to agree as written but somehow down-select between 64 vs 80. Companies are asked to provide ways to converge to a single proposal.

##### **Proposal 1.1-4A)**

* For supported SCS cases of DBTW (if supported), support DBTW lengths {0.5, 1, 2, 3, 4, 5} msec
  + Note: this should be the same as Rel-16 NR-U DBTW lengths.
* Ok: vivo, Spreadtrum, Nokia, LGE, ZTE, Samsung, NEC, Convida, Qualcomm, Futurewei, Ericsson, Lenovo/Motorola Mobility
* Not ok: Intel (only support 5msec), Huawei/HiSilicon (need to scale with SCS)

**Proposal 1.1-5)**

* For 120kHz SSB, the number of candidates for DBTW is:
  + Alt 1) 64
  + Alt 2) 80

##### **Proposal 1.1-2A)**

* No indication for licensed and unlicensed operation in MIB ~~will be performed in SSB (including MIB)~~
  + Whether and/or how LBT/No-LBT is indicated is separately discussed
* Use of LBT by the cell and UEs connected to the cell is not indicated MIB.
  + FFS where and how this is indicated, e.g. SIB1
* For supported SCS cases of DBTW, the indication of use or no use of DBTW will be implicitly indicated (~~deriving that~~ DBTW is used or not used is derived via configuration of MIB ~~(and SIB1)~~ parameter(s) in certain combinations) in MIB.
  + UE assumes DBTW is used prior to deriving implicit indication (Rel-16 NR-U behavior)
  + FFS details of implicit indication in MIB ~~(and in SIB1)~~
  + FFS whether information in SIB1 can be utilized to determine whether DBTW is enabled or disabled
* For both licensed or unlicensed operation and with or without LBT, support the same DCI size for:
  + ~~DCI format 1\_0 scrambled with SI-RNTI~~
  + DCI format 0\_0 monitored in a common search space
  + FFS for DCI format 1\_0 scrambled with other RNTI, and other DCI formats

##### **Proposal 1.1-3A)**

* For supported SCS cases of DBTW, support configuration of in MIB, with at least {16, 64}~~following~~ ~~{8,16,32,64}~~ values
  + FFS whether 64 can be replaced with disable of DBTW indication
  + No more than 4 states of value are to be supported.

**Issue 1)** DBTW lengths and potential values of DBTW

Several companies have outlined issues with applying existing DBTW lengths for 480 and 960kHz. Therefore, updated the Proposal 1.1-4A to be limited to 120kHz cases. For the actual values, companies supportive of the Q indication seems to support at least 2 values, and there are several companies who support up to 4 values. So updated the Proposal 1.1-3A to include all 3 cases.

**Proposal 1.1-4B)**

* For ~~supported SCS cases of~~ DBTW with 120kHz SCS (if supported), support DBTW lengths {0.5, 1, 2, 3, 4, 5} msec
  + Note: this should be the same as Rel-16 NR-U DBTW lengths.

##### **Proposal 1.1-3B)**

* For supported SCS cases of DBTW, support configuration of in MIB, with at least {16, 64}~~following~~ ~~{8,16,32,64}~~ values
  + ~~FFS whether 64 can be replaced with disable of DBTW indication~~
  + ~~No more than 4 states of value are to be supported.~~
  + Alt 1: 2 states of values are supported
  + Alt 2: two additional values, total of 4 states of values are supported
    - FFS on the two additional values
  + Alt 3: one addition value, and reserved state that indicates DBTW disabled, total of 3 states of values and 1 state of DBTW disabled are supported.

**Issue 2)** number of SSB candidate positions

There are more companies in favor of 64 values for 120kHz candidate SSB positions. Let’s see if can conclude in this direction.

**Proposal 1.1-5B)**

* For 120kHz SSB, the number of candidates SSBs in a half frame for DBTW is:
  + ~~Alt 1)~~ 64
  + ~~Alt 2) 80~~

The following is a summary of company views on 64 vs 80 candidate SSB positions.

* Alt 1: Docomo, Spreadtrum, LGE, ~~NEC,~~ ~~Convida~~, Qualcomm, Futurewei, Huawei/HiSilicon, Lenovo/Motorola Mobility, vivo, ZTE/Sanechips, Apple, OPPO, Panasonic
  + Concerns on Alt 2:
    - Ability to indicate the extra entries in MIB
* Alt 2: Nokia, ZTE/Sanechips, Intel, OPPO, NEC, Convida Wireless
  + Concerns on Alt 1:
    - When Q=64, DBTW will function as if it is disabled if only 64 candidate positions are available, therefore not able to handle cases when SSB cannot be transmitted due to LBT

**Issue 3)** LBT/DBTW indication aspects

The indication of DBTW in implicit or explicit manner seems to be the controversial question. So moderator has separated out the DBTW implicit vs explicit issue in Proposal 1.1-6. For the explicit DBTW enable/disable, based on comments and discussions so far, moderator assumes that UE would need to assume that DBTW is enabled until the UE has successfully decoded MIB. However, moderator would like to check this with proponents of explicit signaling.

##### **Proposal 1.1-2B)**

* No indication for licensed and unlicensed operation in MIB ~~will be performed in SSB (including MIB)~~
  + Whether and/or how LBT/No-LBT is indicated is separately discussed
* Use of LBT ~~by the cell and UEs connected to the cell~~ is not indicated in MIB.
  + FFS where and how this is indicated, e.g. SIB1
* ~~For supported SCS cases of DBTW, the indication of use or no use of DBTW will be implicitly indicated (deriving that DBTW is used or not used is derived via configuration of MIB (and SIB1) parameter(s) in certain combinations) in MIB.~~
  + ~~UE assumes DBTW is used prior to deriving implicit indication (Rel-16 NR-U behavior)~~
  + ~~FFS details of implicit indication in MIB (and in SIB1)~~
  + ~~FFS whether information in SIB1 can be utilized to determine whether DBTW is enabled or disabled~~
* For both licensed or unlicensed operation and with or without LBT, support the same DCI size for:
  + ~~DCI format 1\_0 scrambled with SI-RNTI~~
  + DCI format 1\_0 monitored in a common search space
    - Note: existing bit padding/truncation rules are assumed to applied for DCI format 0\_0 monitored in common search space.
  + ~~DCI format 0\_0 monitored in a common search space~~
  + FFS for ~~DCI format 1\_0 scrambled with other RNTI, and~~ other DCI formats

##### **Proposal 1.1-6)**

* For supported SCS cases of DBTW, the indication of use or no use of DBTW will be
  + Alt 1: implicitly indicated ~~(deriving that DBTW is used or not used is derived via configuration of MIB (and SIB1) parameter(s) in certain combinations) in MIB.~~
    - UE assumes DBTW is used prior to deriving implicit indication ~~(Rel-16 NR-U behavior)~~, if unlicensed spectrum operation is identified.
    - FFS details of implicit indication in MIB and/or SIB1 ~~(and in SIB1)~~
  + Alt 2: explicit indicated in MIB
    - [UE assume DBTW is used prior to decoding MIB]
  + ~~FFS whether information in SIB1 can be utilized to determine whether DBTW is enabled or disabled~~
* Proponents of Implicit:
  + Even if DBTW enable/disable is indicated in MIB, UE would not be able to know this information prior to successful decoding of MIB, and information is only available for SIB1 decoding.
  + In Rel-16 NR-U DBTW enable/disable is never explicitly indicated. Such explicit indication is not needed.
* Proponents of Explicit:
  + Assuming NR-U like functionality for licensed band operation (i.e. assume DBTW enable until SIB1 decoding) is problematic
  + Without knowing DBTW on/off before SIB acquisition, UE need to search larger number of MOs of Type0-CSS

|  |  |
| --- | --- |
| Company | Comments |
| Panasonic | Proposal 1.1-4A: We share the concern pointed out by Huawei in 2nd round discussion, i.e., large DBTW lengths may not work well for 480/960 kHz SCS. For example, if Case D pattern is reused, 64 SSB candidate positions are confined within 40 slots. For 960 kHz SCS, 40 slots are corresponding to 0.625ms. Thus, DBTW length {1, 2, 3, 4, 5} ms may not work well because DBTW length is larger than the duration of slots where SSB can be transmitted (i.e., SSB candidate positions). We would like to clarify how DBTW works in such cases (i.e., DBTW length is larger than the duration of SSB candidate positions).  Proposal 1.1-5: Our preference is Alt 1.  Proposal 1.1-2A: We are generally OK with the proposal. In the fourth bullet, “DCI format 1\_0 scrambled with other RNTI, and” would not be needed since RNTI related description was removed.   * For both licensed or unlicensed operation and with or without LBT, support the same DCI size for:   + ~~DCI format 1\_0 scrambled with SI-RNTI~~   + DCI format 0\_0 monitored in a common search space   + FFS for ~~DCI format 1\_0 scrambled with other RNTI, and~~ other DCI formats   Proposal 1.1-3A: We are OK with the proposal. |
| LG Electronics | **P 1.1-4A)** Huawei’s concern seems reasonable. DBTW lengths {0.5, 1, 2, 3, 4, 5} msec can be supported for 120 kHz, but FFS for 480/960 kHz.  However, we cannot understand Intel’s concern. In NR-U, SIB1 configuration was introduced to indicate one of DBTW lengths and the values smaller than 5 msec would be beneficial in terms of UE power saving for RLM/RRM measurement.  **P 1.1-5)** Alt 1, repeatedly, our main concern is whether PBCH payload is available to indicate increased number of SSB candidate positions.  **P 1.1-2A)** It is questionable which Rel-16 NR-U behavior is referring to for DBTW enabling/disabling. From our understanding, Huawei’s explanation is that NR-U UE assumes DBTW is enabled before SIB1 reception, and if DBTW window length (according to received SIB1) is no longer than the time duration spanned by Q SSB candidates (according to received MIB), then UE assumes DBTW disabled. Now, in FR2-2, UE cannot assume DBTW is enabled or disabled without explicit MIB indication or sync raster differentiation, since UE doesn’t know licensed or unlicensed (different from NR-U UE). That’s why we continuously requested how implicit MIB indication works for DBTW enabling/disabling.  In addition, is DCI format 0\_0 correct? Wouldn’t “DCI format **1\_0** monitored in a common search space” be correct?  **P 1.1-3A)** OK with this proposal. |
| Samsung | **Proposal 1.1-4A)**  Based on the comment from Huawei, we are ok with {0.5, 1, 2, 3, 4, 5} msec as the baseline values, and supporting extra smaller values. **Proposal 1.1-5)** We are ok with the proposal. Just some minor editorial changes:  * For 120kHz SSB, the number of candidate SSBs in a half frame for DBTW is:  **Proposal 1.1-2A)** We are ok with the proposal other than the DBTW enable/disable bullet. FR2-2 is quite different from Rel-16 NR-U in the sense that we need to support both licensed and unlicensed band, and LBT-mode and non-LBT-mode for unlicensed band using a unified solution. In Rel-16 NR-U, DBTW is always assumed to be on, and SIB1 is only to further provide information on the duration of the window (for some combinations, the window can be effectively as off), but such mechanism is problematic for FR2-2. DBTW is only needed for unlicensed band, and using Rel-16 NR-U method, the UE would waste lots of power on blind detection using Q before knowing whether the DBTW is on. This is not acceptable for UE operating on the licensed band, and it’s always beneficial to provide the UE with information on whether DBTW is on as early as possible. Also, we are still not clear how implicit indication can work, so we prefer an explicit indication in MIB. We suggest to list implicit indication and explicit indication as two alternatives:  * For supported SCS cases of DBTW, the indication of use or no use of DBTW will be   + Alt 1: implicitly indicated (~~deriving that~~ DBTW is used or not used is derived via configuration of MIB ~~(and SIB1)~~ parameter(s) in certain combinations) in MIB.     - UE assumes DBTW is used prior to deriving implicit indication (Rel-16 NR-U behavior)     - FFS details of implicit indication in MIB ~~(and in SIB1)~~   + Alt 2: explicit indicated in MIB * FFS whether information in SIB1 can be utilized to determine whether DBTW is enabled or disabled  **Proposal 1.1-3A)** We don’t agree with the FFS, since we see the need to support both Q=64 and disabling of the DBTW (i.e., not a replacing operation). To be more precise, we suggest to list the alternatives on the table.   * For supported SCS cases of DBTW, support configuration of in MIB, with at least {16, 64}~~following~~ ~~{8,16,32,64}~~ values   + ~~FFS whether 64 can be replaced with disable of DBTW indication~~   + ~~No more than 4 states of value are to be supported.~~   + Alt 1: 4 states of values are supported   + Alt 2: 3 states of values joint coded with DBTW is disabled. |
| Qualcomm | Proposal 1.1-4A: support the proposal  Proposal 1.1-5: Alt 1  Proposal 1.1-2A: for the last bullet regarding the DCI size alignment, we believe the intent was to align DCI 1\_0 with SI-RNTI where the issue needs to be resolved. So prefer to try to agree on this one.  Proposal 1.1-3A: as indicated in the previous round, it may be premature to agree on details on this one before agreeing on the number of values, the maximum # SSB candidates, and the way to indicate DBTW ON/OFF. Hence, prefer to defer this until the above is agreed. |
| OPPO | **Proposal 1.1-4A)**  We are fine with the proposal. And we think Huawei’s comment is reasonable. For different SCSs, the maximum configurable DBTW length can be different.  **Proposal 1.1-5)**  We are fine with Alt 1 or Alt 2.  **Proposal 1.1-2A)**  For the first bullet, OK.  For the second bullet, we need more clarifications on “Use of LBT by the cell and UEs connected to the cell”, does that mean cell-specific LBT/No-LBT indication?  For the third main bullet, disagree. The aware of DBTW on/off has no impact on UE performing SSB detection during initial access procedure, so we think it is not needed.  For the fourth bullet, disagree. We think the DCI size for DCI format 1\_0 should be discussed first. **Proposal 1.1-3A)** We are fine with the proposal. |
| Intel | **Proposal 1.1-4A)** – We could agree on multiple values for DBTW length, but these values should depend on subcarrier spacing, as pointed out by Huawei, and DBTW length is signalled in SIB1. In this case, DBTW on/off should be indicated as in NR-U Rel-16, i.e., by comparing DBTW length and , i.e., after decoding MIB and SIB1.  **Proposal 1.1-5)** – agree. Our preference is Alt.2. For Alt.1, it seems like DBTW is always off when the number of beams is max (i.e., 64). It would be harmful in situations when LBT is mandatory. Contrary, for Alt.2 there are means to reuse additional space within 5 ms to put more SSB candidates without affecting the existing SSB candidate positions (with indices 0~63), thus, enabling DBTW for 64 beams in deployments with mandatory LBT.  **Proposal 1.1-2A)** – We can’t agree on the 3rd bullet regarding the indication of use or no use of DBTW in its current state.  The problem is that the current version of the bullet states NR-U Rel-16 mechanism is reused only *partially* as “UE assumes DBTW is used prior to deriving implicit indication”, but the implicit indication of DBTW on/off is done in MIB *exclusively*.  As multiple DBTW length values could be supported, we don’t support DBTW on/off indication exclusively in MIB. In our understanding the indication mechanism from NR-U Rel-16 should be reused completely in this case, i.e., indication of DBTW on/off after decoding MIB and SIB1 by comparing the obtained values of DBTW length and . We think from the gNB perspective, the behavior for transmitting SSB could be made identical for both DBTW enable and disable cases. At the same time, for UE at least during SSB acquisition up until SIB1 reception, there is no need to differentiate use of DBTW or not use of DBTW.  Therefore, we don’t fully understand the strong need to explicitly indicate the use of DBTW for SSB reception. In fact, if enable/disable of DBTW is sent over MIB, UE will only realize this after successful decoding of MIB. So, this information is of little use during the PSS/SSS and MIB decoding perspective. If indicated, the information is only available for SIB1 decoding.  From SIB1 decoding perspective, we don’t fully understand the need to know DBTW is used or not, as the SIB1 transmission and reception functionality should not change whether or not DBTW is used.  We would like to ask Ericsson, why it is critical for UE to know whether DBTW is enabled or disabled for SIB1 reception. As far as we understood, having this information inside MIB means it will not be available for PSS/SSS detection, as well as MIB decoding, as it cannot be known until successful decoding of MIB.  **Proposal 1.1-3A)** – agree. |
| DOCOMO | Proposal 1.1-4A): Support. we agree candidate SSB positions can be confined within smaller time duration, but it does not necessarily justify enhancing DBTW length in our view. The only parameter which can be concerned could be 4, 5ms with 960 kHz, however, to configure 2 or 3 ms would be sufficient to deal with it. However, given that a number of companies hope to enhance this point, we are ok with introducing optimized value(s) in addition to the existing ones.  Proposal 1.1-5) Support Alt 1 considering the remaining available fields/payload in MIB/PBCH.  Proposal 1.1-2A) support.  Proposal 1.1-3A) agree with Qualcomm, this is quite independent on #candidate SSB positions to be supported. If more than 64 candidate SSB positions (which we do not prefer), Samsung’s point makes sense. Otherwise we think the current Proposal 1.1-3A would be ok, while not sure whether the discussion point is “whether replaced or not” in FFS. Anyway, it could be discussed after determining about Proposal 1.1-5. |
| Apple | **Proposal 1.1-4A):** Support. **Proposal 1.1-5):** Ok in general and prefer the revision from Samsung to make it more precise. Our preference is Alt.1.**Proposal 1.1-2A):** It is our understanding that there is no hypothetical assumption on DBTW enable/disable for NRU. Instead, it was assumed DBTW is always present. We prefer to indicate the DBTW on/off in MIB to save power for Type0-CSS monitoring to acquire the SIB1. Without knowing DBTW on/off before SIB acquisition, UE need to search larger number of MOs of Type0-CSS.In short, we prefer the modification from Samsung as well.**Proposal 1.1-3A): S**upport Samsung’s revised proposal. |
| InterDigital | **Proposal 1.1-2A)** We share the same concern as LG Electronics and Samsung regarding the indication on the enable/disable of the DBTW. Leaving the UE to assume that the DBTW is enabled could cause ambiguity where the bands are licensed, and the UE would have to go through multiple blind detections. Besides, this proposal was already discussed and agreed in the last meeting and we prefer to go on with selecting between the two options that were supported by most of the companies which are: indication through MIB or indication through sync raster.  **Proposal 1.1-3A)** We prefer the original proposal. We don’t support Samsung’s revised proposal. Especially, we prefer to discuss joint coding after having agreements on DBTW.  **Proposal 1.1-4A)** Support |
| ZTE, Sanechips | Proposal 1.1-4A: We also think Huawei’s concern in 2nd round is reasonable. DBTW lengths {0.5, 1, 2, 3, 4, 5} msec can be supported for 120 kHz. But for 480/960 kHz SCS, smaller values (e.g. scaling with SCS) can be considered. Too large value of DBTW length for 480/960 kHz SCS is not only unable to implicitly indicate DBTW enable/disable, but also deviates from the original intention of introducing DBTW.  Proposal 1.1-5: We are fine with Alt 1 or Alt 2.  Proposal 1.1-2A: We suggest to make the following revise in blue part.   * For supported SCS cases of DBTW, the indication of use or no use of DBTW will be implicitly indicated (~~deriving that~~ DBTW is used or not used is derived via configuration of MIB ~~(and SIB1)~~ parameter(s) in certain combinations) in MIB.   + UE assumes DBTW is used prior to deriving implicit indication ~~(Rel-16 NR-U behavior)~~, if unlicensed spectrum operation is identified.   + FFS details of implicit indication in MIB ~~(and in SIB1)~~   + FFS whether information in SIB1 can be utilized to determine whether DBTW is enabled or disabled * For both licensed or unlicensed operation and with or without LBT, support the same DCI size for:   + ~~DCI format 1\_0 scrambled with SI-RNTI~~   + DCI format 1~~0~~\_0 monitored in a common search space   + FFS for DCI format 1\_0 scrambled with other RNTI, and other DCI formats   Proposal 1.1-3A: We are OK with the proposal. |
| vivo | Proposal 1.1-4A: Agree with the Huawei’s concern. We support to use DBTW lengths {0.5, 1, 2, 3, 4, 5} msec as baseline and FFS smaller values.  Proposal 1.1-5: We support Alt 1.  Proposal 1.1-2A: We support the proposal. From the discussions, the main benefit to indicate DBTW on/off in MIB is to reduce Type 0 PDCCH monitoring. As Qualcomm and Docomo indicates, it is highly dependent on whether to have larger number of candidate SSBs. If not extended (i.e. 64), indication of Q=64 is enough to imply DBTW off and there is no any benefit on Type 0 PDCCH monitoring. If it is extended (e.g. 128), unknown of DBTW off state will have 2 times Type 0 PDCCH MOs with indication of Q=64. This benefit only exists when initial access case, which seems not significant.  Proposal 1.1-3A: We are OK with the proposal. |
| Lenovo, Motorola Mobility | **Proposal 1.1-4A):** Support.  **Proposal 1.1-5):** We supportAlt 1  **Proposal 1.1-2A):** For the first and second bullet, we agree.  But just a clarification question on 2nd bullet: Does it mean not to indicate cell specific LBT mode to the connected UEs in MIB?  For the 3rd bullet, we agree with Samsung to include both implicit and explicit indication in MIB. Also, the sub-bullet for the 4th bullet can be generalized for other DCI formats:  FFS ~~for DCI format 1\_0 scrambled with other RNTI, and~~ other DCI formats **Proposal 1.1-3A):** agree with Qualcomm |
| Nokia | Proposal 1.1-4A): We are OK with this proposal. Now apart using the window length for disabling the DBTW for low number of SSBs with 480khz or 960kHz, there is not strong justification for changing the value. Noting also that we have not yet agreed the SSB slot pattern for the higher sub-carrier spacings.  Proposal 1.1-5): Our preference would still be to have option to use DBTW when number of SSBs>32, hence Alt-2.  Proposal 1.1-2A):  For the LBT bullet, for my understanding would it be possible to modify the wording as follows:   * Use of LBT ~~by the cell and UEs connected to the cell~~ is not indicated in MIB.   Regarding DBTW derivation, based on the FL proposal and extensions made by others, to be fair none of these are a perfect solution. Either we end up restricting the configuration applying implicit indication, or we, in worst case limit to one value. We understand that there could be some merit to have the information for SSB detection, but case of carrying the information in MIB this wont be available. Like also noted earlier, the extra burden for SIB1 reception, even assuming two DCI format 1\_0 size hypotheses does not seem extensive. In any case we would prefer the Samsung proposals to have Alt1 and Alt2 to consider further together with FFS whether SIB1 is accounted as well. This would meet requirement of the earlier agreement to have the information available in IDLE mode. In my understanding, also when UE is doing initial cell selection, it is in IDLE mode (according to 38.304 already at PLMN selection phase), thus if we want to be strict, the information would need to be available at cell selection phase.  Like commented by others, it would be good to clarify the second last bullet, which DCI formats are meant. In my understanding, in CSS, the size of the DCI format 1\_0 and 0\_0 are padded to be aligned according the larger one of the two.  Proposal 1.1-3A):  As noted above, with explicit indication of DBTW in MIB, one option would be to assume =64 to imply no DBTW, thereby having only one additional value for the indication We don’t think having the only available value to be =16 would very well support multi-beam operation. |
| Futurewei | Proposal 1.1-4A: Agree with the Huawei’s concern. We support to use DBTW lengths {0.5, 1, 2, 3, 4, 5} msec as baseline and FFS smaller values.  Proposal 1.1-5: We support Alt 1  Proposal 1.1-2A): For the first and second bullet, we agree. The other bullets may need more discussions. We can discuss after the Proposal 1.1-5 is agreed.  Proposal 1.1-3A: We are OK with the proposal. |
| Huawei, HiSilicon | **Proposal 1.1-4A)**  As we discussed earlier, DBTW lengths of {0.5, 1, 2, 3, 4, 5} msec are acceptable for us ONLY for 120 kHz.  Here is our comments about is issue from earlier rounds of comments with slightly more explanation:  We believe that a similar method as in Rel-16 NR-U should be used to implicitly indicate whether DBTW is enabled or disabled and, if DBTW lengths {0.5, 1, 2, 3, 4, 5} msec is used for all SCSs, such implicit indication would be completely dysfunctional.  Rel-16 NR-U behavior: As explained before in the first round, DBTW enabled/disabled is never explicitly indicated to the UE in Rel-16 NR-U; neither for IDLE UE nor for CONNECTED UE. In Rel-16, UE can infer whether DBTW is enabled/disabled only after reading SIB1 by comparing the maximum number of transmitted SSB indexes (acquired from MIB payload) with the DBTW length (*DiscoveryBurst-WindowLength* provided in SIB1). If DBTW length that is configured in SIB1 is such that DBTW can include more than candidate SSB indexes, UE can infer that DBTW is enabled. In turn, if DBTW length that is configured in SIB1 is such that DBTW cannot include more than candidate SSB indexes, UE can infer that DBTW is disabled. Before reading SIB1, UE assumes that DBTW length is a half frame (includes all candidate SSB positions), and, as such, DBTW is enabled.  Now, assume that DBTW is supported for 960 kHz and = {8,16,32,64} are supported as in Proposal 1.1-3. This means that the first (=8,16,32,64) can be mapped to the first (4, 8, 16, 32) slots where, for the sake of simplicity of the discussion, we assumed that no UL slots are reserved in the first 32 slots. (4, 8, 16, 32) slots in 960 kHz are (*0.0625, 0.125, 0.25, 0.5) ms.*This simply shows that if DBTW lengths {0.5, 1, 2, 3, 4, 5} msec are supported as in Rel-16, since the smallest supported DBTW value is 0.5 ms, UE assumes that DBTW is always enabled if is configured to be any value less than 64.  Other than above, there is also another major problem with supporting {0.5, 1, 2, 3, 4, 5} msec DBTW lengths especially for higher SCSs. Imagine (four slots of SSB) is configured for 960 kHz SCS. Do companies believe that a DBTW length as large as 5 msec is a viable choice for in 960 kHz? We don’t think so. DBTW = 5 msec for in 960 kHz means that UE assumes the pattern of 8 SSBs repeats 80 times!  **Proposal 1.1-5):**  Support Alt 1. **Proposal 1.1-2A)**  * **First bullet:** Support. * **Second bullet:** Support with fixing typo:   + Use of LBT by the cell and UEs connected to the cell is not indicated in MIB. * **Third bullet:** We cannot agree implicit indication only in MIB. As we discussed above in our explanation to Proposal 1.1-4A), in Rel-16 NR-U, DBTW enable/disable is implicitly indicated by comparing the values of in MIB and DBTW length in SIB1 and, before reading SIB1, UE assumes that DBTW is enabled. This is the same behavior for both RRC IDLE and RRC CONNECTED UEs. As discussed before, we don’t see any reason to change this behavior and no company has explained to us why this Rel-16 NR-U behavior has to change in Rel-17. To be flexible, we can suggest the following alternative to the third bullet:  **Suggested modification to the third bullet of Proposal 1.1-2A)**  * For supported SCS cases of DBTW, the indication of use or no use of DBTW will be implicitly indicated ~~(deriving that DBTW is used or not used is derived via configuration of MIB (and SIB1) parameter(s) in certain combinations) in MIB.~~   + UE assumes DBTW is used prior to deriving implicit indication (Rel-16 NR-U behavior)   + FFS details of implicit indication in MIB and/or SIB1 ~~(and in SIB1)~~   + ~~FFS whether information in SIB1 can be utilized to determine whether DBTW is enabled or disabled~~ * **Fourth bullet:** We don’t support it. We don’t understand why the original proposal regarding unifying the size of “DCI format 1\_0 scrambled with SI-RNTI” changed to “DCI format 0\_0 monitored in a common search space”. To our understanding, DCI format 1\_0 with CRC scrambled by SI-RNTI indicates the location of SIB1 and has different sizes for licensed and unlicensed operations in Rel-16 (which needs to be unified unless we want to indicate LBT/No-LBT prior to reading Type0-PDCCH or accept two blind decoding on the sizes of DC1 1\_0):  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | The following information is transmitted by means of the DCI format 1\_0 with CRC scrambled by SI-RNTI:  - Frequency domain resource assignment – bits  -  is the size of CORESET 0  - Time domain resource assignment – 4 bits as defined in Clause 5.1.2.1 of [6, TS38.214]  - VRB-to-PRB mapping – 1 bit according to Table 7.3.1.2.2-5  - Modulation and coding scheme – 5 bits as defined in Clause 5.1.3 of [6, TS38.214], using Table 5.1.3.1-1  - Redundancy version – 2 bits as defined in Table 7.3.1.1.1-2  - System information indicator – 1 bit as defined in Table 7.3.1.2.1-2  - Reserved bits – 17 bits for operation in a cell with shared spectrum channel access; otherwise 15 bits  Table 7.3.1.2.1-2: System information indicator   |  |  | | --- | --- | | Bit field | System information indicator | | 0 | SIB1 [9, TS38.331, Clause 5.2.1] | | 1 | SI message [9, TS38.331, Clause 5.2.1] | |     Moreover, the size of DCI 0\_0 is matched with the size of DCI 1\_0 and not the other way around:   |  | | --- | | If DCI format 0\_0 is monitored in common search space and if the number of information bits in the DCI format 0\_0 prior to padding is less than the payload size of the DCI format 1\_0 monitored in common search space for scheduling the same serving cell, a number of zero padding bits are generated for the DCI format 0\_0 until the payload size equals that of the DCI format 1\_0.  - If DCI format 0\_0 is monitored in common search space and if the number of information bits in the DCI format 0\_0 prior to truncation is larger than the payload size of the DCI format 1\_0 monitored in common search space for scheduling the same serving cell, the bitwidth of the frequency domain resource assignment field in the DCI format 0\_0 is reduced by truncating the first few most significant bits such that the size of DCI format 0\_0 equals the size of the DCI format 1\_0. |   **Proposal 1.1-3A)** We prefer the original version Proposal 1.1-3. It would be a bit strange to support only {16, 64} and still have an FFS on whether 64 can be used to disable DBTW indication. It would simply mean that if SSB burst can slide in a DBTW, has to be 16 and if = 64, SSB burst cannot slide in DBTW. In other words, for 480/960 kHz, if DBTW is supported and = 64, SSB bust cannot slide in a DBTW although, for instance, 64 SSB is only 32 slots (0.5 ms) in 960 kHz. And if it is considered a good design, then why up to 5 ms DBTW still have a strong support among companies? When a DBTW a large as 5 ms would be actually required for 960 kHz? We can accept the following alternative though:   * For supported SCS cases of DBTW, support configuration of in MIB~~, with at least {16, 64}following {8,16,32,64} values~~   + ~~FFS whether 64 can be replaced with disable of DBTW indication~~   + No more than 4 states of value are to be supported.   **Question to Ericsson Regarding DBTW indication:** Can you please explain the reason why DBTW enable/disable needs to be (implicitly) indicated in MIB in Rel-17 while UE would only know DBTW enabled/disabled after comparing in MIB and DBTW length in SIB1 in Rel-16? Note that, in Rel-16, UE would just assume that DBTW is enabled (DBTW length is 5 msec) before reading SIB1 in Rel-16. This is the same behavior for RRC CONNECTED and IDLE UEs in Rel-16. We are wondering why this behavior needs to change. |
| Convida Wireless | Proposal 1.1-4A) We are ok with the proposalProposal 1.1-5) We are ok with the proposal. We prefer Alt 2.Proposal 1.1-2A) We are ok with the proposalProposal 1.1-3A) We prefer to have FFS for states in last sub-bullet (highlighted in yellow)  * For supported SCS cases of DBTW, support configuration of in MIB, with at least {16, 64}~~following~~ ~~{8,16,32,64}~~ values   + FFS whether 64 can be replaced with disable of DBTW indication   FFS: Number of states of value to be supported. |
| DOCOMO | Proposal 1.1-4B) Support  Proposal 1.1-3B) The main bullet itself is fine for us. Not sure which is the moderator’s intention, capturing the alternatives or down-selection?  In case down-selection is intended, we think whether we can (or have to) go with Alt 2 or 3 depends on #candidate SSB positions. 5B-like discussion is needed for larger SCS in advance.  Proposal 1.1-5B) Support  Proposal 1.1-2B) Ok with the proposal. Proposal 1.1-6) Slightly prefer Alt 1 since it is similar to NR-U, but open to discuss. For Alt 2 can reduce Mos, but its benefit depends on #candidate SSB positions in our view. |
| LG Electronics | Proposal 1.1-4B) Support  Proposal 1.1-3B) Support  Proposal 1.1-5B) Support  Proposal 1.1-2B) Support Proposal 1.1-6) We suggest to add one more alternative, Alt 3: synchronization raster, which does not require MIB bit but can inform UE whether DBTW enabling/disabling prior to initial access procedure. |
| Ericsson | These are our comments prior to the 3rd round summary. I would be happy if you could take them into account in the 4th round:  A general comment is to add "if supported" to all proposals (as in 1.1-4A)  **P 1.1-4A)** Support  **P 1.1-5)** Strong preference for Alt-1. We also think some changes to the proposal are needed:   * We are very skeptical that there will be enough bits in MIB / PBCH for increasing the number of candidate positions. From an implementation perspective, we do not support changing the way SSB index is signaled compared to FR2, and increasing the number of candidates to 80 would require this. So we think that it needs to be made clear that if 80 is selected, then it is FFS how to signal the 80 candidate positions. Clearly, if only 64 is supported, no changes w.r.t. Rel-16 are needed. * We agree with Samsung's addition about adding wording about the half frame: * Hence a revised proposal could be:   + For 120kHz SSB, the number of candidate SSBs in a half frame for DBTW (if supported) is one of the following:     - Alt 1) 64     - Alt 2) 80       * FFS: How to indicate more than 64 candidate SSB indices  **P 1.1-2A)**  We have concerns with the 3rd bullet.   * As previously agreed, and as pointed out by Nokia, we have already agreed in RAN1 that DBTW on/off shall be indicated to IDLE mode, and we believe that the following bullet is contradictory to that. During what procedures would the UE need to assume DBTW is on before receiving some indication? During initial cell selection? We don't think so. As commented by many, early indication of DBTW off is beneficial for reducing the UEs Type-0 PDCCH monitoring effort, so we don't see why the following bullet is needed.   + UE assumes DBTW is used prior to deriving implicit indication (Rel-16 NR-U behavior) * Samsung has proposed two alternatives, and we agree with this general direction, except for the sub-bullet on Rel-16 NR-U behavior)   + - Alt 1: implicitly indicated (~~deriving that~~ DBTW is used or not used is derived via configuration of MIB ~~(and SIB1)~~ parameter(s) in certain combinations) in MIB.       * ~~UE assumes DBTW is used prior to deriving implicit indication (Rel-16 NR-U behavior)~~       * FFS details of implicit indication in MIB ~~(and in SIB1)~~     - Alt 2: explicit indicated in MIB   However, we still don't understand what the scope of "implicit" is. Some companies propose signaling multiple values of Q, e.g., {64, val1, val2, val3} and that Q = 64 means DBTW off. This could be a viable solution in our view. Does this count as "implicit" or "explicit?" Does explicit mean that a dedicated bit is used for DBTW on/off indication? We also think that could be a viable solution. In summary, we would like to make sure that there is common understanding on what is implicit and implicit.    In the 4th bullet:   * Shouldn't it be DCI 1\_0? * Also, since the first bullet says "common search space", should the FFS say "FFS for DCI 1\_0 monitored in a USS?"   @Huawei: As answered by LGE and Samsung, the 60 GHz band is fundamentally different than Bands n46/n96 in Rel-16 in that licensed operation is supported, and clearly DBTW does not make sense in licensed operation. Moreover, even in unlicensed operation, not all deployments require use of DBTW. As commented Apple (and also by Samsung), "Without knowing DBTW on/off before SIB acquisition, UE need to search larger number of MOs of Type0-CSS." Furthmore, indication of DBTW on/off for IDLE mode UEs has already been agreed in RAN1, and we do not wish to revert that agreement. As pointed out by Nokia, UEs performing initial cell selection (prior to SIB1 reading) are indeed in IDLE mode  **P 1.1-3A)**  We don't support this proposal as is. As hinted by Qualcomm, Proposal 1.1-3A and 1.1-5 are linked. From a MIB design perspective, the most important factors are (1) Whether or not additional SSB candidate positions need to be indicated, and (2) how many Q values need to indicated rather than what values. However, we think Samsung's proposal could work, except it seems to be a bit contradictory since the main bullet says "at least {16,64}" and then the sub-bullets say 3 states for 4 states. Perhaps the following is more general, and focuses on how many values need to indicated and whether or not DBTW off is jointly encoded with the Q values:   * For supported SCS cases of DBTW (if supported), support X states in MIB at least for indication of values of where 2≤X ≤4. Down-select to one of the following two alternatives:   + Alt-1: All X states indicate valid values of   + Alt-2: X – 1 states indicate valid values of and one state indicates DBTW off * FFS   + Value of X and what field(s) of MIB to use for the X states   + Supported values of |
| Huawei, HiSilicon | **Proposal 1.1.4-B)** Support  **Proposal 1.1.3-B)** Support with the following modification for clarity:   * For supported SCS cases of DBTW, support configuration of in MIB, with at least {16, 64} values   + Alt 1: ~~2 states of~~  No additional values are supported   + Alt 2: two additional values, total of 4 states of values are supported     - FFS on the two additional values   + Alt 3: one addition value, and reserved state that indicates DBTW disabled, total of 3 states of values and 1 state of DBTW disabled are supported.   **Proposal 1.1-5B)** Support  **Proposal 1.1-2B)**   * **First bullet:** Support * **Second bullet:** Support * **Third bullet:** It is unclear for us why “DCI format 1\_0 scrambled with SI-RNTI” is replaced by “DCI format 1\_0 monitored in a common search space”. After reading MIB, UE only needs to figure out the size of “DCI format 1\_0 scrambled with SI-RNTI” (or does two blind decoding on the DCI size) to decode DCI in CORESET#0 and read SIB1. So, we are wondering why unifying the size should also be extended to “DCI format 1\_0 monitored in a common search space” which also includes the cases that DCI format 1\_0 is scrambled with eg, RA-RNTI, P-RNTI, and MsgB-RNTI.   **Proposal 1.1-6)** In our view, in the first sub-bullet of Alt 1, there is no need to add “if unlicensed spectrum operation is identified”.   * UE simply does not need to know if it operates in licensed or unlicensed spectrum prior to reading SIB1 (assuming the ambiguity of size of DCI 1\_0 with CRC scrambled by SI-RNTI is resolved somehow by, eg, unifying the size or by doing two blind decoding). Please also note that strong majority agree on “No indication for licensed and unlicensed operation in MIB” (1.1-2B first bullet). So, how unlicensed spectrum operation would be identified anyway? * In licensed operation, if candidate SSB index “a” (which is also the SSB index “a”) of a PCell is transmitted, the Type0-PDCCH corresponding to candidate SSB index “a” is also supposed to be transmitted. If UE detects candidate SSB index “a”, it goes on to receive Type0-PDCCH corresponding to the same candidate SSB index “a”, then reads SIB1 and moves on to the subsequent steps of cell connection establishment. Therefore, to our understanding, ***whether or not UE assumes DBTW is used or not used has no impact on UE behavior in licensed operation***. In unlicensed operation, if candidate SSB index “a” of a PCell is transmitted, it may happen that the Type0-PDCCH corresponding to candidate SSB index “a” is not transmitted due to LBT failure. In such a case, obviously, UE cannot find the Type0-PDCCH corresponding to candidate SSB index “a”, but, since it knows from the MIB of candidate SSB index “a”, it would know the location of the CORESET#0 corresponding to the candidate SSB index “a+” which would be QCL-D with the detected candidate SSB index “a”. So, UE can go and find the Type0-PDCCH from the CORESET#0 corresponding to the candidate SSB index “a+”. So, all in all, UE would use the assumption that DBTW is used only when it detects a candidate SSB “a” of a PCell but cannot find the Type0-PDCCH corresponding to the detected candidate SSB “a” which typically happens only in unlicensed operation. To summarize, we can agree with this with the following modification * For supported SCS cases of DBTW, the indication of use or no use of DBTW will be   + Alt 1: implicitly indicated     - UE assumes DBTW is used prior to deriving implicit indication~~, if unlicensed spectrum operation is identified.~~     - FFS details of implicit indication in MIB and/or SIB1   + Alt 2: explicit indicated in MIB     - [UE assume DBTW is used prior to decoding MIB] |
| CATT | For Proposal 1.1-3B) support alt 3  Proposal 1.1-4B) Don’t agree, we still prefer single fixed 5ms as DBTW length  **Proposal 1.1-2B) Ok.**  **Proposal 1.1-5B) Still prefer 80. Not sure how to solve the problem of maximum SSB=64 if this proposal is supported.** Proposal 1.1-6) Support Alt1 |
| InterDigital | Proposal 1.1-4B We are fine with the proposal.  Proposal 1.1-3B We are fine with the proposal. We prefer Alt 2.  Proposal 1.1-5B We are fine with the proposal. Proposal 1.1-6 We are generally fine, but prefer to include sync raster based indication method in Alt 2. |
| Ericsson 2 | Comments on 4th round proposals: **Proposal 1.1-4B) – cleaned up** Support **Proposal 1.1-3B) – cleaned up** We prefer the more general proposal we formulated above – leaves out the actual Q values and focuses on the number of states which is what matters for MIB design. Alternatively, the following is acceptable too, although we would prefer to have an FFS on 16 (64 is okay). This is a safe option in case only 1 bit can be found in MIB for repurposing.  We are confused about the relationship to Proposal 1.1-5B. If 5B is agreed, then doesn't it automatically follow that means DBTW disabled for both Alt-1 and Alt-2? **Proposal 1.1-5B) – cleaned up** Support **Proposal 1.1-2B) – cleaned up** Generally okay, regarding the 3rd bullet, what about DCI 1\_0 monitored in USS? In the current spec, the DCI size is 2 / 0 bits if unlicensed / licensed. **Proposal 1.1-6) – cleaned up** Still, we are confused about what "implicit" means. To us, there are only two viable options – use different sync raster points to indicate DBTW on/off, or to indicate in MIB somehow, e.g., through a reserved state of Q (e.g., 64), or directly by a dedicated (re-purposed) bit in MIB. We do not agree that the UE needs to assume DBTW is on prior to receiving any of the above indications. |
| ZTE, Sanechips | **Proposal 1.1-4B) – cleaned up:** Support**Proposal 1.1-3B) – cleaned up:** Support and we prefer Alt 2.**Proposal 1.1-5B) – cleaned up:** Support**Proposal 1.1-2B) – cleaned up:** Support**Proposal 1.1-6) – cleaned up:** Support and we prefer Alt 1. |
| NEC | Proposal 1.1-4B) Support.  Proposal 1.1-3B) Support and be open to discuss three alternatives based on the number of available indication bits in MIB.  Proposal 1.1-5B) We prefer 80 candidates SSB positions and fixed typo relative to NEC’s view in the 3rd Round Discussion Summary. In our understanding, DBTW is used to provide additional SSB transmission positions in case of LBT failure, otherwise it’s not necessary to indicate DBTW on/off or even introduce DBTW at least for Q=64.  Proposal 1.1-2B) Support. Proposal 1.1-6) Support generally, and we also share a similar view as Ericsson’s comment above, maybe the meaning of “implicit” needs to be clarified further. |
| Lenovo, Motorola Mobility | **Proposal 1.1-4B) – cleaned up:** Support**Proposal 1.1-3B) – cleaned up:** We support it with Alt 2 as our preference.**Proposal 1.1-5B) – cleaned up:** Support**Proposal 1.1-2B) – cleaned up:** Support**Proposal 1.1-6) – cleaned up:** We support the proposal, but the term ‘implicit’ need further elaboration. |
| Nokia | Proposal 1.1-4B): Fine with the proposal.  Proposal 1.1-3B): Still concern that in the case of adopting Alt1 (also in light of the majority view in other agreements), we would only have DBTW support for 16 SSBs. We would not prefer to limit the use of DBTW to such a low value. Hence, would prefer 32 as the other value (in addition to 64).  Proposal 1.1-5B): While this evidently is the majority view, this is rather unfortunate agreement and sets a shadow on the general feasibility and necessity of DBTW in general especially if it is via proposal 1.1.3B values is limited to 16.  Proposal 1.1-2B):  In principle fine. Regarding the alignment of the sizes, in the sub-bullet, maybe minor change:  “bit padding/truncation rules for DCI size alignment”  Proposal 1.1-6): We have a bit similar thinking as Ericsson that if we think that knowledge regarding DBTW is beneficial, it should be available before detection of the SSB. If not possible having it at MIB does not differ significantly on having it in SIB1. If we go for indication in SIB1, it is not clear to us why we need to have implicit rather than explicit indication via DBTW window, accounting that we may need to have more/different values window size for higher scs implying redesign of the information element in any case? |
| OPPO | **Proposal 1.1-4B)** Support.  **Proposal 1.1-3B)** Support and we prefer Alt 1.  **Proposal 1.1-5B)** Have concerns. We think additional SSB transmission positions are beneficial for the scenarios that LBT is required, and prefer to keep 80 candidates SSB positions as alternative.  **Proposal 1.1-2B)** Fine with the proposal.  **Proposal 1.1-6)** Not support. The indication of use or no use of DBTW is independent of initial access procedure, so we prefer to remove “in MIB” in Alt 2. |
| Intel | **Proposal 1.1-4B) – cleaned up:** we’re Ok**Proposal 1.1-3B) – cleaned up:** Support. For Alt.1 we slightly prefer the modification made by Huawei, i.e., Alt.1: No additional values are supported**Proposal 1.1-5B) – cleaned up:** Do not support. The proposal unnecessarily limits the DBTW operation for the case of max number of beams. There is technical possibility to shift DB within DBTW window as follows: Original SS burst:    DB shift within DBTW:    As illustrated above, shifting of DB consisting of all 64 SSB up to 1 ms is possible within a half frame if max candidate SSB is 80. BTW, the ordering of the rest candidate SSBs (16~63) is unaffected. **Proposal 1.1-2B) – cleaned up:** we’re Ok**Proposal 1.1-6) – cleaned up:** Support. And also support inclusion of Alt.3 where DBTW on/off is indicated based on sync raster |
| Panasonic | Proposal 1.1-4B) OK with the proposal  Proposal 1.1-3B) OK with the proposal. We share similar view with DOCOMO and Ericsson that the number of candidate SSB positions need to be clarified.  Proposal 1.1-5B) OK with the proposal  Proposal 1.1-2B) OK with the proposal. Proposal 1.1-6) We also share similar view Ericsson that the meaning of “implicit” needs to be clarified. Our understanding of implicit indication is that just Q value is indicated to UE and UE determines DBTW enabled/disabled based on Q value (e.g., {8, 16, 32, 64} can be indicated and Q=64 means DBTW off. Whether to determine based on both Q value and DBTW length is FFS). For explicit indication, reserved state (or something specific state) to indicate DBTW off can be indicated in addition to Q values (e.g., {16, 32, 64, reserved} can be indicated). |

#### **3rd Round Discussion Summary:**

**Issue 1)** DBTW lengths and potential values of DBTW

Several companies have outlined issues with applying existing DBTW lengths for 480 and 960kHz. Therefore, updated the Proposal 1.1-4A to be limited to 120kHz cases. For the actual values, companies supportive of the Q indication seems to support at least 2 values, and there are several companies who support up to 4 values. So updated the Proposal 1.1-3A to include all 3 cases.

**Proposal 1.1-4B)**

* For ~~supported SCS cases of~~ DBTW with 120kHz SCS (if supported), support DBTW lengths {0.5, 1, 2, 3, 4, 5} msec
  + Note: this should be the same as Rel-16 NR-U DBTW lengths.

Companies with concerns on Proposal 1.1-4B:

* CATT

**Proposal 1.1-3C)**

* For supported SCS cases of DBTW, support configuration of in MIB, with at least {16, 64}~~following~~ ~~{8,16,32,64}~~ values. Additionally, down-select among the following alternatives.
  + ~~FFS whether 64 can be replaced with disable of DBTW indication~~
  + ~~No more than 4 states of value are to be supported.~~
  + Alt 1: no additional values are supported, total of 2 states of values are supported (i.e. {16,64})
    - Note: Value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB
  + Alt 2: two additional values, total of 4 states of values are supported (i.e. {16, 64, X, Y})
    - FFS on the two additional values
    - Note: Value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB
  + Alt 3: one addition value, and reserved state that indicates DBTW disabled, total of 3 states of values and 1 state of DBTW disabled are supported. (i.e. {16, 64, X, DBTW disabled})

**Issue 2)** number of SSB candidate positions

There is more companies in favor of 64 values for 120kHz candidate SSB positions. Let’s see if can conclude in this direction.

**Proposal 1.1-5B)**

* For 120kHz SSB, the number of candidates SSBs in a half frame for DBTW is:
  + ~~Alt 1)~~ 64
  + ~~Alt 2) 80~~

The following is a summary of company views on 64 vs 80 candidate SSB positions.

* Alt 1: Docomo, Spreadtrum, LGE, ~~NEC,~~ Convida, Qualcomm, Futurewei, Huawei/HiSilicon, Lenovo/Motorola Mobility, vivo, ZTE/Sanechips, Apple, OPPO, Panasonic
  + Concerns on Alt 2:
    - Ability to indicate the extra entries in MIB
* Alt 2: Nokia, ZTE/Sanechips, Intel, OPPO, NEC
  + Concerns on Alt 1:
    - When Q=64, DBTW will function as if it is disabled if only 64 candidate positions are available, therefore not able to handle cases when SSB cannot be transmitted due to LBT

**Issue 3)** LBT/DBTW indication aspects

The indication of DBTW in implicit or explicit manner seems to be the controversial question. So moderator has separated out the DBTW implicit vs explicit issue in Proposal 1.1-6. For the explicit DBTW enable/disable, based on comments and discussions so far, moderator assumes that UE would need to assume that DBTW is enabled until the UE has successfully decoded MIB. However, moderator would like to check this with proponents of explicit signaling.

Moderator has added explanation on what implicit means based on companies contributions and comments in Proposal 1.1-6, please feel free to provide comments on this, as moderator is not complete sure all companies have the same understanding or not. Companies still had some disagreement on DBTW being implicit and explicit.

Some companies had quoted previous agreement on DBTW (copied below). However, from moderator’s understanding UE in initial access is neither IDLE nor CONNECTED mode. While UE in IDLE mode may need to perform cell re-selection and DBTW information could be said to be provided for UEs during this process. Moderator assumed that was part of the FFS. With that said, moderator would like to solicit comments from companies on this aspect further.

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| * If DBTW is supported   + Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs     - FFS: how to support UEs performing initial access that do not have any prior information on DBTW. |

**Proposal 1.1-2C)**

* No indication for licensed and unlicensed operation in MIB ~~will be performed in SSB (including MIB)~~
  + Whether and/or how LBT/No-LBT is indicated is separately discussed
* Use of LBT ~~by the cell and UEs connected to the cell~~ is not indicated in MIB.
  + FFS where and how this is indicated, e.g. SIB1
* ~~For supported SCS cases of DBTW, the indication of use or no use of DBTW will be implicitly indicated (deriving that DBTW is used or not used is derived via configuration of MIB (and SIB1) parameter(s) in certain combinations) in MIB.~~
  + ~~UE assumes DBTW is used prior to deriving implicit indication (Rel-16 NR-U behavior)~~
  + ~~FFS details of implicit indication in MIB (and in SIB1)~~
  + ~~FFS whether information in SIB1 can be utilized to determine whether DBTW is enabled or disabled~~
* For both licensed or unlicensed operation and with or without LBT, support the same DCI size for:
  + ~~DCI format 1\_0 scrambled with SI-RNTI~~
  + DCI format 1\_0 monitored in a common search space
    - Note: existing bit padding/truncation rules are assumed to applied for DCI format 0\_0 monitored in common search space.
  + ~~DCI format 0\_0 monitored in a common search space~~
  + ~~FFS for DCI format 1\_0 scrambled with other RNTI, and other DCI formats~~
  + FFS for DCI format 1\_0 monitored in USS

**Proposal 1.1-6A)**

* For supported SCS cases of DBTW, the indication of use or no use of DBTW will be
  + Alt 1: implicitly indicated ~~(deriving that DBTW is used or not used is derived via configuration of MIB (and SIB1) parameter(s) in certain combinations) in MIB.~~
    - UE assumes DBTW is used prior to deriving implicit indication ~~(Rel-16 NR-U behavior)~~, ~~if unlicensed spectrum operation is identified~~.
    - [Note: implicit indication means that specification should support gNB that wishes to disable DBTW can operate identically with DBTW enabled and with specific set of parameters configured for DBTW during initial access. UE may be able to determine that gNB is not using DBTW from detected SSBs and set of parameters configured for DBTW, but use of this knowledge may not necessarily change UE behavior during initial access.]
    - FFS details of implicit indication in MIB and/or SIB1 ~~(and in SIB1)~~
  + Alt 2: explicit indicated in MIB
    - [UE assume DBTW is used prior to decoding MIB]
    - [Note: explicit indication means that gNB operation behavior when DBTW is indicated to be disabled is not completely the same as when DBTW is enabled, as a consequence indication is needed to inform UE of change in behavior to operation during initial access.]
  + ~~FFS whether information in SIB1 can be utilized to determine whether DBTW is enabled or disabled~~
  + Alt 3: indication via synchronization raster entry
* Proponents of Implicit:
  + Even if DBTW enable/disable is indicated in MIB, UE would not be able to know this information prior to successful decoding of MIB, and information is only available for SIB1 decoding.
  + In Rel-16 NR-U DBTW enable/disable is never explicitly indicated. Such explicit indication is not needed.
* Proponents of Explicit:
  + Assuming NR-U like functionality for licensed band operation (i.e. assume DBTW enable until SIB1 decoding) is problematic
  + Without knowing DBTW on/off before SIB acquisition, UE need to search larger number of MOs of Type0-CSS

#### **4th Round Discussion:**

Please continue to provide comments on Proposal 1.1-4B, 1.1-3C, 1-1.5B, 1-1-2C, and 1-1-6A.

Also, moderator would like to ask companies to **clarify the** **meaning of implicit and also explicit indication** of DBTW and comment on whether moderator’s note and understanding is correct or not.

**Proposal 1.1-4B) – cleaned up**

* For DBTW with 120kHz SCS (if supported), support DBTW lengths {0.5, 1, 2, 3, 4, 5} msec
  + Note: this should be the same as Rel-16 NR-U DBTW lengths.

##### **Proposal 1.1-3C) – cleaned up**

* For supported SCS cases of DBTW, support configuration of in MIB, with at least {16, 64}values. Additionally, down-select among the following alternatives.
  + Alt 1: no additional values are supported, total of 2 states of values are supported (i.e. {16,64})
    - Note: Value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB
  + Alt 2: two additional values, total of 4 states of values are supported (i.e. {16, 64, X, Y})
    - FFS on the two additional values
    - Note: Value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB
  + Alt 3: one addition value, and reserved state that indicates DBTW disabled, total of 3 states of values and 1 state of DBTW disabled are supported. (i.e. {16, 64, X, DBTW disabled})

**Proposal 1.1-5B) – cleaned up**

* For 120kHz SSB, the number of candidates SSBs in a half frame for DBTW is 64

##### **Proposal 1.1-2C) – cleaned up**

* No indication for licensed and unlicensed operation in MIB
  + Whether and/or how LBT/No-LBT is indicated is separately discussed
* Use of LBT is not indicated in MIB.
  + FFS where and how this is indicated, e.g. SIB1
* For both licensed or unlicensed operation and with or without LBT, support the same DCI size for:
  + DCI format 1\_0 monitored in a common search space
    - Note: existing bit padding/truncation rules are assumed to applied for DCI format 0\_0 monitored in common search space.
  + FFS for DCI format 1\_0 monitored in USS

##### **Proposal 1.1-6A) – cleaned up**

* For supported SCS cases of DBTW, the indication of use or no use of DBTW will be
  + Alt 1: implicitly indicated
    - UE assumes DBTW is used prior to deriving implicit indication.
    - [Note: implicit indication means that specification should support gNB that wishes to disable DBTW can operate identically with DBTW enabled and with specific set of parameters configured for DBTW during initial access. UE may be able to determine that gNB is not using DBTW from detected SSBs and set of parameters configured for DBTW, but use of this knowledge may not necessarily change UE behavior during initial access.]
    - FFS details of implicit indication in MIB and/or SIB1
  + Alt 2: explicit indicated in MIB
    - [UE assume DBTW is used prior to decoding MIB]
    - [Note: explicit indication means that gNB operation behavior when DBTW is indicated to be disabled is not completely the same as when DBTW is enabled, as a consequence indication is needed to inform UE of change in behavior to operation during initial access.]
  + Alt 3: indication via synchronization raster entry

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | **Proposal 1.1-4B)**  We are ok with this proposal, and also ok with these values for 480/960 kHz as a baseline.  **Proposal 1.1-3C)**  One clarification question for the note in Alt 1 and Alt 2: Does the note only hold for 64 candidate SSB locations in half frame? If so, why not just explicitly indicate UE the DBTW is off but using an implicit way? We still have concern with the way of stating the proposal in the main bullet, since the value of 64 is not needed when the number of candidate SSB in a half frame is only 64, i.e., this issue is still depending on the discussion on the number of candidate SSB in a half frame, and we are not ready to put 64 as an agreed number.  **Proposal 1.1-5B)**  We are not ok with this proposal. Supporting only 64 SSB candidate locations for DBTW is restricting its use case. To address companies’ concern on how to support more than 64 candidate locations, we have the following suggestion:   * For 120kHz SSB, the number of candidates SSBs in a half frame for DBTW is:   + Alt 1) 64   + Alt 2) 80     - Using a physical layer bit in PBCH payload to indicate the extra candidate SSB index, e.g. the 4th LSB of SFN.   **Proposal 1.1-2C)**  We are ok with the proposal.  **Proposal 1.1-6A)**  The UE assumption of DBTW is used prior to decoding MIB for Alt 2 is not needed. In our understanding, it’s up to UE’s implementation, e.g. if sync raster can imply the band is licensed, the UE doesn’t need to perform such assumption.  Also, the wording “during initial access” is not needed in both notes, since the impact can be more than initial access.  To be more precise, the wording we are thinking of is as follow:   * For supported SCS cases of DBTW, the indication of use or no use of DBTW will be   + Alt 1: implicitly indicated     - UE assumes DBTW is used prior to deriving implicit indication.     - [Note: implicit indication means that specification should support gNB that wishes to disable DBTW can operate identically with DBTW enabled and with specific set of parameters configured for DBTW during initial access. UE may be able to determine that gNB is not using DBTW from detected SSBs and set of parameters configured for DBTW, but use of this knowledge may not necessarily change UE behavior ~~during initial access~~.]     - FFS details of implicit indication in MIB and/or SIB1   + Alt 2: explicit indicated in MIB     - ~~[UE assume DBTW is used prior to decoding MIB]~~     - [Note: explicit indication means that gNB operation behavior when DBTW is indicated to be disabled is not completely the same as when DBTW is enabled, as a consequence indication is needed to inform UE of change in behavior to operation ~~during initial access~~.]   + Alt 3: indication via synchronization raster entry |
| Qualcomm | Proposal 1.1-4B: support  Proposal 1.1-3C: as mentioned in previous comments, still believe this is premature. We need to agree on the number of bits (and where to get them), the number of candidate SSBs first, and Q indication method  Proposal 1.1-5B: support  Proposal 1.1-2C: support, but prefer to have “DCI format 1\_0 monitored in **~~a common search space~~ SI-RNTI**”  Proposal 1.1-6A: do not support as is as it is not very clear on the purpose here for Alt 1. We prefer the original text for Alt 1 of something like: “*For supported SCS cases of DBTW, the indication of use or no use of DBTW will be implicitly indicated (DBTW is used or not used is derived via configuration of MIB parameter(s) in certain combinations) in MIB.*” |
| Lenovo, Motorola Mobility | Proposal 1.1-4B) – cleaned up: support  Proposal 1.1-3C) – cleaned up: support with Alt 2 preference  Proposal 1.1-5B) – cleaned up: support |
| Futurewei | Proposal 1.1-4B) – cleaned up: supportProposal 1.1-3C) – cleaned up: support - Alt 1preferred Proposal 1.1-5B) – cleaned up: support  Proposal 1.1-2C) – cleaned up: support  Proposal 1.1-6A) – cleaned up: support – Alt 1 preferred; OK with Samsung proposed change |
| Ericsson | Proposal 1.1-4B): Support Proposal 1.1-3C): Support as an intermediate step.  However, we think it is needed to have aligned sizes for licensed/unlicensed for DCI 1\_0 CRC scrambled with all RNTIs. Our understanding is that there is a limitation on the number of DCI sizes that the UE is expected to handle, so it would be preferrable to have the same size for licensed/unlicensed in all cases for DCI 1\_0.  Proposal 1.1-5B):  Support 64 candidate positions.    We have strong concerns against 80 candidate positions. Regarding the following approach suggested by Samsung above: "Using a physical layer bit in PBCH payload to indicate the extra candidate SSB index, e.g. the 4th LSB of SFN", it seems that this will imply a change to the basic assumption in Rel-15 that the MIB does not change more often than 80 ms. Furthermore, we have concerns that this will result in changes to low level physical layer processing, e.g., scrambling, compared to Rel-15, which is not preferred from an implementation reuse perspective.  Proposal 1.1-2C):  It seems that the same note Proposal 1.1-6A): We still have confusion about the meaning of implicit, and further, it seems like there is a inter-connection between Proposal 3C and 6A. In 3C there are notes saying " Value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB." Is this the same meaning of implicit as in 6A? The definitions of implicit and explicit in 6A are really vague.  We think a lot of confusion would be eliminated if we took agreements in the following step-wise approach to avoid confusion:   1. Decide on # of candidate SSB positions first 2. Once this is known, Proposal 3C can be made more concrete, i.e., we can determine alternatives for the number of Q values, and we can concretely decide if Q = 64 means DBTW off, or if it represents a valid value of Q 3. Once the number of Q values are known and whether or not Q = 64 means DBTW off, then we may not even need Proposal 6A.   In summary, we see no need for Proposal 6A at this stage, and we do not support having a proposal that is vague and creates confusion. |
| LG Electronics | Proposal 1.1-4B): Support Proposal 1.1-3C): We also have a concern on the NOTEs which require separate discussion and can be captured in Proposal 1.1-6A if clarification for implicit manner is needed.  Proposal 1.1-5B): Support, same concern with Ericsson for 80 SSB positions  Proposal 1.1-2C): Support, OK with Qualcomm’s suggestion  Proposal 1.1-6A): We are generally fine once we can have the same understanding on what implicit indication implies. Alt 1 can be FFS until other aspects (such as the maximum number of SSB candidate positions) are settled down. |
| NEC | Proposal 1.1-4B): Support. Proposal 1.1-3C): We also think it is premature to make a decision on this proposal before identifying the number of candidate SSBs. And as such, we share the same views with Qualcomm and Ericsson, namely the number of candidate SSBs and SSB index indication should be determined firstly.  Proposal 1.1-5B) We still prefer to keep the alternative of 80 and support the Samsung’s revising suggestion on this proposal. Regarding the concern of SSB index indication, we are open to discuss it further based on reusing or repurposing a bit in MIB separately or jointly coded with other indication.  Proposal 1.1-2C) Support. |
| ZTE, Sanechips | Proposal 1.1-4B) – cleaned up: supportProposal 1.1-3C) – cleaned up: support and prefer Alt 2 (Alt 1 can be accepted if there are not enough bits in MIB to indicate ). Proposal 1.1-5B) – cleaned up: support  Proposal 1.1-2C) – cleaned up: support  Proposal 1.1-6A) – cleaned up: three parts “during initial access” should be deleted (Samsung pointed out two of them) as the indication of use or no use of DBTW is not only applied in initial access case. |
| InterDigital | Proposal 1.1-4B) Support.  Proposal 1.1-3C) Support.  Proposal 1.1-5B) Support.  Proposal 1.1-2C) Support. Proposal 1.1-6A) As Samsung has mentioned, we don’t see the need to include “UE assume DBTW is used prior to decoding MIB” in Alt2. |
| Nokia | Proposal 1.1-4B): We are OK.  Proposal 1.1-3C): With the risk of sounding like a broken record I don’t really understand why the lower value for the would need to be fixed to 16 if there are only two values indicated? I understand that in NR-U, only 8 were supported, but it would seem that when going to one decade larger frequency range it would be preferable to consider larger value, e.g. 32, (which could also be used with lower number of SSBs).  Hence, maybe we should first try reach consensus how many values can at least indicated e.g .2 or 4. After that has been agreed (possibly after we have also concluded the number of candidate locations), we can further discuss which values are supported.   |  | | --- | | **Proposal 1.1-3C) – cleaned up**  * For supported SCS cases of DBTW, support configuration of in MIB, ~~with at least {16, 64}values. Additionally,~~ down-select among the following alternatives.   + Alt 1: ~~no additional values are supported,~~ total of 2 states of values are supported ~~(i.e. {16,64})~~     - FFS the exact values e.g. {16,64} or {32,64}     - Note: Value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB   + Alt 2: ~~two additional values,~~ total of 4 states of values are supported ~~(i.e. {16, 64, X, Y})~~     - FFS on the ~~two additional~~ values, e.g. {16,64,X,Y}     - Note: Value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB or single state may be reserved e.g. (e.g. {16, 64, X, DBTW disabled}) to explicitly indicate that DBTW is disabled   + ~~Alt 3: one addition value, and reserved state that indicates DBTW disabled, total of 3 states of values and 1 state of DBTW disabled are supported. (i.e. {16, 64, X, DBTW disabled})~~ |   Proposal 1.1-5B): We still think this is rather restrictive, in terms of applying DBTW with larger number of beams.  Proposal 1.1-2C): We share the same view as Qualcomm that if we need to align we focus to the DCI format 1\_0 monitored for SI-RNTI as it will reduce the number of hypothesis (which we don’t think is a major issue considering that this would be unknown only during cell selection phase). As the DCI size budget is per cell, it does not seem necessary to extend this size alignment to other DCI formats.  Proposal 1.1-6A):  As general comment regarding DBTW indication, if the information is provided in MIB, it is not clear what is the benefit in terms on SIB1 acquisition. The for NR-U the Type0-PDCCH search space is defined based on candidate SSB block index . Hence, we don’t see it necessary to provide this explicitly in MIB. It could be possible to provide this explicitly in SIB1, if the indication is not deemed necessary for initial cell search (=initial access).  Thus we would propose to change Alt 2 as follows:   * + Alt 2: explicit indicated in MIB or SIB1 |
| Intel | **Proposal 1.1-4B) –** We are fine. **Proposal 1.1-3C) –** Support.  **Proposal 1.1-5B) –** Do not support.  To address some companies’ concerns about larger number of candidate SSB indices (i.e., 80) and especially Ericsson’s concerns regarding the suggestion from Samsung, we propose the following modification:   * For 120kHz SSB, the number of candidates SSBs in a half frame for DBTW is:   + Alt 1) 64   + Alt 2) 80     - Using a MIB bit to indicate the extra candidate SSB index, e.g., the *subCarrierSpacingCommon* bit.   In this case, there is no changes for the low-level processing of SSB and the MIB does not change more often than 80 ms for the SSBs with *the same candidate index*.  There is one more thing we would like to bring up. This is the max number of SSB candidates for SCS 480 kHz/960 kHz. It’s expected that the operation based on the max number of beams (64) would be typical for these SCS values. However, if the max number of candidate SSBs is limited to 64, e.g., motivated by concerns regarding MIB content changing from one candidate SSB to another candidate SSB, we will effectively get the operation without DBTW. Of course, this is something that some companies prefer. But we would like to mention that there are scenarios with mandatory LBT operation for SCS 480 kHz/960 kHz.  **Proposal 1.1-2C) –** Support  **Proposal 1.1-6A)** – Support |
| DOCOMO | Proposal 1.1-4B) Support  Proposal 1.1-3C): We tend to agree with Nokia regarding smaller Q value. Why 16 is not very clear to us. Also agree deciding the number of candidate SSB positions would be 1st step for this proposal.  Proposal 1.1-5B): Support. We do not think Intel’s proposal would be good since it is much different from the design in Rel-16 NR-U without clear benefit. By doing this, it raises another question like “how to indicate Q?”. Just to resolve the number of candidate SSB positions is not very good in our view.  Proposal 1.1-2C): We are fine with the Proposal. Also ok with Qualcomm’s point, i.e. focusing on DCI 1\_0 with CRC scrambled by SI-RNTI. Proposal 1.1-6A): We think Ericsson has a valid point. Once the number of candidate SSB positions is decided, possibility of such explicit/implicit indication could be much clearer. |
| Huawei, HiSilicon | **Proposal 1.1-4B)** Support  **Proposal 1.1-3C)** For the sake of progress, we can accept this if the “Note” in Alt 2 and Alt 3 is changed to “FFS”:   * For supported SCS cases of DBTW, support configuration of in MIB, with at least {16, 64}values. Additionally, down-select among the following alternatives.   + Alt 1: no additional values are supported, total of 2 states of values are supported (i.e. {16,64})     - ~~Note:~~ FFS: Value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB   + Alt 2: two additional values, total of 4 states of values are supported (i.e. {16, 64, X, Y})     - FFS on the two additional values     - ~~Note:~~ FFS: Value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB   + Alt 3: one addition value, and reserved state that indicates DBTW disabled, total of 3 states of values and 1 state of DBTW disabled are supported. (i.e. {16, 64, X, DBTW disabled})   **Proposal 1.1-5B)** Support  **Proposal 1.1-2C)** Support the first and second bullets. For the third bullet, we think it is more accurate to change “DCI format 1\_0 monitored in a common search space” to “DCI format 1\_0 ~~monitored in a common search space~~ with CRC scrambled with SI-RNTI”. However, if we are OK if the current form has a strong majority support.  **Proposal 1.1-6A)** Support with the following modifications on the notes. In particular, we don’t see how implicit indication or explicit indication to the UE may have impact on the gNB’s operation. gNB can have a mode of operation and depending on what is agreed in 3GPP indicate that mode of operation to the UE implicitly or explicitly:   * For supported SCS cases of DBTW, the indication of use or no use of DBTW will be   + Alt 1: implicitly indicated     - UE assumes DBTW is used prior to deriving implicit indication.     - [Note: implicit indication means that ~~specification should support gNB that wishes to disable DBTW can operate identically with DBTW enabled and with specific set of parameters configured for DBTW during initial access.~~ UE may be able to determine that gNB is not using DBTW from detected SSBs and/or the values of set of configured parameters where each individual parameter value in the set can be used for a purpose other than indicating whether or not DBTW is used ~~configured for DBTW,~~ ~~but~~ The use of this knowledge may not necessarily change UE behavior during initial access.]     - FFS details of implicit indication in MIB and/or SIB1   + Alt 2: explicit indicated in MIB     - [UE assume DBTW is used prior to decoding MIB]     - [Note: explicit indication means that a specific parameter value is dedicated to exclusively indicate to the UE whether or not DBTW is in use. ~~that gNB operation behavior when DBTW is indicated to be disabled is not completely the same as when DBTW is enabled, as a consequence indication is needed to inform UE of change in behavior to operation during initial access.~~]   + Alt 3: indication via synchronization raster entry   **Further reply to Ericsson:**  Thank you for your earlier reply to our questions. Please see our further inline comments to your reply.  **[Ericsson]:** As answered by LGE and Samsung, the 60 GHz band is fundamentally different than Bands n46/n96 in Rel-16 in that licensed operation is supported, and clearly DBTW does not make sense in licensed operation. Moreover, even in unlicensed operation, not all deployments require use of DBTW. As commented Apple (and also by Samsung), "Without knowing DBTW on/off before SIB acquisition, UE need to search larger number of MOs of Type0-CSS."  **[Huawei]:** We appreciate the fact that in 60 GHz spectrum a band maybe unlicensed in one region and licensed in another region. However, as we explained in our earlier comments, in our view, whether or not UE assumes DBTW is used or not used has no impact on UE behavior in licensed operation during initial access: In licensed operation, if candidate SSB index “a” (which is also the SSB index “a”) of a PCell is transmitted, the Type0-PDCCH corresponding to candidate SSB index “a” is also supposed to be transmitted. If UE detects candidate SSB index “a”, it goes on to receive Type0-PDCCH corresponding to the same candidate SSB index “a”, then reads SIB1 and moves on to the subsequent steps of cell connection establishment. Therefore, to our understanding, ***whether or not UE assumes DBTW is used or not used has no impact on UE behavior in licensed operation***. In unlicensed operation, if candidate SSB index “a” of a PCell is transmitted, it may happen that the Type0-PDCCH corresponding to candidate SSB index “a” is not transmitted due to LBT failure. In such a case, obviously, UE cannot find the Type0-PDCCH corresponding to candidate SSB index “a”, but, since it knows from the MIB of candidate SSB index “a”, it would know the location of the CORESET#0 corresponding to the candidate SSB index “a+” which would be QCL-D with the detected candidate SSB index “a”. So, UE can go and find the Type0-PDCCH from the CORESET#0 corresponding to the candidate SSB index “a+”. ***So, all in all, during initial access, UE would use the assumption that DBTW is used only when it detects a candidate SSB “a” of a PCell but cannot find the Type0-PDCCH corresponding to the detected candidate SSB “a” which typically happens only in unlicensed operation.***  **[Ericsson]:** Furthmore, indication of DBTW on/off for IDLE mode UEs has already been agreed in RAN1, and we do not wish to revert that agreement. As pointed out by Nokia, UEs performing initial cell selection (prior to SIB1 reading) are indeed in IDLE mode  **[Huawei]:** There is no need to revert any agreement. The agreement in RAN1 104b-e states “If DBTW is supported Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs”. The simplest way to support this agreement is that (IDLE) UE assume DBTW is enabled until DBTW enabled/disabled is (implicitly) indicated to the UE. We don’t understand how such mechanism would be reverting an agreement specially if such a mechanism is simple, used in Rel-16 NR-U (already supported in specifications), and works perfectly (please see the first part of our answer on how). |
| Samsung2 | We would like to respond to Huawei’s comment on the Type0-PDCCH monitoring. Following Rel-16 NR-U, clearly there is a difference on the UE behavior on whether to use Q on Type0-PDCCH monitoring. When DBTW is not enabled (e.g. Rel-15 legacy behavior), a UE only needs to monitor the single associated Type0-PDCCH with the detected SSB; while when DBTW is enabled (e.g. Rel-16 NR-U), a UE needs to monitor all the Type0-PDCCH associated with the candidate SSB QCLed with the detected SSB. Please also note that decoding Type0-PDCCH also rely on soft combining up to 160 ms TTI, which is 8 times combining e.g. for pattern 1, then the issue of blind detection will increase exponentially when using a small value of Q. Let’s assume a simple case Q=16 is indicated but the UE doesn’t know whether DBTW is off, then the UE needs to perform up to 4^8 blind detection to decode Type0-PDCCH, which is a disaster for the case DBTW is actually off (which doesn’t require blind detection at all). |
| OPPO | Proposal 1.1-4B: support  Proposal 1.1-3C: support  Proposal 11-5B: we also think that 64 is restrictive. In particular for the FR2.2 where the analogue beam is quite narrow, fixing 64 seems to trade the channel access opportunity with coverage.  Proposal 1.1-2C: we agree with DCI 1\_0 with SI-RNTI should be discussed.  Proposal 1.1-6A: For Alt-1, does the note restrict that the UE behavior should not be changed no matter whether the UE determines the DBTW is enabled or disabled? Then our follow-up question is what the point is to determine the DBTW? |
| Convida Wireless | Proposal 1.1-4B) – cleaned upWe are ok with the proposal.Proposal 1.1-3C) – cleaned upWe are generally ok with the proposal.Proposal 1.1-5B) – cleaned up We share the same view with other companies. Concern to cope with channel uncertainty and LBT failure may need to be addressed. We prefer to keep the alternative of 80 in the proposal.  Proposal 1.1-2C) – cleaned up  We are ok with the proposal  Proposal 1.1-6A) – cleaned up  We are ok with the proposal |

#### **4th Round Discussion Summary:**

Based on comments received, Proposal 1.1-4B seems to be agreeable and Proposal 1.1-2C is generally agreeable. Moderator has updated Proposal 1.1-2C to 5D to change back DCI format 1\_0 size alignment for DCI format 1\_0 scrambled with SI-RNTI. From moderator’s understanding, even for companies who prefers even wider alignment for other formats, should be in principle ok with Proposal 1.1-2D.

Moderator suggest Proposal 1.1-4B and Proposal 1.1-2D for email approval. Only provide comments if you have serious problems with Proposal 1.1-4B and Proposal 1.1-2D.

**-**

* For DBTW with 120kHz SCS (if supported), support DBTW lengths {0.5, 1, 2, 3, 4, 5} msec
  + Note: this should be the same as Rel-16 NR-U DBTW lengths.
* Support: Ericsson, Futurewei, Lenovo/Motorola Mobility, Qualcomm, Samsung, LGE, Futurwei, NEC, ZTE/Sanechips, Interdigital, Nokia, Intel, Docomo, Huawei/HiSilicon, OPPO, Convida Wireless
* Not ok: -

**Proposal 1.1-2D)**

* No indication for licensed and unlicensed operation in MIB
  + Whether and/or how LBT/No-LBT is indicated is separately discussed
* Use of LBT is not indicated in MIB.
  + FFS where and how this is indicated, e.g. SIB1
* For both licensed or unlicensed operation and with or without LBT, support the same DCI size for:
  + DCI format 1\_0 scrambled with SI-RNTI monitored in a common search space
    - Note: existing bit padding/truncation rules are assumed to applied for DCI format 0\_0 monitored in common search space.
  + FFS for other cases ~~DCI format 1\_0 monitored in USS~~
* Support: Ericsson, LGE, Futurwei, Qualcomm, Futurewei, NEC, ZTE/Sanechips, [Nokia/NSB], Intel, Huawei/HiSilicon, Docomo, Convida Wireless
* Not ok: -

As for DBTW, we are still somewhat split in views including how the signaling would be supported. However, moderator thinks it will be difficult to get progress on other proposals without making some progress on at least number of candidates and number of states needed for Q indication. Moderator suggests trying to conclude on this this meeting (without listing alternatives), so that other aspects of DRS design can be resolved.

**Proposal 1.1-5B)**

* For 120kHz SSB, the number of candidates SSBs in a half frame for DBTW is 64
* Support: Ericsson, LGE, Futurwei, Qualcomm, ZTE/Sanechips, Interdigital, Docomo, Huawei/HiSilicon, Xiaomi, Panasonic, Mediatek, Charter
* Not ok: Samsung, NEC, Nokia, Intel, OPPO
  + Reasons for concern:
    - Number of candidates are too restrictive

**Proposal 1.1-5C)**

* For 120kHz SSB, the number of candidates SSBs in a half frame for DBTW is 80
* Support: Intel, OPPO, Convida Wireless, Sony, Nokia, NEC, ZTE/Sanechips
* Not ok: Ericsson, LGE
  + Reasons for concern:
    - Number of bits available in PBCH

On the values supported for there was at least one company who had concerns of potentially only supporting {16,64}, especially the 16 as the numbers were thought to be too low. Moderator has listed Proposal 1.1-3D based on comments received.

**Proposal 1.1-3D)**

* For supported SCS cases of DBTW, support configuration of in MIB, ~~with at least {16, 64}values. Additionally,~~ down-select among the following alternatives (after number of candidate SSB positions have been determined).
  + Alt 1: ~~no additional values are supported,~~ total of 2 states of values are supported ~~(i.e. {16,64})~~
    - FFS the exact values e.g. {16,64} or {32,64}
    - ~~Note:~~ FFS Value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB
  + Alt 2: ~~two additional values,~~ total of 4 states of values are supported ~~(i.e. {16, 64, X, Y})~~
    - FFS on the ~~two additional~~ values, e.g. ~~{16,64,X,Y}~~ {8,16,32,64}
    - ~~Note:~~ FFS Value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB or single state may be reserved e.g. (e.g. {16, 32, 64, ~~X,~~ DBTW disabled}) to explicitly indicate that DBTW is disabled
  + ~~Alt 3: one addition value, and reserved state that indicates DBTW disabled, total of 3 states of values and 1 state of DBTW disabled are supported. (i.e. {16, 64, X, DBTW disabled})~~

Also there was at least four companies (Samsung, LGE, Qualcomm, NEC) who wanted to defer this conclusion until we were able to determine the number of SSB candidates. This seems to be because of the bit count available for PBCH. From moderator’s understanding below table is the bit count for PBCH. I believe, companies have identified based on Plenary decision, the SCS common field may not have a use for 60GHz operations as we only support same SCS between SSB and CORESET. Samsung also commented that there is 1 bit for future use (i.e. “spare” bit) available. Moderator would like to ask companies to also provide information on which bits are to be used from PBCH to support the preferred values for . Previously in NR-U, the four states of were indicated using 1 bit from SSB SCS offset field and SCS common field.

|  |  |  |  |
| --- | --- | --- | --- |
| Fields in PBCH (PHY) | Fields in BCH (MAC) | Number of bits | Note |
|  | Message Class Extension | 1 |  |
|  | 5 MSB of SFN | 6 |  |
|  | SCS common | 1 | used in Rel-16 NR-U for |
|  | SSB SCS offset | 4 | LSB 1 bit used in Rel-16 NR-U for |
|  | DMRS Type-A position | 1 |  |
|  | PDCCH config –CORESET#0 | 4 |  |
|  | PDCCH config –  SS#0 | 4 |  |
|  | Cell-barred | 1 |  |
|  | Intra-freq. re-selection | 1 |  |
|  | Spare | 1 |  |
|  | Total MAC bits | 24 |  |
| 4 LSB of SFN |  | 4 |  |
| Half radio frame |  | 1 |  |
| MSB of SSB index |  | 3 |  |
| CRC |  | 24 |  |
| Total PHY bits |  | 32 |  |
| Total PBCH bits | | 56 |  |

Moderator thinks that further discussion to find out what exactly companies would like to support for how is indicated in MIB and how DBTW may or may not be potentially enabled/disabled in MIB would be helpful.

While based on comments it might be not possible to agree to Proposal 1.1-6B, moderator still thinks having further discussion on this would aid progression of the discussion and help make decisions.

**Proposal 1.1-6B)**

* For supported SCS cases of DBTW, the indication of use or no use of DBTW will be
  + Alt 1: implicitly indicated
    - UE assumes DBTW is used prior to deriving implicit indication.
    - [Note: implicit indication means that ~~specification should support gNB that wishes to disable DBTW can operate identically with DBTW enabled and with specific set of parameters configured for DBTW during initial access.~~ UE may be able to determine that gNB is not using DBTW from detected SSBs and/or the values of set of configured parameters where each individual parameter value in the set can be used for a purpose other than indicating whether or not DBTW is used ~~configured for DBTW,~~ ~~but~~ The use of this knowledge may not necessarily change UE behavior ~~during initial access~~.]
    - FFS details of implicit indication in MIB and/or SIB1
  + Alt 2: explicit indicated in MIB
    - ~~[UE assume DBTW is used prior to decoding MIB]~~
    - [Note: explicit indication means that a specific parameter value is dedicated to exclusively indicate to the UE whether or not DBTW is in use. ~~that gNB operation behavior when DBTW is indicated to be disabled is not completely the same as when DBTW is enabled, as a consequence indication is needed to inform UE of change in behavior to operation during initial access.~~]
  + Alt 3: indication via synchronization raster entry

#### **5th Round Discussion – Part 1:**

Any concerns on approving Proposal 1.1-4B and Proposal 1.1-2D. Moderator will ask for email approval for the following proposals.

**Proposal 1.1-4B)**

* For DBTW with 120kHz SCS (if supported), support DBTW lengths {0.5, 1, 2, 3, 4, 5} msec
  + Note: this should be the same as Rel-16 NR-U DBTW lengths.

##### **Proposal 1.1-2D)**

* No indication for licensed and unlicensed operation in MIB
  + Whether and/or how LBT/No-LBT is indicated is separately discussed
* Use of LBT is not indicated in MIB.
  + FFS where and how this is indicated, e.g. SIB1
* For both licensed or unlicensed operation and with or without LBT, support the same DCI size for:
  + DCI format 1\_0 scrambled with SI-RNTI monitored in a common search space
    - Note: existing bit padding/truncation rules are assumed to applied for DCI format 0\_0 monitored in common search space.
  + FFS for other cases

**Proposal 1.1-2E)**

* No indication for licensed and unlicensed operation in MIB
  + Whether and/or how LBT/No-LBT is indicated is separately discussed
* Use of LBT is not indicated in MIB.
  + FFS where and how this is indicated, e.g. SIB1
* For both licensed or unlicensed operation and with or without LBT, support the same DCI size for:
  + DCI format 1\_0 ~~scrambled with SI-RNTI~~ monitored in a common search space
    - Note: existing bit padding/truncation rules are assumed to applied for DCI format 0\_0 monitored in common search space.
  + FFS for other cases

**Only provide comments if you have issues/concerns.**

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| Company | Comments |
| Ericsson | Proposal 1.1-2D:  As we stated previously in this email discussion and on the reflector, we share a similar view as Apple and LGE regarding DCI 1\_0 size alignment for licensed/unlicensed. It seems like the simplest solution is to align the size for all cases. We proposed this earlier in the email discussion with a similar argument that there is a limited number of DCI sizes that the UE is expected to handle.  We understand that Proposal 1.2-2D is meant as an intermediate step, and we still have to discuss other use cases; however, to address our concerns, perhaps the FFS could be amended as follows:   * + FFS for other cases including accounting for limitations on the total number of DCI sizes the UE is expected to handle |
| Apple | We are ok with the proposal and just document the discussions over email on **Proposal 1.1-2D) – cleaned up, as suggested by FL.**  As commented in email reflector, our understanding that the same size rule defined for ‘DCI format 1\_0 scrambled with SI-RNTI’ should be applied for all DCI format 1\_0 with other RNTIs in CSS due to the DCI size budget limitation i.e., ‘3 (for C-RNTI) +1 (for other RNTIs)’; Otherwise, it violates the budget of ‘1’ for other RNTIs. Other solution mentioned in email reflector by Qualcomm is to indicate ‘licensed vs. unlicensed’ in SIB1 and then determine the DCI format 1\_0 based on the indication. However, we do not think it works because it results in two DCI format sizes for DCI format 1\_0 with other RNTIs in licensed band, one size is for DCI format 1\_0 with SI-RNTI (Size A) with alignment and other size is for DCI format 1\_0 with other RNTI except C-RNTI (Size B). It exceeds the size budget.  The proposal can be as follows:   * For both licensed or unlicensed operation and with or without LBT, support the same DCI size for:   + DCI format 1\_0 ~~scrambled with SI-RNTI~~ monitored in a common search space |
| vivo | For Proposal 1.1-2D, we share the same view as Ericsson and Apple. As commented in the 1st round, DCI 1\_0 size is not associated with a specific RNTI but CSS/USS. We support Apple’s change. |
| OPPO | We are fine with 1.1-4B and 2D |
| ZTE, Sanechips | We share similar view as Ericsson, Apple, LGE and vivo on Proposal 1.1-2D. We prefer Apple’s modification. |
| Moderator | Added Proposal 1.1-2E to address concerns from companies. Please comment if companies have concern on 1.1-2E or not. |

#### **5th Round Discussion – Part 2:**

Please provide comments on the main reasons for concern for Proposal 1.1-5B and 1.1-5C, which are alternatives that we should try to narrow down between.

**Proposal 1.1-5B)**

* For 120kHz SSB, the number of candidates SSBs in a half frame for DBTW is 64
* Support: Ericsson, LGE, Futurwei, Qualcomm, ZTE/Sanechips, Interdigital, Docomo, Huawei/HiSilicon
* Not ok: Samsung, NEC, Nokia, Intel
  + Reasons for concern:
    - Number of candidates are too restrictive

**Proposal 1.1-5C)**

* For 120kHz SSB, the number of candidates SSBs in a half frame for DBTW is 80
* Support: Nokia, ZTE/Sanechips, Intel, Samsung, NEC
* Not ok: Ericsson, LGE, Qualcomm, NTT DOCOMO
  + Reasons for concern:
    - Number of bits available in PBCH unclear
    - Gap between set of SSBs transmission is needed for uplink transmissions

Please provide comments on the **reasons for concern to accepting the proposals**. Also please directly correct the support/not support summary above if there are any mistakes or missing company names in RED.

Moderator will summarize the main reasons and ask for Chairman guidance on path forward.

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| Company | Comments |
| Qualcomm | Do not support Proposal 1.1-5C. We need to retain the gaps and the number of bits. |
| Samsung | We support 1.1-5C and don’t support 1.1-5B.  Other than the restriction on using the DBTW as explained in the previous comment, we also want to note that current SSB pattern in half frame for 120 kHz has slot-level gaps in the burst, which requires additional LBT when transmitting on the unlicensed spectrum. We want to at least provide a possibility to transmit a burst of SSB without slot level gap.  We are thinking whether the following can be a compromised proposal:  For 120kHz SCS,   * If one bit in PBCH payload can be reinterpreted to indicate the MSB of candidate SSB index, the number of candidates SSBs in a half frame for DBTW is 80; * Otherwise, the number of candidates SSBs in a half frame for DBTW is 64. |
| NEC | We added our support in Proposal 1.1-5C. As our comment in last round discussion, the available bits to indicate 80 candidate SSBs positions is the basis of this issue, as for this point, we share the same view as Samsung’s comment above, we can go with Proposal 1.1-5B for the sake of progress after it’s identifed that indeed no enough bits in MIB can be used to indicate 80 candidates SSBs. |
| Ericsson | We cannot accept Proposal 1.1-5C  As we stated before, we have strong concerns against 80 candidate positions. Regarding the following approach suggested by Samsung above: "Using a physical layer bit in PBCH payload to indicate the extra candidate SSB index, e.g. the 4th LSB of SFN", it seems that this will imply a change to the basic assumption in Rel-15 that the MIB does not change more often than 80 ms. Furthermore, we have concerns that this will result in changes to low level physical layer processing, e.g., scrambling, compared to Rel-15, which is not preferred from an implementation reuse perspective. |
| ZTE, Sanechips | Our original preference is Proposal 1.1-5C because it provides more opportunities for SSB transmission. We can accept the Proposal 1.1-5B as well if it’s identified that there is not enough bits in MIB for signaling. |
| Nokia | Proposals 1.1-5B) and 1.1-5C): Our position here would still be to consider 80 (as per 1.1-5C). Regarding bit to indicate SSB index, we could consider using one bit from SSB offset similar as in case of NR-U, but acknowledge that this results a dependency to RAN4 (or vice-versa). We would be fine with Samsung’s proposal. |
| DOCOMO | Do not support Proposal 1.1-5C. From our perspective, gaps for other purposes like UL transmissions should be kept. |
| Moderator | Added reasons for concern on 1.1-5C explained by Qualcomm and Docomo |
| Intel | We support Proposal 1.1-5C) because it is more flexible than Proposal 1.1-5B), which is too restrictive and may result in loss of SSB transmission with specific beams under LBT scenarios, which is the whole point of having DBTW, and that’s why we don’t support it.  Regarding the gaps, Proposal 1.1-5C) still allows having gaps. If gNB is aware about high-priority UL traffic for UE, it always can de-prioritize transmission of SSB candidate, doesn’t it? For other UEs it would look like LBT event.  Regarding additional bit, as we commented previously, using a MIB bit to indicate the extra candidate SSB index, e.g., the *subCarrierSpacingCommon* bit, would not require changes for the low-level processing of SSB and the MIB does not change more often than 80 ms for the SSBs with the same candidate index. |

#### **5th Round Discussion – Part 3:**

Moderator asks to provide further comments on Proposal 1.1-3D. Even if it is determined we are unable to agree to the proposals are this time, moderator believe there is value in trying to further narrow down and get better understanding among companies.

##### **Proposal 1.1-3D)**

* For supported SCS cases of DBTW, support configuration of in MIB, down-select among the following alternatives (after number of candidate SSB positions have been determined).
  + Alt 1: total of 2 states of values are supported
    - FFS the exact values e.g. {16,64} or {32,64}
    - FFS Value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB
  + Alt 2: total of 4 states of values are supported
    - FFS on the values, e.g. {8,16,32,64}
    - FFS Value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB or single state may be reserved e.g. (e.g. {16, 32, 64, DBTW disabled}) to explicitly indicate that DBTW is disabled

##### **Proposal 1.1-6B)**

* For supported SCS cases of DBTW, the indication of use or no use of DBTW will be
  + Alt 1: implicitly indicated
    - UE assumes DBTW is used prior to deriving implicit indication.
    - [Note: implicit indication means that UE may be able to determine that gNB is not using DBTW from detected SSBs and/or the values of set of configured parameters where each individual parameter value in the set can be used for a purpose other than indicating whether or not DBTW is used. The use of this knowledge may not necessarily change UE behavior]
    - FFS details of implicit indication in MIB and/or SIB1
  + Alt 2: explicit indicated in MIB
    - [Note: explicit indication means that a specific parameter value is dedicated to exclusively indicate to the UE whether or not DBTW is in use]
  + Alt 3: indication via synchronization raster entry

Moderator has made clarification to 1.1-3D in Proposal 1.1-3E based on comments received.

##### **Proposal 1.1-3E)**

* For supported SCS cases of DBTW, support configuration of in MIB, down-select among the following alternatives (after number of candidate SSB positions have been determined).
  + Alt 1: total of 2 states of values are supported
    - FFS the exact values e.g. {16,64} or {32,64}
    - Note: ~~FFS~~ v~~V~~alue of 64 (if supported) may be used as implicit determination by the UE that DBTW is not enabled by gNB if maximum number of candidate SSB is 64
  + Alt 2: total of 4 states (including any potential reserved state) of values are supported
    - FFS on the values, e.g. {8,16,32,64}
    - FFS whether or not a single state will be reserved to explicitly indicate that DBTW is disabled e.g. (e.g. {16, 32, 64, reserved/DBTW disabled})
      * Note: v~~V~~alue of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB if maximum number of candidate SSB is 64; or single state may be reserved e.g. (e.g. {16, 32, 64, DBTW disabled}) to explicitly indicate that DBTW is disabled

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| Company | Comments on Proposal 1.1-3D and Proposal 1.1-6B |
| Qualcomm | Proposal 1.1-3D: generally ok, but this sentence “*FFS Value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB*” is only valid if the number of candidates is 64, right? i.e., if # candidates = 80, it may not work?  Proposal 1.1-6B: support Alt 1. |
| LG Electronics | We are fine with Proposal 1.1-3D and Proposal 1.1-6B, but prefer Alt 1 for Proposal 1.1-3D and Alt 2 or Alt 3 for Proposal 1.1-6B. |
| Samsung | We thank FL addressed our comments.  First, we want to note that from our perspective, the discussion of 1.1-3D should happen after the conclusion of 1.1-6B, i.e., whether a UE can determine DBTW is disabled after reading MIB. This is the most essential issue for us in implementation. If a UE cannot know whether DBTW is disabled or not after reading MIB, we don’t see the need to support any alternative in 1.1-3D, since knowing Q value without knowing DBTW on/off is useless.  For 1.1-3D, the FFS in Alt 2 seems contradicting with the statement of 4 states of Q values, since Q value is not applicable when DBTW is not enabled. We still prefer the original organization of the proposal to leave with 3 alternatives.   * For supported SCS cases of DBTW, support configuration of in MIB, down-select among the following alternatives (after number of candidate SSB positions have been determined).   + Alt 1: total of 2 states of values are supported     - FFS the exact values e.g. {16,64} or {32,64}     - FFS Value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB   + Alt 2: total of 4 states of values are supported     - FFS on the values, e.g. {8,16,32,64}     - FFS Value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB ~~or single state may be reserved e.g. (e.g. {16, 32, 64, DBTW disabled}) to explicitly indicate that DBTW is disabled~~   + Alt 3: total of 3 states of values are jointly coded with DBTW disabled     - FFS on the values, e.g. {16,32,64}   For 1.1-6B, we are ok with current formulation, but has a question on Alt 3 (actually we provided comment before). The sync raster information is fixed per band, but DBTW on/off can be controllable by network, then how to use sync raster to indicate DBTW on/off? We can understand using sync raster to indicate licensed/unlicensed, but need clarification on DBTW on/off. |
| Ericsson | **Proposal 1.1-3D)**  We have the same question as Qualcomm: “*FFS Value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB*” is only valid if the number of candidates is 64, right? i.e., if # candidates = 80, it may not work?  Hence, we really must conclude on the number of candidate SSB positions first.  If 64 is supported, then we support Alt-1 with {32,64} where 64 is used as an implicit determination by the UE that DBTW is not enabled. This will require one bit in MIB, and we know already that at least one is available, i.e., *ssbSubcarrierSpacingCommon*  If magically, 2 bits can be found in MIB, then Alt-2 can be viable, where again 64 indicated DBTW is not enabled.  @Samsung: Could you please explain the difference between Alt-2 and Alt-3?  **Proposal 1.1-6B)**  We agree with Samsung that the essential thing for the UE to know is whether DBTW is disabled or not after reading MIB since it affects the Type0-PDCCH monitoring effort for the UE prior to decoding SIB1.  However, we are still struggling to understand whether or not Alt-1, 2, and 3 in Proposal 3D is equivalent to the implicit approach in Proposal 6D or to the explicit approach.  Let's say Alt-1/2/3 are equivalent to the explicit approach, then the following wording change would be needed:   * + Alt 2: explicit indicated in MIB     - [Note: explicit indication means that a specific value/state of one or more parameters ~~value~~ is dedicated to exclusively indicate to the UE whether or not DBTW is in use]   Alternatively, let's say Alt-1/2/3 are equivalent to the implicit approach, then we really don't understand the Note. Additionally the following changes would be needed:   * + Alt 1: implicitly indicated     - ~~UE assumes DBTW is used prior to deriving implicit indication.~~     - [Note: implicit indication means that UE may be able to determine that gNB is not using DBTW from detected SSBs and/or the values of set of configured parameters where each individual parameter value in the set can be used for a purpose other than indicating whether or not DBTW is used. The use of this knowledge may not necessarily change UE behavior]     - FFS details of implicit indication in MIB ~~and/or SIB1~~   We are very uncomfortable with this confusing proposal. |
| Apple | **Proposal 1.1-3D) – cleaned up:** Support.**Proposal 1.1-6B) – cleaned up:** Support. |
| LG Electronics | To Samsung, I think the same question can be asked for MIB indication. Do you think gNB can change its mind from DBTW enabling to DBTW disabling, even semi-statically? If this is the case, MIB can be changed. As far as I know, UE implementation according to MIB change is not specified, but typically, it is similar to cell reselection. Going back to sync raster option, if gNB changes its mind, gNB can change center frequency of SSB and UE may perform cell reselection procedure due to RLF. |
| vivo | We are generally fine with the proposal here. However, we agree that number of candidate SSBs is highly related. |
| Nokia | Proposal 1.1-3D): OK with the proposal, we can postpone this after Proposal 1.1-6B is concluded. We are also OK with the Samsung modifications.  Proposal 1.1-6B): Like pointed earlier, it is not clear to us, if the DBTW on/off status is known only after SIB1 (and MIB) reception, why we cannot assume explicit indication in SIB1? One bit in DBTW window length (or lack of the optional discoveryBurstWindowLength IE) could inform the assumption.  Regarding [Samsung2] comment on soft combining the Type0-PDCCH, in my understanding this cannot be assumed as there is no guarantee that the PDCCH content is always the same e.g. PDSCH allocation may change, while the SI message in PDSCH is kept the same.  The only difference would be that UE would be required to monitor more Type0-PDCCH MO locations i.e. MOs corresponding the ‘normal’ and ‘additional’ SSB candidate locations if the SSB index >. Thus, as this should in practice happen only in initial cell selection phase, I don’t see that there is a big difference between SIB1 reception between DBTW on and off.  On the Alt3; in our understanding this would imply having separate/additional SS-raster positions for the cells that apply DBTW. Not sure if this is any more feasible based on the limit on number of SS raster positions agreed in last RAN plenary. |
| DOCOMO | Proposal 1.1-3D) Support  Proposal 1.1-6B) We think it would be good to discuss after fixing #candidate SSB positions. |
| Moderator | Added Proposal 1.1-3E based on discussion.  From the comments, it seems use of Q=64 can be utilized as implicit method to indicate DBTW off by the gNB if the total number of candidate positions for SSB is also equal to 64. I’ve reformulated the Proposal based on this information. Hopefully, this can also address Samsung’s concern.  There seems to be some difference in opinion, in case larger than 64 candidate positions for SSB is supported where use of Q=64 cannot be utilized as implicit method to indicate DBTW off by the gNB, whether we need to support an explicit indication or not.  Nokia comments that the extra monitoring of the Type0-PDCCH occasions only happens for initial access when no other PDCCH occasions are monitored, since DBTW off can be indicated in SIB1 and UE does not need to perform extra monitoring after.  Ericsson comments that there is a difference for the UE know DBTW on or off and UE should know this information prior to SIB1 decoding. |

Additionally, moderator would like to ask companies to provide more information about ‘implicit’ and ‘explicit’ indication of DBTW enable/disable. Huawei and few other companies provided their thoughts on how implicit would function. Moderator would like to also solicit inputs on how ‘explicit’ would function as well.

Moderator tried to put information based on comments and reading of the Tdoc. However, moderator would like to get feedback from companies whether this is the same understanding among companies. Especially for the explicit indication. Moderator was able to not figure out the difference in UE assumption/behavior.

Please provide comments on whether moderator’s description is incorrect or if there are additional aspects that requires consideration. If we determine the difference between two are small, maybe there are ways to close the gap and make further progress. If we determine the difference is large, at least we are able to technically assess the pros and cons of the proposal better.

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| Company | Explanation of Implicit including UE assumption/behavior at following stages  (1) initial cell selection/acquisition prior to MIB decoding)  (2) initial cell selection/acquisition after MIB decoding, and prior to SIB1 decoding  (3) initial cell selection/acquisition after SIB1 decoding  (4) CONNECTED mode  (5) IDLE mode | Explanation of Explicit indication including UE assumption/behavior at following stages  (1) initial cell selection/acquisition prior to MIB decoding)  (2) initial cell selection/acquisition after MIB decoding, and prior to SIB1 decoding  (3) initial cell selection/acquisition after SIB1 decoding  (4) CONNECTED mode  (5) IDLE mode |
| Moderator | **(1)** UE assumes maximum DBTW length and maximum value, detects SSB **#k** (candidate SSB index), and tries to decode PBCH of SSB #k,  **(2)** After MIB decoding UE obtains information, UE obtains SSB index **#i** (= candidate SSB index #k mod ).  Note: #i may or may not equal to #k.  In case gNB is not using DBTW, #i should always equal to #k as and gNB will not send SSB with k > 64.  **(2-A)** if DBTW used at gNB  UE monitors Type0-PDCCH for multiple SSB #k (candidate SSB index) that corresponds to SSB #i  **(2-B)** if DBTW is not used at gNB  UE monitors Type0-PDCCH for SSB #i=#k (candidate SSB index)  **(3)** after SIB1 decoding by monitoring CSS, UE obtains DBTW length, L,  if L <= time length needed to support = 64 number of SSB, UE may assume DBTW is disabled (invalid DBTW configuration).  **(4)** UE determines use of DBTW or not by using same logic as described in **(3)**  **(5)** UE determines use of DBTW or not for the camped cell from SIB 1 decoding of camped cell (anyway needed to obtain paging CSS) by using same logic as described in **(3).** Prior to obtaining DBTW enable/disable information for the to be camped cell, UE assumes maximum DBTW length and maximum value.  Note: paging occasion is determined using “k-th transmitted SSB (38.304 Section 7)” | **(1)** UE assumes maximum DBTW length and maximum value, detects SSB #k (candidate SSB index), and tries to decode PBCH of SSB **#k**, **(Moderator question: it is correct that assumption is the same as implicit case?)**  **(2)** after MIB decoding UE obtains or knowledge DBTW is disabled.  UE obtains SSB index **#i** (= candidate SSB index #k mod ) when DBTW is enabled.  Note: #i may or may not equal to #k.  UE obtains SSB index #i=k when DTW is disabled.  **(2-A)** if DBTW used at gNB  UE monitors Type0-PDCCH for multiple SSB #k (candidate SSB index) that corresponds to SSB #i  **(2-B)** if DBTW is not used at gNB  UE monitors Type0-PDCCH for SSB #i=#k (candidate SSB index)  **(3)** after SIB1 decoding by monitoring CSS, UE obtains DBTW length L (not provided if DBTW is disabled in MIB)  **(4)** UE determine use of DBTW or not by indication in MIB  **(5)** UE determine use of DBTW of not by MIB decoding of camped cell MIB. Note UE is required to also decode SIB1 of camped cell for paging CSS information.  Prior to obtaining DBTW enable/disable information for the to be camped cell, UE assumes maximum DBTW length and maximum value.  Note: paging occasion is determined using “k-th transmitted SSB (38.304 Section 7)”  **(Moderator question: prior to obtaining DBTW enable/disable information, is it correct that UE assumes use of DBTW, which is effectively same as implicit case?)** |
| Moderator additional comments | In (2) moderator assumed that whether UE monitor’s CSS corresponding to SSB #k (candidate SSB index) or all SSB #k corresponding to SSB #i is somewhat UE implementation and not specified in specification.  In the above, moderator assumes that when DBTW is not used by gNB, it will not be possible for UE to detect candidate SSB #k, where k is not equal to SSB index #i, as the |  |
| Samsung | We believe the difference depends on when a UE can determine DBTW is implicitly indicated to be disabled. If the implicit method can let the UE know DBTW on/off is in MIB, then the implicit method and explicit method have no essential difference, from the procedure point of view. | |
| Apple | Our view on the difference between ‘implicit’ and ‘explicit’ approach is on the Type0 CSS monitoring behavior and the associated power consumption at UE side i.e., Step (2-B). As one example assuming the DBTW is NOT enabled by network (Step 2-B),   * Implicit approach: UE does not know whether DBTW is enabled or not and needs to monitor all Type0 CSS associated with candidate SSB index #k mod . * Explicit approach: UE only monitor one Type0 CSS with SSB index #k.   A UE can only monitor one single Type0 CSS with SSB index #k even with ‘implicit’ approach but at the risk of increased initial access latency and worse user experience. In addition, the necessity of signaling Q in MIB is questionable, even for NRU. | |
| LG Electronics | Precisely speaking, we have four options.   * Option 1: Flag bit in MIB to explicitly indicate DBTW enabling or disabling (maybe suitable option if more than 64 SSB candidates are introduced) * Option 2: A codepoint (Q=64) in a field in MIB to explicitly? or implicitly? indicate DBTW enabling or disabling (maybe suitable option if up to 64 SSB candidates are introduced) * Option 3: Sync raster entry * Option 4: Same as NR-U, i.e., UE always assumes DBTW enabled and based on SIB1 information for DBTW length, UE determines DBTW enabled or disabled.   From our point of view, Option 1 to Option 3 don’t have any difference for UE to proceed until SIB1 reading.  In addition, for connected mode UE, we think cell-common or UE-dedicated signaling is additionally needed to inform whether DBTW is enabled or disabled for neighbor cell or Scell. | |
| vivo | Regarding the benefit on Type 0 PDCCH monitoring and power consumption, actually one clarification question from our side: Assuming the DBTW is not enabled, if a UE decode one Type 0 PDCCH in the first position associated with candidate SSB index #k mod , will it continue to monitor next one within the same period? If DBTW is not enabled, network will always send it in the first Type 0 PDCCH position, correct? | |
| ZTE, Sanechips | We share similar understanding with LG about the options. The point is whether UE could know the DBTW on/off before decoding SIB 1, there is no difference between explicit and implicit indication in MIB. | |
| Moderator | From the comments, it seems use of Q=64 can be utilized as implicit method to indicate DBTW off by the gNB if the total number of candidate positions for SSB is also equal to 64.  There seems to be some difference in opinion, in case larger than 64 candidate positions for SSB is supported where use of Q=64 cannot be utilized as implicit method to indicate DBTW off by the gNB, whether we need to support an explicit indication or not.  I’ve provided an summary of discussion so far and moderator has added his observation of the situation so far.  Discussion on indication of DBTW on/off in MIB.   * In case number of candidate SSB positions is 64, Q=64 can be used by gNB to implicitly disable DBTW. In this case, there is no difference for the gNB and UE behavior between whether DBTW is enabled or disabled. * In case number of candidates SSB position is larger than 64,   + Case 1) use of Q=64 by gNB for implicit DBTW disable, may cause UE to perform extra Type0-PDCCH monitoring. The extra Type0-PDCCH monitoring only happens in initial access prior to reading of SIB1 (where DBTW disable can be indicated)     - If number of candidate SSB position is equal or less than 128, the additional Type0-PDCCH monitoring position is 2 more occasions per 20msec period. (since there can only be up to 2 candidate SSB index that results in same SSB index)     - It was commented (by vivo) that in case DBTW is not utilized by gNB, gNB will send SIB1 in the first instance of the Type0-PDCCH monitoring occasion, and so if UE detected Type0-PDCCH (and corresponding PDSCH) in the first monitoring occasion, it is not clear UE needs to be detect Type0-PDCCH (and corresponding PDSCH) in the 2nd monitoring occasion.   + Case 2) Use of a reserved state of Q to indicate DBTW disable, will allow UE to decode Type0-PDCCH monitoring only on monitoring occasions gNB will send Type0-PDCCH   + Between two cases supported UE functionality does not change. The only potential difference is UE may need to monitor more Type0-PDCCH occasions in initial access prior to reading of SIB1. Since no company has proposed maximum candidate number of SSB to be larger than 128, this would be at most 2 more monitoring occasions per 20msec period for initial access prior to SIB1 decoding (when UE does not monitor any other PDCCH search space).   Please provide further comments on whether the above summary is missing something. | |
| Huawei, HiSilicon | 1. **How to implicitly indicate DBTW enable/disable (by comparing in MIB and DBTW length in SIB1)**    * As we discussed in earlier rounds, we think NR-U mechanism to implicitly indicate DBTW enable/disable by comparing the value of in MIB with the value of DBTW length is SIB1 would also perfectly work in 60 GHz. As explained before in the first round, DBTW enabled/disabled is never explicitly indicated to the UE in Rel-16 NR-U. In Rel-16, UE can infer whether DBTW is enabled/disabled only after reading SIB1 by comparing the maximum number of transmitted SSB indexes (acquired from MIB payload) with the DBTW length (*DiscoveryBurst-WindowLength* provided in SIB1). If DBTW length that is configured in SIB1 is such that DBTW can include more than candidate SSB indexes, UE can infer that DBTW is enabled. In turn, if DBTW length that is configured in SIB1 is such that DBTW cannot include more than candidate SSB indexes, UE can infer that DBTW is disabled. 2. **What is UE’s assumption regarding DBTW enable/disable before Reading SIB1?**    * If necessary, similar to NR-U, UE can assume that DBTW is enabled (in NR-U, UE assumes that DBTW length is half-frame, and, hence DBTW is enabled if DBTW length is not provided). 3. **Does UE actually require to make an assumption that DBTW is enabled prior to reading SIB1 in licensed operation? Why?**    * The answer is “No”.    * **When it comes to licensed vs. unlicensed spectrum, the only difference between 60 GHz and Rel-16 NR-U is that in 60 GHz UE does not know if it operates in licensed or unlicensed band at least prior to reading SIB1.** However, note that UE simply does not need to know if it operates in licensed or unlicensed spectrum prior to reading SIB1 (assuming the ambiguity of size of DCI 1\_0 with CRC scrambled by SI-RNTI is resolved somehow by, eg, unifying the size or by doing two blind decoding). In licensed operation, if candidate SSB index “a” (which is also the SSB index “a”) of a PCell is transmitted, the Type0-PDCCH corresponding to candidate SSB index “a” is also supposed to be transmitted. If initial access UE detects candidate SSB index “a” in its 20 ms buffer, it goes on to receive Type0-PDCCH corresponding to the same candidate SSB index “a”, then reads SIB1 and moves on to the subsequent steps of cell connection establishment. **Therefore, whether or not UE assumes DBTW is used or not used has no impact on UE behavior in licensed operation.** 4. **Does UE actually require to make an assumption that DBTW is enabled prior to reading SIB1 in unlicensed operation? Why?**  * It can help. * In unlicensed operation, if candidate SSB index “a” of a PCell is transmitted, UE still detects it in its 20 ms default buffer that UE uses regardless of licensed or unlicensed operation. It may happen that the Type0-PDCCH corresponding to candidate SSB index “a” is not transmitted due to LBT failure. In such a case, obviously, UE cannot find the Type0-PDCCH corresponding to candidate SSB index “a”, but, since it knows from the MIB of candidate SSB index “a”, it would know the location of the CORESET#0 corresponding to the candidate SSB index “a+”. So, UE can go and find the Type0-PDCCH from the CORESET#0 corresponding to the candidate SSB index “a+**”. So, all in all, before reading SIB1, UE would use the assumption that DBTW is enabled only when it detects a candidate SSB “a” of a PCell but cannot find the Type0-PDCCH corresponding to the detected candidate SSB “a” which typically happens in unlicensed operation due to LBT failure.**  1. **To more clearly answer our Feature lead questions:**     * **initial cell selection/acquisition prior to MIB decoding:**    * As explained above, UE does not need to know whether DBTW is enabled or disabled. UE searches for SSB in its 20 ms buffer anyway. This buffer has nothing to do with whether or not DBTW is actually enabled or disabled and is always used during initial access. Remember that UE does not have any timing reference at this stage anyway. However, if companies are uncomfortable with the idea of UE not knowning DBTW enable/disable prior to MIB decoding, we can agree that UE assumes DBTW is enabled although such an assumption has no impact on UE behavior    * **initial cell selection/acquisition after MIB decoding, and prior to SIB1 decoding:**    * UE can assume that DBTW is enabled. However, this assumption would help UE only when UE has detected a SSB but cannot find corresponding Type0-PDCCH. This mainly happens in unlicensed spectrum due to LBT failure. Please see our answer in 3 and 4.    * **initial cell selection/acquisition after SIB1 decoding**    * UE would know if BTW is enabled or disabled by comparing the value of in MIB with the value of DBTW length is SIB1. Similar to Rel-16 NRU.    * **CONNECTED mode**    * As discussed above, UE would know whether DBTW is enabled or disabled after reading SIB1. Dedicated RRC messaging may also be used in RRC CONNECTED STATE.    * **IDLE mode**    * This case is already covered above. An Idle UE at any stage before reading SIB1 can assume that DBTW is enabled. However, if, unbeknown to UE, UE operates in licensed spectrum, this assumption does not change its behavior. If, unbeknown to UE, UE operates in licensed spectrum, this assumption may help it to find other Type0-PDCCHs that are QCL-D with its detected SSB. An Idle UE after reading SIB1 and before RRConnection would know if DBTW enabled/disabled. | |

#### **5th Round Discussion Summary:**

**Part 1 discussion)**

Proposal 1.1-4B and Proposal 1.1-2E from Part 1 discussion are suggested to be approved over email.

**Part 2 discussion)**

Moderator suggests resolving the following issue over GTW (if possible)

**Proposal 1.1-5B)**

* For 120kHz SSB, the number of candidates SSBs in a half frame for DBTW is 64
* Support: Ericsson, LGE, Futurwei, Qualcomm, ZTE/Sanechips, Interdigital, Docomo, Huawei/HiSilicon
* Not ok: Samsung, NEC, Nokia, Intel
  + Reasons for concern:
    - Number of candidates are too restrictive

**Proposal 1.1-5C)**

* For 120kHz SSB, the number of candidates SSBs in a half frame for DBTW is 80
* Support: Nokia, ZTE/Sanechips, Intel, Samsung, NEC
* Not ok: Ericsson, LGE, Qualcomm, NTT DOCOMO
  + Reasons for concern:
    - Number of bits available in PBCH unclear
    - Gap between set of SSBs transmission is needed for uplink transmissions

**Part 3 discussion)**

The updated formulation from 1.1-3E seems to be able to cover the proposal 1.1-6B. Therefore, moderator suggests focusing on Proposal 1.1-3E.

##### **Proposal 1.1-3E)**

* For supported SCS cases of DBTW, support configuration of in MIB, down-select among the following alternatives (after number of candidate SSB positions have been determined).
  + Alt 1: total of 2 states of values are supported
    - FFS the exact values e.g. {16,64} or {32,64}
    - Note: value of 64 (if supported) may be used as implicit determination by the UE that DBTW is not enabled by gNB if maximum number of candidate SSB is 64
  + Alt 2: total of 4 states (including any potential reserved state) of values are supported
    - FFS on the values, e.g. {8,16,32,64}
    - FFS whether or not a single state will be reserved to explicitly indicate that DBTW is disabled e.g. (e.g. {16, 32, 64, reserved/DBTW disabled})
      * Note: value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB if maximum number of candidate SSB is 64; or single state may be reserved e.g. (e.g. {16, 32, 64, DBTW disabled}) to explicitly indicate that DBTW is disabled

The following is a summary of comparison of implicit versus explicit DBTW enable/disable indication in MIB.

* In case number of candidate SSB positions is 64, Q=64 can be used by gNB to implicitly disable DBTW. In this case, there is no difference for the gNB and UE behavior between whether DBTW is enabled or disabled.
* In case number of candidates SSB position is larger than 64,
  + Case 1) use of Q=64 by gNB for implicit DBTW disable, may cause UE to perform extra Type0-PDCCH monitoring. The extra Type0-PDCCH monitoring only happens in initial access prior to reading of SIB1 (where DBTW disable can be indicated)
    - If number of candidate SSB position is equal or less than 128, the additional Type0-PDCCH monitoring position is 2 more occasions per 20msec period. (since there can only be up to 2 candidate SSB index that results in same SSB index)
    - It was commented (by vivo) that in case DBTW is not utilized by gNB, gNB will send SIB1 in the first instance of the Type0-PDCCH monitoring occasion, and so if UE detected Type0-PDCCH (and corresponding PDSCH) in the first monitoring occasion, it is not clear UE needs to be detect Type0-PDCCH (and corresponding PDSCH) in the 2nd monitoring occasion.
  + Case 2) Use of a reserved state of Q to indicate DBTW disable, will allow UE to decode Type0-PDCCH monitoring only on monitoring occasions gNB will send Type0-PDCCH
  + Between two cases supported UE functionality does not change. The only potential difference is UE may need to monitor more Type0-PDCCH occasions in initial access prior to reading of SIB1. Since no company has proposed maximum candidate number of SSB to be larger than 128, this would be at most 2 more monitoring occasions per 20msec period for initial access prior to SIB1 decoding (when UE does not monitor any other PDCCH search space).

Based on summary of observations on DBTW enable/disable discussions, moderator suggest discussing on Proposal 1.1-7. While moderator realizes there could be concerns of the proposal 1.1-7, given the discussion so far that MIB indication is precious and the difference in being able to indicate in MIB seems to be subjectively minor (2 additional PDCCH monitoring per 20msec only when initial access prior to SIB1 decoding)

##### **Proposal 1.1-7)**

* Conclude that DBTW enable/disable is not explicitly indicated in MIB.
* DBTW enable/disable is indicated in SIB1.

#### **6th Round Discussion – Part 1:**

Proposal 1.1-4B and Proposal 1.1-2E from Part 1 discussion are suggested to be approved over email. Please comment if you have any concerns.

##### **Proposal 1.1-4B) – suggest for email approval**

* For DBTW with 120kHz SCS (if supported), support DBTW lengths {0.5, 1, 2, 3, 4, 5} msec
  + Note: this should be the same as Rel-16 NR-U DBTW lengths.

##### **Proposal 1.1-2E) – suggest for email approval**

* No indication for licensed and unlicensed operation in MIB
  + Whether and/or how LBT/No-LBT is indicated is separately discussed
* Use of LBT is not indicated in MIB.
  + FFS where and how this is indicated, e.g. SIB1
* For both licensed or unlicensed operation and with or without LBT, support the same DCI size for:
  + DCI format 1\_0 ~~scrambled with SI-RNTI~~ monitored in a common search space
    - Note: existing bit padding/truncation rules are assumed to applied for DCI format 0\_0 monitored in common search space.
  + FFS for other cases

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| Company | Comments |
| Samsung | We are ok with both of the proposals. |
| Qualcomm | We are ok with both of the proposals. |
| Huawei, HiSilicon | **Proposal 1.1-4B)** We support it  **Proposal 1.1-2E)** We can accept it if it has the majority support. Our first preference would be the original Proposal 1.1-2D though. |

#### **6th Round Discussion – Part 2:**

Let’s continue discussion on Proposals 1.1-5B and 1.1-5C.

##### **Proposal 1.1-5B)**

* For 120kHz SSB, the number of candidates SSBs in a half frame for DBTW is 64
* Support: Ericsson, LGE, Futurwei, Qualcomm, ZTE/Sanechips, Interdigital, Docomo, Huawei/HiSilicon
* Not ok: Samsung, NEC, Nokia, Intel
  + Reasons for concern:
    - Number of candidates are too restrictive

##### **Proposal 1.1-5C)**

* For 120kHz SSB, the number of candidates SSBs in a half frame for DBTW is 80
* Support: Nokia, ZTE/Sanechips, Intel, Samsung, NEC
* Not ok: Ericsson, LGE, Qualcomm, NTT DOCOMO
  + Reasons for concern:
    - Number of bits available in PBCH unclear
    - Gap between set of SSBs transmission is needed for uplink transmissions

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| Company | Comments |
| Samsung | We want to respond to the comment on the gap between set of SSB transmissions for uplink. Supporting 80 candidate location didn’t preclude such implementation, but provide more flexibility on choosing which candidate SSB locations not used and for uplink transmission. In this sense, we don’t think that’s a valid concern. |
| Huawei, HiSilicon | We support **Proposal 1.1-5B).**  **To Samsung:**  We don’t think Supporting 80 candidate locations would provide flexibility for UL transmission. Using 80 candidate locations means that, depending on LBT result, any slot within the 5 ms DBTW may be used for SSB. Then, how network could configure any UL slot/symbol for the UE during this interval? |

#### **6th Round Discussion – Part 3:**

Continue discussion on proposal 1.1-3E. If the proposal is stable, moderator would like to also suggest this proposal for email approval.

##### **Proposal 1.1-3E) – potentially for email approval**

* For supported SCS cases of DBTW, support configuration of in MIB, down-select among the following alternatives (after number of candidate SSB positions have been determined).
  + Alt 1: total of 2 states of values are supported
    - FFS the exact values e.g. {16,64} or {32,64}
    - Note: value of 64 (if supported) may be used as implicit determination by the UE that DBTW is not enabled by gNB if maximum number of candidate SSB is 64
  + Alt 2: total of 4 states (including any potential reserved state) of values are supported
    - FFS on the values, e.g. {8,16,32,64}
    - FFS whether or not a single state will be reserved to explicitly indicate that DBTW is disabled e.g. (e.g. {16, 32, 64, reserved/DBTW disabled})
      * Note: value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB if maximum number of candidate SSB is 64; or single state may be reserved e.g. (e.g. {16, 32, 64, DBTW disabled}) to explicitly indicate that DBTW is disabled

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| Company | Comments |
| Samsung | As indicated in the previous comments, we are not ready to go with this detailed proposal until the number of candidate SSB and DBTW on/off are resolved. The feasibility of some of the proposals highly depend on the outcome from these two discussion, and we can keep this proposal in notes and further discuss after the other two issues are resolved. |
| Qualcomm | We are generally ok, but also prefer to defer any agreements until the number of candidate SSBs is agreed |
| Huawei, Hisilicon | We support the earlier version **Proposal 1.1-3D)** If Proposal 1.1-3D) is not agreeable, we can accept **Proposal 1.1-3E** by changing the following “Notes” to FFS: **Proposal 1.1-3E)** (modified)  * For supported SCS cases of DBTW, support configuration of in MIB, down-select among the following alternatives (after number of candidate SSB positions have been determined).   + Alt 1: total of 2 states of values are supported     - FFS the exact values e.g. {16,64} or {32,64}     - ~~Note:~~ FFS: value of 64 (if supported) may be used as implicit determination by the UE that DBTW is not enabled by gNB if maximum number of candidate SSB is 64   + Alt 2: total of 4 states (including any potential reserved state) of values are supported     - FFS on the values, e.g. {8,16,32,64}     - FFS whether or not a single state will be reserved to explicitly indicate that DBTW is disabled e.g. (e.g. {16, 32, 64, reserved/DBTW disabled})       * ~~Note:~~ FFS: value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB if maximum number of candidate SSB is 64; or single state may be reserved e.g. (e.g. {16, 32, 64, DBTW disabled}) to explicitly indicate that DBTW is disabled |

#### **6th Round Discussion – Part 4:**

Also please comment further on the discussion on implicit versus explicit indication for DBTW in MIB. The following is summary of observations from round 5 discussions. Please comment on the observations if there is anything missing or incorrect.

* In case number of candidate SSB positions is 64, Q=64 can be used by gNB to implicitly disable DBTW. In this case, there is no difference for the gNB and UE behavior between whether DBTW is enabled or disabled.
* In case number of candidates SSB position is larger than 64,
  + Case 1) use of Q=64 by gNB for implicit DBTW disable, may cause UE to perform extra Type0-PDCCH monitoring. The extra Type0-PDCCH monitoring only happens in initial access prior to reading of SIB1 (where DBTW disable can be indicated)
    - If number of candidate SSB position is equal or less than 128, the additional Type0-PDCCH monitoring position is 2 more occasions per 20msec period. (since there can only be up to 2 candidate SSB index that results in same SSB index)
    - It was commented (by vivo) that in case DBTW is not utilized by gNB, gNB will send SIB1 in the first instance of the Type0-PDCCH monitoring occasion, and so if UE detected Type0-PDCCH (and corresponding PDSCH) in the first monitoring occasion, it is not clear UE needs to be detect Type0-PDCCH (and corresponding PDSCH) in the 2nd monitoring occasion.
  + Case 2) Use of a reserved state of Q to indicate DBTW disable, will allow UE to decode Type0-PDCCH monitoring only on monitoring occasions gNB will send Type0-PDCCH
  + Between two cases supported UE functionality does not change. The only potential difference is UE may need to monitor more Type0-PDCCH occasions in initial access prior to reading of SIB1. Since no company has proposed maximum candidate number of SSB to be larger than 128, this would be at most 2 more monitoring occasions per 20msec period for initial access prior to SIB1 decoding (when UE does not monitor any other PDCCH search space).

Based on summary of observations on DBTW enable/disable discussions, moderator suggest discussing on Proposal 1.1-7. While moderator realizes there could be concerns of the proposal 1.1-7, given the discussion so far that MIB indication is precious and the difference in being able to indicate in MIB seems to be subjectively minor (2 additional PDCCH monitoring per 20msec only when initial access prior to SIB1 decoding). Discuss further on the Proposal 1.1-7

##### **Proposal 1.1-7)**

* Conclude that DBTW enable/disable is not explicitly indicated in MIB.
* DBTW enable/disable is indicated in SIB1.

Moderator has added Proposal 1.17A based on Samsung’s comments. Please provide comments on Proposal 1.1-7 and 1.1-7A.

##### **Proposal 1.1-7A)**

* Conclude that DBTW enable/disable is not explicitly indicated in MIB.
* DBTW enable/disable is indicated in SIB1.
* Conclude that is not indicated in MIB.
* is indicated in SIB1.

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| Company | Comments |
| Samsung | We have a question: if the UE cannot know DBTW disable/enable in MIB, what’s the point to indicate the UE with the value of Q in MIB? As moderator commented bits in MIB is precious, then why 1 or 2 bits are used for indicating a value of Q without even knowing the DBTW is on? We didn’t any difference in UE behavior without knowing Q after reading MIB.  If this is the direction to discuss, we would like to add bullets on the indication of Q, and UE’s behavior on decoding Type0-PDCCH is totally up to implementation.   * Conclude that DBTW enable/disable is not explicitly indicated in MIB. * DBTW enable/disable is indicated in SIB1. * Conclude that is not indicated in MIB. * is indicated in SIB1. |
| Moderator | I wanted to provide my understanding, as the proposal for 1.1-7 just came from me (after reviewing the discussion so far).  I assumed the purpose of the Q in MIB was for measurement purposes, so that UE can make appropriate measurement accumulation/filtering for neighbor cells (i.e. L3 filter measurements that belong to the same beam).  UE typically does not read neighbor cell SIB1 as part of the RRM process to find out the whether specific SSBs are in fact for the same beam or not.  For FR1 and FR2-1, decoding of neighbor cell MIB/SIB1 was not completely necessary (with the possible exception of FR1 NR-U). This is due the fact that in FR1, SSB index is obtained from DMRS of PBCH and no information is needed from PBCH and in FR2, because it is a TDD network only deployments, cell are synchronized and the SSB index can be implicitly derived from serving cell transmission timing without needing to obtain full SSB index (3 bits in DMRS and 3 bits in MIB).  I assumed this (decoding of PBCH) might not be completely avoidable for FR2-2 since TDD cell phase synchronization requirement would only apply to gNBs from the same operator, and there is no guarantee gNBs from other operator would be time synchronized and without cell phase synchronization, the 3 MSB bits of SSB index would need to be directly read from PBCH.  So for unlicensed operation in FR2-2, I assumed UE would need to decode neighbor cell PBCH at least once to learn the timing and Q value, so that proper RRM measurements can take place.  With that said, I would like to hear comments from companies as well. |
| Samsung | Response to moderator:  According to Rel-16 NR-U, for RRM measurement purpose, there will be separate Q values configured (e.g. in OSI and MeasureObject), and we guess the same feature will be carried over for 60 GHz when DBTW is on. In this sense, a UE doesn’t have to read MIB of neighboring when performing measurement, which is even better for saving the UE’s complexity in RRM measurement. |
| Moderator | Yes. I have the same understanding that Q values will be provided by the serving cell for measurements. However, I assumed this would be only valid for cells from the same operator.  As I have mentioned, I’ve assumed for inter-operator measurements, cell phase synchronization might not be mandated. Therefore, UE will be required to decode MIB (even if Q is not indicated in MIB) for the 3 MSB bits of SSB index (at for FR2-2). So I assumed there is still value of indicating Q in MIB, and this was my understanding why NR-U had indicated Q in MIB and in measurement purposes as well.  With that said, if the companies are ok to move Q out from the MIB, I (moderator) will not be the one that will object to the proposal. Actually, not having Q indicated in MIB would solve lot of issues that are pending in RAN1.So I’ve listed Samsung’s suggestion as Proposal 1.1-7A.  Let’s see what other companies have to say. |
| Qualcomm | Since this is dependent on the number of candidate SSBs, may be it makes sense to defer the discussion on this on until the number of candidate SSBs is agreed. |
| Huawei, HiSilicon | We can agree with only the first bullet of Proposal 1.1-7). We can also agree with the second bullet with the following change: **Proposal 1.1-7)**  * Conclude that DBTW enable/disable is not explicitly indicated in MIB. * DBTW enable/disable is indicated in SIB1.   + Note: this does not preclude UE’s inference on DBTW enable/disable from SIB1 and earlier stages of initial access.   Please note that we again explained the detailed procedure of implicit indication in SIB1 and MIB (NR-U behavior) in great details in our input to Table in “Explanation of Implicit including UE assumption/behavior at following stages” provided in “5th Round Discussion – Part 3” We don’t agree with **Proposal 1.1-7A)** |

#### **6th Round Discussion Summary:**

To be filled.

### 2.1.2 SSB Resource Pattern

* From [1] Huawei/HiSilicon:
  + Support following patterns for SSB with 480 kHz and 960 kHz SCS:
    - For operations without shared spectrum:
      * {2,9}+14n, (n=0,1,2,…,31) for both 480 kHz and 960 kHz SCS.
    - For operations with shared spectrum:
      * {2,9}+14n, (n=0,1,2,…,31,40,…,71) for 480 kHz SCS;
      * {2,9}+14n, (n=0,1,2,…,63) for 960 kHz SCS.
* From [2] vivo:
  + For initial cell search in 52.6-71GHz, a UE may assume that half frames with SSB occur with smaller period than FR2 (e.g. 5ms), or lower RAN4 requirement for the cell search time.
  + If CP length of at least one SCS (e.g. 960K) can’t afford beam switching time that is finally determined in RAN4, the following way could be considered for ALT1 and ALT2 respectively:
    - For ALT1, leave enough time gap between any consecutive candidate SSBs by specifying proper value of X and Y;
    - For ALT2, the same QCL (i.e. the same beam) for contiguous candidate SSBs is assumed to achieve time gap for any consecutive candidate SSBs with different QCL assumption.
  + The exact value of ‘n’ should be determined after RAN4 concludes the exact DL-UL switching time for NR operation in FR2-2.
* From [3] Spreadtrum:
  + The SSB pattern for SSB with 480/960kHz SCS can reuse Case A/C in the current spec, i.e. ALT 1) with X=2 and Y=8.
* From [4] Interdigital:
  + Support Alt 1 for the SSB resource patterns for 480/960kHz SCS SSB blocks.
    - First symbols of the candidate SSB have index {X, Y} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame. value of X and Y are identical for 480kHz and 960kHz
* From [5] Sony:
  + Candidate SSB positions should be extended when DBTW is enabled.
    - For 120 kHz SCS,
      * The number of candidate SSB positions should be 80
      * additional n values (4, 9, 14, 19) should be supported when DBTW is enabled
    - For 480/960 kHz SCS,
      * The number of candidate SSB positions should be 128
      * First symbols of the candidate SSB have index {4, 8, 16,20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
      * n = {0, 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 15, 16, 17, 18} when DBTW is disabled.
      * n = 0 - 31 when DBTW is enabled
* From [6] Lenovo/Motorola Mobility
  + For supporting NR from 52.6 GHz to 71 GHz in Rel. 17, for higher subcarrier spacings (numerologies) such as 960kHz for SSB, to allow the beam switching between contiguous SSBs, a gap (for example a symbol gap or post-fix) should be supported before beam switching at least for 960kHz
* From [7] Samsung:
  + For 480 kHz and 960 kHz,
    - Support the same SS/PBCH block pattern in a slot, and the same pattern is given by Case A/C (i.e., Alt 1 with X=2 and Y=8).
    - Support larger number of slots including candidate SS/PBCH block, when DBTW is enabled.
* From [8] CATT:
  + For SSB pattern, considering SCS= 960KHz SSB is not supported for initial access，ALT-2 is preferred.
    - ALT 2) First symbols of the candidate SSB have index {4, 8, 16,20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
  + More than 64 SSB transmission opportunities shall be defined within a 5ms SSB burst set to support up to 64 beams for SSB beam sweeping in case of LBT failure. The issue of supporting additional bit(s) for the indicating SSB candidate index needs further study.
  + For no-LBT operation or licensed spectrum operation, value “n” can keep the same value as for the 120KHz SCS case.
  + Additional n value such as #4, #9, #14, and #19 can be used for new SSB candidates if LBT/DBTW is needed for SSB transmission.
  + For up to 71GHz operation and at least for NO-LBT operation, some values of ‘n’ can be reserved for uplink grant scheduling.
* From [9] ZTE/Sanechips:
  + For SSB with 120kHz SCS for NR 52.6 GHz to 71 GHz: the first symbols of the candidate SS/PBCH blocks have indexes {4, 8,16, 20} + 28×n, where index 0 corresponds to the first symbol of the first slot in a half-frame. For carrier frequencies within 52.6 GHz to 71GHz,
    - if DBTW is not supported or disabled, 𝑛 = 0, 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 15, 16, 17, 18
    - if DBTW is enabled, the additional n values can be equal to 4, 9, 14, 19 to define 16 additional candidate SSB positions
  + For 480kHz/960kHz SSB, the following alternatives can be considered:
    - Alt 1: First symbols of the candidate SSB have index {X, Y} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
      * value of X and Y are identical for 480kHz and 960kHz
        + X=2, Y=8
      * if DBTW is not supported or DBTW is disabled
        + For 480kHz SCS, the 64 candidate SSBs are located in 32 slots, with 2 slots spacing between every 8 consecutive slots to avoid prolonged occupation, i.e. n=0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 20, 21, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 34, 35, 36, 37
        + For 960kHz SCS, the 64 candidate SSBs are located in 32 slots, with 4 slots spacing between every 16 consecutive slots to avoid prolonged occupation, i.e. n=0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35
      * if DBTW is supported and it is enabled
        + Additional 64 candidate SSB can be defined after the above original 64 candidate SSB in the half frame
    - Alt 2: First symbols of the candidate SSB have index {4, 8, 16, 20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
      * if DBTW is not supported or DBTW is disabled
        + For 480kHz SCS, the 64 candidate SSBs are located in 32 slots (i.e. 16 slot pairs, where 1 slot pair = 2 slots), with 2 slots spacing between every 4 consecutive slot pairs to avoid prolonged occupation, i.e n=0, 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 15, 16, 17, 18
        + For 960kHz SCS, the 64 candidate SSBs are located in 32 slots (i.e. 16 slot pairs, where 1 slot pair = 2 slots), with 4 slots spacing between every 8 consecutive slot pairs to avoid prolonged occupation, i.e n=0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 16, 17
      * if DBTW is supported and it is enabled
        + Additional 64 candidate SSB can be defined after the above original 64 candidate SSB in the half frame
  + The following options can be considered for supporting beam switching for SSB with SCS 480 kHz and 960 kHz if the CP cannot cover beam switching and other functions simultaneously.
    - Option 1: In a half-frame, any two candidate SSBs are discontinuous in the time domain
    - Option 1-1: SSB pattern with SCS 480/960 kHz can adopt the existing pattern of Case A and Case C in one or two slots defined in Rel-15 NR
    - Option 1-2: SSB pattern with SCS 480/960 kHz should be re-designed to reserve at least one symbol between any two candidate SSBs, e.g. only defining one candidate SSB per slot, or shift the existing SSB by one or more symbols
    - Option 2: Multiple adjacent candidate SSBs are defined to have a same SSB index or QCL assumption
  + In order to reduce the impact of standardization caused by indicating candidate SSB indices, the maximum number of candidate SSB defined in the half-frame can be kept unchanged (maintain 64) or limited to 128 for 480/960 kHz SSB SCS.
* From [11] Ericsson:
  + For SS/PBCH block with 120 kHz SCS, support Case D pattern as defined in Rel-15. No new values of n are supported.
  + Pending confirmation from RAN4 on 59 ns beam switching times, support the FR2 Case D pattern (ALT 2) for time domain pattern for SSB transmissions with 480 kHz and 960 kHz SCS.
  + Conclude that no additional (compared to the already supported 64) candidate SS/PBCH block positions are introduced.
* From [13] Nokia/NSB:
  + Make a working assumption that no beam switching gap need to be assumed between consecutive SSBs at 480kHz and 960kHz sub-carrier spacing.
  + Support in for 480kHz and 960kHz SSB pattern design empty slots without SSB candidate locations at 0.25ms.
  + Define SSB slot patter for 480kHz and 960kHz sub-carrier spacing so that 8 consecutive slots are contain SSB candidate locations, followed by 4 slots are left unoccupied (by SSBs), until all SSBs locations are accounted
    - The slot indexes n={0,1,2,3,4,5,6,7,
      * 12,13,14,15,16,17,18,19,
      * 24,25,26,27,28,29,30,31,
      * 36,37,38,39,40,41,42,43}
    - Note: The additional candidate locations for DBTW are not accounted above.
  + Define SSB symbol level pattern for 480kHz and 960kHz so that first symbols of the candidate SSB locations are {2,8}+14\*n
    - where index 0 corresponds to the first symbol of the first slot in a half-frame, and n is the corresponding SSB slot index
  + For 120kHz SSB pattern, introduce additional candidate locations for SSB transmission support for 𝑛 = 4, 9, 14, 19, where n is the slot index in half-frame.
    - The first symbols of the additional candidate SS/PBCH blocks have indexes {4, 8,16, 20} + 28×n.
  + For 480kHz and 960kHz SSB pattern, introduce additional candidate locations for SSB transmission support for 𝑛 = [{8, 9, 10, 11} ,{32,33,34,35}], where n is the slot index in half-frame.
* From [14] Charter:
  + Support Alt-1 for 480/960 kHz SSB with first symbols of the candidate SSB have index {X, Y} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame. The value of n is the same for LBT and no-LBT operation.
* From [16] Panasonic:
  + For SSB symbol position, Case D SSB pattern is reused (i.e., Alt 2).
  + For SSB slot position, Case D SSB patten is reused (i.e., n = 0, 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 15, 16, 17, 18).
* From [17] OPPO:
  + for SSB pattern design, support Alt-1 {X,Y}+14\*n, with X=1, Y=8.
  + for SSB candidate number within half frame, support the followings
    - For 480kHz, SSB candidate index {1,8}+14\*n, with n=0~63
    - For 120kHz, SSB candidate index {4, 8,16, 20} + 28\*n, with n=0~19
* From [18] Qualcomm:
  + for 480kHz/960kHz SSB, select the following alternative:
    - ALT 1) First symbols of the candidate SSB have index {X, Y} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
      * value of X and Y are identical for 480kHz and 960kHz
      * X = 2 and Y = 9
      * Values of ‘n’ shall not be all consecutive integer values (i.e. non-candidate SSB slots are positioned every few candidate SSB slots)
* From [19] LG Electronics:
  + Support of additional n values for the time domain pattern of SS/PBCH block with 120 kHz SCS can be considered to increase SS/PBCH block’s transmission opportunities, only if PBCH payload is sufficient to indicate the increased number of candidate SS/PBCH block indexes.
  + For 480/960 kHz SSB, first symbols of the candidate SSB have index are {4, 8, 16, 20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame (i.e., Alt 2 in previous agreement), and values of ‘n’ are consecutive integers (i.e., n = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15).
* From [20] ETRI:
  + Prefer to keep the current 64 SSB candidate positions for 120kHz.
  + Propose to support ALT 1 as SSB patterns for 480kHz and 960kHz SSB.
    - Details on values for X, Y, and n should be further studied.
* From [21] Mediatek:
  + For SSB SCS=120 kHz, additional SSB candidate positions is not needed.
  + For SSB SCS=480/960 kHz, Alt 2 should be supported as the baseline scheme.
* From [22] Intel:
  + Consider at least 1 symbol gap between consecutive SSBs within a slot.
  + Consider at least 1 symbol gap between SSB and the start of the next slot, where PDCCH could be transmitted.
  + Consider SSB pattern in a slot with 3 SSB containing slots, each slot with 2 SSB position, followed by 1 non-SSB carrying slot for 480 kHz and 6 SSB carrying slots followed by 2 non-SSB carrying slots for 960kHz, to accommodate Rx-Tx switching gap.
    - For 480kHz and 960kHz SCS based SSB, first symbols of the candidate SSB have indexes {2,9} + 14×n, where index 0 corresponds to the first symbol of the first slot in a half-frame.
    - For 480kHz, n = {0,1,2, 4,5,6, 8,9,10, 12,13,14, 16,17,18, 20,21,22, 24,25,26, 28,29,30, 32,33,34, 36,37,38, 40,41}, {42, 44,45,46, 48,49,50, 52,53,54, 56,57,58, 60,61,62, 64,65,66, 68,69,70, 72,73,74, 76,77,78, 80}.
      * The second set of n values could be used to enable larger number of candidate SSBs, i.e.,
    - For 960kHz, n = {0,1,2,3,4,5, 8,9,10,11,12,13, 16,17,18,19,20,21, 24,25,26,27,28,29, 32,33,34,35,36,37, 40,41}, {42,43,44,45, 48,49,50,51,52,53, 56,57,58,59,60,61, 64,65,66,67,68,69, 72,73,74,75,76,77, 80,81,82,83}.
      * The second set of n values could be used to enable larger number of candidate SSBs, i.e.,
* From [23] Apple:
  + Support to introduce a unified SSB Pattern for 480kHz SCS and 960kHz SCS (if supported):
    - The first symbol of candidate SSB have indexes {2,9,16,23} within each SSB burst.
    - Reserve 2 slots for DL/UL and UL/DL switching to allow for fast UL transmission between two SSB bursts.
* From [24] Sharp:
  + Based on SSB resource pattern Case D of FR2, other values of n (e.g., 4, 9, 14, 19) should be added for the SSB with 120kHz SCS in above 52.6GHz.
* From [25] NTT Docomo:
  + On down-selection regarding SSB symbol definition, whether to reuse Case D should be discussed considering whether to practically support SSB-CORESET#0 multiplexing within the same slot
  + With 120 kHz SCS, ‘n’ value(s) which can be added on top of the ones agreed already are limited, i.e., ‘n’ = {4, 9, 14, 19} only
  + With 120 kHz SCS, no significant need to support additional ‘n’ values on top of the ones agreed already
  + With 480/960 kHz SCS, non-consecutive SSB slots should be defined to e.g., make UL transmissions possible in the middle of SSB burst.
    - Larger number of consecutive non-SSB slots can be defined during SSB burst can be defined to obtain scheduling flexibility of a DCI (e.g., with repetition and/or multi-PDSCH/PUSCH scheduling)
  + With 480/960 kHz SCS, not support more than 64 candidate SSB positions
* From [26] Xiaomi:
  + For 480 kHz SSB design, we support the option 1 and the n should be no difference for LBT/no LBT operation.
    - [Moderator Note: This might be Alt 1, instead of option 1]
* From [28] WILUS:
  + At least one symbol gap in time domain between SS/PBCH blocks with different SSB indices should be considered for higher subcarrier spacing by taking a beam switching gap into account due to a RF interruption time of Tx/Rx beams and/or LBT gap in unlicensed spectrum.
  + We prefer to have Alt-1 of two alternatives for SS/PBCH block pattern in time domain
    - ALT 1) First symbols of the candidate SSB have index {X, Y} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
    - value of X and Y are identical for 480kHz and 960kHz
      * FFS: exact value of X and Y

#### Summary of Contribution Discussions

In RAN1 #105e the following agreement was made.

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| **Agreement:**  For 480kHz/960kHz SSB, select one of the following alternatives:   * ALT 1) First symbols of the candidate SSB have index {X, Y} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame   + value of X and Y are identical for 480kHz and 960kHz     - FFS: exact value of X and Y * ALT 2) First symbols of the candidate SSB have index {4, 8, 16,20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame * Values of n for 480kHz and 960kHz for ALT 1 and 2   + FFS: whether number of values for ‘n’ depend on LBT operation (i.e. LBT vs no-LBT)   + FFS: exact values of ‘n’ for each SCS   + Values of ‘n’ for one mode of operation shall be strictly a subset of values for another mode of operation, if two mode of operation exist for number of candidate SSBs   + FFS: whether values of ‘n’ shall not be all consecutive integer values (i.e. non-candidate SSB slots are positioned every few candidate SSB slots) |

* SSB pattern for 480/960kHz
  + ALT 1)
    - {X, Y} + 14\*n
      * Interdigital, [Lenovo/Motorola Mobility], Charter, ETRI, [Xiaomi], WILUS, Futurewei
    - (Alt 1-A) {2, 9} + 14\*n



* + - * Huawei/HiSilicon, Qualcomm, Intel, [Apple], Samsung, ZTE/Sanechips
    - (Alt 1-B) {1,8} + 14\*n, Futurewei



* + - * OPPO, Samsung, Futurewei
    - (Alt 1-C) {2, 8} + 14\*n



* + - * Spreadtrum, Samsung, ZTE/Sanechips, Nokia/NSB
  + ALT 2) Case D {4, 8, 16,20} + 28\*n



* + - Sony, CATT, ZTE/Sanechips, Ericsson, Panasonic, LGE, Sharp, MTK
* Supported values of ‘n’
  + Several companies suggested to have few slots that does not have SSB candidates every few slots that have SSB candidates.
  + Moderator notes that supported values of ‘n’ seems to be heavily dependent on DBTW discussion, and therefore suggest to discuss in Section 2.1.1.

#### **1st Round Discussion:**

Moderator suggest to discuss further based on the alternatives presented (above). Also moderator asks if companies who expressed opinion on ALT 1, can support one of the patterns suggested by companies or not.

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| Company | Comments |
| Samsung | * We support Alt 1-C since it’s one of the supported pattern in Rel-15. We are also supporting Alt 1-A or Alt 1-C if any of them can get consensus. Comparing the three alternatives in Alt 1, Alt 1-A is the best, but we discussed this issue before in Rel-16 NR-U… * For Alt 2, our concern is this pattern is not compatible with the Type0-PDCCH configuration in MIB, i.e., a Type0-PDCCH starting from symbol 7 has collision with the SSB symbol. Also, we want to point out that this pattern is mainly for mixed numerology multiplexing, but this is not a design target in FR2-2. |
| Qualcomm | We are supportive of Alt 1-A ({2, 9} + 14\*n) for the following reasons:   * Allow for gNB beam switching gaps (for slower gNBs)   Allow for possibility of back-to-back multiplexing of CORESET0 + SSB of the same beam (2 symb CORESET0 beam 1 + 4 symb SSB beam 1 + GAP + 2 symb CORESET0 beam 2 + 4 symb SSB beam 2) |
| Panasonic | We think the necessity of a gap symbol due to beam switching time needs to be clarified. According to agreed LS in RAN4(R4-2107985), RAN4 tentatively agreed [59 ns] for gNB beam switching time. “59 ns” fulfils the condition where no explicit switching gap is needed between consecutive SSBs for 960 kHz SCS according to TR38.808 section 4.2.2.4. Thus, we support Alt 2 because potential specification works can be reduced. If a gap symbol is needed due to other factors (e.g., UE Rx beam switching time), we slightly prefer Alt 1-A taking into account allocating a gap symbol and PDCCH between SSBs. |
| Mediatek | Our view was missed in the above summary. We share similar view with Panasonic. Currently RAN 4 has a tentative agreement for beam switching gap, which does not exceed the CP length when SSB SCS is 960 kHz. We are open for further discussion, but we don’t see strong motivation to reserve additional symbol gap for other reasons except for beam switching gap. |
| Sharp | Our original preference is Alt 2 for the minor spec effort, but we could also support Alt 1-A. |
| NTT Docomo | * Maybe good to have a consensus on how to interpret RAN4 LS reply, which says smaller value than CP with 960 kHz SCS is agreed although it is “tentative”. Since it is an important factor to decide the direction here, it would be worth discussing how to treat the tentative value in RAN1 in our view. * Once the tentative value is treated as something we should follow, then we fail to see the motivation to change SSB symbols from case D, which is already supported in 120 kHz SCS. * Otherwise we agree to consider something other than case D. among them, our best preference is {2, 9} since “reuse of the existing NR” is no longer a justification in this case. We believe we can pursue a kind of optimized spec here. |
| ZTE, Sanechips | From the perspective of reducing the impact of standardization, Alt 1-C and Alt 2 are better. However, since RAN4 does not fully determine the value of beam switching time at gNB/UE sides, we can not guarantee that case D can work for beam switching at this stage. Therefore, at least one symbol interval between any two neighbor SSBs should be reserved. So Alt 1-A and Alt 1-C seem more appropriate. Compared with Alt 1-A and Alt 1-C, Alt 1-A is a half-slot symmetric structure, which has many advantages e.g. reduced beam switching times and low detection complexity, so we slightly prefer Alt 1-A.  Please see our added support above using “ZTE/Sanechips” |
| Nokia | In our understanding RAN4 has not concluded that there is a need to assume gap for the gNB beam switching. That being said, while our preference would be alt 1-C, we could also consider alt 1-A.  We do not prefer Alt 1-B as it would limit the PDCCH transmission to single symbol at the start of the slot. |
| OPPO | We support Alt-1B, the design principle is similar to QC’s suggestion, i.e. back-to-back multiplexing. With Alt-1B, the network can also multiplex RMSI with SSB and CORESET for 480kHz SCS. |
| LG Electronics | We strongly support ALT 2. It should be noted that we accepted the introduction of new SCS SSB by adding a NOTE below.  Agreement:  For the case where SSB location and SCS are explicitly provided to the UE (non-initial access) and SSB does not configure Type-0 PDCCH, support 480 kHz and 960 kHz numerologies for the SSB   * Note: Strive to minimize specification impact due to the new SCS for SSB   If we go with Alt 1-A or Alt 1-B, it is a totally different design compared to legacy SSB pattern. Furthermore, based on RAN4 LS, RAN4 tentatively agreed 59 ns for gNB beam switching time and this value is not a problem even for 960 kHz SCS since it is less than 80 % of CP portion. Regarding the back-to-back transmission of SSB and CORESET#0, this issue was extensively discussed in NR-U but was not adopted since how to multiplex SSB and CORESET#0 is up to gNB’s implementation. |
| NEC | Considering the pending requirement from RAN4 for the beam switching gap, we still cannot conclude Alt 2 is applicable now, although it has the less impact on specification. As to the other alternatives, we prefer Alt 1-A with a structure convenient for implement and detection, and considering the beam switching gap as well. |
| Xiaomi | We support Alt1, and Alt 1-A is preferred for one symbol switching time can be supported. |
| Lenovo, Motorola Mobility | We support ALT1 and within that we prefer Alt 1-A, but we are also fine with Alt 1-C if majority of companies support it. |
| Intel | We don’t support Alt2 and we could discuss the variant of Alt1 though our preference is Alt1-A.  We do see strong necessity in time gaps in the DL not because of beam switching only but also because of MIMO TAE. As we tried to explain in our tdoc, MIMO TAE in combination with beam switching together may cause signal distortion if no gaps are placed as illustrated below for 2 Tx port at gNB:    To accommodate MIMO TAE and beam switching some large time interval is needed than just a CP because whether MIMO TAE is late or early is not known at the Tx. This could be illustrated as follows for late and early MIMO TAE:    To be safe, the time interval between symbols should cover 2 times MIMO TAE plus beam switching transient period. Considering current MIMO TAE for gNB of 65 ns, neither CP of SCS 480 kHz nor CP of SCS 960 kHz is suitable. We also need to consider Rx beam switching that could occur at the UE. UE may need to use different beams for different SSB measurements, and we know UE beam switching is expected to be larger than gNB beam switching, especially if it is inter-panel beam switching. Therefore, we support SSB patterns with gaps between consecutive SSBs. |
| Futurewei | Please see our added support above using “Futurewei”. We support ALT 1, more precisely we prefer Alt 1-C, however we are OK with the other options in ALT 1 if they get consensus |
| Ericsson | We share a similar view as LGE, and we would like to maintain similar design as FR2, i.e., Case D pattern (Alt-2). We also agree with the comments on RAN4's discussion on beam switching time – 59 ns (even if still unconfirmed) is less than the CP for both 480 kHz and 960 kHz. We don't think that MIMO TAE is a correct argument given that that requirement is left over from 3G days, and it is not clear that it is relevant for modern active antenna systems. Regarding multiplexing of RMSI and SSB, considering the minimum bandwidth channels for 120 and 480 kHz (100 and 400 MHz), it is not clear that there is sufficient number of RBs available for carrying typical RMSI payloads (~700 or more bits) if one wants to configure 2 SSBs per slot. So, we don't think that optimizing an SSB pattern to fit two Type0-PDCCH monitoring locations, two SSBs, and two RMSI PDSCHs is the correct design goal. |
| CATT | Similar view with LGE and Ericsson. ALT2 because this bring the least impact for specification. |
| Sony | Our 1st preference is Alt 2 because of small specification impact. If there is critical issue on gNB beam switching time, we are fine with Alt 1-C as 2nd preference. |
| Huawei, HiSilicon | We support Alt 1-A. We prefer two have three symbols gap between SSBs in a slot:   * One symbol as a beam switching gap given the fact that, according to ongoing discussions in RAN4, UE’s beam switching time can be in the order of 100-200 ns. Even if the beam switching delay at the UE and gNB are the same (tentatively [59ns]), 72 ns CP for 960 kHz SSB may not be able to absorb DL asynchrony, channel spread, and beam switching time.   Two more symbols to facilitate configuration of up to a two-symbol CORESET#0 prior to the second SSB in the slot. |

#### **1st Round Discussion Summary:**

Companies supportive of Alt 1 generally seems to be ok with Alt 1-A. Other than Alt 1-A, Alt 2 seems to also have some support. The WID explicitly stated to minimize specification impact therefore suggest that we take Alt 2 unless problems are identified for Alt 2. At the same time, companies pointed out the beam switching gap information from RAN4 is currently incomplete so there is risk Alt 2 could have problems later. One company pointed out issues with beam switching gap in conjunction with MIMO TAE which may pose problems if there is no gap between SSBs. Between Alt 1-A and Alt 2, the company split is 14 versus 9. Moderator suggests to see if we can converge to Alt 1-A.

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| * SSB pattern for 480/960kHz   + ALT 1)     - {X, Y} + 14\*n       * Interdigital, [Lenovo/Motorola Mobility], Charter, ETRI, [Xiaomi], WILUS, Futurewei     - (Alt 1-A) {2, 9} + 14\*n       * Huawei/HiSilicon, Qualcomm, Intel, [Apple], Samsung, ZTE/Sanechips, [Panasonic (if gap is needed)], Sharp (2nd preference), [NTT Docomo (2nd preference)], Nokia (2nd preference), NEC, Xioami, Lenovo/Motorola Mobility, Futurewei     - (Alt 1-B) {1,8} + 14\*n,       * OPPO, Samsung, Futurewei     - (Alt 1-C) {2, 8} + 14\*n       * Spreadtrum, Samsung, ZTE/Sanechips, Nokia/NSB, Lenovo/Motorola Mobility (2nd preference), Futurewei   + ALT 2) Case D {4, 8, 16,20} + 28\*n     - Sony, CATT, ZTE/Sanechips, Ericsson, Panasonic, LGE, Sharp, MTK, [NTT Docomo] |

##### **Proposal 1.2-1)**

* First symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame.



#### **2nd Round Discussion:**

Please provide further comments on Proposal 1.2-1.

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| Company | Comments |
| vivo | We suggest to defer the discussion when RAN4 has a clear conclusion. An important factor to impact the SSB time pattern design is the actually required beam switching time, which is still under discussion in RAN 4. Thus, we think it is better to discuss the SSB time pattern design after RAN4 has a clear-out conclusion. |
| DOCOMO | We tend to agree with Ericsson – may still not be well justified why we need to have beam switching gap. |
| Spreadtrum | Alt 1-C is our preference. |
| Nokia | Proposal 1.2-1: We are OK with this proposal with a minor edit that we indicate that this applies to both, 480kHz and 960kHz sub-carrier spacing, e.g.:   * For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame |
| LG Electronics | We do not support Proposal 1.2-1, which is not aligned with previous RAN1 agreement. |
| ZTE, Sanechips | We support Proposal 1.2-1 as it is the best choice before RAN4 makes a final decision. In addition, even if RAN4 finally conclude that beam switching gap is not needed, Alt 1-A can still work well. |
| Samsung | We are ok with the proposal and Nokia’s modification. We are also ok with Alt 1-C.  For the beam sweeping gap, we believe supporting any of Alt 1 can be independent of RAN4’s decision – no matter beam sweeping gap is needed or not, Alt 1 always works.  Also, we really don’t understand the reasoning why 120 kHz SCS SSB pattern is a baseline for 480 kHz and 960 kHz. If 240 kHz SSB pattern is scaled from 120 kHz, we can accept this argument, but obviously it’s not the case.  For multiplexing 2 Type0-PDCCH and 2 SSB in a slot, we believe this is the most fundamental scenario to be supported for FR2, especially for unlicensed band. Please note that a Type0-PDCCH starting from symbol 7 is in particularly supported for FR2 ONLY, and Alt 2 is not compatible with such configuration. |
| Intel | Support Proposal 1.2-1.  As mentioned previously, RAN4 LS only tentatively concludes on simple beam switching gap, but we need to factor into account MIMO TAE + beam switching (both intra-panel and inter-panel), and also beam switching at the UE (both intra-panel and inter-panel). While the LS from RAN4 is not conclusive, we think it has ample evidence that 74ns CP for 960kHz will not be enough for inter-panel beam switching and once we consider MIMO TAE.  We ask companies, who think gap is not needed, on what their understand is regarding inter-panel beam switching values for gNB and UE. |
| NEC | We support the Proposal 1.2-1, namely Alt 1-A, and share the similar view as ZTE. |
| Apple | We support Proposal 1.2-1.  It should be noted that 59ns beam switching gap is defined for gNB, instead of UE side as clearly written in LS. |
| Qualcomm | We support Proposal 1.2-1 (also with Nokia’s edits).  As for previous RAN1 agreement “*Note: Strive to minimize specification impact due to the new SCS for SSB*”, we agree that specification impact should be minimized as long as we maintain the same level of performance/functionality, which Alt2 may not be able to for some gNB implementations. |
| Sharp | We are fine with Proposal 1.2-1 and Nokia’s modifications. |
| Futurewei | We are fine with the Proposal 1.2-1. |
| Ericsson | We prefer Alt-2 for the reasons already stated. If companies are really worried about beam switching gap, we can wait for RAN4 to confirm the [59 ns] gNB beam switching time. |
| Huawei, HiSilicon | We support the proposal with Nokia’s modification.  As we pointed out in the first round of discussion and by multiple other companies, according to ongoing discussions in RAN4, UE’s beam switching time can be in the order of 100-200 ns. Even if the beam switching delay at the UE and gNB would be the same (tentatively [59ns]), 72 ns CP for 960 kHz SSB may not be able to absorb DL asynchrony, channel spread, beam switching time, and MIMO TAE. Please note that SSB design should also take into account UE beam switching time and not only the gNB bema switching time.  Also, we agree with ZTE that even if it turns out that beam switching gap is not required, the design in Proposal 1.2-1 would still works perfectly. |

#### **2nd Round Discussion Summary:**

Moderator suggests to further discuss based on Proposal 1.2-1A (minor edit of Proposal 1.2-1). Below is a summary of company preferences.

**Proposal 1.2-1A)**

* For 480kHz and 960kHz sub-carrier spacing, f~~F~~irst symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame.



Ok: ZTE/Sanechips, Samsung, Intel, NEC, Apple, Qualcomm, Sharp, Futurewei, Huawei/HiSilicon

Not Ok: Docomo, LGE, Ericsson,

Defer discussion: vivo

#### **3rd Round Discussion:**

Please provide further comments for Proposal 1.2-A.

Moderator would like to also solicit methods that would allow to converge without waiting for RAN4 indefinitely. Ideally waiting for RAN4 input is preferred. However, RAN1 may need to also try to make progress as we are waiting for RAN4 inputs. In the worst case, RAN4 inputs may not arrive to RAN1 in the next meeting, which only leaves 1 RAN1 meeting to complete the entire design. So, moderator is open for suggestions on how to make progress under the circumstance.

Moderator would like to ask the objecting companies to Proposal 1.2-1A to ask what would be the most concerning aspect of Proposal 1.2-1A that would break the system in your opinion. If the concern is not able to reuse existing pattern D, but also agree that Proposal 1.2-1A is functional and work, then moderator would like to ask to reconsider their position so that we can progress.

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| Company | Comments |
| Panasonic | We are OK with Proposal 1.2-A for the sake of progress. |
| LG Electronics | We disagree with Proposal 1.2-A   * Inter-panel beam switching: From our understanding, any alternative cannot absorb inter-panel beam switching time, which could be a few usec and longer than 1 OFDM symbol duration for 960 kHz. * UE RX beam switching delay: Based on RAN4 discussion, it may or may not be larger than 59 ns. Nevertheless, do we need to consider UE RX beam switching delay every SSB? Even in Rel-15, it’s up to UE implementation whether or not to switch UE’s RX beam per SSB. * [59 ns] beam switching delay: In TR 38.808 Section 4.2.2.4,   TR 38.817-02 also has captured simulation results that to prevent degradation to system performance, switching time must be less than 80% of the CP length. For 960 kHz SCS this results in approximately 59 ns time window. Given that 10 ns is given for the phase shifter to react, there is still sufficient time available that all the delays of the phase shifter control interface can be accommodated and no explicit switching gap is needed between successive SSB blocks. |
| Samsung | We are ok with the proposal, and want to provide some extra comments: RAN4 only decides the beam switching time from the network point of view, and the UE beam switching time is still under discussion. If finally the UE beam sweeping time is larger than CP, then Alt 2 excludes the UE implementation on beam sweeping from the UE side, which is not acceptable. In this sense, Alt 1 (any sub-alternative) is a safer choice, on top of all other benefits explained in the previous comment, and independent of RAN4’s decision. |
| Qualcomm | We support Proposal 1.2-1A |
| Mediatek | We can’t support Proposal 1.2-1A. We would like to clarify Huawei’s concern and the relation between UE’s beam switching time with the beam switching gap at gNB side. In our understanding, there will be several symbol gaps between the end of a SSB burst transmission and the start of the next SSB burst, which means the gap for UE’s beam switching should be sufficient. Besides, to address Intel’s concern on MIMO TAE problem, we propose to ask RAN 4 to tighten TAE requirement, which is already considered to be feasible in 4.2.2.5 of TR 38.808 and quoted as follows.   It has been discussed in [100] that the current requirement has been in place since UMTS and is the same as quarter of the UMTS chip rate time, i.e. 65 ns matches to 1/(4x3.84) Mcps rate. Improvement in performance has taken place in the past 20 years, and therefore it would be reasonable to consider improvements to TAE requirements. |
| OPPO | We can accept Proposal 1.2-1A for sake of progress. |
| Sharp | We are fine with Proposal 1.2-1A. |
| Intel | Proposal 1.2-1A) – support.  The gaps of 3 symbols could be used to transmit CORESET within the same beam as the corresponding time-multiplexed SSB and avoid potential overlapping between CORESET and SSB (please see our response in discussion about CORESET#0 configuration). |
| DOCOMO | Ok with Proposal 1.2-1A. |
| Apple | We support Proposal 1.2-1A |
| ZTE, Sanechips | We are fine with Proposal 1.2-1A |
| vivo | Understand the risk of delayed RAN1 progress depending on RAN4 input. We are fine with Proposal 1.2-1A for sake of progress. |
| Lenovo, Motorola Mobility | We support Proposal 1.2-1A. |
| Nokia | We would be fine with Proposal 1.2-1A |
| Futurewei | We are fine with Proposal 1.2-1A. |
| InterDigital | We are fine with Proposal 1.2-1A. |
| Huawei, HiSilicon | We support Proposal 1.2-1A |
| Convida Wireless | We are ok with Proposal 1.2-1A |
| LG Electronics | In our view, all alternatives are functional, work, and don’t make the system broken.   * Alt 2 is aligned with previous agreement, that is, to minimize specification impact. * 480/960 kHz is optional SCS for FR2-2, optimization of SSB pattern for optional SCSs is not acceptable. * We didn’t change SSB pattern for 120 kHz considering multiplexing SSB with SIB1, even though the length of DL burst to transmit SSB and SIB1 for 120 kHz SCS can be longer than that for 480/960 kHz, which is more critical for unlicensed band operation.   Therefore, we cannot accept totally new SSB pattern for 480/960 kHz SCS. |
| Mediatek | We are open for discussions if companies see severe issues. However, we would like to point out that based on the agreement for minimizing the spec effort mentioned by LG in the first round discussion, unless there are unacceptable or fatal problem that causes system broken when reusing FR 2 design, directly adopting Proposal 1.2-1 A is not acceptable for us. Currently, the beam switching issue has been resolved based on RAN 4 ‘s agreement. If the MIMO TAE issue can be tackled by tightening gNB’s TAE requirement, there are no other issues when reusing FR2 design. |

#### **3rd Round Discussion Summary:**

**Proposal 1.2-1A)**

* For 480kHz and 960kHz sub-carrier spacing, f~~F~~irst symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame.



Other than following companies, all other company support or can accept Proposal 1.2-1A for sake of progress. The following are companies to object to 1.2-1A:

* LGE: 38.808 Section 4.2.2.4 concludes no gaps are needed for 960kHz, if inter-panel switching is needed than 1 symbol gap may not be sufficient. Existing case D pattern should be equally functional as Proposal 1.2-1A.
* Mediatek: gaps between SSB bursts (string of SSB transmission in 5msec) is sufficient for UE beam switching. Existing case D pattern should be equally functional as Proposal 1.2-1A and should consider new pattern only if something is broken.

#### **Conclusion from GTW (Week 2 - Monday):**

**Agreement:**

* For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, X} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame.
  + Alt 1: X = 8
  + Alt 2: X = 9

#### **4th Round Discussion:**

Please provide further comments so that RAN1 can down-select between Alt 1 (X = 8) and Alt 2 (X = 9).

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| --- | --- |
| Company | Comments |
| Samsung | We support Alt 2 as our first preference, and ok with Alt 1 as a compromise. |
| Qualcomm | We strongly support Alt 2 for the following reasons:   * Can support the case of 1 symbol gap + 2 symbol CORESET0 (Alt1 cannot) * Implementation-wise, Alt 2 is very much similar to Alt 1 .. so cannot see any clear implementation complexity reduction benefits for Alt 1 * For the case of 2 symbols CORESET + 2 search space per slot (using starting symbols 0 and 7), Alt 1 cannot support that, while Alt 2 can. So to minimize spec changes, Alt 2 is better with regards * In spec, anyway, we need to add text for patterns for the new SCS   Hence, Alt 2 has benefits that Alt 1 cannot support. At the same time Alt 1 does not have any spec or implementation simplification benefits |
| Lenovo, Motorola Mobility | We support the proposal with Alt 2 as our preferred choice. |
| Futurewei | We are OK with both alternatives. Alt 2 preferred. We agree with Qualcomm that Alt 2 offers a better CORESET multiplexing flexibility at no additional complications for its implementations. |
| Sharp | Our first preference is Alt 2 and can go with Alt 1 for the sake of progress. |
| Ericsson | As we commented in the GTW, we have a strong preference with whatever pattern is agreed, to reuse Rel-15 Type0-PDCCH starting symbol locations and default PDSCH mapping starting/symbol durations\. We do not wish to repeat the long discussions from Rel-16 on defining new settings. e.g., a Type0-PDCCH starting at symbol index 6 or a length-7 PDSCH starting at symbol 7. |
| LG Electronics | We support Alt 1, to reuse legacy NR design.  As to SSB/CORESET#0 TDM in a slot,   * We didn’t bring up this issue when 120 kHz SCS SSB is discussed, even though containing 2 SSBs + 2 CORESETs in a 120 kHz SCS slot is more essential than that in a 480/960 kHz SCS slot, due to the longer burst length. * Any optimization for optional SCS (i.e., 480/960 kHz SCS) needs to be refrained. * Still gNB has a choice to transmit 1-symbol CORESET#0 in the same slot with SSB at symbol 0/7, or to transmit CORESET#0 with different DL burst from SSB DL burst (i.e., by using O values as in Table 13-12 in TS 38.213 specification). |
| ZTE, Sanechips | We prefer Alt 2 and share similar views with Qualcomm. |
| InterDigital | Support the proposal. |
| Mediatek | Support Alt 1. |
| Nokia | Our preference would be also to have Alt 2 as it would enable supporting 2 symbol CORESET in a slot with (two) SSBs. |
| Intel | We strongly support Alt. 2.  We don’t see technical merits in Alt. 1 comparing to Alt. 2. At the same time, there is no technical concerns with Alt. 2. The only concern about Alt. 2, expressed by opposing the companies, is minimization of standardization efforts by reusing legacy NR design. However, we think that this point, i.e., minimizing standardization efforts by reusing legacy NR design, could be well accounted in other area, in particular, CORESET#0 configuration, as Alt 1 will create conflicts with existing CORESET#0 configuration. |
| Huawei, HiSilicon | We support Alt 2. Besides comments from Qualcomm, we would also like to mention that Alt 2 allows one symbol CORESET#0 on symbol 7 and PDSCH corresponding to Type0-PDCCH in symbol 8. We also think that a gap symbol is necessary at symbol 6. The need for gap symbol for 960 kHz is quite evident as CP cannot accommodate beam switching time of 59 ns + MIMO TAE. For 480 kHz, the need for gap symbol may be more debatable but we think it is more practical and requires less specification effort if same SSB design is used for 480 and 960 kHz. |
| OPPO | Alt2 is preferred. Alt-1 will make the number of CORESET symbols imbalanced for the two SSB in a slot. |

#### **4th Round Discussion Summary:**

Company views:

* Alt 1: X = 8
  + Samsung (ok as well), Futurewei (ok as well), Sharp (ok as well), LGE, Mediatek
  + Reasons for support:
    - Re-use legacy SSB pattern (for 120kHz), optimization for 480/960kHz not warranted
    - Can support CORESET#0 starting location {0,7} with 1 symbol CORESET or with different O values.
* Alt 2: X = 9
  + Samsung, Qualcomm, Lenovo/Motorola Mobility, Futurewei, Sharp, ZTE/Sanechip, Nokia, Intel, Huawei/HiSilicon, OPPO
  + Reasons for support
    - Can support 2 symbol CORESET#0 (at starting location 0, 7), alternatively can support 2 symbol CORESET#0 with 1 symbol gap
    - Better CORESET multiplexing flexibility
    - Allows support for potential beam switching gap (+ MIMO TAE)

Ericsson mentioned for either of the proposals, they do not wish to optimize the PDCCH starting locations for Type0-PDCCH. I believe this can be taken care of with Proposal 1.3-3A. So let’s discuss PDCCH starting location in Section 2.1.3.

#### **5th Round Discussion:**

Moderator would like to hear from companies on how to proceed. RAN1 must make a decision otherwise RAN1 has failed one of the main objectives of the WID. RAN1 is also running out of time for discussions. Please provide comments on any suggestions or comments that could move us forward.

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| --- | --- |
| Company | Comments |
| LG Electronics | Before narrowing down, we would like to have a further discussion.  To Qualcomm,  As we stated before, the same problem occurs for 120 kHz SCS which is mandatory SCS for FR2-2. What is the gNB’s choice for 120 kHz SCS to transmit SSB and CORESET#0 with multiplexing pattern 1? gNB can use O values other than 0 to avoid overlap between SSB and CORESET#0 in the same slot. The same method can still hold for 480/960 kHz in Alt 1. We don’t see the serious problem for Alt 1 since it already provides symbol gap between SSBs, and Alt 2 seems optimization for optional SCSs.  To Intel,  The agreement having NOTE saying RAN1 strive to minimize specification impact is not for CORESET#0 but for SSB design. As commented earlier, the same conflict occurs also for 120 kHz SCS.  To Huawei,  Alt 1 also provides the possibility to convey CORESET#0 on symbol 7 and SIB1 PDSCH on symbol 8. Furthermore, SIB1 PDSCH cannot be rate-matched with SSB, thus, available resource on symbol 8 is the same for both alternatives.  Regarding the symbol gap, both alternatives allow symbol gap between SSBs at symbol 6. |
| Ericsson | We support Alt-1   * Re-use legacy SSB pattern (for 120kHz), optimization for 480/960kHz not warranted * We think that designing for beam switching gaps are not needed in the first place   + We don’t think MIMO TAE is an important consideration for modern active antenna systems * For practical RMSI payloads, we don't think mux of 2 SSBs + 2 RMSI PDSCHs + 2 Type0-PDCCH MOs is a practical configuration given that RAN4 has not and will most likely not optimize GSCNs to be at the channel edge like in Rel-16. We think a more practical configuration is to use a non-zero value of O and put RMSI in separate slots using Mux Pattern 1. * That being said, if the someone really wants the above configuration, Alt-1 still allows it, albeit with a 1 symbol CORESET starting at symbol index 7 |
| OPPO | From technical point of view, I think that the group may reach the consensus that what Alt-1 can do, Alt-2 can also achieve. But not the other way around, due to the 1 symbol CORESET at symbol index 7. In this sense, Alt-2 provides better usage/flexibility for the network to operate. If this can be agreed by the group, i.e. Alt-2 is more advantageous than Alt-1, the only part is the spec impact. According to 38.213, the SSB pattern is defined per SCS. It implies that either Alt-1 or Alt-2 will anyway require a new case in the spec, given that Alt-1 and Alt-2 are only different at the Y value, it seems that both alternatives have similar spec impact. None is significantly smaller than the other in terms of the spec impact. In this regards, is it more reasonable to adopt a more advantageous alternative? |
| Intel | We support Alt.2.  Below is the citation of the agreement made by RAN plenary about SCS 480 kHz for SSB:   * + In addition to 120kHz, support 480 kHz SSB for initial access with support of CORESET#0/Type0-PDCCH configuration in the MIB with following constraints:     - Limited sync raster entry numbers       * It is assumed that RAN4 supports a channelization design which results in the total number of synchronization raster entries considering both licensed and unlicensed operation in a 52.6 – 71 GHz band no larger than 665 (Note: the total number of synchronization raster entries in FR2 for band n259 + n257 is 599). If the assumption cannot be satisfied, it’s up to RAN4 to decide its applicability to bands in 52.6 – 71 GHz.     - only 480kHz CORESET#0/Type0-PDCCH SCS supported for 480 kHz SSB SCS.     - Prioritize support SSB-CORESET#0 multiplexing pattern 1. Other patterns discussed on a best effort basis.     - 960 kHz numerology for the SSB is not supported by the UE for initial access in Rel-17.     - **Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible**     - Note: 480 kHz is an optional SSB numerology for initial access for the UE. A UE supporting a band in 52.6-71 GHz must at least support 120 kHz SCS (for initial access and after initial access)     - Note: Dependency or lack thereof for a UE supporting 480kHz and/or 960kHz numerology for data and control to also support 480kHz SSB numerology for initial access is to be tackled as part of UE capability discussion.   The NOTE says that minimization of specification efforts should be achieved by reusing CORESET#0 configuration tables. It says NOTHING about reusing SSB patterns. Moreover, Alt.2 allows reusing CORESET#0 configurations, therefore, it is fully compliant with the agreement of RAN plenary.  The specification impact from X=9 is completely identical as X = 8. At the same time, X=9 clear provides all the functionality that X=8 can provide and provide more benefits.  Companies commented that there is some benefit from re-using existing pattern. However, we don’t quite understand what is the benefit other than pattern looks similar. From implementation perspective, any changes to SCS will mean implementation will need to change. |

#### **5th Round Discussion Summary:**

The following is a summary of company views.

* Alt 1: X = 8
  + Samsung (ok as well), Futurewei (ok as well), Sharp (ok as well), LGE, Mediatek
  + Reasons for support:
    - Re-use legacy SSB pattern (for 120kHz), optimization for 480/960kHz not warranted
    - Can support CORESET#0 starting location {0,7} with 1 symbol CORESET or with different O values.
    - MIMO TAE consideration is not important for modern active antenna system
    - Multiplexing 2 SIB1 PDSCH + 2 SSB is a practical configuration, rather use of non-zero O value to multiplex SIB1 and SSB in different slots is more practical
    - Both X=8 and X=9 support symbol gap between SSB for beam switching at symbol 6
* Alt 2: X = 9
  + Samsung, Qualcomm, Lenovo/Motorola Mobility, Futurewei, Sharp, ZTE/Sanechip, Nokia, Intel, Huawei/HiSilicon, OPPO
  + Reasons for support
    - Can support 2 symbol CORESET#0 (at starting location 0, 7), alternatively can support 2 symbol CORESET#0 with 1 symbol gap
    - Better CORESET multiplexing flexibility
    - Allows support for potential beam switching gap (+ MIMO TAE)
    - WID objective is to minimize spec effort for CORESET, and does not mention SSB pattern related aspects
    - X=9 provides all functionality that X=8 provides, and further provides additional advantages

Moderator suggests further discussing Proposal 1.2-1A and 1.2-1B.

##### **Proposal 1.2-1A)**

* For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame.

##### **Proposal 1.2-1B)**

* For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, 8} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame.

#### **6th Round Discussion:**

Please provide additional comments for Alt 1 and Alt 2.

* Alt 1: X = 8
  + Samsung (ok as well), Futurewei (ok as well), Sharp (ok as well), LGE, Mediatek
  + Reasons for support:
    - Re-use legacy SSB pattern (for 120kHz), optimization for 480/960kHz not warranted
    - Can support CORESET#0 starting location {0,7} with 1 symbol CORESET or with different O values.
    - MIMO TAE consideration is not important for modern active antenna system
    - Multiplexing 2 SIB1 PDSCH + 2 SSB is a practical configuration, rather use of non-zero O value to multiplex SIB1 and SSB in different slots is more practical
    - Both X=8 and X=9 support symbol gap between SSB for beam switching at symbol 6
* Alt 2: X = 9
  + Samsung, Qualcomm, Lenovo/Motorola Mobility, Futurewei, Sharp, ZTE/Sanechip, Nokia, Intel, Huawei/HiSilicon, OPPO
  + Reasons for support
    - Can support 2 symbol CORESET#0 (at starting location 0, 7), alternatively can support 2 symbol CORESET#0 with 1 symbol gap
    - Better CORESET multiplexing flexibility
    - Allows support for potential beam switching gap (+ MIMO TAE)
    - WID objective is to minimize spec effort for CORESET, and does not mention SSB pattern related aspects
    - X=9 provides all functionality that X=8 provides, and further provides additional advantages

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | Our position didn’t change, and we can be ok with either option. But we don’t agree with the statement that “Multiplexing 2 SIB1 PDSCH + 2 SSB is not a practical configuration”. Actually for unlicensed band, this is a very essential configuration to construct a “burst” and save LBT procedure. |
| Spreadtrum | We support Alt 1. The legacy pattern is beneficial for UE implementation. |
| Qualcomm | Same comments are before leading to our strong support for Alt 2. |
| Huawei, HiSilicon | We still support Alt 2.  Three symbols between the first SSB and second SSB in the slot allows for a two-symbol CORESET#0 + gap. The need for gap symbol for 960 kHz is quite evident as CP cannot accommodate beam switching time of 59 ns + MIMO TAE. For 480 kHz, the need for gap symbol may be more debatable but we think it is more practical and requires less specification effort if same SSB design is used for 480 and 960 kHz.  We find that specification work of Alt 1 and Alt 2 is the same and don’t see any technical advantage of Alt 1 compared to Alt 2. |

#### **6th Round Discussion Summary:**

To be filled.

### 2.1.3 CORESET#0 Configuration

* From [1] Huawei/HiSilicon:
  + For CORESET for Type0-PDCCH in 52.6GHz to 71GHz spectrum, support the following:
    - For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {120, 120} kHz, support multiplexing pattern 1 and multiplexing pattern 3 as per Agreement in RAN1 104-e.
    - For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {480, 480} kHz, support multiplexing pattern 1 only.
    - For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {960, 960} kHz, support multiplexing pattern 1 only.
  + For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {120, 120} kHz, in addition to the supported values of (, ) from Rel-15, support with .
  + Support the following CORESET#0 RB offsets values for {SSB, CORESET#0} SCS={120, 120} kHz:
    - For CORESET#0 with 24 RBs and 48 RBs: the same as supported values in Table 13-8 of 38.213.
    - For CORESET#0 with 96 RBs: 0, 38, 76 RBs for multiplexing pattern 1 and -20 (-21) RBs when for multiplexing pattern 3.
    - Note: All above RB offsets are nominal and may need to be modified after finalizing synch raster and channel raster design in FR2-2.
  + Support at least the following combinations in 52.6GHz to 71GHz spectrum:
    - for {SSB, CORESET#0} ={480, 480} kHz with multiplexing pattern 1, , ={1,2};
    - for {SSB, CORESET#0} ={960, 960} kHz with multiplexing pattern 1, , ={1,2}.
  + To find the offset between an off-synch raster SSB and the corresponding CORESET#0 in 60GHz unlicensed spectrum, RAN1 should uniquely determine the hypothetical on-synch raster SSB that serves as the reference for the offset to the off-synch raster SSB in case more than one synch rasters are included in a channel bandwidth.
* From [2] vivo:
  + Dedicated signalling can’t be used for conveying the Type-0 PDCCH configuration to read the SIB1.
  + The following SSB-Coreset 0 multiplexing patterns are supported for each SCS pair when operation in FR2-2 (52.6-71GHz):
    - (120K, 120K): Pattern 1, Pattern 3
    - (480K, 480K): Pattern 1, Pattern 3
    - (960K, 960K): Pattern 1, Pattern 3
  + For {SSB, PDCCH} SCS {120, 120} kHz, {480, 480} kHz and {960, 960} kHz in licensed band, the tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2-1 in Rel-15 can be reused.
  + For the un-licensed band operation from 52.6GHz to 71GHz, the CORESET design principle should consider two aspects: 1. Occupy as much bandwidth as possible; 2. Use as few bits as possible in the CORESET configuration.
  + For {SSB, PDCCH} SCS {120, 120} kHz, {480, 480} kHz and {960, 960} kHz, the tables for PDCCH monitoring occasions for type0-PDCCH CSS set configuration defined for FR2-1 in Rel-15 can be reused with little adjustment.
* From [3] Spreadtrum:
  + The mechanism of two offsets in MIB defined for NR-U, i.e. Alt 2 (use configuration in MIB to support CORESET#0/Type0-PDCCH), can be reused for UE to determine CORESET#0/Type0-PDCCH.
* From [4] Interdigital:
  + Support Alt 2 on using the CORESET#0/Type0-PDCCH configuration in MIB.
  + Introduce the enhancements on SS/PBCH block transmission patterns to deliberately include the CORESET#0 and SIB1 in fixed time locations along with the corresponding SS/PBCH block to ensure the channel occupancy as much as possible, in the initial access operations for unlicensed spectrum in beyond 52.6GHz.
* From [7] Samsung:
  + For SS/PBCH block with 120 kHz SCS,
    - only support CORESET#0 SCS as 120 kHz;
    - additional CORESET#0 RB offsets are needed;
    - support 96 RB as the number of RBs for CORESET#0.
  + For SS/PBCH block with 480 kHz SCS and 960 kHz,
    - only support CORESET#0 SCS same as SS/PBCH block SCS;
    - support at least the same SS/PBCH block and CORESET#0 multiplexing patterns, number of RBs for CORESET#0, and number of symbols as in 120 kHz SCS;
    - support 96 RB as the number of RBs for CORESET#0;
    - Further study the RB offset based on RAN4 design of channel and synchronization rasters.
* From [8] CATT:
  + Multiplexing pattern 2 or 3 can be used for further multiplexing SSB/CORSET#0 with periodic CSI-RS/paging PDCCH&PDSCH in frequency.
  + For SSB and CORESET#0/Type0-PDCCH with 120 KHz SCS, support the following combinations of SSB/CORESET multiplexing pattern, number of RB and symbols for CORESET.
    - {mux pattern 1, 48 PRB CORESET, 1 symbol CORESET}
    - {mux pattern 1, 48 PRB CORESET, 2 symbol CORESET}
    - {mux pattern 3, 48 PRB CORESET, 2 symbol CORESET}
* From [9] ZTE/Sanechips:
  + The multiplexing pattern 1 and 3 for three approved SCS combinations of SSB and Type0-PDCCH can be considered for Rel-17 NR above 52.6 GHz.
    - (SSB, Type0-PDCCH): SCS (120 kHz, 120 kHz)
    - (SSB, Type0-PDCCH): SCS (480 kHz, 480 kHz)
    - (SSB, Type0-PDCCH): SCS (960 kHz, 960 kHz)
  + For {SSB, CORESET#0 for Type0-PDCCH} SCS = {120, 120} kHz, even though RAN4 has agreed the minimum CBW is increased to 100 MHz, at least SSB and CORESET#0 multiplexing patterns, number of RBs for CORESET#0, number of symbols (duration of CORESET#0) that are supported in Rel-15/16 should still be supported.
* From [11] Ericsson:
  + RAN1 should strive to design a common CORESET0 configuration table for use for all 3 supported SCS combinations (120,120), (480,480), and (960, 960).
  + Reuse existing Table 13-12 in 38.213 for operation with 480 and 960 kHz SCS. For subcarrier spacings 480 and 960 kHz. Use and , respectively, instead of when determining the PDCCH monitoring occasions using offset values from the table.
* From [12] Futurewei:
  + In FR2-2 CORESET#0, PDCCH SIB1 support the same SCS as the SCS for SS/PBCH.
* From [13] Nokia/NSB:
  + Consider also SSB and CORESET#0 multiplexing pattern 3 for 120kHz SSB.
  + Pending on the UE minimum BW capability, consider also SSB and CORESET#0 multiplexing pattern 3 for 480kHz SSB.
  + For CORESET#0 with 120kHz sub-carrier spacing, consider supporting also ={96} for multiplexing pattern 1.
  + For SSB and CORESET#0 with 480kHz sub-carrier spacing with SSB and CORESET#0 multiplexing pattern 1, support following options:
    - ={[1],2, 3}
    - ={24, 48}.
  + For SSB and CORESET#0 with 480kHz sub-carrier spacing with SSB and CORESET#0 multiplexing pattern 3, following configuration options could be considered:
    - ={1,2}
    - ={24, 48}.
  + For SSB and CORESET#0 with 960kHz sub-carrier spacing, with SSB and CORESET#0 multiplexing pattern 1 support
    - ={2, 3}.
    - ={24}.
* From [18] Qualcomm:
  + for FR2-2, CORESET0 SCS = SSB SCS for all SCSs
  + consider minimizing the overhead of beam switching gaps by:
    - Supporting multiplexing pattern 3
    - Introducing an SSB/CORESET0 multiplexing pattern for higher SCS SSB (480 and 960 kHz), where TDM grouping of the SSB and the corresponding CORESET0 is considered
* From [19] LG Electronics:
  + Reuse Table 13-8 in TS 38.213 specification for CORESET#0 configuration with 120/480/960 kHz, except for RB offset values.
  + Reuse Table 13-12 in TS 38.213 specification for type0-PDCCH CSS set configuration with 120/480/960 kHz, except for O values for 480/960 kHz.
* From [21] Mediatek:
  + Support only 1 SCS for CORESET#0/Type0-PDCCH for a given SSB SCS.
* From [22] Intel:
  + Consider using Type0-PDCCH search space in symbols {0,1} and {7, 8} for each SSB.
* From [23] Apple:
  + In addition to 24 and 48 PRBs, 96 PRBs can be considered for CORESET#0 BW with 120kHz SCS.
* From [25] NTT Docomo:
  + On down-selection regarding SSB symbol definition, whether to reuse Case D should be discussed considering whether to practically support SSB-CORESET#0 multiplexing within the same slot
  + With all SCSs supported in 52.6 – 71 GHz and with the restriction agreed in RAN#91-e, the existing SSB-CORESET#0 multiplexing pattern 1 specified in 38.213 with Table 13-8 and 13-12 works as it is.
    - Feasibility of a certain case, where e.g., 2 pairs of {Type0-PDCCH, SIB1 PDSCH} are allocated in a slot, is not clear
    - With 960 kHz SCS, smaller ’O’ value can be added considering shorter time duration SSB beam sweeping
* From [26] Xiaomi:
  + It should be clarified that {480,120} kHz combination of SSB with CORESET#0/Type0-PDCCH SCS is not supported.
* From [28] WILUS:
  + We propose that SS/PBCH block and CORESET#0/RMSI can be multiplexed in TDM/FDM within a slot considering multi-beam operation and it can be closely located without the gap between SSB and CORESET#0/RMSI for not allowing any in-between channel access operation in the unlicensed band.

#### Summary of Contribution Discussions

The following are a summary of company views on CORESET#0 configuration aspects.

* For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz
  + controlResourceSetZero
    - Addition of 96 PRB CORESET#0
      * Support: Huawei/HiSilicon, Samsung, Nokia/NSB, Apple
      * Do not support: Ericsson
* For {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz
  + controlResourceSetZero
    - Support {24, 48} PRB with {1,2} symbol durations
      * Huawei/HiSilicon
    - Use Table 13-8 (originally intended for {120,120} kHz) except RB offset
      * {mux pattern 1, 24 PRB, 2 symbol}
      * {mux pattern 1, 48 PRB, 1 symbol}
      * {mux pattern 1, 48 PRB, 2 symbol}
      * {mux pattern 3, 24 PRB, 2 symbol}
      * {mux pattern 3, 48 PRB, 2 symbol}
      * [vivo], ~~[~~Samsung (with 96 RB as well)~~]~~, ~~[~~Ericsson~~]~~, LGE, NTT Docomo, Qualcomm
    - Support mux pattern 1 with {24, 48} PRB and {[1],2,3} symbol duration
      * Nokia/NSB
    - Support mux pattern 3 with {24, 48} PRB and {1,2} symbol duration
      * Nokia/NSB, Samsung
    - Support mux pattern 3
      * Qualcomm, Samsung
  + searchSpaceZero
    - Use Table 13-12 (originally intended for {120,120} kHz)
      * NTT Docomo, Ericsson
    - Use Table 13-12 (originally intended for {120,120} kHz) except O values
      * LGE, Samsung, Huawei/HiSilicon
    - Use symbols {0,1} and {7,8} for Type0-PDCCH for each SSB
      * Intel, Qualcomm, Huawei/HiSilicon
* For {SSB, CORESET#0/Type0-PDCCH} = {960, 960} kHz
  + controlResourceSetZero
    - Support {24} PRB with {1,2} symbol durations
      * Huawei/HiSilicon
    - Use Table 13-8 (originally intended for {120,120} kHz) except RB offset
      * {mux pattern 1, 24 PRB, 2 symbol}
      * {mux pattern 1, 48 PRB, 1 symbol}
      * {mux pattern 1, 48 PRB, 2 symbol}
      * {mux pattern 3, 24 PRB, 2 symbol}
      * {mux pattern 3, 48 PRB, 2 symbol}
      * [vivo], ~~[~~Samsung (with 96 RB as well)~~]~~, ~~[~~Ericsson~~]~~, LGE, NTT Docomo, Qualcomm [24 RB only]
    - Support mux pattern 1 with {24~~8~~} PRB and {2,3} symbol duration
      * Nokia/NSB, Samsung
    - Support mux pattern 3
      * Qualcomm, Samsung
  + searchSpaceZero
    - Use Table 13-12 (originally intended for {120,120} kHz)
      * NTT Docomo, Ericsson,
    - Use Table 13-12 (originally intended for {120,120} kHz) except O values
      * LGE, Samsung, Huawei/HiSilicon
    - Use symbols {0,1} and {7,8} for Type0-PDCCH for each SSB
      * Intel, Qualcomm, Huawei/HiSilicon

#### **1st Round Discussion:**

There were some suggestions on mux pattern 3 support. Since the updated WID explicitly mentions to prioritize mux pattern 1, moderator suggests it is suggested to discuss mux pattern 1 aspects first and once concluded continue further discussion mux pattern 3 aspects.

Companies are asked to comment further on the following issues:

Q1) addition of 96 PRB CORESET#0 for {120kHz, 120kHz}={SSB, PDCCH} pair to ‘controlResourceSetZero’ field

Q2) Supported PRB and symbol duration with mux pattern 1 for {480kHz, 480kHz}={SSB, PDCCH} pair and {960kHz, 960kHz}={SSB, PDCCH} pair

Q3) supported search space configurations for {480kHz, 480kHz}={SSB, PDCCH} pair and {960kHz, 960kHz}={SSB, PDCCH} pair. For example, whether Table 13-12 can be used with little or no modifications.

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | Q1) We support adding 96 RB CORESET#0 for better coverage.  Q2) The same RB and symbol duration with Pattern 1 for {120, 120} can be supported for {480, 480} and {960, 960}.  Q3) Table 13-12 can be used as a baseline with necessary modifications, e.g. the O value. |
| Qualcomm | Q1: we do not think there is a strong need to introduce 96 RB option, however, it can be considered if needed  Q2:   * For 480 + 480 kHz: support the same combinations as for 120 + 120 kHz   + 24 RB + 2 symbols   + 48 RB + 1 or 2 symbols * For 960 + 960 kHz: due to min UE BW constraint (400 MHz) and to compensate for coverage,   + 24 RB + 1 or 2 or [3] symbols   Q3: Start with table 13-12 as baseline. However, for the values of “O”, since the SSB beam sweep time for 480 and 960 kHz is short (1 and 0.5 ms), the values of “O” of 2.5, 5, and 7.5 ms may be too long and we may to consider some reduction factor.  In addition, we can also support “Use symbols {0,1} and {7,8} for Type0-PDCCH for each SSB” as indicated above using “Qualcomm” |
| Sharp | Q1: we consider adding 96 PRB as optimization rather than necessity.  Q2: Firstly reuse Table 13-8 with multiplexing pattern 1 as baseline. Limited modifications could be further discussed.  Q3: Firstly reuse Table 13-12 as baseline. Further discuss necessary modifications to accommodate higher SCS. |
| Docomo | Q1) support for better coverage.  Q2) generally fine.  Q3) O value can be revisited. |
| ZTE, Sanechips | Q1) It can be introduced only when there is a strong demand.  Q2) The same RB and symbol duration with Pattern 1 for {120, 120} in Table 13-8 in TS 38.213 can be supported for {480, 480} and {960, 960}.  Q3) Table 13-12 can be used as a baseline with necessary enhancements. Except the O value mentioned by Samsung and Qualcomm, DRS/SSB pattern design discussed in 2.1.2 may also have impacts on search space configurations. |
| Nokia | Q1) We would support adding 96PRB option for 120kHz.  Q2) We would propose to support for {SSB, CORESET#0}={480kHz, 480kHz} multiplexing pattern 1 {,} configurations (in order of priority):   * {48,2} * {24,2}, {48,1} * {24,3}   For {SSB, CORESET#0}={960kHz, 960kHz} multiplexing pattern 1 {,} configurations (in order of priority):   * {24,2} * {24,3}   Q3) Enabling scheduling SIB1 in the same slot as SSB could be considered. Thus PDCCH monitoring occasion option with PDCCH first symbol indexes corresponding to the free symbols in the slot with SSBs should be considered i.e. with Alt 1-C {0,6} or with Alt 1-A {0,7}. In respect to Table 13-12, smaller ‘O’ values could be considered for the 480kHz and 960kHz sub-carrier spacing.  Note minor correction in above summary:  “Support mux pattern 1 with {24~~8~~} PRB and {2,3} symbol duration” |
| LG Electronics | Q1) We don’t think 96 PRB CORESET#0 is additionally needed.  Q2) Same as in NR Rel-15, i.e., 24 RB + 2 symbols or 48 RB + 1 or 2 symbols  Q3) Table 13-12 can be reused with some modifications to O values. |
| Lenovo, Motorola Mobility | Q1) We do not see a need for 96 PRB for 120 kHz.  Q2) We are fine with it.  Q3) The table 13-12 cab be used as a baseline with necessary modifications for O value for 480 and 960 kHz. |
| Intel | Q1) We support adding 96 RB CORESET#0.  For SCS 120 kHz, 96 RBs occupy bandwidth of 138.24 MHz which is larger than 100 MHz that can achieve the conducted power limit of 27 dBm according to US regulation. Without support of 96 PR, we are penalizing the conducted power for all US deployments with 120kHz.  Also, for {120, 120} we would like to suggest removing configurations with 24 RB because there is no more limitation on the min channel bandwidth  Q2) The same RB and symbol duration with Pattern 1 for the current configuration of {120, 120} can be supported for {480, 480} and {960, 960}.  Q3) Table 13-12 can be used as a baseline with necessary modifications. |
| Futurewei | Q1) We are OK with adding 96 PRB CORESET#0 (even we do not think that is a necessity) if the majority wants it.  Q2) The same Pattern 1 for {120, 120} Table 13-8 in TS 38.213 can be supported for {480, 480} and {960, 960} as baseline.  Q3) Use Table 13-12 as a baseline with necessary modifications |
| Ericsson | Please see our added support above using "Ericsson"  Q1) We don't think 96 RB CORESET0 it is needed. Based on link budget analysis, we have found that in terms of coverage, it is not Type0-PDCCH that is limiting; rather, it is RMSI PDSCH. Hence, we don't see a coverage improvement for RMSI by enabling 96 RB CORESET0.  Q2) We think a common table design should be used for 120/480/960 kHz SCS, and that Table 13-8 is the right starting point. It may be necessary to add a new SSB-CORESET0 offset for the 48 RB case (based on RAN4 channelization design) to fully enable use of the minimum bandwidth channels.  Q3) We think that Table 13-12 can be used without modification. For 480 and 960 kHz, additional specification text can be added to re-interpret the offset values (the O values) if it is desired to enable a RMSI beam sweep to start soon after the SSB beam sweep. The proposal in our paper is as follows:   1. Reuse existing Table 13-12 in 38.213 for operation with 480 and 960 kHz SCS. For subcarrier spacings 480 and 960 kHz. Use and , respectively, instead of when determining the PDCCH monitoring occasions using offset values from the table. |
| CATT | Q1) We don’t think 96 PRB CORESET#0 need to be needed.  Q2) Same as in legacy specification TS 38.213  Q3) Table 13-12 can be reused . |
| Sony | Q1) We don’t see strong demand to add 96 PRB CORESET#0 for 120 kHz SCS.  Q2) The same RB and symbol duration with Pattern 1 in Table 13-8 should be considered as baseline.  Q3) Table 13-12 can be reused as baseline. |
| Huawe/HiSilicon | Q1) Support. To maximize Tx power given PSD constraint.  Q2) Support. It is OK to support (PRB, symbol) ={(24,2), (48, 1), (48, 2)} for Mux 1 as in Rel-15 for 120 kHz.  Q3) Support with the following change  “supported search space configurations with mux pattern 1 for {480kHz, 480kHz}={SSB, PDCCH} pair and {960kHz, 960kHz}={SSB, PDCCH} pair. For example, whether Table 13-12 can be used ~~with little or no modifications~~ as a starting point.  In our view, Table 13-12 may be used only as a starting point. However, larger O values can be removed to avoid unnecessary large latency during initial access. We also believe that larger O values are not useful for 120 kHz in FR2-2 and may be removed to “free up” a bit which may be used toward indicating other values such as .  We also agree to use symbols {0,1} and {7,8} for Type0-PDCCH as discussed in Section 2.1.2. We have added our support in the Summary. |

#### **1st Round Discussion Summary:**

**Issue 1)** On whether or not to additionally support 96 PRB for CORESET#0 for {120, 120} = {SSB, PDCCH} case. Few companies mentioned that addition of this is more of optimization rather than necessity. Many companies commented they can consider if it is needed, and several companies expressed support for this. Four company explicitly mentioned they do not think it is needed. Moderator suggest to continue discussion on this topic, at the same time it is suggested that it to be treated with lower priority compared to other proposals during GTW. Continue discussion on Proposal 1.3-1.

|  |
| --- |
| * For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz   + controlResourceSetZero     - Addition of 96 PRB CORESET#0       * Support: Huawei/HiSilicon, Samsung, Nokia/NSB, Apple, NTT Docomo, Lenovo/Motorola Mobility, Intel       * Do not support: Sharp (optimization), LGE, Ericsson, CATT, Sony       * Maybe: Qualcomm, ZTE/Sanechips, Futurewei |

**Proposal 1.3-1)**

* Support inclusion of 96 PRB CORESET#0 with appropriate RB offset for {120 kHz, 120 kHz} = {SSB,PDCCH} case to ‘controlResourceSetZero’ field of MIB

**Issue 2)** For the CORESET#0 and Type0-PDCCH SS configurations, companies views are summarized as below. There is good support in using existing Table 13-8 and 13-12 as much as possible. Some companies mentioned certain parameters such as ‘O’ in 13-12 will need to be revisited. Since the RB offset values are pending RAN4 channelization discussion, moderator has formulate a proposal for further discussion in Proposal 1.3-2 and 1.3-3.

|  |
| --- |
| * For {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz   + controlResourceSetZero     - Support {24, 48} PRB with {1,2} symbol durations       * Huawei/HiSilicon     - Use Table 13-8 (originally intended for {120,120} kHz) except RB offset       * {mux pattern 1, 24 PRB, 2 symbol}       * {mux pattern 1, 48 PRB, 1 symbol}       * {mux pattern 1, 48 PRB, 2 symbol}       * {mux pattern 3, 24 PRB, 2 symbol}       * {mux pattern 3, 48 PRB, 2 symbol}       * [vivo], ~~[~~Samsung (with 96 RB as well)~~]~~, ~~[~~Ericsson~~]~~, LGE, NTT Docomo, Qualcomm, ZTE/Sanechips, Sharp, CATT, Sony (baseline)     - Support mux pattern 1 with {24, 48} PRB and {[1],2,3} symbol duration       * Nokia/NSB     - Support mux pattern 3 with {24, 48} PRB and {1,2} symbol duration       * Nokia/NSB, Samsung     - Support mux pattern 3       * Qualcomm, Samsung   + searchSpaceZero     - Use Table 13-12 (originally intended for {120,120} kHz)       * NTT Docomo, Ericsson     - Use Table 13-12 (originally intended for {120,120} kHz) except O values       * LGE, Samsung, Huawei/HiSilicon     - Use symbols {0,1} and {7,8} for Type0-PDCCH for each SSB       * Intel, Qualcomm, Huawei/HiSilicon |

For reference, the following is Table 13-8 and 13-12 from TS38.213

Table 13-8: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) |
| 0 | 1 | 24 | 2 | 0 |
| 1 | 1 | 24 | 2 | 4 |
| 2 | 1 | 48 | 1 | 14 |
| 3 | 1 | 48 | 2 | 14 |
| 4 | 3 | 24 | 2 | -20 if  -21 if |
| 5 | 3 | 24 | 2 | 24 |
| 6 | 3 | 48 | 2 | -20 if  -21 if |
| 7 | 3 | 48 | 2 | 48 |
| 8 | Reserved | | | |
| 9 | Reserved | | | |
| 10 | Reserved | | | |
| 11 | Reserved | | | |
| 12 | Reserved | | | |
| 13 | Reserved | | | |
| 14 | Reserved | | | |
| 15 | Reserved | | | |

Table 13-12: Parameters for PDCCH monitoring occasions for Type0-PDCCH CSS set - SS/PBCH block and CORESET multiplexing pattern 1 and FR2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Index |  | Number of search space sets per slot |  | **First symbol index** |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | 2.5 | 1 | 1 | 0 |
| 3 | 2.5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 4 | 5 | 1 | 1 | 0 |
| 5 | 5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 6 | 0 | 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 7 | 2.5 | 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 8 | 5 | 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 9 | 7.5 | 1 | 1 | 0 |
| 10 | 7.5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 11 | 7.5 | 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 12 | 0 | 1 | 2 | 0 |
| 13 | 5 | 1 | 2 | 0 |
| 14 | Reserved | | | |
| 15 | Reserved | | | |

##### **Proposal 1.3-2)**

* For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support the following set of parameters.

|  |  |  |
| --- | --- | --- |
| SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols |
| 1 | 24 | 2 |
| 1 | 48 | 1 |
| 1 | 48 | 2 |
| 3 | 24 | 2 |
| 3 | 48 | 2 |

* + - Note: the number of entries corresponding the same {mux pattern, number of RB, number of symbol} tuple (listed above) will depend on required RB offsets that needs to be supported based on channel and sync raster design.
  + FFS: addition of any the following set of parameters

|  |  |  |
| --- | --- | --- |
| SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols |
| 1 | 24 | 3 |
| 1 | 96 | 1 |
| 1 | 96 | 2 |
| 3 | 96 | 2 |

**Proposal 1.3-3)**

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support the following set of parameters are supported for SS/PBCH block and CORESET multiplexing pattern 1:

|  |  |  |
| --- | --- | --- |
| Number of search space sets per slot |  | **First symbol index** |
| 1 | 1 | 0 |
| 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 1 | 2 | 0 |

* + - Note: the number of entries corresponding the same {number of SS per slot, M, first symbol index} tuple (listed above) will depend on supported ‘O’ for each tuple.
    - FFS: Values of supported ‘O’ and supported combination of ‘O’ and number of SS per slot, M, first symbol index} tuple.

#### **2nd Round Discussion:**

Please provide further comments for Proposal 1.3-1 ~ 1.3-3. Proposal 1.3-1 is copied below for convenience.

**Proposal 1.3-1)**

* Support inclusion of 96 PRB CORESET#0 with appropriate RB offset for {120 kHz, 120 kHz} = {SSB,PDCCH} case to ‘controlResourceSetZero’ field of MIB

|  |  |
| --- | --- |
| Company | Comments |
| vivo | Support the proposal for better coverage and OCB requirement for unlicensed band. |
| DOCOMO | Support the proposal. |
| Spreadtrum | Fine |
| Nokia | Proposal 1.3-1: Still OK  Proposal 1.3-2: In principle OK, not sure if we need the table for the FFS combinations.  Proposal 1.3-3: OK with the proposal with the assumption that Proposal 1.2-1 for SSB resource pattern is agreed. |
| LG Electronics | Proposal 1.3-1) Still we don’t think support of 96 PRBs is essential for FR2-2. Without clear majority support, we cannot accept this proposal.  Proposal 1.3-2) We prefer to reuse all of indexes as in Rel-15, with some modification for RB offset values, if deemed necessary.  Proposal 1.3-3) We prefer to reuse all of indexes as in Rel-15, with some modification for O values. |
| ZTE, Sanechips | For Proposal 1.3-1, we can accept it if most companies think it is necessary.  For Proposal 1.3-2, we are fine with it.  For Proposal 1.3-3, we suggest to defer the discussion as the first symbol index of CORESET#0 is also depending on SSB pattern design discussed in 2.1.2. |
| Samsung | Proposal 1.3-1) Support.  Proposal 1.3-2) Support.  Proposal 1.3-3) We are ok with the proposal, and want to clarify that this proposal is same as reusing Rel-15 table with possible medication on O values right? |
| Intel | **Proposal 1.3-1)** – agree  **Proposal 1.3-2)** – agree  **Proposal 1.3-3) –** agree  For 1.3-1, we would like to comment that, while Ericsson mentioned that RMSI/SIB1 PDSCH is the real bottleneck, the CORESET#0 bandwidth essentially also dictates the maximum bandwidth usage for SIB1 PDSCH, as CORESET#0 bandwidth is the initial BWP. So, we fail to understand why it is ok not to support maximum conducted power transmission for important channels such as PDCCH for SIB1 and PDSCH for SIB1. Both PDCCH and PDSCH get impacted from CORESET#0 bandwidth. |
| Apple | Proposal 1.3-1: Support  Proposal 1.3-2: Ok.  Proposal 1.3-3: Support. |
| Qualcomm | Proposal 1.3-1: fine  Proposal 1.3-2: for 960 kHz, mux pattern 1 with 48 RB and mux pattern 3 with 24 RB exceed the 400 MHz minimum BW capability.  Proposal 1.3-3: fine |
| Sharp | Proposal 1.3-1: Ok if this proposal presents the majority view.  Proposal 1.3-2: Support.  Proposal 1.3-3: Support. |
| Futurewei | Proposal 1.3-1: Not essential but we are OK if the majority wants.  Proposal 1.3-2: OK.  Proposal 1.3-3: OK. |
| Ericsson | Proposal 1.3-1: We still don't see the benefit of this optimization, and it seems like there is not a clear majority.  Proposal 1.3-2: The 96 RBs in the FFS are dependendent on Proposal 1.3-1  Proposal 1.3-3: We think a much simpler solution is to use the existing table 13-12 "as is" and simplify modify the associated procedure text that says :  the UE determines an index of slot  as  that is in a frame with system frame number  by replacing /mu with /mu – 2 for 480 kHz and by /mu – 3 for 960 kHz. This preserves the relative timing of the SSB beam sweep and the Type0-PDCCH monitoring locations for 120 kHz. |
| Huawei, HiSilicon | **Proposal 1.3-1)** Support.  **Proposal 1.3-2)** At this stage, we prefer to support only the first three rows of the Table  (mux pattern, number of RB, number of symbol) = {(1, 24, 2), (1, 48, 1), (1, 48, 2)}. First, according to WID, “Prioritize support SSB-CORESET#0 multiplexing pattern 1. Other patterns discussed on a best effort basis”. So, we don’t see the urgency of supporting Mux 3 combinations when many other aspects of initial access design are not agreed yet. Note that, if possible, we should avoid supporting unnecessary (mux pattern, number of RB, number of symbol) tuples which results in using all four bits of ‘controlResourceSetZero’ while, in other initial access discussion, a major challenge is how to repurpose a bit in MIB for shared spectrum access purposes. |

#### **2nd Round Discussion Summary:**

The following is a summary of company preference for Proposal 1.3-1, 1.3-2A, and 1.3-3. Proposal 1.3-2 has been edited to reformulate the FFS.

**Proposal 1.3-1)**

* Support inclusion of 96 PRB CORESET#0 with appropriate RB offset for {120 kHz, 120 kHz} = {SSB,PDCCH} case to ‘controlResourceSetZero’ field of MIB
* Ok: vivo, Docomo, Spreadtrum, Nokia, Samsung, Intel, Apple, Qualcomm, Sharp, Samsung, Intel, Apple, Qualcomm, Sharp, Futurewei, Huawei/HiSilicon
* Not ok: LGE, Ericsson
* Maybe: ZTE/Sanechips

##### **Proposal 1.3-2A)**

* For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support the following set of parameters.

|  |  |  |
| --- | --- | --- |
| SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols |
| 1 | 24 | 2 |
| 1 | 48 | 1 |
| 1 | 48 | 2 |
| 3 | 24 | 2 |
| 3 | 48 | 2 |

* + - Note: the number of entries corresponding the same {mux pattern, number of RB, number of symbol} tuple (listed above) will depend on required RB offsets that needs to be supported based on channel and sync raster design.
  + FFS: addition of any the following set of parameters
    - {mux pattern, number of RB, number of symbol} = {1, 24, 3}
    - {mux pattern, number of RB, number of symbol} = {1, 96, 1}
    - {mux pattern, number of RB, number of symbol} = {1, 96, 2}
    - {mux pattern, number of RB, number of symbol} = {3, 96, 2}
* Ok: vivo, Docomo, Spreadtrum, ZTE/Sanechips, Samsung, Intel, Apple, Sharp, Futurewei
* Maybe: Nokia (reformulate FFS?), [LGE?], [Qualcomm (commented some config will exceed 400MHz)?] [Ericsson?]
* Not ok: Huawei/HiSilicon (decision on mux pattern 3 should be postponed)

##### **Proposal 1.3-3)**

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support the following set of parameters are supported for SS/PBCH block and CORESET multiplexing pattern 1:

|  |  |  |
| --- | --- | --- |
| Number of search space sets per slot |  | **First symbol index** |
| 1 | 1 | 0 |
| 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 1 | 2 | 0 |

* + - Note: the number of entries corresponding the same {number of SS per slot, M, first symbol index} tuple (listed above) will depend on supported ‘O’ for each tuple.
    - FFS: Values of supported ‘O’ and supported combination of ‘O’ and number of SS per slot, M, first symbol index} tuple.
* Ok: vivo, Docomo, Spreadtrum, Nokia, Samsung, Intel, Apple, Sharp, Futurewei
* Maybe: [LGE?]
* Not ok: Ericsson (use 13-12 as is)
* Defer: ZTE/Sanechips (discuss together with SSB pattern)

#### **3rd Round Discussion:**

Please provide further comments for Proposal 1.3-1, 1.3-2A, and 1.3-3.

A side note on comments regarding using the same entries as Table 13-8 and 13-12 except some parameters. From moderator’s understanding, the proposal in 1.3-2A and 1.3-3 are exactly the same entries except parameters, O and RB offset. If value of O is removed, we would just have duplicate entries which may or may not be needed depending on the value of RB offset and O. Therefore, the formulation in 1.3-2A and 1.3-3 are more appropriate. With that said, if the goal is to keep all the values the same, that is a different matter.

|  |  |
| --- | --- |
| Company | Comments |
| LG Electronics | **P 1.3-1)** Introduction of 96 PRBs seems optimization. It could be beneficial in limited cases in certain region (e.g., US) where transmit power is restricted for BW smaller than 100 MHz or in case that channel bandwidth is larger than 138.24 MHz. We should have a high bar to change MIB information and change of MIB is not the simple extension of FR2-1.  **P 1.3-2A and 1.3-3)** We have the different understanding with Moderator. These proposals don’t describe how many entries can be composed of. It may give an impression that eventually we can end up with more or less entries (compared to Tables 13-8 and 13-12). We prefer to keep the number of entries for each table same as in Rel-15 and some values can be replaced (or re-interpreted) if needed. |
| Samsung | We are ok with all the proposals.  FR2-2 is operating with much higher frequency and channel bandwidth, comparing to FR2-1. Increasing the number of RB for CORESET#0 is a natural consequence from our point of view. We don’t quite understand the motivation that we have to restrict everything from FR2-1. |
| Qualcomm | We are ok with all the proposals. However, it should be noted that some configurations exceed the UE minimum BW capability for that SCS |
| Sharp | We are fine with Proposal 1.3-1, 1.3-2A, and 1.3-3. |
| Intel | **Proposal 1.3-1)** – agree  **Proposal 1.3-2)** – agree  **Proposal 1.3-3) –** agree in principle. However, the use of position 7 will not work with SSB pattern D, as the CORESET will collide with SSBs. This is another reason to consider the new SSB pattern with gap. |
| DOCOMO | Support Proposal 1.3-1), Proposal 1.3-2A) and Proposal 1.3-3) |
| Apple | Ok with all these proposals. |
| ZTE, Sanechips | We are fine with Proposal 1.3-1) and Proposal 1.3-2A).  For Proposal 1.3-3), we still think it is related to SSB pattern design. If Proposal 1.2-1A for SSB pattern in section 2.1.2 is agreed, we think Proposal 1.3-3 can be accepted. But if other SSB patterns are adopted, the first symbol index in Proposal 1.3-3 may need to be revised. |
| Vivo | We are OK with all the proposals. The introduction of 96 PRBs in necessary for better coverage and OCB requirement. |
| Lenovo, Motorola Mobility | We are fine with Proposal 1.3-1, 1.3-2A, and 1.3-3. However, we also agree with Qualcomm that some configurations for mux pattern 3 may exceed the UE minimum BW capability for that SCS. |
| Nokia | Proposal 1.3-1): Support  Proposal 1.3-2A): In principle fine, but like note earlier not sure if it is mandatory to list the FFS options. But no strong view on this aspect.  Proposal 1.3-3): Support |
| Futurewei | OK with all the proposals. |
| InterDigital | Proposal 1.3-1: We also believe that the support of 96 RBs is not essential. Given the limited benefits, we prefer to deprioritize the support of 96 RBs in Rel-17.  Proposal 1.3-2: We are generally fine with the proposal, but, as Nokia mentioned, we prefer to revise the FFS bullet as follows:   * + FFS: addition of any ~~the following~~ set of parameters     - ~~{mux pattern, number of RB, number of symbol} = {1, 24, 3}~~     - ~~{mux pattern, number of RB, number of symbol} = {1, 96, 1}~~     - ~~{mux pattern, number of RB, number of symbol} = {1, 96, 2}~~     - ~~{mux pattern, number of RB, number of symbol} = {3, 96, 2}~~   Proposal 1.3-3: We agree with ZTE that this may be related to SSB pattern design. We can discuss the issue after SSB pattern in section 2.1.2 is agreed. |
| Huawei, HiSilicon | **Proposal 1.3-1):** Support  **Proposal 1.3-2A):** We still prefer to only support the first three rows and leave (Mux, #RB, #symbol)= (3, 24, 2) and (3, 48, 2) corresponding to Mux 3 as FFS, because:   * As Qualcomm pointed out (3, 24, 2) and (3, 48, 2) rows exceed the 400 MHz minimum BW for 960 kHz. Maybe (1, 24, 3) that is just in FFS would be more practical for 960 kHz. * According to WID, “Prioritize support SSB-CORESET#0 multiplexing pattern 1. Other patterns discussed on a best effort basis”. * We think that it is good to be conservative in using bits of ‘controlResourceSetZero’. Note that depending on the supported RB offsets, each supported tuples of (Mux, #RB, #symbol) may result in using 2 or 3 rows of the total available 16 rows of CORESET#0 Table. Supporting new tuples of (Mux, #RB, #symbol) can be done in the next two meetings too. This is quite an isolated design problem that does not impact other initial access aspects. |
| Moderator | @LG Electronics:  Regarding to keep the table as is with removal of RB offset and O values. Not sure how RAN1 conclude that we will have exactly the same number of entries when we don’t know what value RB offset will need to be supported or the O values. For example, because of channelization design RAN4, if we need 3 sets of RB offset per entry instead of 2, then moderator assumes we will need to discuss how many entries and how to support them, which may increase or decrease entries compared to Rel-15. So while I understand LGE’s concern, from moderator’s understanding the proposals describe doesn’t necessarily prohibit what LGE is proposing.  If the proposal is the keep number of entries to be identical, I think this could be discussed and agreed separately. |
| DOCOMO | Support all of Proposal 1.3-1), Proposal 1.3-4), Proposal 1.3-2B) and Proposal 1.3-3). We agree the latter two can be treated over email given the current atmosphere. |
| LG Electronics | Proposal 1.3-2B) and Proposal 1.3-3): According to Moderator’s comments, we can accept those proposals, for the sake of progress.  Proposal 1.3-4): Support, and support for 120 kHz as well.  Proposal 1.3-1): Support of 96 PRBs is not essential. |
| Ericsson | These are our comments prior to the 3rd round summary. I would be happy if you could take them into account in the 4th round:  Our general views on all of the proposals are:   * 96 RBs is an optimization, and can be de-prioritized for all SCSs * The WID is clear that mux pattern 1 should be prioritized, therefore mux pattern 3 should be de-prioritized * 3 symbol CORESET0 should be de-prioritized   Based on this, we think the focus should be on a working design using the existing Tables 13-8 and 13-12, and if possible support common tables for all SCSs. In fact, we think that we could make a working assumption on the existing tables, and if the SSB-CORESET0 offsets need to be revised, or additional ones need to be added, that can be done once RAN4 concludes on channelization design. We prefer that approach rather than building the tables from ground up.  If that is not agreeable, then our view on building the tables up from the 3 proposals is as follows, and this is based on keeping a very narrow scope on the remaining design work as was deemed necessary in the RAN plenary. We have 2 meetings left.  **Proposal 1.3-1**  Do not support  **Proposal 1.2-2A**   * For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,   + Support the following set of parameters.  |  |  |  | | --- | --- | --- | | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | | 1 | 24 | 2 | | 1 | 48 | 1 | | 1 | 48 | 2 | | ~~3~~ | ~~24~~ | ~~2~~ | | ~~3~~ | ~~48~~ | ~~2~~ |  * + - Note: the number of entries corresponding the same {mux pattern, number of RB, number of symbol} tuple (listed above) will depend on required RB offsets that needs to be supported based on channel and sync raster design. * For the existing FR2 {mux pattern, number of RB, number of symbol} values = {3, 24, 2} and {3,48,2}, required SSB-CORESET0 offsets are specified on a best-effort-basis   + ~~FFS: addition of any the following set of parameters~~     - ~~{mux pattern, number of RB, number of symbol} = {1, 24, 3}~~     - ~~{mux pattern, number of RB, number of symbol} = {1, 96, 1}~~     - ~~{mux pattern, number of RB, number of symbol} = {1, 96, 2}~~     - ~~{mux pattern, number of RB, number of symbol} = {3, 96, 2}~~   **Proposal 1.2-3**   * For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, down-select from the following two alternatives: * Alt-1   + Support the following set of parameters are supported for SS/PBCH block and CORESET multiplexing pattern 1:  |  |  |  | | --- | --- | --- | | Number of search space sets per slot |  | **First symbol index** | | 1 | 1 | 0 | | 2 | 1/2 | {0, if  is even}, {7, if  is odd} | | 2 | 1/2 | {0, if  is even}, {, if  is odd} | | 1 | 2 | 0 |  * + - Note: the number of entries corresponding the same {number of SS per slot, M, first symbol index} tuple (listed above) will depend on supported ‘O’ for each tuple.     - FFS: Values of supported ‘O’ and supported combination of ‘O’ and number of SS per slot, M, first symbol index} tuple. * Alt-2   + Adopt same table 13-12 for 120/480/960 kHz SCS. For 480 and 960 kHz, re-interpret offsets as O = O\_from\_table/4 and O = O\_from\_table/8, respectively. |
| Huawei, HiSilicon | **Proposal 1.3-1)** Support**Proposal 1.3-4)** We cannot support this proposal. We are not sure if we correctly understand the purpose of this proposal. Why the number of valid entries of ‘controlResourceSetZero’ configuration and ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, should be the same as Table 13-8 and Table 13-12 in TS38.213 v16.6.0 (8 and 14, respectively)? What we need to agree is that ‘controlResourceSetZero’ and ‘searchSpaceZero’ should not occupy more than 4 bits in MIB (which we assume that everyone agrees on as it was not a subject of debate so far). Other than that, we should discuss which ‘controlResourceSetZero’ configurations and which ‘searchSpaceZero’ configurations would make sense for 480 and 960 kHz. The number of supported configurations for ‘controlResourceSetZero’ may be concluded to be 8, less, or more than 8(<=16). Similarly, the number of supported configurations for ‘searchSpaceZero’ may be concluded to be 14, less, or more than 14(<=16).  **Proposal 1.3-3)** We can agree with this proposal if the third row removed. The third row configures two search spaces associated with two different SSB indexes (generally with two different beams) on adjacent symbols. It means that UE should switch its beam without a beam switching gap to search for CORESET#0 of SSB i and SSB i+1. Further, if SSB i is configured in the second symbol (current strong majority), third row would mean that CORESET#0 of SSB i is configured in symbol 0, CORESET#0 of SSB i+1 is configured in symbol 1, and SSB i is transmitted starting from symbol 2. This requires two beamswitches 1->2->1 on three adjacent symbols in 960 or 480 kHz which we don’t think is practical.   * For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,   + Support the following set of parameters are supported for SS/PBCH block and CORESET multiplexing pattern 1:  |  |  |  | | --- | --- | --- | | Number of search space sets per slot |  | **First symbol index** | | 1 | 1 | 0 | | 2 | 1/2 | {0, if  is even}, {7, if  is odd} | | ~~2~~ | ~~1/2~~ | ~~{0, if  is even}, {, if  is odd}~~ | | 1 | 2 | 0 |  * + - Note: the number of entries corresponding the same {number of SS per slot, M, first symbol index} tuple (listed above) will depend on supported ‘O’ for each tuple.     - FFS: Values of supported ‘O’ and supported combination of ‘O’ and number of SS per slot, M, first symbol index} tuple. |
| CATT | **Proposal 1.3-2B) : Prefer not support** (Mux, #RB, #symbol)= (3, 24, 2) and (3, 48, 2) corresponding to Mux 3. These can be FFS |
| InterDigital | Proposal 1.3-1 Our previous concern on this proposal is not properly captured. We also believe that support of 96 RBs is not essential.  Proposal 1.3-2B We are fine with the proposal.  Proposal 1.3-3: As mentioned, we prefer to discuss this issue after SSB pattern in section 2.1.2 is agreed. |
| Sharp | We are fine with Proposal 1.3-1 for the sake of progress.  Regarding Proposal 1.3-4, we are either not clear on why the number of valid entries (instead of the number of entries) should be kept the same. |
| ZTE, Sanechips | We are fine with Proposal 1.3-1) and Proposal 1.3-2B)-clean up.  For Proposal 1.3-4), we expect more clarifications on why we should make such restrictions, but we are open for it.  For Proposal 1.3-3), we still think it is related to SSB pattern design. It should be decided after SSB pattern design discussed in section 2.1.2 is concluded. |
| Lenovo, Motorola Mobility | We support Proposal 1.3-1 andProposal 1.3-4). We agree with Ericson to prioritize the proposal only for mux pattern 1 and deprioritize for mux pattern 3. Especially in our view, the suggested entries for mux pattern 3 will exceed min channel bandwidth requirements. Therefore, we agree with the suggested changes by Ericson for Proposal 1.3-2B. |
| Nokia | Proposal 1.3-1): We are still OK with this proposal.  Proposal 1.3-4): Like commented also by Huawei, I don’t know if read the proposal correctly, but to me it seems also to suggest that we would have on 8 entries for number of RBs, symbols and (frequency) offsets and 14 entries for monitoring occasions. Now in my understanding we have not yet concluded if more (frequency) offsets are need even of 120kHz case, thus it would be bit premature to take this step.  Proposal 1.3-2B): We are fine with the proposal, but also OK to consider multiplexing pattern 3 later.  Proposal 1.3-3): We are OK in principle with the proposal, as noted earlier, it has a good symmetry with the SSB pattern considered. As per case with first symbol index set as ‘{0, if  is even}, {, if  is odd}’, we are fine to consider this later if companies feel strongly about it. |
| Intel | We support all Proposals 1.3-1), 1.3-2B), 1.3-3). In Proposal 1.3-2B), the entries corresponding to mux Pattern 3 could be left FFS if this means getting further progress.  We don’t agree with 1.3-4 as values of RB offset cannot be determined yet (as channelization design is not complete in RAN4). We suggest leaving the total number of entries open, especially more so if mux pattern 3 is going to be left FFS as well. |

#### **3rd Round Discussion Summary:**

**Issue 1)** Inclusion of 96 PRB CORESET

Many companies seems to be ok with inclusion of 96PRB CORESET#0. At least one company still had reservations on the proposal, mentioned that support of 96 PRB CORESET#0 is an optimization and not something essential to be considered. Moderator suggest to discuss this in GTW.

**Proposal 1.3-1)**

* Support inclusion of 96 PRB CORESET#0 with appropriate RB offset for {120 kHz, 120 kHz} = {SSB,PDCCH} case to ‘controlResourceSetZero’ field of MIB
* Not ok: LGE, Interdigital, Ericsson
  + Main reasons for objection: support 96PRB is more of optimization and not essential

**Issue 2)** CORESET#0/Type0-PDCCH Configuration parameters for 480 and 960kHz.

Most companies seem to be ok with Proposal 1.3-2A and 1.3-3. Moderator has received comment from LGE that the currently formulation leaves door open for to discuss the exact number of entries for controlResourceSetZero and searchSpaceZero. However, that was the intentional as moderator understood that values of O and RB offset are FFS, and therefore not possible to conclude the number of entries. Moderator suggests to keep Proposal 1.3-2B and 1.3-3 as is, as it is a broader agreement, and have a separate proposal 1.3-4 to discuss the number of entries for controlResourceSetZero and searchSpaceZero.

**Proposal 1.3-2C)**

* For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support the following set of parameters.

|  |  |  |
| --- | --- | --- |
| SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols |
| 1 | 24 | 2 |
| 1 | 48 | 1 |
| 1 | 48 | 2 |
| ~~3~~ | ~~24~~ | ~~2~~ |
| ~~3~~ | ~~48~~ | ~~2~~ |

* + - Note: the number of entries corresponding the same {mux pattern, number of RB, number of symbol} tuple (listed above) will depend on required RB offsets that needs to be supported based on channel and sync raster design.
  + FFS: addition ~~of any the following~~ other set of parameters
    - ~~{mux pattern, number of RB, number of symbol} = {1, 24, 3}~~
    - ~~{mux pattern, number of RB, number of symbol} = {1, 96, 1}~~
    - ~~{mux pattern, number of RB, number of symbol} = {1, 96, 2}~~
    - ~~{mux pattern, number of RB, number of symbol} = {3, 96, 2}~~

**Proposal 1.3-3A)**

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support the following set of parameters are supported for SS/PBCH block and CORESET multiplexing pattern 1:

|  |  |  |
| --- | --- | --- |
| Number of search space sets per slot |  | **First symbol index** |
| 1 | 1 | 0 |
| 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 1 | 2 | 0 |

* + - Note: the number of entries corresponding the same {number of SS per slot, M, first symbol index} tuple (listed above) will depend on supported ‘O’ for each tuple.
    - For the support values of ‘O’ (as part of supported combination of {‘O’, number of SS per slot, M, first symbol index} tuple support either Alt 1, 2, or 3
      * Alt 1:
        + Adopt same Table 13-12 for 120/480/960 kHz SCS
      * Alt 2:
        + Adopt same Table 13-12 for 120 kHz SCS. For 480 and 960 kHz, re-interpret offsets as O = O’/4 and O = O’/8, respectively, where O’ are values of O from Table 13-12.
      * Alt 3:
        + Option not covered by Alt 1 and 2.
    - ~~FFS: Values of supported ‘O’ and supported combination of ‘O’ and number of SS per slot, M, first symbol index} tuple.~~

**Proposal 1.3-4)**

* The number of valid entries ‘controlResourceSetZero’ configuration and ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, is the same as Table 13-8 and Table 13-12 in TS38.213 v16.6.0

There were few companies that are not ok with Proposal 1.3-4.

#### **4th Round Discussion:**

Moderator suggests continuing discussion on Proposal 1.3-1 and 1.3-4.

**Proposal 1.3-1)**

* Support inclusion of 96 PRB CORESET#0 with appropriate RB offset for {120 kHz, 120 kHz} = {SSB,PDCCH} case to ‘controlResourceSetZero’ field of MIB

##### **Proposal 1.3-4)**

* The number of valid entries ‘controlResourceSetZero’ configuration and ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, is the same as Table 13-8 and Table 13-12 in TS38.213 v16.6.0

While Proposal 1.3-2C and 1.3-3A is somewhat stable, if there are additional comments, please provide them. Once the proposals are stable, moderator will suggest for approval over email.

**Proposal 1.3-2C)**

* For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support the following set of parameters.

|  |  |  |
| --- | --- | --- |
| SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols |
| 1 | 24 | 2 |
| 1 | 48 | 1 |
| 1 | 48 | 2 |

* + - Note: the number of entries corresponding the same {mux pattern, number of RB, number of symbol} tuple (listed above) will depend on required RB offsets that needs to be supported based on channel and sync raster design.
  + FFS: addition other set of parameters

##### **Proposal 1.3-3A)**

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support the following set of parameters are supported for SS/PBCH block and CORESET multiplexing pattern 1:

|  |  |  |
| --- | --- | --- |
| Number of search space sets per slot |  | **First symbol index** |
| 1 | 1 | 0 |
| 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 1 | 2 | 0 |

* + - Note: the number of entries corresponding the same {number of SS per slot, M, first symbol index} tuple (listed above) will depend on supported ‘O’ for each tuple.
    - For the support values of ‘O’ (as part of supported combination of {‘O’, number of SS per slot, M, first symbol index} tuple support either Alt 1, 2, or 3
      * Alt 1:
        + Adopt same Table 13-12 for 120/480/960 kHz SCS
      * Alt 2:
        + Adopt same Table 13-12 for 120 kHz SCS. For 480 and 960 kHz, re-interpret offsets as O = O’/4 and O = O’/8, respectively, where O’ are values of O from Table 13-12.
      * Alt 3:
        + Option not covered by Alt 1 and 2.

Please provide further comments on above issues.

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | **Proposal 1.3-1)** We support the proposal. **Proposal 1.3-4)** We don’t agree with the proposal for ‘controlResourceSetZero’ configuration. Whether the number of valid entries for ‘controlResourceSetZero’ configuration is same among 120/480/960 kHz depends on the required number of RB offsets, but so far the sync raster design is not clear yet, so it’s too pre-mature to conclude the number of valid entries can be the same. We are ok with the statement for Type0-PDCCH configuration. **Proposal 1.3-2C)** Support. **Proposal 1.3-3A)** We don’t think the scaling method in Alt 2 is correct. O can be {0, 2.5, 5, 7.5} in current supported table, and 0 and 5 are the baseline values to guarantee same half frame operation with associated SSB, and should be scaled by SCS. 2.5 and 7.5 offsets are mainly used for consecutive transmission of broadcast channel burst and SSB burst, e.g. for 240 kHz SCS, the SSB burst duration is roughly 2.5 ms. In this sense, this 2.5 ms should be scaled down according the SCS. More precisely, we propose the following alternative:   * Alt 3: O is from the set {0, 5, 2.5, 7.5} for 120 kHz, {0, 5, 2.5/2, 5+2.5/2} for 480 kHz, and {0, 5, 2.5/4, 5+2.5/4} for 960 kHz. |
| Qualcomm | Proposal 1.3-1: fine Proposal 1.3-4: do not support. Still early for such agreements. It makes more sense to agree not to exceed the number bits  Proposal 1.3-2C: fine, but prefer to re-insert mux pattern 3  Proposal 1.3-3A: we agree with Samsung comments, may be something like **this**:   * Alt 2:   + Adopt same Table 13-12 for 120 kHz SCS. For 480 and 960 kHz, re-interpret offsets as O = O’/**X1** and O = O’/**X2**, respectively, where O’ are values of O from Table 13-12.     - **FFS for X1 and X2**     - **FFS on where it applies to all O’ values or some subset of O’ values** |
| Lenovo, Motorola Mobility | Proposal 1.3-1): supportProposal 1.3-4): supportProposal 1.3-2C): supportProposal 1.3-3A): We support the proposal with suggested changes for Alt 2 by Qualcomm. |
| Futurewei | Proposal 1.3-1): supportProposal 1.3-4): we prefer to postpone discussion after more design decisions are agreed.Proposal 1.3-2C): supportProposal 1.3-3A): We support the proposal, fine with Qualcomm clarification for Alt 2. |
| Sharp | Proposal 1.3-1): supportProposal 1.3-4): FFSProposal 1.3-2C): supportProposal 1.3-3A): Support in principle and fine with Qualcomm’s suggestion on Alt 2. |
| Ericsson | Proposal 1.3-1): Do not support. This is an optimization.Proposal 1.3-4): Too early to decide this. The required SSB-CORESET0 offsets depend on the RAN4 sync raster design, and we don't know that yet.Proposal 1.3-2C): SupportProposal 1.3-3A): Support the proposal with the generalized revision of Alt-2 suggested by Qualcomm. Furthermore, we don't think Alt-3 is useful (this is equivalent "other options not precluded"). Let's try to focus the solutions. |
| LG Electronics | Proposal 1.3-1): Support of 96 PRBs is not essential. Proposal 1.3-4): We are OK to defer the decision on CORESET#0 configuration considering RB offset values but at least we can keep the same number of entries for type0-PDCCH CSS set configuration.  Proposal 1.3-2C): Support  Proposal 1.3-3A): We are fine with Qualcomm’s modification |
| ZTE, Sanechips | Proposal 1.3-1): supportProposal 1.3-4): The decision/discussion can be postponed. We don't think we need to make a decision when some other parameter configurations (e.g. RB offset, SS configuration) are still uncertain. Further, we don't understand why they need to be kept the same as in Rel-16.Proposal 1.3-2C): support Proposal 1.3-3A): We are fine with Qualcomm’s modification. |
| InterDigital | Proposal 1.3-1): Support the proposal.Proposal 1.3-4): Support the proposal.Proposal 1.3-2C): Support the proposal.Proposal 1.3-3A): We share the same concern as Samsung and Qualcomm. We support the suggested version of Alt2 from Qualcomm. |
| Nokia | Proposal 1.3-1): Still OK. Proposal 1.3-4): Like commented earlier, we don’t support this proposal.  Proposal 1.3-2C): OK  Proposal 1.3-3A): We are OK with the proposal. |
| Intel | **Proposal 1.3-1)** – Support. **Proposal 1.3-4)** – Do not support. RB offset values depend on sync raster design which is still under discussion in RAN4.  **Proposal 1.3-2C)** – Support. **Proposal 1.3-3A)** – Support. We are supportive of considering Samsung’s addition or something along the line of Samsung’s addition to replace Alt 3. We are also Qualcomm’s modification for Alt 2. |
| DOCOMO | Proposal 1.3-1): supportProposal 1.3-4): Seems premature to agree this.Proposal 1.3-2C): supportProposal 1.3-3A): We are fine with the proposal with suggested changes for Alt 2 by Qualcomm. |
| Huawei, HiSilicon | **Proposal 1.3-1):** Support. **Proposal 1.3-4):** Not support.  As we discussed in earlier rounds, We are not sure why the number of valid entries of ‘controlResourceSetZero’ configuration and ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, should be the same as Table 13-8 and Table 13-12 in TS38.213 v16.6.0 (8 and 14, respectively). What we need to agree is that ‘controlResourceSetZero’ and ‘searchSpaceZero’ should not occupy more than 4 bits in MIB (which we assume that everyone agrees on as it was not a subject of debate so far). Other than that, we should discuss which ‘controlResourceSetZero’ configurations and which ‘searchSpaceZero’ configurations would make sense for 480 and 960 kHz. The number of supported configurations for ‘controlResourceSetZero’ may be concluded to be 8, less, or more than 8(<=16). Similarly, the number of supported configurations for ‘searchSpaceZero’ may be concluded to be 14, less, or more than 14(<=16).  **Proposal 1.3-2C)** Support  **Proposal 1.3-3A)** As discussed in earlier rounds, the third row of the Table configures two search spaces associated with two different SSB indexes (generally with two different beams) on adjacent symbols. It means that UE should switch its beam without a beam switching gap to search for CORESET#0 of SSB i and SSB i+1. Further, if SSB i is configured in the second symbol, third row would mean that CORESET#0 of SSB i is configured in symbol 0, CORESET#0 of SSB i+1 is configured in symbol 1, and SSB i is transmitted starting from symbol 2. This requires two beamswitches 1->2->1 on three adjacent symbols in 960 or 480 kHz which we don’t think is practical.  Further, we don’t understand the technical reason behind Alt 1 and Alt 2. Adopting the same Table as in Rel-16 for 480/960 means very long delay (up to 7.5\*64 = 480 slots for 960 kHz and 7.5 \* 32 = 240 slots for 480 kHz) between SSB and the Type0-PDCCH CSS. Supporting up to (240) 480 slots delay between SSB and the corresponding Type0-PDCCH CSS for (480) 960 kHz is certainly at odds with the very reason (higher throughput/ lower latency) that higher SCSs are used for. Alt 2 reduces this latency by a factor of 4 or 8 but we still believe that the maximum latency of 240/4 = 480/8=60 slots for 480 and 960 kHz is too much. This is equal to the maximum value of latency for 120 kHz but, in our view, even 60 slots latency for 120 kHz is too much although it is supported in the spec.  We can support Proposal 1.3-3A with these changes:   * For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,   + Support the following set of parameters are supported for SS/PBCH block and CORESET multiplexing pattern 1:  |  |  |  | | --- | --- | --- | | **Number of search space sets per slot** |  | **First symbol index** | | 1 | 1 | 0 | | 2 | 1/2 | {0, if  is even}, {7, if  is odd} | | 2 | 1/2 | {0, if  is even}, {, if  is odd} | | 1 | 2 | 0 |  * + - Note: the number of entries corresponding the same {number of SS per slot, M, first symbol index} tuple (listed above) will depend on supported ‘O’ for each tuple.     - ~~For the support values of ‘O’ (as part of supported combination of {‘O’, number of SS per slot, M, first symbol index} tuple support either Alt 1, 2, or 3~~       * ~~Alt 1:~~          + ~~Adopt same Table 13-12 for 120/480/960 kHz SCS~~       * ~~Alt 2:~~          + ~~Adopt same Table 13-12 for 120 kHz SCS. For 480 and 960 kHz, re-interpret offsets as O = O’/4 and O = O’/8, respectively, where O’ are values of O from Table 13-12.~~       * ~~Alt 3:~~         + ~~Option not covered by Alt 1 and 2.~~ |

#### **4th Round Discussion Summary:**

The following is a summary of company views.

**Proposal 1.3-1)**

* Support inclusion of 96 PRB CORESET#0 with appropriate RB offset for {120 kHz, 120 kHz} = {SSB,PDCCH} case to ‘controlResourceSetZero’ field of MIB
* Support: Samsung, Qualcomm, Lenovo/Motorola Mobility, Sharp, Intel, Docomo, Huawei/HiSilicon
* Not ok: Ericsson, LGE

##### **Proposal 1.3-4)**

* The number of valid entries ‘controlResourceSetZero’ configuration and ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, is the same as Table 13-8 and Table 13-12 in TS38.213 v16.6.0
* Support: Lenovo/Motorola Mobility
* Not ok: Samsung (for controlResourceSetZero), Qualcomm, Intel, Huawei/HiSilicon
  + Reasons
    - Number of RB offsets requires has not yet been determined
* Defer decision: Futurewei, Sharp, Ericsson, Docomo

All companies were ok with Proposal 1.3-2C. While moderator understands that some companies wished to get further progress and also agree to other parameters sets (96, mux pattern 3, etc), it would good for RAN1 to make progress by agreeing to parameters sets that all companies agree to.

**Proposal 1.3-2C)**

* For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support the following set of parameters.

|  |  |  |
| --- | --- | --- |
| SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols |
| 1 | 24 | 2 |
| 1 | 48 | 1 |
| 1 | 48 | 2 |

* + - Note: the number of entries corresponding the same {mux pattern, number of RB, number of symbol} tuple (listed above) will depend on required RB offsets that needs to be supported based on channel and sync raster design.
  + FFS: addition other set of parameters
* Support: Samsung, Qualcomm, Lenovo/Motorola Mobility, Sharp, Ericsson, LGE, Intel, Docomo, Huawei/HiSilicon
* Not ok:

Moderator has updated Proposal 1.3-3A to 1.3-3B based on comments received. As for Qualcomm’s update compared with what Samsung suggested, moderator realized that they are not completely the same. Qualcomm’s update for Alt 2 is changes to the scaling of the offset value O, whereas Samsung’s suggestion is to consider scaling on top of offset value. So moderator has listed them into different alternatives. With the addition of different alternative 1, 2, and 3, moderator is wondering if the proposal is ok for Huawei, who had expressed concerns on the proposal.

**Proposal 1.3-3B)**

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support the following set of parameters are supported for SS/PBCH block and CORESET multiplexing pattern 1:

|  |  |  |
| --- | --- | --- |
| Number of search space sets per slot |  | **First symbol index** |
| 1 | 1 | 0 |
| 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| ~~2~~ | ~~1/2~~ | ~~{0, if  is even}, {, if  is odd}~~ |
| 1 | 2 | 0 |

* + - Note: the number of entries corresponding the same {number of SS per slot, M, first symbol index} tuple (listed above) will depend on supported ‘O’ for each tuple.
    - For the support values of ‘O’ (as part of supported combination of {‘O’, number of SS per slot, M, first symbol index} tuple support either Alt 1, 2, or 3
      * Alt 1:
        + Adopt same Table 13-12 for 120/480/960 kHz SCS
      * Alt 2:
        + Adopt same Table 13-12 for 120 kHz SCS. For 480 and 960 kHz, re-interpret offsets as O = O’/~~4~~X1 and O = O’/~~8~~X2, respectively, where O’ are values of O from Table 13-12.

FFS for X1 and X2

FFS on whether it applied to all O’ values or some subset of O’ values

* + - * ~~Alt 3:~~
        + ~~Option not covered by Alt 1 and 2.~~
      * Alt 3: O is from the set {0, 5, 2.5, 5+2.5} for 120 kHz, {0, 5, 2.5/ X1, 5+2.5/ X1} for 480 kHz, and {0, 5, 2.5/ X2, 5+2.5/ X2} for 960 kHz.

FFS for X1 and X2

* Support: Samsung, Qualcomm, Lenovo/Motorola Mobility, Futurewei, Sharp, Ericsson, LGE, Interdigital, Intel, Docomo
* Not ok:
* Maybe: [Huawei/HiSilicon]

#### **5th Round Discussion – Part 1:**

Moderator would like to separate more stable proposal from proposal that may be more difficult to get consensus. From the looks of it Proposal 1.3-2C and 1.3-3B could be quite stable.

##### **Proposal 1.3-2C) – suggest for email approval**

* For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support the following set of parameters.

|  |  |  |
| --- | --- | --- |
| SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols |
| 1 | 24 | 2 |
| 1 | 48 | 1 |
| 1 | 48 | 2 |

* + - Note: the number of entries corresponding the same {mux pattern, number of RB, number of symbol} tuple (listed above) will depend on required RB offsets that needs to be supported based on channel and sync raster design.
  + FFS: addition other set of parameters

##### **Proposal 1.3-3B)**

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support the following set of parameters are supported for SS/PBCH block and CORESET multiplexing pattern 1:

|  |  |  |
| --- | --- | --- |
| Number of search space sets per slot |  | **First symbol index** |
| 1 | 1 | 0 |
| 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| ~~2~~ | ~~1/2~~ | ~~{0, if  is even}, {, if  is odd}~~ |
| 1 | 2 | 0 |

* + - Note: the number of entries corresponding the same {number of SS per slot, M, first symbol index} tuple (listed above) will depend on supported ‘O’ for each tuple.
    - For the support values of ‘O’ (as part of supported combination of {‘O’, number of SS per slot, M, first symbol index} tuple support either Alt 1, 2, or 3
      * Alt 1:
        + Adopt same Table 13-12 for 120/480/960 kHz SCS
      * Alt 2:
        + Adopt same Table 13-12 for 120 kHz SCS. For 480 and 960 kHz, re-interpret offsets as O = O’/X1 and O = O’/X2, respectively, where O’ are values of O from Table 13-12.

FFS for X1 and X2

FFS on whether it applied to all O’ values or some subset of O’ values

* + - * Alt 3: O is from the set {0, 5, 2.5, 5+2.5} for 120 kHz, {0, 5, 2.5/X1, 5+2.5/X1} for 480 kHz, and {0, 5, 2.5/X2, 5 + 2.5/X2} for 960 kHz.

FFS for X1 and X2

**Proposal 1.3-3C)**

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support the following set of parameters are supported for SS/PBCH block and CORESET multiplexing pattern 1:

|  |  |  |
| --- | --- | --- |
| Number of search space sets per slot |  | **First symbol index** |
| 1 | 1 | 0 |
| 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 1 | 2 | 0 |

* + - FFS: whether third row above needs to be updated to {0, if  is even}, {**+X**, if  is odd}, where X is X>= 0 and FFS
    - Note: the number of entries corresponding the same {number of SS per slot, M, first symbol index} tuple (listed above) will depend on supported ‘O’ for each tuple.
    - For the support values of ‘O’ (as part of supported combination of {‘O’, number of SS per slot, M, first symbol index} tuple support either Alt 1, 2, or 3
      * Alt 1:
        + Adopt same Table 13-12 for 120/480/960 kHz SCS
      * Alt 2:
        + Adopt same Table 13-12 for 120 kHz SCS. For 480 and 960 kHz, re-interpret offsets as O = O’/X1 and O = O’/X2, respectively, where O’ are values of O from Table 13-12.

FFS for X1 and X2

FFS on whether it applied to all O’ values or some subset of O’ values

* + - * Alt 3: O is from the set {0, 5, 2.5, 5+2.5} for 120 kHz, {0, 5, 2.5/X1, 5+2.5/X1} for 480 kHz, and {0, 5, 2.5/X2, 5 + 2.5/X2} for 960 kHz.

FFS for X1 and X2

Please comment on the proposal **only if you have serious concerns or have suggestions for change** (e.g. minor edits) that would help to get to agreement. Once stable, moderator will ask for email approval for the stable proposal.

|  |  |
| --- | --- |
| Company | Comments |
| Qualcomm | Proposal 1.3-2C: fine  Proposal 1.3-3B: may be the 3rd row setup makes sense to still have in some cases, may be better to keep as FFS for now and have something like:  FFS: {0, if  is even}, {**+X**, if  is odd}, where X>= 0 is FFS |
| LG Electronics | Proposal 1.3-2C): Support  Proposal 1.3-3B): We have a concern on the removed entry in the table. With 59 ns beam switching gap, gNB does not have any problem to switch TX beam 1🡪2🡪1. Furthermore, it is one of gNB’s choices, so we don’t need to reconsider that entry for 480/960 kHz SCS. |
| Samsung | We are ok with 1.3-2C.  For 1.3-3B, we don’t agree to remove a supported configuration in Rel-15 (actually that’s one of the most basic configurations in Rel-15, and supported for both FR1 and FR2) |
| Ericsson | **Proposal 1.3-2C)**  Support  **Proposal 1.3-3B)**  We object to modification of the 3rd row. Agree with Samsung. Furthermore, it seems this was suggested by Huawei based potential issue with UE beam switching time. But that doesn't make any sense. The UE would only monitor one of Type0-PDCCH positions corresponding to the detected SSB index. |
| ZTE, Sanechips | We are fine with Proposal 1.3-2C.  For Proposal 1.3-3B, we also think that the 3rd row should not be removed. We share similar view with Ericsson that there is no UE beam switching issue. |
| Nokia | Proposal 1.3-2C): We are OK.  Proposal 1.3-2B): We are OK to keep the third row in the table, but could consider also alternatively adding to the end if companies have a strong view:   * + FFS: addition other set of parameters |
| Huawei, Hisilicon | **Proposal 1.3-2C)** We support it.  **Proposal 1.3-3C)** We do not support it  **Proposal 1.3-3B)** We can only support it without the last bullet regarding the alternatives for the supported values of ‘O’. Here is our suggested proposal: **Proposal 1.3-3B)**  * For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,   + Support the following set of parameters are supported for SS/PBCH block and CORESET multiplexing pattern 1:  |  |  |  | | --- | --- | --- | | Number of search space sets per slot |  | **First symbol index** | | 1 | 1 | 0 | | 2 | 1/2 | {0, if  is even}, {7, if  is odd} | | ~~2~~ | ~~1/2~~ | ~~{0, if  is even}, {, if  is odd}~~ | | 1 | 2 | 0 |  * + - Note: the number of entries corresponding the same {number of SS per slot, M, first symbol index} tuple (listed above) will depend on supported ‘O’ for each tuple.     - FFS: Supported values of ‘O’     - ~~For the support values of ‘O’ (as part of supported combination of {‘O’, number of SS per slot, M, first symbol index} tuple support either Alt 1, 2, or 3~~       * ~~Alt 1:~~         + ~~Adopt same Table 13-12 for 120/480/960 kHz SCS~~       * ~~Alt 2:~~         + ~~Adopt same Table 13-12 for 120 kHz SCS. For 480 and 960 kHz, re-interpret offsets as O = O’/X1 and O = O’/X2, respectively, where O’ are values of O from Table 13-12.~~   ~~FFS for X1 and X2~~  ~~FFS on whether it applied to all O’ values or some subset of O’ values~~   * + - * ~~Alt 3: O is from the set {0, 5, 2.5, 5+2.5} for 120 kHz, {0, 5, 2.5/X1, 5+2.5/X1} for 480 kHz, and {0, 5, 2.5/X2, 5 + 2.5/X2} for 960 kHz.~~   ~~FFS for X1 and X2~~  The reason for removal of the Alternatives for ‘O’ is that, as explained in earlier rounds, adopting the same Table as in Rel-16 for 480/960 (Alt 1) means very long delay (up to 7.5\*64 = 480 slots for 960 kHz and 7.5 \* 32 = 240 slots for 480 kHz) between SSB and the Type0-PDCCH CSS. Supporting up to (240) 480 slots delay between SSB and the corresponding Type0-PDCCH CSS for (480) 960 kHz is certainly at odds with the very reason (higher throughput/ lower latency) that higher SCSs are used for. Alt 2 and Alt 3 reduce the (larger values of) latency by a factor of X1 or X2 which is a move in the right direction but we do not think we should support every row of Table 13-12 by taking the value of ‘O’ from a row the Table and just scale it down.  First note that Table 13-12 is for FR2 that is supposed to support all combinations of {SSB, CORESET#0} SCS = {240, 120}, {120, 120}, {240, 60}, and {120, 60} kHz and the number of supported PDCCH monitoring occasions for Type0-PDCCH CSS set may need to be higher than in FR2-2 in which SSB and CORESET#0 only have the same SCS. Second, we believe that a Type0-PDCCH CSS set monitoring occasions should either be in the same slot as the corresponding SSB or after the SSB burst to avoid CSS/SSB collision. We cannot see how this is taken into account in Alt 2 and Alt 3 and we need further detailed verifications before agreeing to these imited options.  **Regarding Ericsson comment:**  **“**We object to modification of the 3rd row. Agree with Samsung. Furthermore, it seems this was suggested by Huawei based potential issue with UE beam switching time. But that doesn't make any sense. The UE would only monitor one of Type0-PDCCH positions corresponding to the detected SSB index.”  **Huawei:**  In our view, third row should be removed not only because of beam switching problem at the UE but also the same problem at the gNB. We don’t think that gNB can beamswitch from Type0-PDCCH of SSB i in symbol 0 to Type0-PDCCH n of SSB i+1 in symbol 1 and then back to the transmission of SSB i in symbol 2. From UE side, A connected UE may need to perform RRM measurement on SSB i and also receive the adjacent Type0-PDCCH of SSB i+1 for ANR purposes or it may even have to receive Type0-PDCCH of SSB i and SSB i+1 that would be on adjacent symbols for the same ANR purpose. So, UE being required to perform two beam switching for Type0-PDCCH i, Type0-PDCCH i+1, SSB i on the first three symbols is not impossible in the third row is supported. |

#### **5th Round Discussion – Part 2:**

For proposal 1.3-4, its pretty clear several company have concerns on agreeing to this until further progress has been made on raster and other proposals. Therefore, moderator ask to discuss it once further progress has been made in RAN1 and RAN4.

For Proposal 1.3-1, there are still concerns from at least two companies on the inclusion of 96PRB.

##### **Proposal 1.3-1)**

* Support inclusion of 96 PRB CORESET#0 with appropriate RB offset for {120 kHz, 120 kHz} = {SSB,PDCCH} case to ‘controlResourceSetZero’ field of MIB
* Support: Samsung, Qualcomm, Lenovo/Motorola Mobility, Sharp, Intel, Docomo, Huawei/HiSilicon, vivo, ZTE/Sanechips
* Not ok: Ericsson, LGE

Updated proposal based on Samsung’s comments.

**Proposal 1.3-1A)**

* At the end of the WI, if the table for ‘controlResourceSetZero’ field of MIB still has enough number of reserved rows, support inclusion of 96 PRB CORESET#0 with appropriate RB offset for {120 kHz, 120 kHz} = {SSB,PDCCH} case to ‘controlResourceSetZero’ field of MIB

Please provide comments on any suggestions or comments that could move us forward.

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | We believe the benefit of adding 96 RBs has been discussed a lot, and maybe the following can be a way forward if the concern is the number of available rows in the table?   * At the end of the WI, if the table for ‘controlResourceSetZero’ field of MIB still has enough number of reserved rows, support inclusion of 96 PRB CORESET#0 with appropriate RB offset for {120 kHz, 120 kHz} = {SSB,PDCCH} case to ‘controlResourceSetZero’ field of MIB |
| Ericsson | We still view this an optimization, and should not be prioritize. If there are table rows left over after determining SSB-CORESET0 offsets, we can come back to it then. |
| vivo | We support the proposal and OK with Samsung’s proposal |
| ZTE, Sanechips | We are fine with the proposal and Samsung’s suggestion. |
| Moderator | I’ve added Proposal 1.3-1A based on Samsung’s comments. |
| Intel | Ok with Samsung’s proposal. |

#### **5th Round Discussion Summary:**

**Part 1 discussion)**

Proposal 1.3-2C is suggested to be approved over email. Moderator suggests checking whether Proposal 1.3-3C is acceptable.

**Proposal 1.3-3C)**

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support the following set of parameters are supported for SS/PBCH block and CORESET multiplexing pattern 1:

|  |  |  |
| --- | --- | --- |
| Number of search space sets per slot |  | **First symbol index** |
| 1 | 1 | 0 |
| 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 1 | 2 | 0 |

* + - FFS: whether third row above needs to be updated to {0, if  is even}, {**+X**, if  is odd}, where X is X>= 0 and FFS
    - Note: the number of entries corresponding the same {number of SS per slot, M, first symbol index} tuple (listed above) will depend on supported ‘O’ for each tuple.
    - For the support values of ‘O’ (as part of supported combination of {‘O’, number of SS per slot, M, first symbol index} tuple support either Alt 1, 2, or 3
      * Alt 1:
        + Adopt same Table 13-12 for 120/480/960 kHz SCS
      * Alt 2:
        + Adopt same Table 13-12 for 120 kHz SCS. For 480 and 960 kHz, re-interpret offsets as O = O’/X1 and O = O’/X2, respectively, where O’ are values of O from Table 13-12.

FFS for X1 and X2

FFS on whether it applied to all O’ values or some subset of O’ values

* + - * Alt 3: O is from the set {0, 5, 2.5, 5+2.5} for 120 kHz, {0, 5, 2.5/X1, 5+2.5/X1} for 480 kHz, and {0, 5, 2.5/X2, 5 + 2.5/X2} for 960 kHz.

FFS for X1 and X2

**Part 2 discussion)**

Samsung has provided a potential compromise for conclusion in Proposal 1.3-1A. Moderator suggest checking to see if this is ok.

**Proposal 1.3-1A)**

* At the end of the WI, if the table for ‘controlResourceSetZero’ field of MIB still has enough number of reserved rows, support inclusion of 96 PRB CORESET#0 with appropriate RB offset for {120 kHz, 120 kHz} = {SSB,PDCCH} case to ‘controlResourceSetZero’ field of MIB

#### **6th Round Discussion – part 1:**

Please provide further comments for Proposal 1.3-3C. If the proposal is stable, moderator would like to suggest the proposal to be approved over email.

##### **Proposal 1.3-3C) – potentially for email approval**

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support the following set of parameters are supported for SS/PBCH block and CORESET multiplexing pattern 1:

|  |  |  |
| --- | --- | --- |
| Number of search space sets per slot |  | **First symbol index** |
| 1 | 1 | 0 |
| 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 1 | 2 | 0 |

* + - FFS: whether third row above needs to be updated to {0, if  is even}, {**+X**, if  is odd}, where X is X>= 0 and FFS
    - Note: the number of entries corresponding the same {number of SS per slot, M, first symbol index} tuple (listed above) will depend on supported ‘O’ for each tuple.
    - For the support values of ‘O’ (as part of supported combination of {‘O’, number of SS per slot, M, first symbol index} tuple support either Alt 1, 2, or 3
      * Alt 1:
        + Adopt same Table 13-12 for 120/480/960 kHz SCS
      * Alt 2:
        + Adopt same Table 13-12 for 120 kHz SCS. For 480 and 960 kHz, re-interpret offsets as O = O’/X1 and O = O’/X2, respectively, where O’ are values of O from Table 13-12.

FFS for X1 and X2

FFS on whether it applied to all O’ values or some subset of O’ values

* + - * Alt 3: O is from the set {0, 5, 2.5, 5+2.5} for 120 kHz, {0, 5, 2.5/X1, 5+2.5/X1} for 480 kHz, and {0, 5, 2.5/X2, 5 + 2.5/X2} for 960 kHz.

FFS for X1 and X2

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | We are ok with the proposal. |
| Qualcomm | We are ok with the proposal. |
| Huawei, Hisilicon | **Proposal 1.3-3C)** We can only support it without the last bullet regarding the alternatives for the supported values of ‘O’ **and the third row removed** (or the original **1.3-3B** without the last bullet regarding the alternatives for the supported values of ‘O’). Here is our suggested proposal: **Proposal 1.3-3C)**  * For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,   + Support the following set of parameters are supported for SS/PBCH block and CORESET multiplexing pattern 1:  |  |  |  | | --- | --- | --- | | Number of search space sets per slot |  | **First symbol index** | | 1 | 1 | 0 | | 2 | 1/2 | {0, if  is even}, {7, if  is odd} | | ~~2~~ | ~~1/2~~ | ~~{0, if  is even}, {, if  is odd}~~ | | 1 | 2 | 0 |  * + - ~~FFS: whether third row above needs to be updated to {0, if  is even}, {~~**~~+X~~**~~, if  is odd}, where X is X>= 0 and FFS~~     - Note: the number of entries corresponding the same {number of SS per slot, M, first symbol index} tuple (listed above) will depend on supported ‘O’ for each tuple.     - FFS: Supported values of ‘O’     - ~~For the support values of ‘O’ (as part of supported combination of {‘O’, number of SS per slot, M, first symbol index} tuple support either Alt 1, 2, or 3~~       * ~~Alt 1:~~         + ~~Adopt same Table 13-12 for 120/480/960 kHz SCS~~       * ~~Alt 2:~~         + ~~Adopt same Table 13-12 for 120 kHz SCS. For 480 and 960 kHz, re-interpret offsets as O = O’/X1 and O = O’/X2, respectively, where O’ are values of O from Table 13-12.~~   ~~FFS for X1 and X2~~  ~~FFS on whether it applied to all O’ values or some subset of O’ values~~   * + - * ~~Alt 3: O is from the set {0, 5, 2.5, 5+2.5} for 120 kHz, {0, 5, 2.5/X1, 5+2.5/X1} for 480 kHz, and {0, 5, 2.5/X2, 5 + 2.5/X2} for 960 kHz.~~   ~~FFS for X1 and X2~~  The reason for removal of the Alternatives for ‘O’ is that, as explained in earlier rounds, adopting the same Table as in Rel-16 for 480/960 (Alt 1) means very long delay (up to 7.5\*64 = 480 slots for 960 kHz and 7.5 \* 32 = 240 slots for 480 kHz) between SSB and the Type0-PDCCH CSS. Supporting up to (240) 480 slots delay between SSB and the corresponding Type0-PDCCH CSS for (480) 960 kHz is certainly at odds with the very reason (higher throughput/ lower latency) that higher SCSs are used for. Alt 2 and Alt 3 reduce the (larger values of) latency by a factor of X1 or X2 which is a move in the right direction but we do not think we should support every row of Table 13-12 by taking the value of ‘O’ from a row the Table and just scale it down.  First note that Table 13-12 is for FR2 that is supposed to support all combinations of {SSB, CORESET#0} SCS = {240, 120}, {120, 120}, {240, 60}, and {120, 60} kHz and the number of supported PDCCH monitoring occasions for Type0-PDCCH CSS set may need to be higher than in FR2-2 in which SSB and CORESET#0 only have the same SCS. Second, we believe that a Type0-PDCCH CSS set monitoring occasions should either be in the same slot as the corresponding SSB or after the SSB burst to avoid CSS/SSB collision. We cannot see how this is taken into account in Alt 2 and Alt 3 and we need further detailed verifications before agreeing to these limited options.  **Regarding Ericsson comment:**  **“**We object to modification of the 3rd row. Agree with Samsung. Furthermore, it seems this was suggested by Huawei based potential issue with UE beam switching time. But that doesn't make any sense. The UE would only monitor one of Type0-PDCCH positions corresponding to the detected SSB index.”  **Huawei:**  In our view, third row should be removed not only because of beam switching problem at the UE but also the same problem at the gNB. We don’t think that gNB can beamswitch from Type0-PDCCH of SSB i in symbol 0 to Type0-PDCCH n of SSB i+1 in symbol 1 and then back to the transmission of SSB i in symbol 2 considering beam switching delay + MIMO TAE. From UE side, a connected UE may need to perform RRM measurement on SSB i and also receive the adjacent Type0-PDCCH of SSB i+1 for ANR purposes or it may even have to receive Type0-PDCCH of SSB i and SSB i+1 that would be on adjacent symbols for the same ANR purpose. So, UE being required to perform two beam switching for Type0-PDCCH i, Type0-PDCCH i+1, SSB i on the first three symbols is not impossible if the third row is supported. |

#### **6th Round Discussion – part 2:**

Samsung has provided a potential compromise for conclusion in Proposal 1.3-1A. Moderator suggest checking to see if this is ok.

##### **Proposal 1.3-1A)**

* At the end of the WI, if the table for ‘controlResourceSetZero’ field of MIB still has enough number of reserved rows, support inclusion of 96 PRB CORESET#0 with appropriate RB offset for {120 kHz, 120 kHz} = {SSB,PDCCH} case to ‘controlResourceSetZero’ field of MIB

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | We support the proposal. |
| Spreadtrum | Fine |
| Huawei, Hisilicon | We support the original Proposal **1.3-1** and do not support **1.3-1A)**  Currently, based on Proposal 1.3-2C) that we seem to have a consensus on, only three tuples of (Mux#, RB #, Symb #) are used.Even if for each tuple we use 2 different RB offsets, still 10 rows of the table remains. On the other hand, considering that Mux#1 should be prioritized according to the WID and 96 RB for 120 kHz is the only CORESET#0 size larger than 100 MHz (and can benefit from maximum gNB Tx power), we don’t see why it should be down prioritized so much so that even when 10 rows of the Table are available, cannot be supported yet. We would like to know which other combinations have higher priorities and why. |

#### **6th Round Discussion Summary:**

To be filled.

### 2.1.4 ANR/CGI Reporting Aspects

* From [4] Interdigital:
  + Consider introducing the parameters for the neighbor cell SIB1 related to CGI reporting, where the time and frequency allocations and the multiplexing patterns are (pre)configured in fixed settings.
* From [7] Samsung:
  + No need to support extra method for providing the CORESET#0/Type0-PDCCH configuration for ANR purpose.
* From [8] CATT:
  + There is no need to study additional method(s) to enable support to obtain neighbor cell SIB1 contents related to CGI reporting in Rel-17.
* From [17] OPPO:
  + For ANR design, RAN1 considers one of the two options
    - Option 1: RAN1 holds ANR discussion until RAN4 concludes the channelization, LBT bandwidth and sync raster relationship.
    - Option 2: RAN1 does not follow R16 baseline solution and redesign ANR.
* From [18] Qualcomm:
  + for ANR, do not consider additional methods (compared to current NR) to signal the NCGI

#### Summary of Contribution Discussions

The updated WID contains FFS on additional method(s) to enable support to obtain neighbor cell SIB1 contents related to CGI reporting.

Three companies mentioned there is no need to consider further, and two companies mentioned methods to support CGI reporting.

#### **1st Round Discussion:**

Further discuss on “FFS: additional method(s) to enable support to obtain neighbour cell SIB1 contents related to CGI reporting”.

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | We don’t think additional method for CGI reporting is needed.   * First, in the CGI reporting scenario, the serving operator may not have information on the configuration of CORESET#0/Type0-PDCCH of a neighboring operator, so the feasibility of the additional method (e.g. dedicated signaling) is concerned. * Secondly, even if the serving operator knows such CORESET#0/Type0-PDCCH configuration, the dedicated signaling can only provide the same information as the indication in the MIB, otherwise such SSB cannot be used as cell-defining SSB for the neighboring operator. * Lastly, the UE anyway needs to read MIB of the SSB from the neighboring cell, e.g. to acquire timing and other information in MIB, so there is no need to have an additional method to provide the CORESET#0/Type0-PDCCH configuration. |
| Qualcomm | Current NR support is enough and there may not be a need to have any additional methods to support signaling the NCGI |
| Fujitsu | We share the views that no additional signaling on top of MIB is needed for providing CORESET#0/Type0-PDCCH configuration. However, some enhancements on providing CORESET#0/Type0-PDCCH configuration by MIB of off-sync SSB may be needed.  In NR-U, the MIB of an off-sync SSB provides CORESET#0/Type0-PDCCH CSS set configuration based on a nominal SSB on the sync raster in the channel where the off-sync SSB is transmitted. It is feasible since each channel includes one and only one sync raster. But for FR2-2, the relation between channels and sync rasters may be different and thus enhancement for off-sync SSB may be needed. Considering that channels and sync rasters are still under discussion, this discussion point could be deprioritized at the current stage. |
| Mediatek | We don’t see the need for additional mechanism for CGI reporting. |
| Sharp | No need to further discuss additional methods. |
| Docomo | Agree no need to support additional functionality for CGI reporting. |
| ZTE, Sanechips | We do not think it is necessary to study additional method(s) (e.g. using dedicated signaling) to enable support to obtain neighbor cell SIB1 contents related to CGI reporting. But we agree that channelization and sync raster defined in Rel-17 above 52.6GHz may have some impact on the current supported method (i.e. using MIB configuration). RAN1 can discuss if some enhancements are needed after RAN4’s work on channelization and sync raster is completed. |
| Nokia | We don’t see a need for any additional methods related to CGI reporting |
| OPPO | We agree with no additional mechanism is needed. But we see an issue to use the R16 method in FR2.2 ANR. The main issue is that there is no 20MHz LBT bandwidth and a unique GSCN in the 20MHz LBT bandwidth. Thus, it is not clear how the UE can obtain the second offset as defined in TS 38.213. |
| LG Electronics | Current NR specification is enough to support ANR/CGI reporting and we don’t see the need to support additional methods for ANR/CGI reporting. |
| NEC | Agree no need to support additional functionality for CGI reporting. |
| Xiaomi | We don’t see the need for additional mechanism for CGI reporting. |
| Lenovo, Motorola Mobility | We also don’t see any need for additional mechanism for CGI reporting |
| Intel | Additional methods of CGI reporting seem to be optimization which could be de-prioritized at this moment |
| Futurewei | We do not see the need to support additional functionality for CGI reporting. |
| Ericsson | We don't see a need to introduce additional methods; the Rel-15 approach is sufficient.  One observation though: the special solution introduced in Rel-16 NR-U to allow an off-sync raster SSB will not work for Rel-17, since the Rel-16 approach required only a single sync raster point per channel, and a channel was well defined as 20 MHz. |
| CATT | We don’t see the need for additional mechanism. |
| Huawei/HiSilicon | Given the agreements reached in RAN 92-e, there is no need for any additional method. |

#### **1st Round Discussion Summary:**

Majority of the companies seems to think no further discussion is necessary.

#### **2nd Round Discussion:**

Moderator suggest to conclude to not discuss further in RAN1 #106-e. Please provide comments if you have different suggestion on this issue.

|  |  |
| --- | --- |
| Company | Comments |
| vivo | Support Moderator’s suggestion. |
| DOCOMO | Agree with Moderator’s suggestion. |
| Spreadtrum | We are fine for Moderator’s suggestion |
| LG Electronics | Agree with Moderator’s suggestion |
| ZTE, Sanechips | Support Moderator’s suggestion. |
| Samsung | Agree with Moderator’s assessment.  One further comment on the Rel-16 approach to be used for 60 GHz unlicensed band. Our understanding is, in Rel-16 NR-U band, the sync raster is sparse and CORESET#0 BW is close to channel bandwidth such that using default configuration in MIB could not allow flexible allocation of SSB in the channel, such that we designed the special mechanism of using a second offset to address this issue. If any of such restrictions does not hold, i.e., sync raster is not as sparse as single one in the channel, or CORESET#0 bandwidth is much smaller than channel bandwidth, Rel-15 mechanism (i.e. using default configuration in MIB) is sufficient. |
| Intel | Support the conclusion not to discuss. |
| NEC | Support Moderator’s suggestion. |
| Apple | Agree. |
| Qualcomm | Agree with Moderator’s suggestion. |
| Sharp | Agree. |
| Futurewei | Agree |
| Huawei, HiSilicon | Support. |

#### **2nd Round Discussion Summary:**

No summary was made by Moderator.

#### **3rd Round Discussion:**

Continue to provide inputs.

|  |  |
| --- | --- |
| Company | Comments |
| - | - |

None received during 3rd round.

#### **Final Discussion Summary:**

No additional comments were provided. Moderator assumes following conclusion is acceptable and no need to explicitly agree (in GTW) the follow conclusion as it should not impact further RAN1 work in RAN1 #106-e.

Moderator conclusion:

* De-prioritize and do not further discuss issue regarding “FFS: additional method(s) to enable support to obtain neighbour cell SIB1 contents related to CGI reporting” in RAN1 #106-e.

### 2.1.5 Various other aspects on SSB Design

* From [3] Spreadtrum:
  + SSB with 240kHz SCS can be down-prioritized.
  + Supporting initial cell selection with 480kHz SSB should be an optional UE capability separately from supporting other processing with 480/960kHz SCS.
* From [6] Lenovo/Motorola Mobility
  + For supporting NR from 52.6 GHz to 71 GHz in Rel. 17, with higher subcarrier spacings (numerologies), coverage enhancement of channels and signals used for initial access should be considered for NR beyond 52.6 GHz
* From [17] OPPO:
  + The raster step size for 120kHz and 480kHz are 3\*17.28MHz and 15\*17.28MHz, respectively, leading to a total number of raster entries 428.
* From [19] LG Electronics:
  + Discuss how to signal actually transmitted SSBs via ssb-PositionsInBurst when can be indicated to be less than 64 in MIB.
* From [27] Convida:
  + SSB coverage enhancement should be studied for higher SCS.

#### Summary of Contribution Discussions

* Companies have provided the following issues
  + Capability
    - Supporting initial cell selection with 480kHz SSB should be an optional UE capability separately from supporting other processing with 480/960kHz SCS.
  + Coverage enhancement
    - For supporting NR from 52.6 GHz to 71 GHz in Rel. 17, with higher subcarrier spacings (numerologies), coverage enhancement of channels and signals used for initial access should be considered for NR beyond 52.6 GHz
    - SSB coverage enhancement should be studied for higher SCS.
    - Note from Moderator: WID explicitly mentions “Note: coverage enhancement for SSB is not pursued.”, therefore not sure if this needs to be further discussed.
  + Raster
    - The raster step size for 120kHz and 480kHz are 3\*17.28MHz and 15\*17.28MHz, respectively, leading to a total number of raster entries 428.
  + ssb-PositionsInBurst
    - Discuss how to signal actually transmitted SSBs via ssb-PositionsInBurst when can be indicated to be less than 64 in MIB

#### **1st Round Discussion:**

Among the additional issues brought up, Moderator assumes that coverage aspects are excluded by the WID and raster issues are for discussion in RAN4 domain. Moderator suggest to further discuss on the two issues brought up.

* Initial cell selection capability for 480kHz
* Signaling for ssb-PositionsInBurst when is indicated.

If there are other issues that require further discussion, please comment here as well.

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | * The capability of 480 kHz for initial access can be discussed in a later phase of the WI (anyway do not impact RAN1 progress). * The indication and interpretation of ssb-PositionsInBurst can be discussed later when the DBTW is finalized. |
| ZTE, Sanechips | We share same views as Samsung on above two issues. |
| Nokia | In our understanding the initial cell selection capability (if any) should be handled as a part of the UE capability discussions as per WID:  “Note: Dependency or lack thereof for a UE supporting 480kHz and/or 960kHz numerology for data and control to also support 480kHz SSB numerology for initial access is to be tackled as part of UE capability discussion.” |
| OPPO | Agree with Samsung |
| LG Electronics | Same view with Samsung |
| Lenovo, Motorola Mobility | Similar view as of Samsung |
| Intel | Defer the discussion on these points |
| Futurewei | We agree that these points can be discuss later. |
| Ericsson | Defer |
| CATT | Ok to defer |
| InterDigital | Fine to defer |
| Huawei/HiSilicon | * As Nokia pointed out, given the referred note from RAN 92-e, “Initial cell selection capability for 480kHz” should be discussed as a part of UE capability discussion.   In our view, interpretation of *ssb-PositionsInBurst* when is indicated can be discussed in this meeting. |
| Convida Wireless | We are ok to defer the discussions for this. |

#### **1st Round Discussion Summary:**

Several companies think the issues are with lower priority compared to other issues. Suggestion to continue discussion but treat the issue with lower priority during GTW sessions.

#### **2nd Round Discussion:**

Please continue to provide comments as in 1st round discussions.

|  |  |
| --- | --- |
| Company | Comments |
| vivo | Fine to defer |
| Intel | Support moderator’s suggestions after the 1st round of discussions. |
| Qualcomm | Fine to defer |
| Futurewei | Agree to defer. |

#### **2nd Round Discussion Summary:**

No summary was made by Moderator.

#### **3rd Round Discussion:**

Continue to provide inputs.

|  |  |
| --- | --- |
| Company | Comments |
| - | - |

No further comments received.

#### **Final Discussion Summary:**

No additional comments were provided. Moderator assumes following conclusion is acceptable and no need to explicitly agree (in GTW) the follow conclusion as it should not impact further RAN1 work in RAN1 #106-e.

Moderator conclusion:

* De-prioritize discussion on regarding the following issues in RAN1 #106-e. Discussion can continue once other issues have been resolved.
  + Initial cell selection capability for 480kHz
  + Signaling for ssb-PositionsInBurst when is indicated.

## 2.2 PRACH Aspects

### 2.2.1 PRACH Sequence and Format

* From [2] vivo:
  + Support 120KHz and 480KHz as candidate SCS of initial UL BWP.
  + Support 480KHz and 960KHz SCS in addition to 120KHz SCS for PRACH.
* From [7] Samsung:
  + Support short PRACH format for all PRACH sequence lengths and all SCSs , and don’t support long PRACH format.
* From [8] CATT:
  + Consider supporting increasing symbols in time domain to enhance PRACH coverage.
  + Consider repeating and concatenating the PRACH preamble sequence to enhance PRACH coverage for unlicensed spectrum operation.
* From [9] ZTE/Sanechips:
  + Support PRACH with additional SCSs (480 kHz and/or 960 kHz) for both initial and non-initial access cases.
  + For 480kHz and 960kHz, reuse the same RO configuration table as in Rel-15/16 with the same RO density for 120kHz PRACH.
* From [11] Ericsson:
  + For PRACH with 960 kHz SCS for non-initial access use cases, L = 139 is supported, and L = 571 and 1151 are not supported.
  + For 480 kHz SCS for both initial access and non-initial access use cases, L = 139 is supported, and L = 1151 is not supported. It can be further discussed whether or not L = 571 is supported.
* From [12] Futurewei:
  + For initial access and non-initial access use cases, support 120kHz PRACH SCS with sequence length L=571, 1151 (in addition to L=139) for PRACH Formats A1~A3, B1~B4, C0, and C2.
  + For non-initial access use cases, support 480 and 960 kHz PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively.
* From [13] Nokia/NSB:
  + Support L=571 for PRACH with 480kHz.
* From [18] Qualcomm:
  + consider only using PRACH sequence length = 139 for SCS = 480 kHz and 960 kHz
* From [19] LG Electronics:
  + The 120 kHz PRACH SCS with sequence lengths L=571 and L=1151 are not required for the licensed spectrum where the regulatory requirements are not defined on PSD limit.
  + PRACH only with sequence length L=139 is supported for the 480 kHz SCS for initial/non-initial access and 960 kHz SCS for non-initial access.
* From [21] Mediatek:
  + Support only sequence length L=139 when PRACH SCS=480 kHz and 960 kHz.
* From [22] Intel:
  + Support PRACH formats A1~A3, B1~B4, C0, C2 for with SCS 480 kHz, i.e., .
* From [23] Apple:
  + If 480kHz and 960kHz SCS are used for PRACH transmission, support L=139 only.
* From [24] Sharp:
  + Only support L = 139 for PRACH with 480kHz and 960 kHz SSB SCS.

#### Summary of Contribution Discussions

The following are previous agreements on PRACH sequence and formats.

|  |
| --- |
| **Agreement:**   * For initial access and non-initial access use cases, support 120kHz PRACH SCS with sequence length L=571, 1151 (in addition to L=139) for PRACH Formats A1~A3, B1~B4, C0, and C2. * For non-initial access use cases,   + if 480kHz and/or 960 kHz SSB SCS is agreed to be supported, support 480 and/or 960 kHz PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively.     - FFS: support of sequence length L = 571, 1151 * FFS: Support of 480 and/or 960 kHz PRACH SCS for initial access use cases, if 480 and/or 960 kHz SSB SCS is agreed to be supported for initial access |

* Supported sequence lengths
  + Support PRACH lengths L=571, 1151 for 480kHz, and 960kHz PRACH
    - Samsung
  + Support PRACH length L=571 for 480kHz PRACH
    - Intel, Nokia/NSB, Huawei/HiSilicon
  + Do not support PRACH lengths L=571, 1151 for 960kHz PRACH
    - Ericsson, Qualcomm, Apple, Sharp, OPPO, Huawei/HiSilicon
  + Do not support PRACH lengths L=1151 for 480kHz PRACH
    - Ericsson
  + Do not support PRACH lengths L=571, 1151 for 480kHz PRACH
    - Qualcomm, Apple, Sharp, OPPO
* Consideration of additional formats/PRACH repetition lengths
  + CATT

#### **1st Round Discussion:**

Based on previous agreements and updated WID, moderator assume the following can be confirmed.

* Confirm agreement:
  + Support 480 PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively for initial and non-initial access cases
  + Support 960 PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively for non-initial access cases

Also two companies has suggested to support L=571 for 480kHz, while a number of companies suggested not to support L=571 and L=~~1191~~1151 for 480 and 960kHz.

Moderator suggest to discuss on the following options:

* Option 1) Support PRACH length L=571, ~~1191~~1151for 480 and 960 kHz PRACH
* Option 2) Support PRACH length L=571 for 480kHz PRACH, do not support PRACH length L=571, 1191 for 960kHz PRACH and L=~~1191~~1151for 480kHz PRACH.
* Option 3) Do not support PRACH length L=571, ~~1191~~1151for 480 and 960kHz PRACH

|  |  |
| --- | --- |
| Company | Comments |
| Qualcomm | Support option 3, since SCS = 480/960 kHz with sequence length = 139 is enough to achieve the desired BW requirement for the maximum EIRP allowed |
| LG Electronics | Support Option 3 considering the regulatory requirements (e.g., PSD) and the bandwidth occupied by the PRACH. In detail, the 480 kHz PRACH sequence with length L=571 occupies bandwidth of 275 MHz which is larger than 100 MHz that can achieve the conducted power limit of 27 dBm according to US regulation. |
| Fujitsu | 1. Considering BW of PRACH, we slightly prefer Option 3).  2. To confirm the definition of initial access case in the previous agreements:  As discussed in previous meetings, the definition of initial access case for PRACH is ambiguous and confusing. To avoid misunderstanding, could we confirm that initial access case implies that the corresponding ROs are configured by SIB1? |
| Mediatek | Support option 3. We are open for further discussion. However, we don’t see any advantages that can justify the price of excessive bandwidth. |
| Sharp | We prefer option 3, considering PRACH length L=571 for 480kHz PRACH as optimization. |
| Docomo | Support Option 3. |
| ZTE, Sanechips | In these options, 1191 should be changed by 1151.  We prefer Option 2, since 139 long sequence for 480kHz cannot achieve 100MHz emission bandwidth which may lead to limited max peak conducted output power of {500mW × emission-BW / 100MHz} according to US regulation. |
| Nokia | We could consider support for Option 2). Accounting the slightly increased transmission power and processing gain (139 s 571), supporting L=571 for 480kHz, could provide some benefit. |
| OPPO | Support Option 3. |
| Xiaomi | Option 3 is fine for us. |
| Samsung | First, we would like to restate that we don’t think there should be separate design for initial and non-initial access case, because from all the time, the same RACH resource could be used in UE before and after RRC connected mode; NR only introduce there could be additional RACH resource configured for Uplink BWP, but not any specific consideration for initial access or non-initial access.  Then for the SCS and sequence length combination, we believe as long as the channel bandwidth allows, the full flexibility should be supported and the configuration will be up to gNB configuration, so we prefer Option 1. |
| Lenovo, Motorola Mobility | We prefer option 3. |
| Intel | Support Option 2 for the reasons very well explained by LGE |
| Futurewei | Support Option 3. |
| Ericsson | Support Option 3.  Object to Option 1. |
| CATT | We support option 3 |
| InterDigital | Support Option 3. |
| Sony | We support option 3. |
| Huawei/HiSilicon | * Regarding “confirm Agreement”   As Fujitsu also pointed out, which PRACH applications fall into the category of initial access and which RACH applications fall into the category non-initial access has been a subject of lengthy discussions in RAN1 104 and RAN1 104b without any progress. As such, RAN1 could not make an agreement whether or not 480 kHz and/or 960 kHz SCS RACH is supported for initial access. In our view, here are the facts regarding this matter:   * + 480 kHz and 960 kHz SCS PRACH are supported (in an agreement in RAN1 104 at least for “non-initial access” although the definition of “non-initial access” was never fully clarified)   + 960 kHz SSB is not supported for initial access.   + RAN1 specifies PRACH without making distinction between initial access or non-initial access use cases. (This seems to be a general consensus without any formal agreement. At least, to our understanding, Section 6.3.3 of 38.211 does not make such a distinction).   Given above, we cannot “confirm agreement” proposed by FL. Instead, we suggest the following course of action:   * + Continue developing PRACH design for 480/960 kHz in RAN1 without any distinction between initial access and non-initial access use cases.   + In our view, as 960 kHz SSB is not supported for initial access, configuring 960 kHz PRACH in SIB1 for 960 kHz SSB is not required. We are open to further discuss this issue in RAN1 or leave to RAN2 decision. * Regarding supported RACH sequence lengths:   We support Option 2. We do not see any use case for a RACH BW larger than 100 MHz and can’t support Option 1. |

#### **1st Round Discussion Summary:**

There were also two companies who commented that there is no need to distinguish initial and non-initial access for development of physical layer specification. With this moderator assumes that all companies are aligned that

* 480/960 kHz PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2 is supported.

If so no further conclusion and agreement will be needed for the above bullet.

The following is a summary of company views on other PRACH sequence lengths.

* Option 1) Support PRACH length L=571, 1191 for 480 and 960 kHz PRACH
  + Samsung
* Option 2) Support PRACH length L=571 for 480kHz PRACH, do not support PRACH length L=571, 1151 for 960kHz PRACH and L=1151 for 480kHz PRACH.
  + ZTE, Sanechips, Nokia/NSB, Intel
* Option 3) Do not support PRACH length L=571, 1151 for 480 and 960kHz PRACH
  + Qualcomm, LGE, Fujitsu, Mediatek, Sharp, NTT Docomo, OPPO, Xiaomi, Ericsson, Interdigital, Sony, Lenovo/Motorola Mobility

Clear majority of the company think L=139 is sufficient and no further consideration for L=571 and 1151 is needed for 480/960kHz PRACH cases.

#### **2nd Round Discussion:**

Please provide comments on Proposal 1.3-3.

**Proposal 2.1-1)**

* Suggested Conclusion:
  + Do not support PRACH length L=571, 1151 for 480 and 960kHz PRACH

|  |  |
| --- | --- |
| Company | Comments |
| vivo | Support the proposal |
| DOCOMO | Support |
| Nokia | Like noted, we saw some merit in supporting L=571 for 480kHz, but don’t have a strong view. |
| ZTE, Sanechips | There is benefit to support L=571 for 480kHz at least in US region, and we don’t see additional spec effort since L=571 is already supported for 30kHz in Rel-16 NRU. Besides, longer PRACH sequence could also be used in licensed band, we tend to spend limited spec effort to achieve such benefits. |
| Samsung | We are not convinced by the discussion that PRACH is also split by intitial access and non-initial access, and also use the impact of SSB, even though SSB and RACH are belong to initial access, but they are separate design.  There are SSB for initial access (cell defining SSB), and SSB for measurement (non-cell defining SSB); but PRACH, there is only SIB1 configured RACH, no matter whether UE is in initial access or non-initial access, UE performs the RACH using same set of configurations. Even UE can be configured by UE specific signaling for a RACH in a non-initial access BWP, but it requires gNB to ensure it’s cell specific configuration;  Why due to SSB did not support 960khz, then RACH cannot support?  RACH support 1.25khz, 5khz in NR FR1, does SSB support?  SSB support 240khz, does RACH support?  SSB numerology and RACH numerology are independent issue. RACH SCS is independently configured from SSB SCS or even UL BWP SCS.  Again, is there any fundamental concern on supporting the preamble lengths in all SCS regardless of the initial access and non-initial access. |
| Intel | Do not support Proposal 2.1-1.  It seems strange to support 96 RBs for CORESET#0 configuration with SCS 120 kHz and not support L=571 for SCS 480 kHz as both means try to address the same issue, i.e., to provide a bandwidth larger than 100 MHz to avoid power reduction in the US.  For those companies, who do not think this is needed, we would like to understand why supporting the highest conducted power for critical channel such as PRACH which is not only used for initial access but for various other functions (e.g. BFR) somehow not important. |
| Apple | Support the proposal. |
| Qualcomm | Support the proposal |
| Sharp | Support the proposal. |
| Futurewei | Agree with the proposal |
| Ericsson | Support |
| Huawei, HiSilicon | We prefer a more conservative approach and leave it open to support the sequence size of 571 for 480 kHz in next meetings. Therefore, we suggest the following which seems to have a stronger majority: **Proposal 2.1-1)**  * Suggested Conclusion:   + Do not support PRACH length L=571, 1151 for ~~480 and~~ 960kHz PRACH and at least L =1151 for 480kHz PRACH. |

#### **2nd Round Discussion Summary:**

The following is a summary of company preferences and discussion. One company asked what main issue would be to support the different SCS for PRACH, as PRACH SCS is inherently not tied to SCS of SSB in NR. One company commented that support of larger PRACH stems from the same reason larger CORESET bandwidth is proposed, and suggested that it should be considered together. A modification of Proposal 2.1-1 was made by Huawei in Proposal 2.1-1A.

**Proposal 2.1-1)**

* Suggested Conclusion:
  + Do not support PRACH length L=571, 1151 for 480 and 960kHz PRACH
* Ok: vivo, Docomo, Apple, Qualcomm, Sharp, Futurewei, Ericsson, Lenovo/Motorola Mobility
* Not ok: ZTE/Sanechips, Samsung, Intel
* Maybe: Nokia, [Huawei/HiSilicon?]

**Proposal 2.1-1A)**

* Suggested Conclusion:
  + Do not support PRACH length L=571, 1151 for ~~480 and~~ 960kHz PRACH and at least L =1151 for 480kHz PRACH.

#### **3rd Round Discussion:**

Discuss further on Proposal 2.1-1 and 2.1-1A.

**Proposal 2.1-1)**

* Suggested Conclusion:
  + Do not support PRACH length L=571, 1151 for 480 and 960kHz PRACH

**Proposal 2.1-1A)**

* Suggested Conclusion:
  + Do not support PRACH length L=571, 1151 for ~~480 and~~ 960kHz PRACH and at least L =1151 for 480kHz PRACH.

|  |  |
| --- | --- |
| Company | Comments |
| LG Electronics | We are fine with Proposal 2.1-1A considering the L=139 for 480kHz PRACH occupies the bandwidth smaller than the bandwidth required to achieve 27 dBm in the US. |
| Qualcomm | We support Proposal 2.1-1 |
| OPPO | We support Proposal 2.1-1 |
| Sharp | We support Proposal 2.1-1. |
| Intel | Proposal 2.1-1) – don’t support  Proposal 2.1-1A) – Support. Otherwise, there is always power penalty of 1.76 dB when only L=139 for SCS 480 kHz is supported. It’s not clear, what is the technical challenge to support a sequence length of L=571, which is already supported by other SCS and is within specification. We would like to ask companies-opponents of L=571 and SCS 480 kHz about potential benefits they see from artificial restriction to L=139 only for SCS 480 kHz even at the expense of 1.76 dB power reduction. |
| DOCOMO | Ok with 2.1-1A. |
| Apple | We support Proposal 2.1-1 |
| ZTE, Sanechips | We support Proposal 2.1-1A with the same understanding as LG and Intel. |
| vivo | We support Proposal 2.1-1A |
| Lenovo, Motorola Mobility | We prefer Proposal 2.1-1 but are also fine with 2.1-A for the sake of consensus. |
| Nokia | Proposal 2.1-1A): We would be fine to consider L=571 for 480kHz, but don’t have a strong view. |
| Futurewei | We support Proposal 2.1-1 |
| InterDigital | We are fine with proposal 2.1-1A. |
| Huawei, HiSilicon | We support 2.1-1A. |
| Ericsson | Support 2.1-1. However, if there is a strong desire to include L = 571 for 480 kHz, we can be open to it. |
| Huawei, HiSilicon | We support Proposal 2.1-1A |
| CATT | Ok with 2.1-1A |
| LG Electronics | We share the same view with Ericsson. Proposal 2.1-1 is preferred but we can consider Proposal 2.2-1A if the majority of companies support it. |
| ZTE, Sanechips | We are fine with Proposal 2.2-1A |

#### **3rd Round Discussion Summary:**

Company views are split between the two proposals. Suggest discussing during GTW.

##### **Proposal 2.1-1)**

* Suggested Conclusion:
  + Do not support PRACH length L=571, 1151 for 480 and 960kHz PRACH

**Proposal 2.1-1A)**

* Suggested Conclusion:
  + Do not support PRACH length L=571, 1151 for ~~480 and~~ 960kHz PRACH and at least L =1151 for 480kHz PRACH.
* Ok with 2.1-1:
  + Qualcomm, OPPO, Sharp, Apple, Lenovo/Motorola Mobility, Futurewei, LGE, Ericsson
* Ok with 2.1-1A:
  + LGE, Intel, Docomo, ZTE/Sanechips, Lenovo/Motorola Mobility, Nokia/NSB, InterDigital, Huawei/HiSilicon
* Companies supporting 2.1-1 that mentioned that could consider to accept 2.1-1A if majority support it for sake of progress:
  + LGE, Ericsson, Lenovo/Motorola Mobility

#### **4th Round Discussion:**

There has been sufficient discussion and moderator believes there is good understanding of the issue among companies. So instead of repeating the same discussion, it would be better if we can resolve this during GTW.

With that said, if companies wish to provide **additional information/comments not mentioned before**, please provide them below.

|  |  |
| --- | --- |
| Company | Comments |
| Huawei, HiSilicon | We support Proposal 2.1-1A).  Proposal 2.1-1A) does not preclude Proposal 2.1-1). It just leaves the door open for supporting L=571 for 480 kHz. |

#### **4th Round Discussion Summary:**

Moderator concurs with Huawei/Hisilicon comments that Proposal 2-1-1A does not state RAN1 will support L=571 for 480kHz and only conclude to not introduce for others. Let’s try to see if we can agree to Proposal 2.1-1A.

#### **5th/6th Round Discussion:**

##### **Proposal 2.1-1A) – suggest for email approval**

* Do not support PRACH length L=571, 1151 for 960kHz PRACH and at least L =1151 for 480kHz PRACH.

Please provide **comments only if you have serious concern**s with Proposal 2.1-1A. As mentioned by Huawei, agreement of Proposal 2.1-1A does not mean RAN1 will support L=571 for 480kHz PRACH. That is undetermined even with this proposal.

If the proposal is stable, moderator will suggest to approve the proposal over email.

|  |  |
| --- | --- |
| Company | Comments |
|  |  |

#### **5th/6th Round Discussion Summary:**

Suggest approving Proposal 2.1-1A over email. No further discussion on this topic in RAN1 #106e needed if proposal is agreed.

### 2.2.2 RACH Occasion Resources

* From [1] Huawei/HiSilicon:
  + For 480kHz and 960kHz PRACH, support the reference slot duration corresponding to 60 kHz SCS (Option 1 in RAN1 105-e Agreement).
  + Support a gap symbol between consecutive ROs for 480kHz and 960kHz PRACH configurations.
  + For 480kHz and 960kHz PRACH, at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH configuration in FR2 should be supported (Alt 2 in RAN1 105-e Agreement).
  + For 480kHz and 960kHz PRACH configuration, support 1, 2, and 4 PRACH slots per 60kHz reference slot with the following PRACH slot indexes:
    - For 1 PRACH slot per 60kHz reference slot: for 480kHz and for 960kHz PRACH
    - For 2 PRACH slots per 60kHz reference slot: for 480kHz and for 960kHz PRACH.
    - For 4 PRACH slots per 60kHz reference slot: supported values are FFS.
* From [2] vivo:
  + For RO configuration for PRACH with 480/960kHz SCS:
  + Reuse the exiting FR2 RACH configuration table and the location of duration containing PRACH slot pattern within 10ms is same as FR2.
  + How to determine the RACH slot index:
    - Alt.1: Reuse the same reference slot as FR2 and maintain the same number of PRACH slots per reference slot.
    - Alt.2: Reuse the same reference slot as FR2 and increase the number of PRACH slots to more than 2 per reference slot.
  + If gaps between consecutive ROs are needed for LBT and or beam switching, at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported.
* From [4] Interdigital:
  + In PRACH configuration, we support Option 1 as it is in compliance with NR Rel.16.
    - Option 1) The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.
  + In PRACH density configuration, support Alt 2 with the same RO density as 120kHz PRACH. Moreover, support further study for higher PRACH slot density for 480kHz and 960kHz PRACH, compared to the 120kHz PRACH.
    - ALT 2) at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
  + For 52.6 – 71 GHz with 120kHz, 480kHz, and 960kHz PRACH, inserting gaps to achieve non-consecutive RACH occasions is not supported.
  + For 52.6 – 71 GHz, support sharing and extending the COT for LBT-free PRACH transmission in the consecutive ROs.
* From [7] Samsung:
  + Using the RO pattern for SCS = 120 kHz derived from the PRACH configuration table as the reference for larger SCS cases.
  + Option 2 for RO pattern determination should be supported.
    - Option 2) Each 120kHz RO corresponds to 4 and 8 candidate RO positions for 480kHz and 960kHz PRACH, respectively. Information about the number and locations of 480/960kHz candidate RO(s) are configured or pre-selected within each 120kHz RO. The reference 120kHz RO is determined by the current PRACH configuration method in Rel-15/16 specification.
  + Support non-consecutive RO configuration to alleviate the RACH LBT failure.
* From [8] CATT:
  + The reference slot duration corresponds to 60 kHz SCS. PRACH slot index corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.
  + For 480/960 kHz PRACH slots configuration, higher PRACH slot density or higher RO density in time domain can be supported to compensate the impact from MSGS –FDM decreasing and LBT/beam switching GAP.
* From [9] ZTE/Sanechips
  + For 480kHz and 960kHz, reuse the same RO configuration table as in Rel-15/16 with the same RO density for 120kHz PRACH.
  + Proposal 12: Support 60kHz for reference slot as in FR2 with the less spec effort in beyond 52.6GHz.
* From [10] Fujitsu:
  + For 480kHz and 960kHz PRACH, support gaps between consecutive ROs in time domain.
    - If Option 1) supports gaps between consecutive ROs, it is preferred because it is more aligned with the legacy PRACH configuration framework than Option 2).
    - If Option 1) does not support gaps between consecutive ROs, Option 2) is preferred because it supports the gaps by nature.
  + For PRACH density, if gaps between consecutive ROs are supported (by Option 1) or Option 2)), adopt Alt 2) for further discussion on higher density. Otherwise, it is fine to adopt Alt 1) or Alt 2), because there would be no difference between the baseline of the two alternatives.
* From [11] Ericsson:
  + For 480/960 kHz PRACH, support PRACH configurations that allow maintaining the same PRACH processing load (operations/unit time) as for 120 kHz PRACH configurations.
  + For 480/960 kHz PRACH, reuse the current PRACH configuration table in 38.211 for FR2 "as is." Specify rule for which 1 or 2 480/960 kHz slots within a 60 kHz reference slot are used depending on the value in the existing column "Number of PRACH slots within a 60 kHz slot" in the current PRACH configuration table. The rule should be common for all PRACH configurations in the table.
  + Support Option 1 and Alt 1. Regarding the FFS for Alt-1, do not support higher PRACH slot density (number of PRACH slots per reference slot).
  + It is not necessary to optimize PRACH design to allow for LBT gaps between consecutive PRACH occasions within a PRACH slot, especially since PRACH can be classified as short control signaling transmissions consistent with EN 302 567 (see [8]).
  + UE beam switching gaps between consecutive PRACH occasions within a PRACH slot are not needed, since the UE is allowed to send only one PRACH preamble before the end of the RAR window, and will hence not need to transmit in back-to-back PRACH occasions in a slot.
* From [12] Futurewei:
  + For the reference slot duration support Option 1.
  + For PRACH slot density use the same density (i.e. number of PRACH slots per reference slot) as for 120kHz PRACH in FR2-1 is supported (ALT 1).
* From [13] Nokia:
  + Adopt Option 1) The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot. FFS: to have LBT gaps between ROs
  + Adopt ALT 2) i.e. the number of ROs per reference slot is the same as for 120kHz PRACH in FR2.
  + If LBT gaps are needed between ROs, it would be better to define fixed LBT gap time between valid ROs that do not depend on the time domain allocation of the PRACH. In that case the LBT gap length would not depend on the used PRACH format.
* From [18] Qualcomm:
  + a maximum of 4 and 2 FD multiplexed ROs for SCS = 120 kHz and sequence length = 571 and 1151, respectively
  + for SCS = 120 kHz, if the maximum number of FD ROs are reduced, consider ways to increase the TD ROs (to maintain the same capacity) with minimal specification impact
  + for higher RACH SCS (480 and 960 kHz), the gap and CP length may not be long enough to absorb the gNB beam switching delay requirement
  + for higher RACH SCS (480 and 960 kHz), consider including a symbol-level gap between ROs to allow for gNB beam switching delay
  + for 480kHz and 960kHz PRACH:
    - The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot
    - ROs for a given PRACH configuration can span more than one PRACH slot if gaps between consecutive ROs are supported for LBT and/or beam switching purposes
    - The same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
* From [19] LG Electronics:
  + If the reference slot SCS is kept as 60 kHz and the density of PRACH occasion is the same as in 120 kHz in the time-domain (e.g., 2 slots out of 8 slots for 480 kHz), the PRACH slot index for 480 and 960 kHz SCS can be determined based on the selected two values of with the pre-configured rule or based on the configured/indicated value(s) of by the gNB.
  + If the reference slot SCS is kept as 60 kHz and the density of PRACH occasion is increased compared to 120 kHz in the time-domain, the additional PRACH slots for 480 and 960 kHz SCS can be indicated/configured by the parameter X to allocate the consecutive X slots before the last slot given by (e.g., for 480 and 960 kHz SCS, respectively).
  + When LBT is used to transmit the PRACH preamble, consider to insert CCA gap between adjacent RACH occasions in time domain (e.g. X usec or Y symbol) to avoid inter-UE LBT blocking due to the propagation delay of PRACH transmitted in an earlier RO.
  + Considering the potential gap to account for LBT is needed to be inserted between the adjacent RACH occasions, at least the same RO density (i.e. number of RO per reference slot) as for 120 kHz PRACH in FR2-2 is supported for the PRACH density.
* From [20] ETRI:
  + Support Option 1 and ALT 2 for 480kHz and 960kHz PRACH slot configurations.
* From [22] Intel:
  + For 480kHz and 960kHz PRACH, select Option 1) The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.
  + For PRACH SCS 480 kHz and 960 kHz, introduce optional time gaps between consecutive ROs;
  + Modify equation defining the first OFDM symbol of PRACH RO given Section 5.3.2 from TS 38.211 as follows:
    - ,
    - where is the gap duration (number of OFDM symbols) and for no gap.
  + On PRACH density for 480kHz and 960kHz PRACH, select ALT 2) at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported.
* From [23] Apple:
  + Maximum 4 PRACH ROs can be configured for 120kHz SCS with .
  + Maximum 2 PRACH ROs can be configured for 120kHz SCS with .
  + Reuse the existing FR2 PRACH configuration Table to indicate the time-domain PRACH slot location.
  + Support to keep the same PRACH capacity as Rel-16 FR2 for 480kHz and 960kHz SCS to minimize the signaling overhead.
  + The configured PRACH slots should be distributed over the 60kHz reference slot.
* From [24] Sharp:
  + Option 1 for RO design is preferred. Reuse Table 6.3.3.2-4 (Random access configurations for FR2 and unpaired spectrum) in Rel-16 38.211 as much as possible. 60kHz reference slot should be also inherited.
  + Regarding PRACH configuration design for 480/960kHz SCS, keep the same RO density and Alt 2 is preferred.
  + Gaps between consecutive ROs are needed at least for beam switching purposes, which should be considered during RO design.
  + A starting symbol index of a PRACH occasion is given by If non-zero duration gaps are configured between consecutive ROs and the ROs would span multiple PRACH slots, for 480 and 960 kHz SCS, respectively. Otherwise, for 480 and 960 kHz SCS, respectively.
* From [25] NTT Docomo:
  + For RO configuration for PRACH with 480/960 kHz SCS,
    - Support Option 1 to specify only 480/960 kHz PRACH slot within a 60 kHz referenced slot in addition to the existing RO configuration in FR2.
    - Only one or two 480/960 kHz PRACH slot(s) within the 60 kHz referenced slot is sufficient.
    - No need to enhance RA-RNTI calculation for NR operation in 52.6 – 71 GHz
    - No need to consider either LBT or beam switching gap for RO design in 52.6 – 71 GHz
* From [26] Xiaomi:
  + Inconsecutive RO time domain configuration should be supported at least for 480 kHz case.

#### Summary of Contribution Discussions

The following are previous agreements on PRACH sequence and formats.

|  |
| --- |
| **Agreement:**   * PRACH configuration for 480/960 kHz SCS (if agreed)   + The minimum PRACH configuration period is 10 ms (as in FR2)   + For RO configuration for PRACH with 480/960kHz SCS,     - FFS: details of how to configure the 480/960 kHz PRACH ROs using [60 or 120 kHz] reference slot considering at least:       * location of 480/960 kHz PRACH slot per reference slot       * location of duration containing 480/960khz PRACH slot pattern within 10ms       * potential impact to RA-RNTI calculation   **Agreement:**  For 480kHz and 960kHz PRACH,   * Down-select among option 1 and 2   + Option 1) The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.  * + - FFS: supported values of the starting PRACH slot index within reference slot and whether or not the ROs for a given PRACH configuration can span more than one PRACH slot if gaps between consecutive ROs are supported for LBT and/or beam switching purposes  * + Option 2) Each 120kHz RO corresponds to 4 and 8 candidate RO positions for 480kHz and 960kHz PRACH, respectively. Information about the number and locations of 480/960kHz candidate RO(s) are configured or pre-selected within each 120kHz RO. The reference 120kHz RO is determined by the current PRACH configuration method in Rel-15/16 specification. * Following alternatives are considered on PRACH density   + ALT 1) At least the same density (i.e. number of PRACH slots per reference slot) as for 120kHz PRACH in FR2 is supported     - FFS: support for higher PRACH slot density (number of PRACH slots per reference slot)   + ALT 2) at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported     - FFS: support for higher RO density   + An “example” illustration of PRACH slots for 480/960kHz is shown below:      * FFS: whether and how to account for LBT in RO configuration (if needed) * FFS: whether and how to account for beam switching gap in RO configuration (if needed) |

The following is a summary of company views.

* RO definition for 480 and 960kHz
  + Option 1) The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.



* + - Huawei/HiSilicon, Interdigital, Ericsson, Futurewei, Nokia/NSB, [Qualcomm], ETRI, Intel, [Apple], Sharp, NTT Docomo, LGE, Fujitsu (1st preference, with configurable gaps between ROs), ZTE/Sanechips, OPPO, CATT
  + Option 2) Each 120kHz RO corresponds to 4 and 8 candidate RO positions for 480kHz and 960kHz PRACH, respectively. Information about the number and locations of 480/960kHz candidate RO(s) are configured or pre-selected within each 120kHz RO. The reference 120kHz RO is determined by the current PRACH configuration method in Rel-15/16 specification.
    - Samsung, Fujitsu (2nd preference), OPPO
* PRACH density
  + ALT 1) At least the same density (i.e. number of PRACH slots per reference slot) as for 120kHz PRACH in FR2 is supported
    - Ericsson, Futurewei, MTK, ZTE/Sanechips
  + ALT 2) at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
    - Interdigital, Nokia/NSB, ETRI, Intel, Sharp, LGE, Fujitsu, OPPO, CATT, Huawei/HiSilicon
* Gap between consecutive ROs
  + Support: Huawei/HiSilicon, Samsung, Qualcomm, LGE, Intel (Configurable gap between consecutive RO), [Sharp], Fujitsu, OPPO, Xiaomi, Futurewei
  + Do not support: Interdigital, Ericsson, NTT Docomo, MTK, ZTE/Sanechips
* Slot index for 480/960 kHz PRACH
  + for 480kHz and for 960kHz PRACH
    - Huawei/HiSilicon (For 1 PRACH slot per 60kHz reference slot), Sharp (gap not configured)
  + for 480kHz and for 960kHz PRACH.
    - Huawei/HiSilicon (For 2 PRACH slots per 60kHz reference slot)
  + Depends on , i.e., the number of time domain PRACH occaions within a 60 kHz reference slot (1 or 2) as specified in the 2nd last column of Table 6.3.3.2-4 in 38.211.
    - If
      * for 480kHz and for 960kHz PRACH
    - If
      * for 480kHz and for 960kHz PRACH
    - Ericsson, [it seems this is also supported by Huawei/HiSilicon]
  + for 480 and 960 kHz SCS, respectively
    - Sharp (gap configured)
  + The selected two values of with the pre-configured rule or based on the configured/indicated value(s) of by the gNB
    - LGE
* Maximum FDM of ROs
  + 4 FDM and 2 FDM ROs for 120kHz PRACH with L=571 and 1151, respectively
    - Qualcomm, Apple

#### **1st Round Discussion:**

Suggest to continue discussion on the above issues. Moderator asks companies to provide further comments. Moderator will provide a suggested proposal once the summary captures all company opinion correctly.

If the above summary is directly edited (please use a color to highlight changes, e.g. RED) and mention the changes/additions in the comment below.

|  |  |
| --- | --- |
| Company | Comments |
| Qualcomm | RO definition for 480 and 960kHz: Support 60 kHz reference slot in order to minimize the spec changes  PRACH density: Alt 2 |
| LG Electronics | We added our preference for Option 1 and Alt 2 in the above summary.  We prefer to keep the reference slot subcarrier spacing as 60 kHz and if the density of PRACH occasion is the same as in 120 kHz in the time-domain (e.g., 2 slots out of 8 slots for 480 kHz), the PRACH slot index for 480 and 960 kHz SCS can be determined based on the selected two values of with the pre-configured rule or based on the configured/indicated value(s) of by the gNB. For PRACH density, at least the same RO density (i.e. number of RO per reference slot) as for 120 kHz PRACH in FR2-2 is supported considering the potential gap to account for LBT is needed to be inserted between the adjacent RACH occasions. |
| Fujitsu | We added our preferences in the above summary. |
| Mediatek | Our preferences have been added in the above summary |
| Sharp | We support gap between consecutive ROs. |
| Docomo | For gap between Ros, we are struggling to understand its necessity because of the following:   * In terms of LBT, it is something discussed in Rel-16 NR-U but not supported in our understanding. In 52.6 – 71 GHz, given that much narrower beam is likely used, the case where a PRACH at a RO interferes another PRACH at later RO would barely happen. * In terms of beam switching (at gNB reception), this is depending on RAN4 reply regarding beam switching. As discussed in 2.1.2, we would like to hear companies’ views on how to treat it. With the current value RAN4 told us, beam switching time does not need to be considered here in our view. |
| ZTE/Sanechips | Please see our added support above using “ZTE/Sanechips” |
| Nokia | Our preference is Option 1 with 60kHz reference slot and ALT 2 for PRACH density. We don’t currently see that LBT gaps are absolutely mandatory. |
| OPPO | Please see our added support above using “OPPO” |
| Xiaomi | Please see our added support above using “Xiaomi” |
| Samsung | 1. Even though we still believe Option 2 has benefits, it seems the Option 2 is not preferred by companies, thus, we can live with Option 1 for RO definition for 480 and 960kHz;  2. For RACH density, we want to clarify that, it’s for maximum RACH density instead of every RACH density; with this assumption, we prefer Alt.2; suggested change:  ALT 2) at least the same maximum RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported  3. For slot index, {7,15} for one PRACH slot and {3,7; 7,15} for 2 PRACH slot seem fine.  4. When gap is needed, it should be designed on top of the configured ROs. |
| Intel | Regarding slot index, although we didn’t propose particular values, our requirement is that the slot index should be aligned with the SSB slot patterns in order to avoid systematic overlapping between SSBs and ROs. |
| Futurewei | Please see our added support above using “Futurewei”. |
| Ericsson | Please see our added support above using "Ericsson". For the slot index for 480/960 kHz, I have merged the first two options into a new option. I believe this is also supported by Huawei/HiSilicon. This option aligns with the following diagram from the agreement, i.e., slots 7 or 3+7 are used for 480 kHz, and slots 7 or 7 + 15 are used for 960 kHz.    Regarding gaps, we agree with DOCOMO's view in terms of LBT. In fact, gaps were not introduced in Rel-16 NR-U, and the system is not broken. Gaps are even less motivated for Rel-17. In terms of beam switching, gaps are not needed from a UE perspective since the UE transmits PRACH in only one RO, so no beam switching needed. From a gNB perspective, RAN4 is discussing 59 ns as a beam switching requirement which is less then the CP for 960 kHz. Hence, gaps are not needed.  We observe that if no gaps are introduced, Alt-2 is equivalent to Alt-1 which is our preference. |
| CATT | Please see our added support above using “CATT”. |
| Huawei/HiSilicon | * Reference slot   + We support Option 1 for PRACH reference slot as in Rel-15. * Beam switching gap   + We believe that beam switching gap symbol is required between consecutive ROs for both 480/960 kHz PRACH. Although beam switch time at gNB is tentatively [59ns], up to 200ns beam switch time at the UE side is suggested in ongoing discussions in RAN4. Comparing these values with the 73ns (146ns) CP length of 960kHz (480kHz) OFDM symbols, the introduction of a beam switching gap symbol for PRACH seem required. Although the CP lengths of different PRACH formats are longer than that of the OFDM symbol, such larger CP lengths are mainly devised to additionally cope with the timing uncertainty that can be up to the maximum round-trip delay in the cell. For instance, the CP of Format A1 is 146ns (292ns) in 960kHz (480kHz) and the CP of Format B1 is 110ns (220ns) in 960kHz (480kHz). Such CP lengths are not enough to accommodate up to 200ns of beam switch time in addition to round-trip time delay, DL time synchronization, and channel dispersion effects. * PRACH density   + We support ALT 2 at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 * Number of PRACH slots and PRACH slots indexes in a reference slot   + We support keeping at least the same number of ROs per reference slot and, at the same time, propose to use beam switching gap. Therefore, number of PRACH slots within the PRACH reference slot may need to be increased for some PRACH configuration indexes in Table 6.3.3.2-4:     - There are PRACH configuration indexes where starting symbol is symbol 0 and PRACH duration is 6 symbols with 2 ROs per PRACH slots (e.g. PRACH configuration indexes 68 and 69). In these cases, beam switching gap + number of ROs can be supported within the same slot and the number of PRACH slots in a reference slot does not need to increase. For such cases, for 480kHz and for 960kHz PRACH when the number of PRACH slots in a reference slot is 1 and for 480kHz and for 960kHz PRACH when the number of PRACH slots in a reference slot is 2.     - There are PRACH configuration indexes where the same number of ROs per PRACH slot as in Table 6.3.3.2-4 + beam switching gap cannot be accommodated within a single PRACH slot. In such cases, number of PRACH slots per reference slot should increase to e.g. 4. One way to choose the new PRACH slots is to use the slots immediately after the original PRACH slots to let the ROs in the original PRACH slot spill over to the subsequent slot. However, this is not the only solution and any solution that can support keeping the RO density per reference slot at least the same as in Rel-15 without any (or with minimum) change to Table 6.3.3.2-4 can be discussed. |

#### **1st Round Discussion Summary:**

**Issue 1)** RO definition for 480 and 960kHz. Clear majority of the companies prefer option 1. Suggest to continue discussion based on proposal for option 1.

|  |
| --- |
| * RO definition for 480 and 960kHz   + Option 1) The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.  * + - Huawei/HiSilicon, Interdigital, Ericsson, Futurewei, Nokia/NSB, [Qualcomm], ETRI, Intel, [Apple], Sharp, NTT Docomo, LGE, Fujitsu (1st preference, with configurable gaps between ROs), ZTE/Sanechips, OPPO, CATT   + Option 2) Each 120kHz RO corresponds to 4 and 8 candidate RO positions for 480kHz and 960kHz PRACH, respectively. Information about the number and locations of 480/960kHz candidate RO(s) are configured or pre-selected within each 120kHz RO. The reference 120kHz RO is determined by the current PRACH configuration method in Rel-15/16 specification.     - Samsung, Fujitsu (2nd preference), OPPO |

**Proposal 2.2-1)**

* For 480 and 960kHz PRACH:
  + The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.



**Issue 2)** Regarding the PRACH density, majority of the companies prefer Alt 2. The distinction between the two alternatives seems to be minor and seems to depend on whether RO can span more than 1 PRACH slot, which is related to RO density.

Regarding whether or not to support gap between consecutive ROs, more companies prefer to define gaps. One company explicitly mentioned that gap should be configurable.

Moderator suggest continuing discussion based on Alt 2 for density and supporting resource gap between consecutive ROs.

|  |
| --- |
| * PRACH density   + ALT 1) At least the same density (i.e. number of PRACH slots per reference slot) as for 120kHz PRACH in FR2 is supported     - Ericsson, Futurewei, MTK, ZTE/Sanechips   + ALT 2) at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported     - Interdigital, Nokia/NSB, ETRI, Intel, Sharp, LGE, Fujitsu, OPPO, CATT, Huawei/HiSilicon, vivo |

**Proposal 2.2-2)**

* For 480 and 960kHz PRACH:
  + at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
  + Support resource gap between consecutive ROs.
    - FFS whether this gap can be configured by gNB.

**Issue 3)** Regarding the slot index for 480/960 kHz PRACH, further discussion is needed. One company identified that there are some PRACH configuration entries where all ROs and beam switching gap can be accommodated within PRACH slot and there are some PRACH configuration entries where it may not be possible. For the former cases, few companies suggest to use 7, 15 for 480 and 960kHz, respectively, when 1 occasion is defined for a 60kHz reference and {3,7} and {7,15} for 480 and 960kHz, respectively, when \*2 occasion is defined for a 60kHz reference. Hopefully, even for companies who do not think beam switching gap is needed, if the Proposal 2.2-3 would still be ok.

**Proposal 2.2-3)**

* For 480 and 960kHz PRACH when number of time domain PRACH occasions and potential beam switching gap can be placed within a PRACH slot,
  + and number of PRACH slots in a reference slot is 1,
    - for 480kHz and for 960kHz PRACH
  + And when the number of PRACH slots in a reference slot is 2,
    - for 480kHz and for 960kHz PRACH
* FFS: values when number of time domain PRACH occasions and potential beam switching gap cannot be placed within a PRACH slot.

#### **2nd Round Discussion:**

Please provide further comments on Proposal 2.2-1 ~ 2.2-3.

|  |  |
| --- | --- |
| Company | Comments |
| vivo | Support the proposal |
| DOCOMO | * Support Proposal 2.2-1 * For Proposal 2.2-2, still not sure why beam switch gap is needed. Maybe the decision can be discussed with 2.1.2 in terms of beam switching gap. Not sure why UE-side beam switching needs to be considered. * Proposal 2.2-3 should be discussed after Proposal 2.2-2. |
| Nokia | Proposal 2.2-1: We are OK with this proposal.  Proposal 2.2-2: We are OK with this proposal.  Proposal 2.2-3: In principle we are OK with this proposal, but maybe the beam switching text could put as FFS or removed. This can be further discussed of course, but based on latest RAN4 feedback on gNB beam switching gap, this would not seem necessary. |
| ZTE, Sanechips | We are fine with Proposal 2.2-1.  For Proposal 2.2-2, we still don’t quite understand the motivation to introduce the gap between ROs. RAN4 has sent an LS about the gNB beam switching time as 59ns, this can be covered by the CP length of PRACH sequence. As for UE beam switching, it should not be considered for gap between ROs since UE will randomly select only one of these ROs and there is no beam switching issue.  We are fine with Proposal 2.2-3. |
| Samsung | For 2.2-1, we expressed the compromise to option1, but however, we see some proponents raised the additional points for extra design on spilling the RO in more slots than configured in order to accommodate the beam switching gap (or other gap). If this is the case, we will insist on the option2, which can solve the problem once for all.  For 2.2-2, as we commented before, we want to clarify that, it’s for maximum RACH density instead of every RACH density; with this assumption, we prefer Alt.2; suggested change:   * For 480 and 960kHz PRACH:   + at least the same maximum RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported   + Support ~~resource~~ gap between consecutive ROs in time domain.     - FFS the details to derive the gap ~~whether this gap can be configured by gNB.~~   For 2.2.-3, as we commented in above, we did not see the need to separate the cases based on “when number of time domain PRACH occasions and potential beam switching gap can be placed within a PRACH slot”, and there could be multiple ways to create the gap (e.g., odd or even number indication), which needs no additional spec effort. So suggest:   * For 480 and 960kHz PRACH ~~when number of time domain PRACH occasions and potential beam switching gap can be placed within a PRACH slot~~,   + and number of PRACH slots in a reference slot is 1,     - for 480kHz and for 960kHz PRACH   + And when the number of PRACH slots in a reference slot is 2,     - for 480kHz and for 960kHz PRACH * ~~FFS: values when number of time domain PRACH occasions and potential beam switching gap cannot be placed within a PRACH slot.~~ |
| Intel | Proposal 2.2-1) – agree  Proposal 2.2-2) – agree  Proposal 2.2-3) – don’t agree.  We prefer to defer agreement on this proposal until it is clarified whether time gaps between consecutive ROs are needed or not. We prefer to have a single solution which would cover both cases with and without gaps. |
| Apple | Proposal 2.2-1: Support.  Proposal 2.2-2: Support in principle.  Regarding the ‘gap’, our understanding is that it mainly targets to provide flexibility at gNB for Rx beam switching, instead of UE side. Another potential benefit is to reduce the blocking probability for two consecutive ROs for unlicensed operation. If it was defined as ‘configurable’, we do not see strong concern as gNB/operator can disable or configure it as ‘0’ by proper configuration if wants.  Proposal 2.2-3: Support. |
| Qualcomm | Proposal 2.2-1: fine  Proposal 2.2-2: fine  Proposal 2.2-3: This is fine assuming no gaps between ROs, if RO gaps are allowed and the same number of ROs (compared to 120 kHz) is desired, then ROs for some configurations will need more than 1 RA slot, hence, this (Proposal 2.2-3) may not work. Suggest we defer this discussion until the following are concluded: 1) RO gaps need and design, 2) to allow (or not) for ROs to spill into adjacent slots |
| Sharp | Proposal 2.2-1: Support  Proposal 2.2-2: Support  Proposal 2.2-3: We also think that detailed discussion should be after concluding Proposal 2.2-1 and Proposal 2.2-2. |
| Futurewei | Proposal 2.2-1 OK  Proposal 2.2-2 OK  Proposal 2.2-3 Fine to discuss further |
| Ericsson | **Proposal 2.2-1**: Support  **Proposal 2.2-2**: We do not support the 2nd sub-bullet, i.e., we still do not support gaps. If companies are worried about gNB beam switching gap, then we can wait for RAN4 to confirm [59 ns].  We can be open to the first sub-bullet with the following clarification:   * For 480 and 960kHz PRACH:   + For a given configured number of frequency domain ROs, at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported   **Proposal 2.2-3**: Support conditioned on the following changes:   * For 480 and 960kHz PRACH when number of time domain PRACH occasions and ~~potential~~ beam switching gap (if supported) can be placed within a PRACH slot,   + and number of time domain PRACH ~~slots~~ occasions in a reference slot is 1,     - for 480kHz and for 960kHz PRACH   + And when the number of time domain PRACH ~~slots~~ occasions in a reference slot is 2,     - for 480kHz and for 960kHz PRACH * FFS: values when number of time domain PRACH occasions and ~~potential~~ beam switching gap (if supported) cannot be placed within a PRACH slot. |
| Huawei, HiSilicon | Proposal 2.2-1: Agree  Proposal 2.2-2: Agree  Proposal 2.2-3: We prefer to support this with the following modification. Otherwise, the time domain PRACH occasions can always be modified (reduced) such that the PRACH occasions and potential beam switching gap can be placed within a PRACH slots **Proposal 2.2-3)**  * For 480 and 960kHz PRACH when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and potential beam switching gap can be placed within a PRACH slot,   + and number of PRACH slots in a reference slot is 1,     - for 480kHz and for 960kHz PRACH   + And when the number of PRACH slots in a reference slot is 2,     - for 480kHz and for 960kHz PRACH * FFS: values when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and potential beam switching gap cannot be placed within a PRACH slot. |

#### **2nd Round Discussion Summary:**

Below is a summary of company preferences. Proposal 2.2-2A and 2.2-3A are alternative proposals from Samsung. Moderator suggest to continue discuss based on the proposal listed.

##### **Proposal 2.2-1)**

* For 480 and 960kHz PRACH:
  + The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.



* Ok: vivo, Docomo, Nokia/NSB, ZTE/Sanechips, Intel, Apple, Qualcomm, Sharp, Futurewei, Ericsson, Huawei/HiSilicon
* Not Ok: Samsung (if gaps are needed option 2 would be better design)

##### **Proposal 2.2-2)**

* For 480 and 960kHz PRACH:
  + at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
  + Support resource gap between consecutive ROs.
    - FFS whether this gap can be configured by gNB.
* Ok: vivo, Nokia/NSB, Intel, Apple, Qualcomm, Sharp, Futurewei, Huawei/HiSilicon
* Not Ok: Docomo, ZTE/Sanechips, Ericsson (gaps not needed, [ok for2.2-2A??])

**Proposal 2.2-2A)**

* For 480 and 960kHz PRACH:
  + For a given configured number of frequency domain ROs, at least the same maximum RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
  + Support ~~resource~~ gap between consecutive ROs in time domain.
    - FFS the details to derive the gap
    - ~~FFS whether this gap can be configured by gNB.~~

**Proposal 2.2-3)**

* For 480 and 960kHz PRACH when number of time domain PRACH occasions and potential beam switching gap can be placed within a PRACH slot,
  + and number of PRACH slots in a reference slot is 1,
    - for 480kHz and for 960kHz PRACH
  + And when the number of PRACH slots in a reference slot is 2,
    - for 480kHz and for 960kHz PRACH
* FFS: values when number of time domain PRACH occasions and potential beam switching gap cannot be placed within a PRACH slot.
* Ok: vivo, Apple, Qualcomm, [Huawei/HiSilicon]
* Maybe: Docomo, Ericsson (Proposal 2.2-3B)
* Not Ok: Intel (prefer to defer)
* Defer: Intel, Sharp, Futurewei

**Proposal 2.2-3A)**

* For 480 and 960kHz PRACH ~~when number of time domain PRACH occasions and potential beam switching gap can be placed within a PRACH slot,~~
  + and number of PRACH slots in a reference slot is 1,
    - for 480kHz and for 960kHz PRACH
  + And when the number of PRACH slots in a reference slot is 2,
    - for 480kHz and for 960kHz PRACH
* ~~FFS: values when number of time domain PRACH occasions and potential beam switching gap cannot be placed within a PRACH slot.~~

**Proposal 2.2-3B)**

* For 480 and 960kHz PRACH when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ beam switching gap (if supported) can be placed within a PRACH slot,
  + and number of time domain PRACH ~~slots~~ occasions in a reference slot is 1,
    - for 480kHz and for 960kHz PRACH
  + And when the number of time domain PRACH ~~slots~~ occasions in a reference slot is 2,
    - for 480kHz and for 960kHz PRACH
* FFS: values when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ beam switching gap (if supported) cannot be placed within a PRACH slot.

#### **Conclusion from GTW (Week 1 - Thursday):**

**Agreement:**

* For 480 and 960kHz PRACH:
  + The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.



The following proposal was discussed during GTW.

**Proposal 2.2-2B)**

* For 480 and 960kHz PRACH:
  + ~~For a given configured number of frequency domain ROs,~~ at least the same maximum RO density in time domain (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
    - FFS: Support ~~resource~~ gap between consecutive ROs in time domain and ~~FFS~~ the details to derive the gap
    - ~~FFS whether this gap can be configured by gNB.~~

No summary was made by Moderator.

#### **3rd Round Discussion:**

Please provide further comments on Proposal 2.2-2A and 2.2-2B, and Proposal 2.2-3, 2.2-3A, and 2.2-3B.

##### **Proposal 2.2-2A)**

* For 480 and 960kHz PRACH:
  + For a given configured number of frequency domain ROs, at least the same maximum RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
  + Support ~~resource~~ gap between consecutive ROs in time domain.
    - FFS the details to derive the gap
    - ~~FFS whether this gap can be configured by gNB.~~

##### **Proposal 2.2-2B)**

* For 480 and 960kHz PRACH:
  + ~~For a given configured number of frequency domain ROs,~~ at least the same maximum RO density in time domain (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
    - FFS: Support ~~resource~~ gap between consecutive ROs in time domain and ~~FFS~~ the details to derive the gap
    - ~~FFS whether this gap can be configured by gNB.~~

##### **Proposal 2.2-3)**

* For 480 and 960kHz PRACH when number of time domain PRACH occasions and potential beam switching gap can be placed within a PRACH slot,
  + and number of PRACH slots in a reference slot is 1,
    - for 480kHz and for 960kHz PRACH
  + And when the number of PRACH slots in a reference slot is 2,
    - for 480kHz and for 960kHz PRACH
* FFS: values when number of time domain PRACH occasions and potential beam switching gap cannot be placed within a PRACH slot.

##### **Proposal 2.2-3A)**

* For 480 and 960kHz PRACH ~~when number of time domain PRACH occasions and potential beam switching gap can be placed within a PRACH slot,~~
  + and number of PRACH slots in a reference slot is 1,
    - for 480kHz and for 960kHz PRACH
  + And when the number of PRACH slots in a reference slot is 2,
    - for 480kHz and for 960kHz PRACH
* ~~FFS: values when number of time domain PRACH occasions and potential beam switching gap cannot be placed within a PRACH slot.~~

##### **Proposal 2.2-3B)**

* For 480 and 960kHz PRACH when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ beam switching gap (if supported) can be placed within a PRACH slot,
  + and number of time domain PRACH ~~slots~~ occasions in a reference slot is 1,
    - for 480kHz and for 960kHz PRACH
  + And when the number of time domain PRACH ~~slots~~ occasions in a reference slot is 2,
    - for 480kHz and for 960kHz PRACH
* FFS: values when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ beam switching gap (if supported) cannot be placed within a PRACH slot.

**Proposal 2.2-2C)**

* For 480 and 960kHz PRACH:
  + ~~For a given configured number of frequency domain ROs,~~ at least the same ~~maximum~~ RO density in time domain (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
    - FFS: Support ~~resource~~ gap between consecutive ROs in time domain and ~~FFS~~ the details to derive the gap
    - ~~FFS whether this gap can be configured by gNB.~~

##### **Proposal 2.2-3C)**

* For 480 and 960kHz PRACH when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ beam switching gap (if supported) can be placed within a PRACH slot (i.e., the number of ROs in the PRACH slot is not affected),
  + and number of time domain PRACH slots ~~occasions~~ in a reference slot is 1,
    - for 480kHz and for 960kHz PRACH
  + And when the number of time domain PRACH slots ~~occasions~~ in a reference slot is 2,
    - for 480kHz and for 960kHz PRACH
* FFS: values when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ beam switching gap (if supported) cannot be placed within a PRACH slot (i.e., the number of ROs in the PRACH slot is affected).

|  |  |
| --- | --- |
| Company | Comments |
| LG Electronics | We support Proposal 2.2-2B. For Proposal 2.2-3/3A/3B, the LBT gap should be considered in addition to the beam switching gap. As Samsung mentioned during GTW session, the short control signaling rules are not always applicable to the transmission of msg1/msgA since it depend on the local regulations. Furthermore, the necessity of LBT gap to the consecutive ROs in order to prevent LBT blocking between the UEs is not enough discussed yet. Therefore, we suggest to change the words “beam switching gap” in Proposal 2.2-3/3A/3B to “the potential gap to account for LBT/beam switching gap”. If at least the same maximum RO density in time domain (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported, we support Proposal 2.2-3. |
| Qualcomm | Proposal 2.2-2A/B: we believe that the same RO density should be maintained for both time x frequency dimensions (not just time as in both proposals). If only time RO density is preserved, if RO gaps are introduced or if # ROs in FD has to be smaller (e.g., due to limited BW), then the RO capacity will be reduced. This is not preferred.  Proposal 2.2-3B: support with the following **modification**:   * For 480 and 960kHz PRACH when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ beam switching gap (if supported) can be placed within a PRACH slot **(i.e., the number of ROs in the PRACH slot is not affected),**   + and number of time domain PRACH ~~slots~~ occasions in a reference slot is 1,     - for 480kHz and for 960kHz PRACH   + And when the number of time domain PRACH ~~slots~~ occasions in a reference slot is 2,     - for 480kHz and for 960kHz PRACH * FFS: values when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ beam switching gap (if supported) cannot be placed within a PRACH slot **(i.e., the number of ROs in the PRACH slot is affected)** |
| Sharp | We support Proposal 2.2-3B and Okay with Qualcomm’s modifications. |
| Intel | **Proposal 2.2-2B**) – support but the word “maximum” should be removed as it’s misleading.  Before agreement on either Proposal 2.2-3), Proposal 2.2-3A) or Proposal 2.2-3B), we prefer to have an understanding whether the time gaps between the consecutive ROs is needed as a common solution for RO configuration covering both cases with and without time gaps is possible.  In our opinion, RAN4 only provide information about simple gNB beam switching. We expect inter-panel gNB beam switching to be larger than the simple beam switching case. In order to allow supporting for various RF configurations at the gNB, we think it would be safer to support the gaps, and if it helps to get further progress have the gap configurable so that not all gNB need to support the gaps.  As potential introduction of beam switching gaps would spread RO across two consecutive PRACH slots, we think it is safer to shift starting slots. Therefore, our proposal is as follows: **Proposal 2.2-3A)** – Modified  * For 480 and 960kHz PRACH ~~when number of time domain PRACH occasions and potential beam switching gap can be placed within a PRACH slot,~~   + and number of PRACH slots in a reference slot is 1,     - for 480kHz and for 960kHz PRACH   + And when the number of PRACH slots in a reference slot is 2,     - for 480kHz and for 960kHz PRACH * ~~FFS: values when number of time domain PRACH occasions and potential beam switching gap cannot be placed within a PRACH slot.~~ |
| DOCOMO | Proposal 2.2-2A/B) we are ok with Proposal 2.2-2B. On whether gap is needed between Ros, in Rel-16 NR-U, the necessity of LBT gap to the consecutive Ros was extensively discussed, and not supported as a result. Rel-16 NR-U assumes omni-directional sensing/transmit beam only, thus LBT gap was possibility more, while the situation is different in 60 GHz since the common understanding is the use of narrower beam for both sensing and transmission. We can rather see less motivation to support LBT gap here. For beam switching gap, the potential valid issue is gNB RX beam switching only. Why UE TX beam switching should be considered is unclear for us. For gNB beam switching, although SSB symbols may take beam switching gap into consideration, it does not necessarily mean RO should also consider beam switching gap since CP for PRACH is longer than NCP. Given that, we still fail to see the necessity to add guard period between Ros.  Proposal 2.2-3/3A/3B) Prefer 3A, i.e. we do not want to touch anything about beam switching gap at this stage. We can also live with 3B. |
| Apple | Proposal 2.2-2A/B:  We do not see the need of ‘For a given configured number of frequency domain ROs’ and ‘maximum’ in the proposal as explained below and recommend to remove them:   * The frequency density of RO and time domain density of RO were separately configured by different parameter for PRACH resource, one is ‘msg1-FDM’ and the other is ‘prach-ConfigurationIndex’, which are totally independent. We assume the same framework would be reused for FR2-2. * Proposal 2.2-2A/B is talking about the time-domain parameter ‘prach-ConfigurationIndex’, i.e., for a given value, how to determine the time-domain ROs for new SCSs. It is decoupled with frequency domain parameter, which is controlled by ‘msg1-FDM’. * On ‘maximum’, we do not think it is needed because the number of time-domain ROs is deterministic for a given value of ‘prach-ConfigurationIndex’ parameter and not a range of values. It is very confusing of ‘maximum’.  **Proposal 2.2-3B):** Prefer the modification from Qualcomm and add ‘LBT’ as recommended by LGE. |
| InterDigital | Proposal 2.2-2A/B) Do not support the insertion of gaps between consecutive ROs. Considering gaps to account for the LBT failure risks the efficiency as multiple symbols in 480kHz/960kHz SCS will be required for the CCA. The beam switching gap is not required either, as ROs with longer CP and guard time can be used to accommodate the beam switching delay, if required.  Proposal 2.2-3B) We support the proposal and we are ok with the revisions made by Qualcomm. |
| ZTE, Sanechips | We prefer Proposal 2.2-2B with ‘maximum’ removed because we strive to reuse the existing PRACH configuration as much as possible, if only maximum RO density is reused, this may lead to various number of PRACH configurations needed to discuss.  We support Proposal 2.2-3A. From our understanding, this proposal mainly talks about the relative PRACH slot location for 480kHz/960kHz within a 60kHz reference slot. Proposal 2.2-3B is problematic since the number of PRACH occasions in a slot depends on the PRACH format, e.g. 7 ROs for Format A1/B1, we don’t understand why the PRACH slot location relates to the number of PRACH occasions in a slot. So Proposal 2.2-3B is not acceptable. |
| vivo | **Proposal 2.2-2A/B**: we don’t see the need of ‘maximum’ here; **Proposal 2.2-3B):** Support Qualcomm’s modification and add ‘LBT’ by LGE |
| Lenovo, Motorola Mobility | We support Proposal 2.2-3B with Qualcomm modifications. |
| Nokia | I would have few questions for my clarification.  Proposal 2.2-3A), if we support having gaps, and end up spreading the RO’s to two slots, would we need to reflect this in the values? Regarding the absolute indexes of the RACH slots, reflecting the Intel proposal, maybe we could place the values in square brackets?  Regarding the Proposal 2.2-3B), I’m not sure, in my reading these would seem to severely restrict the number of RO’s in slot (e.g. to 1)? |
| Futurewei | We support Proposal 2.2-2A/B  OK with the Proposal 2.2-3B with Qualcomm modifications. |
| Huawei, HiSilicon | **Proposal 2.2-2A and 2.2-2B)** As discussed in last GTW, we don’t understand what “maximum” means here. This maximum is taken over what? Is it over all supported RACH configuration indexes with the same PRACH format? It is quite confusing and we cannot support either of Proposal 2.2-2A and 2.2-2B in this form.  We can support this modified version of 2.2-2A where “maximum” is removed and we use “PRACH frequency resources ” to align the proposal with spec language.  **Proposal 2.2-2A (Modified):**   * For 480 and 960kHz PRACH:   + ~~For a given configured number of frequency domain ROs~~, For the same PRACH frequency resources , at least the same ~~maximum~~ RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported   + Support ~~resource~~ gap between consecutive ROs in time domain.     - FFS the details to derive the gap     - ~~FFS whether this gap can be configured by gNB.~~   **Proposal 2.2-3B)** We would support this proposal (which actually was our modification on 2.2-3) and we would be OK with Qualcomm modification but we noticed that RACH slots in the sub-bullets has changed to RACH occasions which, in our view, is incorrect and we cannot justify it. We think “PRACH slots” is correct.  **Proposal 2.2-3B (further modification):**   * For 480 and 960kHz PRACH when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ beam switching gap (if supported) can be placed within a PRACH slot **(i.e., the number of ROs in the PRACH slot is not affected),**   + and number of time domain PRACH slots ~~occasions~~ in a reference slot is 1,     - for 480kHz and for 960kHz PRACH   + And when the number of time domain PRACH slots ~~occasions~~ in a reference slot is 2,     - for 480kHz and for 960kHz PRACH   FFS: values when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ beam switching gap (if supported) cannot be placed within a PRACH slot **(i.e., the number of ROs in the PRACH slot is affected)** |
| DOCOMO | We generally agree with both, while just an editorial proposal as below: **Proposal 2.2-3C) – cleaned up (updated by NTT DOCOMO)**  * For 480 and 960kHz PRACH when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ beam switching gap (if supported) can be placed within a PRACH slot (i.e., the number of ROs in the PRACH slot is not affected),   + and when number of time domain PRACH slots in a reference slot is 1,     - for 480kHz and for 960kHz PRACH   + And when the number of time domain PRACH slots in a reference slot is 2,     - for 480kHz and for 960kHz PRACH * FFS: values when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ beam switching gap (if supported) cannot be placed within a PRACH slot (i.e., the number of ROs in the PRACH slot is affected). |
| Ericsson | These are our comments prior to the 3rd round summary. I would be happy if you could take them into account in the 4th round:  **Proposal 2.2-2A/2B**  **We support Proposal 2.2-2B with the word "maximum" removed**. It is still our strong view that gaps are not needed neither for LBT nor for gNB beam switching for similar reasons as described by DOCOMO.  **Proposal 2.2-3/3A/3B**  I must apologize for making a misleading comment previously about wording changes; I was looking at the wrong column in Table 6.3.3.2.4. Huawei is completely correct, that the proper wording for all of Proposal 3/3A/3B is the following.   * + and number of PRACH slots in a reference slot is 1,     - for 480kHz and for 960kHz PRACH   + And when the number of PRACH slots in a reference slot is 2,     - for 480kHz and for 960kHz PRACH   This aligns the wording in the 3rd last column of Table 6.3.3.2-4 in 38.211. It also aligns with the wording in 38.211 Section 5.3.2  is given by  - if kHz, then  - if kHz and either of "Number of PRACH slots within a subframe" in Tables 6.3.3.2-2 to 6.3.3.2-3 or "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 1, then  - otherwise,  Based on this, correction, we do not support Qualcomm's changes in **green**. This was exactly the point we tried to make in the GTW that just because it might not be possible to configure as many ROs in the frequency domain (e.g., only 4 instead of 8), it doesn't mean that there is a need to compensate for this in the time domain by introducing a higher time domain density. Frequency domain multiplexing is not important in the 60 GHz band where there may not be very many users occupying the same beam.  In summary, **we can support the following**:   * 2.2-3A   2.2-3B without Qualcomm's addition in **green** and with the above correction from Huawei (change "PRACH occasions" back to "PRACH slots"). In fact "time domain" can be removed since it is redundant |
| Huawei, HiSilicon | **Proposal 2.2-2C)** Support  **Proposal 2.2-3C)** Support |
| CATT | **Proposal 2.2-3C) – cleaned up**  * For 480 and 960kHz PRACH when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ beam switching gap (if supported) can be placed within a PRACH slot (i.e., the number of ROs in the PRACH slot is not affected),   + When the ~~and~~ number of time domain PRACH slots in a reference slot is 1,     - for 480kHz and for 960kHz PRACH   + When the ~~And~~ when the number of time domain PRACH slots in a reference slot is 2,     - for 480kHz and for 960kHz PRACH * FFS: values when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ beam switching gap (if supported) cannot be placed within a PRACH slot (i.e., the number of ROs in the PRACH slot is affected). |
| InterDigital | We are fine with Proposal 2.2-2C and Proposal 2.2-3C. |
| Ericsson 2 | Here are comments on the 4th round proposals: **Proposal 2.2-2C) – cleaned up** Support **Proposal 2.2-3C) – cleaned up** We can accept this proposal with the following modifications. As we commented in the 3rd round, we disagree with Qualcomm's assertion that if the #ROs in the frequency domain has to be smaller (e.g., due to limited BW), then the RO density in the time domain should somehow be increased. In 60 GHz, the number of users in the same beam is expected to be low, hence it is not needed to configure a large number of ROs in the frequency domain in the first place.   * For 480 and 960kHz PRACH when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ beam switching gap (if supported) can be placed within a PRACH slot ~~(i.e., the number of ROs in the PRACH slot is not affected)~~,   + and number of time domain PRACH slots in a reference slot is 1,     - for 480kHz and for 960kHz PRACH   + And when the number of time domain PRACH slots in a reference slot is 2,     - for 480kHz and for 960kHz PRACH * FFS: values when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ beam switching gap (if supported) cannot be placed within a PRACH slot ~~(i.e., the number of ROs in the PRACH slot is affected)~~. |
| Sharp | We are fine with the proposals and support the further edits from Docomo. |
| LG Electronics | It seems that our previous 3rd round comments on the gap are not properly reflected for Proposal 2.2-2B. Therefore, we have copied the previous comments here again and hope to reflect them in the proposal.  The LBT gap should be considered in addition to the beam switching gap. As Samsung mentioned during GTW session, the short control signaling rules are not always applicable to the transmission of msg1/msgA since it depend on the local regulations. Furthermore, the necessity of LBT gap to the consecutive ROs in order to prevent LBT blocking between the UEs is not enough discussed yet. Therefore, we suggest to change the words “beam switching gap” in Proposal 2.2-2C and 2.2-3C to “the gap to account for LBT or beam switching gap”.  Regarding the number of RO in the time-frequency domain, we share the same view with Ericsson. We do not see the necessity of Qualcomm’s modifications in **green** that the frequency domain's RO should be compensated with additional ROs in the time domain because it may be reduced.  Therefore, we can support Proposal 2.2-3C with following modifications:   * For 480 and 960kHz PRACH when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ ~~beam switching~~ gap to account for LBT or beam switching gap (if supported) can be placed within a PRACH slot ~~(i.e., the number of ROs in the PRACH slot is not affected),~~   + and when number of time domain PRACH slots in a reference slot is 1,     - for 480kHz and for 960kHz PRACH   + And when the number of time domain PRACH slots in a reference slot is 2,     - for 480kHz and for 960kHz PRACH   FFS: values when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ ~~beam switching~~ gap to account for LBT or beam switching gap (if supported) cannot be placed within a PRACH slot ~~(i.e., the number of ROs in the PRACH slot is affected).~~ |
| ZTE, Sanechips | We are fine with Proposal 2.2-2C.  Since the “PRACH occasions” has been changed by “PRACH slots” in the sub-bullets, we are generally fine with Proposal 2.2-3C. We also think the “time domain PRACH slots” does not make sense, so we suggest the following modifications: **Proposal 2.2-3C) – cleaned up**  * For 480 and 960kHz PRACH when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ beam switching gap (if supported) can be placed within a PRACH slot (i.e., the number of ROs in the PRACH slot is not affected),   + When the ~~and~~ number of ~~time domain~~ PRACH slots in a reference slot is 1,     - for 480kHz and for 960kHz PRACH   + ~~And w~~When the number of ~~time domain~~ PRACH slots in a reference slot is 2,     - for 480kHz and for 960kHz PRACH * FFS: values when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ beam switching gap (if supported) cannot be placed within a PRACH slot (i.e., the number of ROs in the PRACH slot is affected). |
| Lenovo, Motorola Mobility | We support both proposals and further edits by ZTE for Proposal 2.2-2C. |
| Nokia | Proposal 2.2-2C) – cleaned up: We are OK with this proposal. Proposal 2.2-3C) – cleaned up: We would be OK with this proposal accounting the updates suggested by DCM or CATT, and the removal of the text in brackets proposed by Ericsson (2). |
| Intel | **Proposal 2.2-2C) – cleaned up.** Support**Proposal 2.2-3C) – cleaned up.** If the assumption that the numbers in the square brackets are kind of FFS, we’re Ok with the proposal |

#### **3rd Round Discussion Summary:**

Several companies have concerning comments on the addition of ‘maximum’. Moderator has updated Proposal in 2.2-2C.

**Proposal 2.2-2C)**

* For 480 and 960kHz PRACH:
  + ~~For a given configured number of frequency domain ROs,~~ at least the same ~~maximum~~ RO density in time domain (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
    - FFS: Support ~~resource~~ gap between consecutive ROs in time domain and ~~FFS~~ the details to derive the gap
    - ~~FFS whether this gap can be configured by gNB.~~

Between Proposal 2.2-3, 2.2-3A, and 2.2-3B. Proposal 2.2-3B seem to leave the most room for further discussions. Moderator has updated the proposal in 2.2-3D. There was an alternative proposal from Intel to resolve the issue for cases when gap is supported. Nokia’s suggestion to put in brackets to work this these numbers as working assumption might be a good approach.

**Proposal 2.2-3D)**

* For 480 and 960kHz PRACH when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ ~~beam switching~~ gap to account for LBT and/or beam switching gap (if supported) can be placed within a PRACH slot ~~(i.e., the number of ROs in the PRACH slot is not affected),~~
  + and when number of ~~time domain~~ PRACH slots ~~occasions~~ in a reference slot is 1,
    - for 480kHz and for 960kHz PRACH
  + and when the number of ~~time domain~~ PRACH slots ~~occasions~~ in a reference slot is 2,
    - for 480kHz and for 960kHz PRACH
* FFS: values when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and ~~potential~~ ~~beam switching~~ gap to account for LBT and/or beam switching gap (if supported) cannot be placed within a PRACH slot ~~(i.e., the number of ROs in the PRACH slot is affected)~~.

Company expressed objection/concern on Proposal 2.2-3B (and 2.2-3C/D):

* ZTE/Sanechips
  + The number of PRACh occasions in a slot depends on the PRACH format, so cannot understand why the PRACH slot location should depend on this.

#### **4th Round Discussion:**

Please continue to further provide comments based on Proposal 2.2-2C and 2.2-3C.

**Proposal 2.2-2C) – cleaned up**

* For 480 and 960kHz PRACH:
  + at least the same RO density in time domain (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
    - FFS: Support gap between consecutive ROs in time domain and the details to derive the gap

##### **Proposal 2.2-3D) – cleaned up**

* For 480 and 960kHz PRACH when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and gap to account for LBT and/or beam switching gap (if supported) can be placed within a PRACH slot~~,~~
  + and when number of PRACH slots in a reference slot is 1,
    - for 480kHz and for 960kHz PRACH
  + and when the number of PRACH slots in a reference slot is 2,
    - for 480kHz and for 960kHz PRACH
* FFS: values when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and gap to account for LBT and/or beam switching gap (if supported) cannot be placed within a PRACH slot.

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| Company | Comments |
| Qualcomm | Proposal 2.2-2C: fine  Proposal 2.2-3D: still not very clear on what does “*gap to account for LBT and/or beam switching gap (if supported) can be placed within a PRACH slot*” mean? We think it needs to be clarified. In addition, as for the higher SCS capacity, we think that due to lack of any evaluation on the RACH capacity needed for 480/960 SCS compared to 120 SCS, we should strive to keep the same capacity (RO’s in time x frequency) unless otherwise proven. This includes the case if gaps are used. |
| Lenovo, Motorola Mobility | Support for both proposals |
| Futurewei | Proposal 2.2-2C): support  Proposal 2.2-3D): support |
| Sharp | We are fine with both the proposals. |
| Ericsson | Proposal 2.2-2C:  Support  Proposal 2.2-3D:  Support.  Still disagree with Qualcomm's assertion on the need to potentially increase the time domain density for cases where it may not be possible to configure the full number of ROs (8) in the frequency domain. Use of a large number of frequency domain ROs for the 60 GHz band when typically analog beamforming would be used is not motivated. It will be very rare that there are so many users in the same beam to benefit from having a large number of FDM'd ROs. |
| ZTE, Sanechips | Proposal 2.2-2C): Support  Proposal 2.2-3D): We are generally fine with the proposal. The current wording on gap seems a bit confusing since LBT gap is FFS as well, so we suggest the following modifications: **Proposal 2.2-3D) – cleaned up**  * For 480 and 960kHz PRACH when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and gap (if supported) to account for LBT and/or beam switching ~~gap (if supported)~~ can be placed within a PRACH slot~~,~~   + and when number of PRACH slots in a reference slot is 1,     - for 480kHz and for 960kHz PRACH   + and when the number of PRACH slots in a reference slot is 2,     - for 480kHz and for 960kHz PRACH * FFS: values when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and gap (if supported) to account for LBT and/or beam switching ~~gap (if supported)~~ cannot be placed within a PRACH slot. |
| Interdigital | Proposal 2.2-2C) Support the proposal.  Proposal 2.2-3D) Support the proposal. |
| Nokia | Proposal 2.2-2C): Support.  Proposal 2.2-3D): Support.  We also share similar view as Ericsson in regards on the need to increase the frequency domain RO’s. |
| Intel | **Proposal 2.2-2C)** – Support.  **Proposal 2.2-3D)** – Acceptable with the assumption that the numbers in square brackets are FFS and could be adjusted based on further information |
| DOCOMO | Proposal 2.2-2C: Support  Proposal 2.2-3D: Support. |
| Samsung | Proposal 2.2-2C: could be fine, one question to clarify.  Since companies did not like the word “maximum”; then may I ask one clarification question. Does this proposal imply that for a given PRACH configuration index, if for example the 120khz RO density is 6 ROs at one slot; then in the new SCS slot, does it require the new SCS to have exactly 6 ROs per slot no matter what other conditions, e.g., collision or others? Or it only requires the originally configured RO number to be the same.  Proposal 2.2-3D: we are fine in principle, but we are not fine to already separate the gap-based criteria. Since the gap related discussion already listed in 2.2-2C, we can simplified the version.   * For 480 and 960kHz PRACH when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 ~~and gap to account for LBT and/or beam switching gap (if supported) can be placed within a PRACH slot,~~   + and when number of PRACH slots in a reference slot is 1,     - for 480kHz and for 960kHz PRACH   + and when the number of PRACH slots in a reference slot is 2,     - for 480kHz and for 960kHz PRACH * FFS: the impact of gap (if supported)  ~~values when number of time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 and gap to account for LBT and/or beam switching gap (if supported) cannot be placed within a PRACH slot.~~ |

#### **4th Round Discussion Summary:**

Proposal 2.2-2C seems to be agreeable by all. Moderator will suggest agreeing to this proposal over email.

There was a question from Samsung on removal of ‘maximum’. Moderator would like to here companies inputs on the question. Moderator assumes if RO is determined be invalid, we skip over them, which is what existing NR specification has done. Of course, this is moderator’s understanding. If would be good to get clarification from other companies on this.

Proposal 2.2-3D may require further clarification. Moderator has updated Proposal 2.2-3D based on comments.

As for Qualcomm’s comments on PRACH overall capability in a unit time/frequency resource. Moderator is not sure how to address them in Proposal 2.2-3E, since the proposal only discusses the configuration of values for a given PRACH configuration. If Qualcomm can suggest text for a proposal, moderator will add it as another proposal.

**Proposal 2.2-3E)**

* For 480 and 960kHz PRACH,
  + when a PRACH slot contains all number of time domain PRACH occasions, corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211, and gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching ~~gap~~ ~~(if supported)~~ ~~can be placed within a PRACH slot,~~
    - and when number of PRACH slots in a reference slot is 1,
      * for 480kHz and for 960kHz PRACH
    - and when the number of PRACH slots in a reference slot is 2,
      * for 480kHz and for 960kHz PRACH
  + FFS: values when a PRACH slot cannot contain all number of time domain PRACH occasions, corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211, and gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching ~~gap (if supported)~~ ~~cannot be placed within a PRACH slot~~.

#### **5th Round Discussion Summary – part 1:**

Please comment on the proposal 2-2-2C **only if you have serious concerns**. Moderator will ask for email approval for the stable proposal.

Also please provide inputs to Samsung’s question “Does this proposal imply that for a given PRACH configuration index, if for example the 120khz RO density is 6 ROs at one slot; then in the new SCS slot, does it require the new SCS to have exactly 6 ROs per slot no matter what other conditions, e.g., collision or others? Or it only requires the originally configured RO number to be the same.”

Moderator assumes the RO density is referring to what is configured and not referring to “valid PRACH occasions”, which is something entirely different. With that said, if companies have different understanding, please comment as well.

##### **Proposal 2.2-2C)**

* For 480 and 960kHz PRACH:
  + at least the same RO density in time domain (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
    - FFS: Support gap between consecutive ROs in time domain and the details to derive the gap

Updated 2.2-2C to Proposal 2.2-2D based on Samsung’s comments. Hopefully this should not be an issue as it seems to simply add clarity.

**Proposal 2.2-2D)**

* For 480 and 960kHz PRACH:
  + at least the same RO density in time domain (i.e. number of configured RO per reference slot according the PRACH configuration index)as for 120kHz PRACH in FR2 is supported
    - FFS: Support gap between consecutive ROs in time domain and the details to derive the gap

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| Company | Comments |
| Samsung | Thx FL provides the understanding which is also common to us, companies might get busy when meeting approaching to the end, so we suggest one clarifying change, to see if ok   * For 480 and 960kHz PRACH:   + at least the same RO density in time domain (i.e. number of configured RO per reference slot according the PRACH configuration index) as for 120kHz PRACH in FR2 is supported     - FFS: Support gap between consecutive ROs in time domain and the details to derive the gap |

#### **5th Round Discussion Summary – part 2:**

Please provide further comments on Proposal 2.2-3E. Hopefully is this bit clearer.

As for Qualcomm’s comments on PRACH overall capability in a unit time/frequency resource. Moderator is not sure how to address them in Proposal 2.2-3E, since the proposal only discusses the configuration of values for a given PRACH configuration. If Qualcomm can suggest text for a proposal, moderator will add it as another proposal.

##### **Proposal 2.2-3E)**

* For 480 and 960kHz PRACH,
  + when a PRACH slot contains all number of time domain PRACH occasions, corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211, and gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching,
    - and when number of PRACH slots in a reference slot is 1,
      * for 480kHz and for 960kHz PRACH
    - and when the number of PRACH slots in a reference slot is 2,
      * for 480kHz and for 960kHz PRACH
  + FFS: values, when a PRACH slot cannot contain all number of time domain PRACH occasions, corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211, and gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching.

Updated based on comments received.

**Proposal 2.2-3F)**

* For 480 and 960kHz PRACH,
  + when a PRACH slot can contain~~s~~ all ~~number of~~ time domain PRACH occasions~~,~~ corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211~~,~~ including ~~and~~ gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching,
    - and when number of PRACH slots in a reference slot is 1,
      * for 480kHz and for 960kHz PRACH
    - and when the number of PRACH slots in a reference slot is 2,
      * for 480kHz and for 960kHz PRACH
  + FFS: values, when a PRACH slot cannot contain all ~~number of~~ time domain PRACH occasions~~,~~ corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211~~,~~ including ~~and~~ gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching.
  + FFS: whether to allow for additional values if the maximum that can be configured for the number of FD RO’s is less than 8 (due to BW limitation)

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| Company | Comments |
| Qualcomm | Proposal 2.2-3E: may be the following FFS can be added as a bullet to the end of the proposal:  *FFS: whether to allow for additional values if the maximum that can be configured for the number of FD RO’s is less than 8 (due to BW limitation)* |
| Ericsson | Support with the following editorial changes for clarity:   * For 480 and 960kHz PRACH,   + when a PRACH slot can contain~~s~~ all ~~number of~~ time domain PRACH occasions~~,~~ corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211~~,~~ including ~~and~~ gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching,     - and when number of PRACH slots in a reference slot is 1,       * for 480kHz and for 960kHz PRACH     - and when the number of PRACH slots in a reference slot is 2,       * for 480kHz and for 960kHz PRACH   + FFS: values~~,~~ when a PRACH slot cannot contain all ~~number of~~ time domain PRACH occasions~~,~~ corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211~~,~~ including ~~and~~ gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching.   We think the FFS suggested by Qualcomm is not needed, since we don't see the value in increasing the number of time domain ROs in case fewer frequency domain ROs can be configured. As we stated before, for 60 GHz with analog beamforming (one gNB receive beam at a time), the probability of multiple UEs in the same beam attempting RACH simultaneously is very low, hence a small number of FD RACH occasions would be configured anyway. The same discussion has happened in other agenda items – e.g., 8.2.3 PUCCH Enhancements, where it was explicitly agreed that user multiplexing is not a priority due to the low probability of multiple users sharing the same beam.  That being said, since it's only an FFS, we can live with it, but we really think this is a non-issue, and we don't think time should be spent on it. |
| Nokia | We would support the editorials from Ericsson for readability, but if wanted changes could also be minimized as follows:  “…PRACH slot contains all ~~number of~~ time domain PRACH occasions…”?  “…PRACH slot cannot contain all ~~number of~~ time domain…” |
| Moderator | Updated based on comments. |

#### **5th Round Discussion Summary:**

**Part 1 discussion)**

Suggest approving Proposal 2.2-2D over email.

**Part 2 discussion)**

Moderator suggest checking whether Proposal 2.2-3F is acceptable and further discuss on the proposal.

##### **Proposal 2.2-3F) – cleaned up**

* For 480 and 960kHz PRACH,
  + when a PRACH slot can contain all time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching,
    - and when number of PRACH slots in a reference slot is 1,
      * for 480kHz and for 960kHz PRACH
    - and when the number of PRACH slots in a reference slot is 2,
      * for 480kHz and for 960kHz PRACH
  + FFS: values, when a PRACH slot cannot contain all time domain PRACH occasions~~,~~ corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching.
  + FFS: whether to allow for additional values if the maximum that can be configured for the number of FD RO’s is less than 8 (due to BW limitation)

#### **6th Round Discussion – part 1:**

Moderator suggest to approve Proposal 2.2-2D over email. Please comment if you have concerns.

##### **Proposal 2.2-2D) – suggest for email approval**

* For 480 and 960kHz PRACH:
  + at least the same RO density in time domain (i.e. number of configured RO per reference slot according the PRACH configuration index)as for 120kHz PRACH in FR2 is supported
    - FFS: Support gap between consecutive ROs in time domain and the details to derive the gap

|  |  |
| --- | --- |
| Company | Comments |
| Qualcomm | We are ok with the proposal |
| Huawei, HiSilicon | We are OK with **Proposal 2.2-2C)**  We are also OK with **Proposal 2.2-2D)** with the following change as ROs are specified and not configured. So, we suggest the following change in Proposal 2.2-2D):   * For 480 and 960kHz PRACH:   + at least the same RO density in time domain (i.e. number of ~~configured~~ specified RO per reference slot according the PRACH configuration index) as for 120kHz PRACH in FR2 is supported     - FFS: Support gap between consecutive ROs in time domain and the details to derive the gap |

#### **6th Round Discussion – part 2:**

Please comment further on Proposal 2.2-3F. if the proposal is stable, moderator suggest to approve the proposal over email.

##### **Proposal 2.2-3F) – potentially for email approval**

* For 480 and 960kHz PRACH,
  + when a PRACH slot can contain all time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching,
    - and when number of PRACH slots in a reference slot is 1,
      * for 480kHz and for 960kHz PRACH
    - and when the number of PRACH slots in a reference slot is 2,
      * for 480kHz and for 960kHz PRACH
  + FFS: values, when a PRACH slot cannot contain all time domain PRACH occasions~~,~~ corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching.
  + FFS: whether to allow for additional values if the maximum that can be configured for the number of FD RO’s is less than 8 (due to BW limitation)

|  |  |
| --- | --- |
| Company | Comments |
| Qualcomm | We are ok with the proposal |
| Huawei, HiSilicon | We can support **Proposal 2.2-3F** |

#### **6th Round Discussion Summary:**

To be filled.

### 2.2.3 RAR Window & RA Preamble ID

* From [1] Huawei/HiSilicon:
  + Introduce additional bits in the DCI scheduling RAR to resolve the issue of RA-RNTI/MsgB-RNTI calculation for 480 kHz and 960 kHz RACH procedure.
  + Support maximum of 40 ms for ra-ResponseWindow for operation with shared spectrum and msgB-ResponseWindow for both operations with and without shared spectrum. Support indicating two LSBs of SFN at which gNB has received msg1 (MsgA) in DCI format 1\_0 with CRC scrambled by RA-RNTI (MsgB-RNTI).
* From [2] vivo:
  + For larger PRACH SCS (480KHz/960KHz), the following options can be considered for RA-RNTI calculation:
    - Alt.1: Modify the RA-RNTI formula as following and introduce some contention resolution mechanism to resolve the conflict.
      * RA-RNTI = (1+s\_id+14×t\_id+14×X×f\_id +14×X×8×ul\_carrier\_id) mod A
    - Alt.2: Reuse the current RA-RNTI formula while introducing additional indicator field to indicate the time-frequency resource together with RA-RNTI.
    - Alt.3: Depending on the RO configuration pattern, reuse/modify the RA-RNTI formula and express the slot indexes t\_id based on a new specific subcarrier spacing.
* From [8] CATT:
  + For supporting Msg1 transmission with 480 KHz/960 KHz SCS, RA-RNTI is divided into two parts. One part of RA-RNTI is carried by DCI, and the remaining 16-bit of RA-RNTI could be used to scramble CRC of the DCI1. Two possible options are:
    - Option A:
      * RA-RNTI = (1 + s\_id + 14 × t\_id + 14 ×× f\_id + 14 × × 8 × ul\_carrier\_id) mod
      * inDCI\_bit = floor ((1 + s\_id + 14 × t\_id + 14 ×× f\_id + 14 × × 8 × ul\_carrier\_id) /)
      * s\_id is the index of the first OFDM symbol of the PRACH occasion (0 ≤ s\_id < 14)
      * t\_id is the index of the first slot of the PRACH occasion in a system frame (0 ≤ t\_id < 640)
    - Option B:
      * RA-RNTI = 1 + s\_id + 14 ×(t\_id mod 80) + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id
      * inDCI\_bit =
      * s\_id is the index of the first OFDM symbol of the PRACH occasion (0 ≤ s\_id < 14)
      * t\_id is the index of the first slot of the PRACH occasion in a system frame (0 ≤ t\_id < 640)
* From [9] ZTE/Sanechips:
  + For higher PRACH SCS (480 and/or 960 kHz), consider the following options for further down-selection of RA-RNTI enhancements:
    - Option 2)
      * Segment the PRACH into N segments
      * Non-overlapping PRACH slot location in each segment(80 slots)
    - Option 3)
      * Segment the PRACH into N segments
      * is the index of the PRACH slot that contains the PRACH occasion in a segment.
      * In DCI: RA-indication = Segment index
    - Option 7)
      * is the index of the first 120kHz slot that contains the PRACH occasion in a system frame.
      * is the index of the first OFDM symbol of the PRACH occasion based on the value of specified in clause 5.3.2 of TS 38.211.
* From [10] Fujitsu:
  + For 480kHz and 960kHz PRACH, the following should be considered to uniquely identify a RO:
    - When calculating RA-RNTI, t\_id is determined in a way that more than one slot can have the same t\_id; and
    - DCI scheduling RAR indicates the local index among the slots having the same t\_id.
* From [11] Ericsson:
  + For 480/960 kHz PRACH, reuse the RA-RNTI expressions from Rel-15/16, with the additional statement that for 480/960 kHz PRACH, t\_id should be determined based on a subcarrier spacing of 120 kHz.
  + Postpone further discussions of RA-RNTI design until the PRACH configuration design is settled.
* From [13] Nokia:
  + Reuse RA-RNTI formula defined for 120 kHz SCS also for the cases PRACH is configured with 480 or 960 kHz SCS where
    - assumes 480/960 kHz SCS
    - assumes 120 kHz SCS
* From [19] LG Electronics:
  + If the reference slot SCS remains as 60 kHz and the density of PRACH occasion is the same as in 120 kHz in the time-domain (e.g., 2 slots out of 8 slots for 480 kHz), the existing RA-RNTI/MSGB-RNTI equation can be reused for 480 and 960 kHz SCS by reinterpreting the slot indexes t\_id based on a new specific subcarrier spacing as the slot indexes of 120 kHz SCS (e.g., floor(t\_id/n) where n=4 for 480 kHz SCS and n=8 for 960 kHz).
  + If the reference slot SCS remains as 60 kHz and the density of PRACH occasion is increased compared to 120 kHz in the time-domain, to calculate RA-RNTI/MSGB-RNTI associated with the PRACH occasion for 480 and 960 kHz SCS using the existing RA-RNTI equation, the following options can be considered:
    - Option 1: Divide the RAR window for RA-RNTI (or msg2 window for MSGB-RNTI) into N sub-periods (where each sub-period is 80 slots using the used SCS) + signal the sub-period index using the DCI that schedules the MSG2/MSGB.
    - Option 2: Divide the frequency index or the symbol index into M subset (if M=4, the subset index 0/1/2/3 can be configured to the frequency index {0, 1}, {2, 3}, {4, 5}, {6, 7}, respectively) + signal the subset index using the DCI that schedules the MSG2/MSGB
* From [20] ETRI:
  + Propose to reuse the current equation with minor modifications for RA preamble ID calculation.
    - RA-RNTI = 1 + s\_id + 14 × t\_id + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id
      * t\_id is the index of 120kHz slot that contains RO in a system frame
      * s\_id is the index of the first OFDM symbol of RO based on the value of specified in clause 5.3.2 of TS 38.211
* From [22] Intel:
  + RA-RNTI computation equation should be adjusted to avoid overflow in case of PRACH SCS 480 kHz and 960 kHz;
  + Support the following modified equation for RA-RNTI computation:
    - ,
    - where t\_id is based on the value of specified in clause 5.3.2 of TS 38.211.
* From [23] Apple:
  + modifying the existing calculation equation or redefine t\_id based on 120kHz SCS to solve the RA-RNTI overflowing problem:
* From [24] Sharp:
  + Assuming RO density per reference slot is unchanged, without modifying the formula and definition of s\_id. Modify the definition of t\_id as the slot index referring to 120kHz SCS.

#### Summary of Contribution Discussions

The following list of options are from last meetings discussion.

|  |
| --- |
| * + **Plain Modulus Category**     - Option 1)   + **PRACH Sub-segmentation Method Category**     - Option 2)       * Segment the PRACH into N segment       * Non-overlapping PRACH slot location in each segment(80 slots)       * ~~The same PRACH slot location in each 120kHz slot duration~~     - Option 3)       * Segment the PRACH into N segments       * is the index of the PRACH slot that contains the PRACH occasion in a segment.       * In DCI: RA-indication = Segment index     - Option 4)       * Segment the PRACH into N segments       * In DCI:     - Option 5)       * Segment the PRACH into N segments       * In DCI:     - Option 6)       * In DCI:   + **Compressing some indices Category (may require a matching RO configuration to work properly)**     - Option 7)       * is the index of the first 120kHz slot that contains the PRACH occasion in a system frame.       * is the index of the first OFDM symbol of the PRACH occasion based on the value of specified in clause 5.3.2 of TS 38.211.     - Option 8)       * RA-RNTI = 1 + s\_id + 14 × floor(t\_id / ) + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id,       * t\_id is based on the value of specified in clause 5.3.2 of TS 38.211. |

The following is summary of company views.

* Alt 1) Plain Modulus Category, some example in option 1
  + Vivo, Apple
* Alt 2) PRACH Sub-segmentation Method Category, some examples in option 2 ~ 6
  + Huawei/HiSilicon, vivo, CATT, ZTE/Sanechips, Fujitsu, LGE
* Alt 3) Compressing some indices Category (may require a matching RO configuration to work properly) , some examples in option 7 ~ 8
  + vivo, ZTE/Sanechips, Ericsson, Nokia/NSB, ETRI, Intel, Sharp

#### **1st Round Discussion:**

Moderator suggest to further discuss the three categories and the detailed options.

|  |  |
| --- | --- |
| Company | Comments |
| Qualcomm | Although requires some extra signaling, but we prefer Alt2.  For Alt 1, the RA-RNTI can be more than FFFF and modular operation needs to be applied. Due to the modular operation, some ROs:   * May have the same RA-RNTI * May collide with FFF0–FFFD (reserved) or P-RNTI (FFFE) or SI-RNTI (FFFF)   Hence, some restrictions need to be applied:   * ROs with RA-RNTI conflicting with the pre-allocated RNTIs should not be used. * When multiple ROs have the same RA-RNTI but not conflicting with the pre-allocated RNTIs, only one of the ROs can be used (e.g., the first RO among those ROs with the same RA-RNTI) or rely on the existing contention resolution mechanisms   For Alt3, some restrictions may be needed to the RO design for it to work |
| Fujitsu | 1. For down selection of options for RA-RNTI calculation, the impact on MSBG-RNTI should be considered. For example, if RA-RNTI is calculated by Alt 1), additional method may be needed for handling collision between RA-RNTI and MSBG-RNTI. From this perspective, Alt 1) is not preferred. Then between Alt 2) and Alt 3), considering flexibility, Alt 2) is preferred.  2. It seems that option 2) should belong to Alt 3) rather than Alt 2). |
| Sharp | We prefer Alt 3 which provides a simple solution with minor specification impact. |
| ZTE, Sanechips | Alt 2 and Alt 3 both work for us.  To better align with the category, Option 2 can be modified as   * Option 2)   + Segment the PRACH into N segments   + Non-overlapping PRACH slot location in each segment(80 slots)   Option 2 can be categorized in either Alt 2) or Alt 3), since it also requires some compression and relies on the RO configuration. |
| Nokia | While we prefer Alt 3, it might be best to wait the conclusion in Section 2.2.2 |
| Samsung | Alt. 3 seems fine.  One simple way is actually, the t\_id could be the logical order index of the PRACH slot. Because based on previous design, the PRACH slot density anyway will not be larger than 80 (i.e., the max one in 120khz case); |
| Lenovo, Motorola Mobility | We support Alt 3. |
| Intel | This decision could be made after the agreement on RACH occasion resources configuration as it may impact parameters constituting RA-RNTI calculation formula (e.g., s\_id and t\_id). |
| Futurewei | We prefer Alt 2, Option 6 |
| Ericsson | Defer until agreement on RO configuration is achieved.  Assuming Option-1 + Alt-1 is adopted, then we observe the following:  Similar to Rel‑15/16, a maximum of one PRACH slot can occur within the duration of a 120 kHz slot, thus the expression for computing RA-RNTI in Rel‑15/16 can be directly reused, with the additional statement that for PRACH subcarrier spacings 480/960 kHz, t\_id should be calculated based on a subcarrier spacing of 120 kHz. |
| LG Electronics | This issue depends on the result of the discussion in the RO configuration for PRACH density in the previous section. We support Alt 3 if the density of PRACH occasion is the same as in 120 kHz in the time-domain (e.g., 2 slots out of 8 slots for 480 kHz), and if the higher density of PRACH occasion is supported, then Option 3 in Alt 2 can be considered. |
| Huawei/HiSilicon | We prefer Alt 2 category:   * It is more straightforward at least because it is usable independent of the parallel discussion of PRACH design and it is forward compatible. * If RA-RNTI formula needs to change, the discussion may actually need to be made in RAN2 as RA-RNTI formula is introduced in 38.321. However, if RA-RNTI ambiguity issue is resolved using, eg, segmentation, then, only adding 3 bits in DCI is required. In such a case, the discussion can be made in RAN1.   Finally, note that the issue of extending RAR window length was resolved in NR-U by adding 2 bits in DCI which, conceptually, is similar to Alt 2. |

#### **1st Round Discussion Summary:**

Here is the summary of company views.

* Alt 1) Plain Modulus Category, some example in option 1
  + Vivo, Apple
* Alt 2) PRACH Sub-segmentation Method Category, some examples in option 2 ~ 6
  + Huawei/HiSilicon, vivo, CATT, ZTE/Sanechips, Fujitsu, LGE (if higher density than 2 is supported), Futurewei, Qualcomm
* Alt 3) Compressing some indices Category (may require a matching RO configuration to work properly) , some examples in option 7 ~ 8
  + vivo, ZTE/Sanechips, Ericsson, Nokia/NSB, ETRI, Intel, Sharp, LGE, Lenovo/Motorola Mobility, Samsung

Company views are somewhat split between Alt 2 and 3. Alt 3 has more supporting companies. At the same time several companies commented that this can be discussed once the RO density for PRACH is concluded.

#### **2nd Round Discussion:**

Moderator suggests continuing discussion on RA-RNTI issue and try to conclude after PRACH RO definition and density discussion has been sufficiently resolved. Please continue to provide comments.

|  |  |
| --- | --- |
| Company | Comments |
| vivo | Support moderator’s suggestion |
| ZTE, Sanechips | Fine with moderator’s suggestion. |
| Samsung | We are ok with moderator’s assessment. |
| Intel | Let’s wait for agreements on PRACH Occasions configuration. |
| Apple | Support moderator’s suggestion. |
| Qualcomm | Support moderator’s suggestion |
| Sharp | Agree with moderator’s suggestion. |
| Futurewei | Fine to discuss further. |
| Huawei, HiSilicon | OK with the proposal |

#### **2nd Round Discussion Summary:**

No summary was made by Moderator.

#### **3rd Round Discussion:**

Continue to provide inputs.

|  |  |
| --- | --- |
| Company | Comments |
| - | - |

No further comments received.

#### **Final Discussion Summary:**

No additional comments were provided. Moderator assumes following conclusion is acceptable and no need to explicitly agree (in GTW) the follow conclusion as it should not impact further RAN1 work in RAN1 #106-e.

Moderator conclusion:

* Deprioritize discussion on RA-RNTI issue in RAN1 #106-e and try to conclude this issue after PRACH RO definition and density discussion has been sufficiently resolved.

### 2.2.4 Other aspects on PRACH

* From [12] Futuerwei:
  + If the UE RACH transmission can be LBT exempt under the short control signaling exclusion, support signaling to indicate UE that LBT is disabled or enabled for the RACH procedure.
* From [13] Nokia/NSB:
  + Discuss whether 960 kHz SCS PRACH procedure is supported from IDLE/Inactive state.

#### Summary of Contribution Discussions

The following are issues that were mentioned by companies.

* Short control signal exemption applicability for PRACH
* Whether 960kHz PRACH is supported for IDLE/inactive state.

#### **1st Round Discussion:**

Moderator assumes applicability of short control signal exemption will be discussed under channel access agenda. Moderator suggest companies to provide comments on the following issue.

* Whether 960kHz PRACH is supported for IDLE/inactive state

If there are other issues that require further discussion, please comment here as well.

|  |  |
| --- | --- |
| Company | Comments |
| Qualcomm | Initial access SSB (and hence PRACH) is limited to 480 kHz. We think this is outside the RAN1 and RAN agreements so far. |
| Nokia | As the physical layer functionality/design for CBRA will be in place/needed for CONNECTED mode operation, we don’t see reason why this should be excluded. In respect to WID, the definition of initial access was not ever clearly concluded for PRACH, while for DL/SSB it was considered in RAN1#104e as:   |  | | --- | | * + - “SSB in non-initial access” here refers to:       * SSB in Scell, where gNB is able to provide assistance information (e.g. SSB center frequency, SCS, etc)       * SSB for neighbor cell RRM measurements, where information is provided by gNB).     - “SSB in initial access” here refers to       * SSB used for “Cell Selection” defined in TS38.133 Section 4.1, which includes stored information cell selection and initial cell selection. | |
| Futurewei | We agree with Qualcomm, 960 kHz SCS PRACH for IDLE/inactive initial access is not supported. |
| Ericsson | Agree with Qualcomm |
| LG Electronics | We also agree with Qualcomm.  Since the 480 kHz SCS SSB was agreed to be supported for the initial access in RAN#92-e, the 480 kHz SCS PRACH can also be supported for the initial access in addition to the 120kHz SCS PRACH while the 960 kHz SCS PRACH is only supported for the non-initial access case. For use cases of 960 kHz SCS PRACH, the PRACH sequence with L=139 for 960 kHz SCS may not provide enough coverage for the initial access use case because the OFDM symbol duration becomes shorter with larger SCS. In addition, in order to support the RACH procedure of the active bandwidth part after initial access, PRACH SCS aligned with data SCS may be beneficial. Therefore, the 960 kHz SCS PRACH can be used for the cases other than initial access (e.g., for SCell) where the coverage is not a concern. |
| Huawei/HiSilicon | We don’t think this issue needs to be discussed but if this has to be discussed, our view is closer to Qualcomm’s view. |
| Samsung | The agreement of supporting 480 kHz SSB and 480 kHz CORESET#0 is only for the configuration by MIB. We believe it needs clarification on whether 960 kHz can be configured for initial BWP as configured by SIB1, and we don’t think this issue was discussed before. After that, the SCS of PRACH should be clear. |

#### **1st Round Discussion Summary:**

Further discussion seems necessary.

#### **2nd Round Discussion:**

Continue discussion.

|  |  |
| --- | --- |
| Company | Comments |
| - | - |

No further comments received.

#### **2nd Round Discussion Summary:**

No summary was made by Moderator.

#### **3rd Round Discussion:**

Continue to provide inputs.

|  |  |
| --- | --- |
| Company | Comments |
| - | - |

No further comments received.

#### **Final Discussion Summary:**

No additional comments were provided. Moderator assumes following conclusion is acceptable and no need to explicitly agree (in GTW) the follow conclusion as it should not impact further RAN1 work in RAN1 #106-e.

Moderator conclusion:

* Deprioritize discussion on the following issues in RAN1 #106-e and continue discussion once other issues in initial access have been resolved
  + Whether 960kHz PRACH is supported for IDLE/inactive state.

## 2.3 Others Aspects

* From [3] Spreadtrum:
  + The SSB-based TRS/CSI-RS validation can be supported.
* From [11] Ericsson:
  + The current RSSI and CO measurement in Rel-16 should be enhanced to support NR unlicensed operation in the spectrum beyond 52.6 GHz in Rel-17. The enhancement at least includes extension of reference SCS and indication of channel bandwidth. The enhancement details of the RRC configuration for RSSI and CO measurement should be decided by RAN2.
* From [12] Futurewei:
  + In 60 GHz shared spectrum band, where the LBT is enabled, allow a COT a gap between consecutive transmissions of at least one slot 480 kHz SCS duration (32us) without LBT.
  + Consider using CSI-RS presence in the discovery burst for possible ways to implement beam refinement during the initial channel access.
* From [13] Nokia:
  + It is proposed that RAN1 discusses whether IDLE mode procedures (camping, reselection) are supported for 960kHz sub-carrier spacing.
* From [7] Samsung:
  + RAN1 clarifies that the configurable SCS for initial BWP configured by SIB1 can be 120 kHz, 480 kHz, and 960 kHz.

#### Summary of Contribution Discussions

The following are issues that were mentioned by companies.

* The SSB-based TRS/CSI-RS validation can be supported.
* The current RSSI and CO measurement in Rel-16 should be enhanced to support NR unlicensed operation in the spectrum beyond 52.6 GHz in Rel-17. The enhancement at least includes extension of reference SCS and indication of channel bandwidth. The enhancement details of the RRC configuration for RSSI and CO measurement should be decided by RAN2.
* In 60 GHz shared spectrum band, where the LBT is enabled, allow a COT a gap between consecutive transmissions of at least one slot 480 kHz SCS duration (32us) without LBT.
* Consider using CSI-RS presence in the discovery burst for possible ways to implement beam refinement during the initial channel access.
* It is proposed that RAN1 discusses whether IDLE mode procedures (camping, reselection) are supported for 960kHz sub-carrier spacing.
* RAN1 clarifies that the configurable SCS for initial BWP configured by SIB1 can be 120 kHz, 480 kHz, and 960 kHz.

#### **1st Round Discussion:**

Moderator suggest to continue discussion on the above issues.

If there are other issues that require further discussion, please comment here as well.

|  |  |
| --- | --- |
| Company | Comments |
| Nokia | The consideration related to support of the IDLE mode procedures for 960kHz relates also to the discussion in Section 2.2.4 |
| Samsung | One of our proposals is missing from the summary (added above), which is related to PRACH SCS in IDLE/INACTIVE, but not limited. Actually we want to clarify the SCS of initial DL/UL BWP configured by SIB1 (the one configured by MIB is clear). If this issue is clarified, we believe the applicable SCS for PRACH in IDLE/INACTIVE is also clear. Based on current agreement, we didn’t see 960 kHz cannot be configured for SCS of initial DL/UL BWP configured by SIB1. |
| Futurewei | 960 kHz support in IDLE/INACTIVE. Same as 2.2.4 We do not see it in the scope of the discussions. We should discuss all other items. |

#### **1st Round Discussion Summary:**

Further discussion seems necessary for the other issues listed.

#### **2nd Round Discussion:**

Continue discussion.

|  |  |
| --- | --- |
| Company | Comments |
| - | - |

No comments received during 2nd round of discussion.

#### **2nd Round Discussion Summary:**

No summary was made by Moderator.

#### **3rd Round Discussion:**

Continue to provide inputs.

|  |  |
| --- | --- |
| Company | Comments |
| - | - |

No comments received during 3rd round of discussion.

#### **Final Discussion Summary:**

No additional comments were provided. Due to lack of comments and discussion, Moderator suggests to de-prioritize the discussion until other issues in initial access have been resolved in RAN1 #106-e.

# Summary of Proposed Agreements/Conclusions

The following are proposals that moderator would like to suggest for email approval.

##### **Proposal 1.1-4B)**

* For DBTW with 120kHz SCS (if supported), support DBTW lengths {0.5, 1, 2, 3, 4, 5} msec
  + Note: this should be the same as Rel-16 NR-U DBTW lengths.

##### **Proposal 1.1-2E)**

* No indication for licensed and unlicensed operation in MIB
  + Whether and/or how LBT/No-LBT is indicated is separately discussed
* Use of LBT is not indicated in MIB.
  + FFS where and how this is indicated, e.g. SIB1
* For both licensed or unlicensed operation and with or without LBT, support the same DCI size for:
  + DCI format 1\_0 ~~scrambled with SI-RNTI~~ monitored in a common search space
    - Note: existing bit padding/truncation rules are assumed to applied for DCI format 0\_0 monitored in common search space.
  + FFS for other cases

##### **Proposal 1.1-3E)**

* For supported SCS cases of DBTW, support configuration of in MIB, down-select among the following alternatives (after number of candidate SSB positions have been determined).
  + Alt 1: total of 2 states of values are supported
    - FFS the exact values e.g. {16,64} or {32,64}
    - Note: value of 64 (if supported) may be used as implicit determination by the UE that DBTW is not enabled by gNB if maximum number of candidate SSB is 64
  + Alt 2: total of 4 states (including any potential reserved state) of values are supported
    - FFS on the values, e.g. {8,16,32,64}
    - FFS whether or not a single state will be reserved to explicitly indicate that DBTW is disabled e.g. (e.g. {16, 32, 64, reserved/DBTW disabled})
      * Note: value of 64 may be used as implicit determination by the UE that DBTW is not enabled by gNB if maximum number of candidate SSB is 64; or single state may be reserved e.g. (e.g. {16, 32, 64, DBTW disabled}) to explicitly indicate that DBTW is disabled

##### **Proposal 1.3-2C)**

* For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support the following set of parameters.

|  |  |  |
| --- | --- | --- |
| SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols |
| 1 | 24 | 2 |
| 1 | 48 | 1 |
| 1 | 48 | 2 |

* + - Note: the number of entries corresponding the same {mux pattern, number of RB, number of symbol} tuple (listed above) will depend on required RB offsets that needs to be supported based on channel and sync raster design.
  + FFS: addition other set of parameters

##### **Proposal 1.3-3C)**

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
  + Support the following set of parameters are supported for SS/PBCH block and CORESET multiplexing pattern 1:

|  |  |  |
| --- | --- | --- |
| Number of search space sets per slot |  | **First symbol index** |
| 1 | 1 | 0 |
| 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 1 | 2 | 0 |

* + - FFS: whether third row above needs to be updated to {0, if  is even}, {**+X**, if  is odd}, where X is X>= 0 and FFS
    - Note: the number of entries corresponding the same {number of SS per slot, M, first symbol index} tuple (listed above) will depend on supported ‘O’ for each tuple.
    - For the support values of ‘O’ (as part of supported combination of {‘O’, number of SS per slot, M, first symbol index} tuple support either Alt 1, 2, or 3
      * Alt 1:
        + Adopt same Table 13-12 for 120/480/960 kHz SCS
      * Alt 2:
        + Adopt same Table 13-12 for 120 kHz SCS. For 480 and 960 kHz, re-interpret offsets as O = O’/X1 and O = O’/X2, respectively, where O’ are values of O from Table 13-12.

FFS for X1 and X2

FFS on whether it applied to all O’ values or some subset of O’ values

* + - * Alt 3: O is from the set {0, 5, 2.5, 5+2.5} for 120 kHz, {0, 5, 2.5/X1, 5+2.5/X1} for 480 kHz, and {0, 5, 2.5/X2, 5 + 2.5/X2} for 960 kHz.

FFS for X1 and X2

##### **Proposal 2.1-1A)**

* Do not support PRACH length L=571, 1151 for 960kHz PRACH and at least L =1151 for 480kHz PRACH.

##### **Proposal 2.2-2D)**

* For 480 and 960kHz PRACH:
  + at least the same RO density in time domain (i.e. number of configured RO per reference slot according the PRACH configuration index)as for 120kHz PRACH in FR2 is supported
    - FFS: Support gap between consecutive ROs in time domain and the details to derive the gap

##### **Proposal 2.2-3F)**

* For 480 and 960kHz PRACH,
  + when a PRACH slot can contain all time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching,
    - and when number of PRACH slots in a reference slot is 1,
      * for 480kHz and for 960kHz PRACH
    - and when the number of PRACH slots in a reference slot is 2,
      * for 480kHz and for 960kHz PRACH
  + FFS: values, when a PRACH slot cannot contain all time domain PRACH occasions~~,~~ corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching.
  + FFS: whether to allow for additional values if the maximum that can be configured for the number of FD RO’s is less than 8 (due to BW limitation)

# Summary of Agreements/Conclusions from RAN1 #106-e

#### **Conclusion from GTW (Week 1 - Thursday):**

**Conclusion:**

RAN1 will continue discussion to develop solutions for supporting DBTW.

**Agreement:**

* For 480 and 960kHz PRACH:
  + The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.



#### **Conclusion from GTW (Week 2 - Monday):**

**Agreement:**

* For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, X} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame.
  + Alt 1: X = 8
  + Alt 2: X = 9

#### **Conclusion from GTW (Week 2 - Wednesday):**

# Reference

1. R1-2106442, “Initial access signals and channels for 52-71GHz spectrum,” Huawei, HiSilicon
2. R1-2106579, “Discussions on initial access aspects for NR operation from 52.6GHz to 71GHz,” vivo
3. R1-2106692, “Discussion on initial access aspects for NR for 60GHz,” Spreadtrum Communications
4. R1-2106766, “Discussions on initial access signals and channels for operation in 52.6-71GHz,” InterDigital, Inc.
5. R1-2106795, “Considerations on initial access aspects for NR from 52.6 GHz to 71 GHz,” Sony
6. R1-2106831, “Initial access aspects for NR from 52.6 GHz to 71GHz,” Lenovo, Motorola Mobility
7. R1-2106873, “Initial access aspects for NR from 52.6 GHz to 71 GHz,” Samsung
8. R1-2106956, “Initial access aspects for up to 71GHz operation,” CATT
9. R1-2107000, “Discussion on the initial access aspects for 52.6 to 71GHz,” ZTE, Sanechips
10. R1-2107032, “Considerations on initial access for NR from 52.6GHz to 71 GHz,” Fujitsu
11. R1-2107050, “Initial Access Aspects,” Ericsson
12. R1-2107097, “Initial access for Beyond 52.6GHz,” FUTUREWEI
13. R1-2107104, “Initial access aspects,” Nokia, Nokia Shanghai Bell
14. R1-2107112, “Further discussion of initial access for NR above 52.6 GHz,” Charter Communications
15. R1-2107149, “Discussion on initial access aspects supporting NR from 52.6 to 71 GHz,” NEC
16. R1-2107176, “Initial access aspects for NR from 52.6GHz to 71 GHz,” Panasonic Corporation
17. R1-2107237, “Discusson on initial access aspects,” OPPO
18. R1-2107330, “Initial access aspects for NR in 52.6 to 71GHz band,” Qualcomm Incorporated
19. R1-2107435, “Initial access aspects to support NR above 52.6 GHz,” LG Electronics
20. R1-2107471, “Discussion on initial access aspects for NR from 52.6 to 71GHz,” ETRI
21. R1-2107517, “Discussion on initial access of 52.6-71 GHz NR operation,” MediaTek Inc.
22. R1-2107577, “Discussion on initial access aspects for extending NR up to 71 GHz,” Intel Corporation
23. R1-2107726, “Initial access signals and channels,” Apple
24. R1-2107789, “Initial access aspects,” Sharp
25. R1-2107845, “Initial access aspects for NR from 52.6 to 71 GHz,” NTT DOCOMO, INC.
26. R1-2107912, “On initial access aspects for NR from 52.6GHz to 71 GHz,” Xiaomi
27. R1-2108008, “NR SSB design consideration from 52.6 GHz to 71 GHz,” Convida Wireless
28. R1-2108148, “Discussion on initial access aspects for NR beyond 52.6GHz,” WILUS Inc.

# Annex: WID objective related to initial access

During the last RAN Plenary, the WID has been updated to reflect the approved numerologies for initial access. The following is copy of the WID objectives relevant for initial access.

|  |
| --- |
| * Physical layer aspects including [RAN1]:   + Support of up to 64 SSB beams for licensed and unlicensed operation in this frequency range.   + Supports 120kHz SCS for SSB and 120kHz SCS for initial access related signals/channels in an initial BWP.     - Study and specify, if needed, additional SCS (480kHz, 960kHz) for SSB for cases other than initial access.     - Note: coverage enhancement for SSB is not pursued.   + In addition to 120kHz, support 480 kHz SSB for initial access with support of CORESET#0/Type0-PDCCH configuration in the MIB with following constraints:     - Limited sync raster entry numbers       * It is assumed that RAN4 supports a channelization design which results in the total number of synchronization raster entries considering both licensed and unlicensed operation in a 52.6 – 71 GHz band no larger than 665 (Note: the total number of synchronization raster entries in FR2 for band n259 + n257 is 599). If the assumption cannot be satisfied, it’s up to RAN4 to decide its applicability to bands in 52.6 – 71 GHz.     - only 480kHz CORESET#0/Type0-PDCCH SCS supported for 480 kHz SSB SCS.     - Prioritize support SSB-CORESET#0 multiplexing pattern 1. Other patterns discussed on a best effort basis.     - 960 kHz numerology for the SSB is not supported by the UE for initial access in Rel-17.     - Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible     - Note: 480 kHz is an optional SSB numerology for initial access for the UE. A UE supporting a band in 52.6-71 GHz must at least support 120 kHz SCS (for initial access and after initial access)     - Note: Dependency or lack thereof for a UE supporting 480kHz and/or 960kHz numerology for data and control to also support 480kHz SSB numerology for initial access is to be tackled as part of UE capability discussion.   + Support ANR and PCI confusion detection for 120, 480 and 960kHz SCS based SSB, support CORESET#0/Type0-PDCCH configuration in MIB of 120, 480 and 960kHz SSB     - FFS: additional method(s) to enable support to obtain neighbour cell SIB1 contents related to CGI reporting     - Only 1 CORESET#0/Type0-PDCCH SCS supported for each SSB SCS, i.e., (120, 120), (480, 480) and (960, 960).     - Prioritize support SSB-CORESET#0 multiplexing pattern 1. Other patterns discussed on a best effort basis.     - Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible     - Note: From UE perspective, ANR detection for 480/960kHz SCS based SSB is not supported if the UE does not support 480/960 SCS for SSB.     - Note: for ANR, when reading the MIB, the cell containing the SSB is known to the UE, as defined in 38.133 specification.   + Specify support for PRACH sequence lengths (i.e. L=139, L=571 and L=1151) and study, if needed, specify support for RO configuration for non-consecutive RACH occasions (RO) in time domain for operation in shared spectrum |