3GPP TSG RAN WG1 Meeting #101-e R1-200xxxx

e-Meeting, May 25th – June 5th, 2020

Agenda Item: 7.2.4.2.1

Source: Moderator (Ericsson)

Title: Thread 2 on Resource allocation for NR sidelink Mode 1

Document for: Discussion, Decision

# Thread 2

[101-e- NR-5G\_V2X\_NRSL-Mode-1-02] Email discussion/approval on DCI aspects

* Contents of DCI format 3\_0:
  + Size of the following agreed fields: Time gap, HARQ process ID, Configuration index, counter SAI (for Type-1 codebook), PSFCH-to-HARQ\_feedback timing indicator
  + Indication of activation/release for Type-2 CG
  + Define the combination of PSFCH-to-HARQ feedback timing indicator and PUCCH resource indicator used to indicate that PUCCH resource is not provided.
  + Whether to include a Resource pool index and, if so, details.
* Alignment of DCI format 3\_0 with other DCI formats

By 5/29, with potential TPs by 6/4 – Ricardo (Ericsson)

## Q1. Contents of DCI format 3\_0. Size of the following agreed fields: Time gap, HARQ process ID, Configuration index, counter SAI (for Type-1 codebook), PSFCH-to-HARQ\_feedback timing indicator.

**Do you agree with the following proposal regarding the contents of DCI 3\_0:**

Proposal:

* Time gap uses 3 bits.
* HARQ process ID uses a fixed number of bits, where the value of corresponds to the maximum number of SL HARQ processes and is up to RAN2.
* Configuration index uses 3 bits.
* When type-1 codebook is configured, counter SAI uses 2 bits.
* PSFCH-to-HARQ\_feedback timing indicator uses bits, where is the number of configured values of the PSFCH to PUCCH gap.

FL comments:

* For the most of the fields, there are no concerns.
* Some companies have a concern that the proposal could be interpreted as having a variable number of bits for the HARQ process ID. This was not the intention, I have clarified it.
* For the size of the field PSFCH-to-HARQ\_feedback timing indicator, my intention was to make it variable 0-3 bits, like for many other fields in other DCI formats. We made the agreement below last meeting. So the proposal above look OK to me. But perhaps I have not understood the concerns from the companies.

Agreements:

* Higher layer signaling is used to configure the values of the PSFCH to PUCCH gap (NOTE: this is referred to as sl-FeedbackToUL-ACK in the following)
* The field PSFCH-to-HARQ\_feedback timing indicator:
  + Selects one of the configured values of the PSFCH to PUCCH gap, except in the case that, together with PUCCH resource indicator, it indicates that no PUCCH resource is provided.

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| **Company** | **Views** |
| Ericsson | Agree |
| Intel | The maximum number of Nprocesses may need to be decided by RAN1  The maximum number of Nconf may need to be decided by RAN1.  Other bullets are fine.  FL reply:  RAN2 is discussing the number of HARQ processes. It would be good to avoid duplicate discussions. |
| Futurewei | Agree with Intel that Nprocesses and Nconf need to be decided by RAN1.  For Nprocesses, our view is that it should be configurable from 0 to 4 bits (like URLLC, as V2X apps have eMBB and URLLC characteristics) |
| Nokia, NSB | Agree. |
| NTT DOCOMO | We are not sure why fixed sizes are proposed for time gap and configuration index, and why SAI is 2 bits for type-1 HARQ-ACK CB, but if majority companies support them, we are OK with the current them.  Regarding N\_processes, it would be dependent on RAN1 UE feature discussion. Not RAN2. |
| OPPO | For Nconf, do we have agreement that gNB configures a set of values, and only the index is indicated by DCI? If no, we need to make related agreement firstly.  FL reply:  We made this agreement in the last meeting  Agreements:   * Higher layer signaling is used to configure the values of the PSFCH to PUCCH gap (NOTE: this is referred to as sl-FeedbackToUL-ACK in the following) * The field PSFCH-to-HARQ\_feedback timing indicator:   + Selects one of the configured values of the PSFCH to PUCCH gap, except in the case that, together with PUCCH resource indicator, it indicates that no PUCCH resource is provided.   + FFS Presence in DCI format 3\_0 and size (0-3 bits).   Do you think something else is missing? |
| CMCC | Agree with Intel’s comments that Nprocesses and Nconf need to be decided by RAN1.  FL reply:  See my reply to Intel |
| Sharp | Agree. |
| Spreadtrum | Agree. |
| Samsung | Agree with Intel’s comments.  FL reply:  See my reply to Intel |
| ASUSTeK | Agree in general.  It would be better to clarity why and how to utilize 2 bit SAI for type-1 codebook.  FL reply:  If something is unclear, it will have to be addressed with a CR next meeting, I guess. |
| CATT | Agree in principle with further clarifications on *N\_processes* and *N\_conf*.  FL reply:  See my reply to Intel |
| Huawei, HiSilicon | As the total HARQ processes number and maximum number of indicator values are not decided, we are not sure and imply fixed values or variables based on configuration. In our understanding, the total number of HARQ processes and of indicator values should be fixed. We do not see the necessity to support configurable number of HARQ process in SL, a fixed value, like 16 HARQ processes, in NR Uu should be supported. We are open the exact HARQ process number is decided by RAN2 or RAN1, but at least it should be captured in RAN1 agreement that is a fixed bit size. For the number of indicator values, we can decide in this meeting as well and is determined on the maximum number of configured values.  Other bits field size are ok with us.  FL reply:  For the HARQ process ID, see my clarififcation above.  For the Nconf, see my comments above. I could not understand what your intention was. Would you like to have it fixed size even the values are configurable? This variable bitwidth is used in may other parts of the spec. |
| Convida | Agree. |
| vivo | Regarding the HARQ processes number, we share the same view as Huawei.  Other bullets are fine.  FL reply:  See my reply to Huawei |
| Apple | Support most of the bullets, with following comments:  Second bullet: HARQ process ID can be 4 bits to support 16 SL HARQ processes.  Last bullet: If PSFCH resources are not configured, PSFCH-to-HARQ\_feedback timing indicator always uses 0 bit. Otherwise, it uses bits, where is the number of configured values of the PSFCH to PUCCH gap.  Since PUCCH resource cannot be configured without PSFCH resource by RAN2 agreement, we think PSFCH-to-HARQ\_feedback\_timing indicator field is also 0 without PSFCH resource.  FL reply:  See my comments above and the reply to Huawei |
| ZTE, Sanechips | Agree. |
| Qualcomm | We agree in general on the field sizes with the clarification from Huawei  FL reply:  See my reply to Huawei  Qualcomm2:  We agree with the proposal after clarification. HARQ process ID size is fixed and PSFCH-to-HARQ\_feedback size depends on the number of configured values. |
| MediaTek | We would like to add wording ‘transmitting’ for the HARQ process ID bullet point, i.e., “…maximum number of *transmitting* SL HARQ processes and...”  We agree with the rest of the bullets. |

## Q2. Contents of DCI format 3\_0. Indication of activation/release for Type-2 CG.

**For activation/release of CG type-2, which of the following options should be used:**

* **Option 1. One bit is included in DCI for explicit activation/release when the UE is configured with SL-CS-RNTI.**
* **Option 2. One combination of values of DCI. Indicate the combination.**

FL comments:

* There was a typo in the options above. I have corrected it.
* Views are split but there is a slight majority for Option 2. Given that there are no technical justifications against any of the options, my suggestion is to take Option 2, which also reduces in smaller payload.

Proposal:

* For DCI format 3\_0 with CRC scrambled with SL-CS-RNTI, the following combination of values indicates activation of a Type-2 CG:
  + HARQ ID set to all zeros.
* For DCI format 3\_0 with CRC scrambled with SL-CS-RNTI, the following combination of values indicates release of a Type-2 CG:
  + HARQ ID set to all ones.

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| **Company** | **Views** |
| Ericsson | We are fine either way as long as scheduling flexibility is not lost. |
| Intel | Option 2, with HARQ ID codepoints indicating activation or release, e.g. all 0 for activation and all 1 for release. We assume that HARQ ID is not used for its purpose during activation and release, only during dynamic ReTX.  Furthermore, for the release many other fields may be set to ‘all 1’ since those are not used after the release. This increases robustness to positive false alarm. |
| Futurewei | Option1 since it is simpler |
| Nokia, NSB | Either option is fine, slightly prefer Option 2 for consistency with Uu. |
| NTT DOCOMO | Support option 2, which is the same as Uu mechanism. |
| OPPO | A typo in the question, it is DCI instead of SCI.  Option 2 is preferred.  FL reply:  Thanks. Corrected. |
| CMCC | Either option is fine, slightly prefer option 1 which is simpler and same design as LTE-V. |
| Sharp | Option 1, i.e. same as in LTE V2X. |
| Spreadtrum | Option 2.  For example, special value of “HARQ process ID field” is used for activation, while special value of “Lowest index of the subchannel allocation to the initial transmission” field is additionally used for deactivation. |
| Samsung | Either option is fine, slightly prefer option 2 to reuse Uu mechanism. |
| ASUSTeK | Option 2 is slightly preferred as similar with Uu. |
| CATT | Supporting Option 1.  Typo: 1 bit in **DCI** for explicit activation/release.  In LTE V2X, DCI to schedule SL contains 1 bit of activation/release SPS, while DCI to schedule Uu applies combination indication.  Thanks. Corrected. |
| Huawei, HiSilicon | Either way is ok, and NR Uu method, i.e. option 2, is slightly preferable. |
| Lenovo/MoTM | Either option is fine, NR Uu method is slightly preferred |
| Convida | Option 1. Since it is simpler and is same as LTE-V design. |
| vivo | Option1. We can reuse the LTE-V design. |
| Apple | Option 2.  Activation: “HARQ process ID” is all 0’s, and “frequency resource assignment” is not all 1’s.  Release: “HARQ process ID” is all 0’s and “frequency resource assignment” is all 1’s.  We think all 1’s is not a valid “frequency resource assignment” codepoint, and hence can be used to distinguish release of CG type-2.  [Apple 2] We support Option 2, but want to add one additional criteria that “frequency resource assignment” field is all 1’s for release of CG type-2. This increases robustness to positive false alarm. |
| ZTE, Sanechips | Option 1 is preferred. |
| Qualcomm | We support option 1 (with the correction to DCI)  Qualcomm2:  Signaling in the proposal is the same for both activation and release and would cause misalignment between UE and gNB if a DCI is missed (in Uu, signalling is different between activation and release). We still support Option 1 for simplicity. If Option 2 is adopted, signalling needs to be updated to differentiate between activation and release. |
| MediaTek | We prefer Option 2 |

## Q3. Contents of DCI format 3\_0. Define the combination of PSFCH-to-HARQ feedback timing indicator and PUCCH resource indicator used to indicate that PUCCH resource is not provided.

**Do you agree with the following proposal:**

Proposal:

* The combination of all-zero bits for PSFCH-to-HARQ feedback timing indicator and all-zero bits PUCCH resource indicator is used to indicate that PUCCH resource is not provided.

FL comments:

* The proposal seems agreeable to a wide majority.
* Some companies have expressed a preference for using only one of the fields (i.e., timing) but this is somewhat against the following agreement made by RAN1.

Agreements:

* For case of DG and type 2 CG: one combination of “timing and resource for PUCCH” is used to indicate that PUCCH resource is not provided
* For type 1 CG: no RRC configuration of PUCCH resources indicates that PUCCH resource is not provided

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| **Company** | **Views** |
| Ericsson | Agree |
| Intel | Agree |
| Futurewei | Agree |
| Nokia, NSB | Agree |
| NTT DOCOMO | Agree |
| OPPO | Not sure why we need the combination of these two fields to indicate no PUCCH resource. Can FL clarify more details?  If only all-zero bits for PSFCH-to-HARQ feedback timing indicator corresponds to 0 timing gap between PSFCH and PUCCH, which is not a valid case in reality because of 0 processing delay, it can be used to indicate no PUCCH resource.  FL reply:  We have the following agreement:  Agreements:   * For case of DG and type 2 CG: one combination of “timing and resource for PUCCH” is used to indicate that PUCCH resource is not provided * For type 1 CG: no RRC configuration of PUCCH resources indicates that PUCCH resource is not provided |
| CMCC | Agree |
| Sharp | Agree |
| Spreadtrum | Agree |
| Samsung | Agree |
| CATT | Agree |
| Huawei, HiSilicon | Agree. |
| Lenovo/MoTM | Agree |
| Convida | Agree. |
| vivo | Agree. |
| Apple | Similar to OPPO, we think a single codepoint of “PSFCH-to-HARQ feedback timing indicator” is enough to indicate PUCCH resource is not provided.  FL reply:  See my reply to OPPO |
| ZTE, Sanechips | Agree. |
| Qualcomm | We share OPPO view that a zero-gap is sufficient  FL reply:  See my reply to OPPO |
| MediaTek | Agree |

## Q4. Contents of DCI format 3\_0. Whether to include a Resource pool index and, if so, details.

**Regarding the possibility of having a resource pool index field in DCI.**

* **Do you think it is necessary? Why?**
* **What functionality would it provide? What happens if the field is not part of DCI?**
* **What should the size be?**

FL comments:

* The majority of companies proposes to have a resource pool index in DCI.
* Nokia, NSB have a valid point that if two pools are defined such that they overlap in time but not in frequency (i.e., there is no potential confusion for the SL transmissions), the DCI does not indicate which of the two pools to use.
* Following the same logic, it seems that such field is necessary for CG Type-1 as well.

Proposal:

* DCI format 3\_0 includes a 3-bit field that carries the index of the resource pool for which the grant is provided. This field applies to both DG and CG Type-2
* For CG type-1, the configuration indicates the resource pool for which the grant is configured.

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| **Company** | **Views** |
| Ericsson | We do not see the need for a pool index. In our understanding, the inclusion of time-frequency allocation information in DCI is everything that is needed. From that allocation, the UE can determine all the necessary pool information. This is the same behaviour as in LTE. |
| Intel | Ttajhe assumption on overlapping of resource pool configurations needs to be clarified first.  It seems this field is only needed in case of possibility of overlapped in time resource pool configurations.  If resource pools overlap in time but not in frequency or in both time and frequency, there is ambiguity, since frequency resource assignment and starting frequency sub-channel are interpreted within resource pool. |
| Futurewei | Including resource index is beneficial for two reasons: 1) as explained by Intel, and 2) even if not overlapping, the receiving UE could be using a different resource pool than the transmitting UE. In such a case, timeslot indexes, subchannel indexes could be different based on each resource pool is used. Having a resource pool index eliminates any ambiguity. |
| Nokia, NSB | Seems to be needed. The difference to LTE is that only a single scheduling pool was configured to a mode 3 UE in LTE, while in NR a mode 1 UE can be configured with multiple (up to maxNrofTXPool-r16=8) scheduling pools (sl-TxPoolScheduling). The field “Lowest index of the subchannel allocation to the initial transmission” in DCI 3-0 currently is relative to the pool, so does not help determine the pool. Adding a 3-bit resource pool index field seems the easiest solution. |
| NTT DOCOMO | Seems to be needed, based on the above companies’ comments. |
| OPPO | Agree with Intel, resource pool index is needed in DCI to resolve the ambiguity. |
| CMCC | Resource pool index in DCI is needed to align the understanding of gNB and UE for which resources are scheduled. As explained by Nokia the bitwidth of FDRA is related to the specific resource pool without that the corresponding resource allocation would be ambiguous. |
| Sharp | Resource pool index is needed in DCI. |
| Spreadtrum | Seems necessary to resolve the ambiguity. |
| Samsung | Seems to be needed. As commented by companies above, the understanding on frequency RA and starting sub-channel, which is part of resource pool configuration, need to be aligned. |
| ASUSTeK | Share the same views with Nokia.  The field size can be 3-bit or depend on number of configured TX pool(s) for mode 1. |
| CATT | It is necessary.  In NR V2X mode 1, multiple resource pools can be configured and scheduled. In LTE V2X mode 3, only one resource pool is scheduled each time. DCI including resource pool index can explicitly indicate it and avoid ambiguity. |
| Huawei, HiSilicon | Yes, the resource pool index field is necessary. Up to 8 transmission resource pool configurations for a UE are provided by high layer and frequency resource assignment of a SL transmission is with respect to a single resource pool only, so additional resource pool index is needed to indicate which resource pool is actually used. Otherwise, UE cannot figure out the frequency resource for SL transmission.  As 8 resource pools can be configured, 3 bits in DCI are enough for resource pool indication. |
| Lenovo/MoTM | Not needed, it is upto gNB configuration whether the resource pools are overlapped in frequency domain or not, even if the resource pools are overlapped, then gNB could make sure there is consistent configuration in the overlapped resource pool. TX UE should be allowed to choose the resource pool based on the priority of the traffic. |
| Convida | Yes, it is necessary. We share the same view with Nokia. 3 bits in DCI seem to be good for resource pool indication. |
| vivo | Yes, it is necessary. We share the same view as Nokia and CMCC. In LTE there is only 1 mode3 pool so the scheduling ambiguity does not exist but in NR mode-1 up to 8 pools can be configured at the same time. The TRI and FRI are dependent on the pool bandwidth and Nmax, thereby pool index is needed to help UE to determine which pool is scheduled and how to read the TRI and FRI field. |
| Apple | It seems necessary. By configuring multiple resource pools for mode 1, we need to indicate which resource pool for the current SL grant in DCI. The frequency resource indication in DCI is relative to the configured and scheduled resource pool, and may not be enough to distinguish resource pools. |
| ZTE, Sanechips | The resource pool index in DCI is necessary as commented by companies.  The size of the DCI field can depend on the number of pools being configured. |
| Qualcomm | We share Ericsson’s view that pool index in DCI is not needed. The gNB is unaware of the desination UE and the pools on which the source and destination UEs can communicate. |

## Q5. Alignment of DCI format 3\_0 with other DCI formats.

In RAN1#99, the following agreement was made:

Agreements:

* Existing DCI size budget is maintained when the UE is configured with SL
* (working assumption): The size of the new DCI format and the size of one of the existing NR DCI formats are aligned.

FL comment:

* The majority of companies prefer to align with respect to DCI format 0\_1.
* However, a few companies prefer to wait until the contents of DCI format 3\_0 is complete or have a generalized framework.
* My preference is not to wait with the issue. Take a working assumption and revisit if things do not work.

Proposal (for a working assumption):

* The sizes of DCI format 3\_0 and DCI format 0\_1 are aligned by zero padding the format with smaller size so that the sizes are equal.

**Which existing NR DCI format should be used for alignment.**

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| **Company** | **Views** |
| Ericson | DCI format 0\_1 |
| Intel | First, we think a generalized framework of alignment can be defined, not limited to alignment to only one of the formats.  Regardless of the agreed format, we would like to allow zero padding to both the SL format and Uu format for alignment in order to avoid truncation. |
| Futurewei | DCI format 0\_1 |
| Nokia, NSB | DCI format 0\_1 |
| Sharp | Agree with Intel. A generalized framework is preferred.  [Sharp 2] Questions/comments on the proposed working assumption:   * (same as vivo) What if DCI format 0\_1 is not configured? * When/how will the size alignment be performed? For example, it seems it cannot be done after the “DCI size alignment” steps (7.3.1.0, TS 38.212), or else the potential padding of 0\_1 may create a new DCI size in addition to those in 7.3.1.0 of 212 (i.e. the DCI size budget may be exceeded). * In our view it would be much simpler NOT to touch the steps in 7.3.1.0 of 212, but to align 3\_0 to one of the sizes determined after the steps there. |
| Spreadtrum | DCI format 0\_1. |
| Samsung | DCI format 0\_1 |
| CATT | DCI format 0\_1 |
| Huawei, HiSilicon | gNB will avoid scheduling a Uu DCI and SL DCI together, and thus avoid exceeding the blind decoding budget, and hence not to align the 3\_0 size as such.  FL reply:  We need to provide details to implement the working assumption above. Or reject it if we have technical concerns about it.  Agreements:   * Existing DCI size budget is maintained when the UE is configured with SL * (working assumption): The size of the new DCI format and the size of one of the existing NR DCI formats are aligned. |
| Convida | Agree with Intel. A generalized framework is preferred. Further decision can be made when the fields in DCI 3\_0 are stable. |
| vivo | Same view as intel, sharp and Convida. We prefer to postpone the DCI size alignment discussion until the DCI 3-0 content is finalized.  [vivo-2]Regarding the updated proposal, I think it assumes that DCI 0-1 must be configured if SL DCI 3-0 is supported? What if DCI 0-1 is not configured? |
| Apple | A generalized framework is preferred. |
| ZTE, Sanechips | DCI 3\_0 aligns with DCI 0\_1 by zero padding when the DCI size budget is not satisfied.  In order not to impact the legacy behavior, UE does not expect a configuration that makes the size of DCI 0\_1 smaller than the size of DCI 3\_0. |
| Qualcomm | DCI format 0\_1. The sizes of the two formats aligned with each other, where the smaller is padded to the larger size |
| MediaTek | We prefer to wait until DCI 3\_0 fields are stable.  Replacing one WA with another WA is not preferable. |

## Q6. Other issues.

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| **Company** | **Views** |
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