3GPP TSG RAN WG1 Meeting #101-e R1-200xxxx

e-Meeting, May 25th – June 5th, 2020

Agenda Item: 7.2.4.2.1

Source: Moderator (Ericsson)

Title: Thread 2 on Resource allocation for NR sidelink Mode 1

Document for: Discussion, Decision

# Thread 2

[101-e- NR-5G\_V2X\_NRSL-Mode-1-02] Email discussion/approval on DCI aspects

* Contents of DCI format 3\_0:
  + Size of the following agreed fields: Time gap, HARQ process ID, Configuration index, counter SAI (for Type-1 codebook), PSFCH-to-HARQ\_feedback timing indicator
  + Indication of activation/release for Type-2 CG
  + Define the combination of PSFCH-to-HARQ feedback timing indicator and PUCCH resource indicator used to indicate that PUCCH resource is not provided.
  + Whether to include a Resource pool index and, if so, details.
* Alignment of DCI format 3\_0 with other DCI formats

By 5/29, with potential TPs by 6/4 – Ricardo (Ericsson)

## Q1. Contents of DCI format 3\_0. Size of the following agreed fields: Time gap, HARQ process ID, Configuration index, counter SAI (for Type-1 codebook), PSFCH-to-HARQ\_feedback timing indicator.

**Do you agree with the following proposal regarding the contents of DCI 3\_0:**

Proposal:

* Time gap uses 3 bits.
* HARQ process ID uses bits, where the value of is up to RAN2.
* Configuration index uses 3 bits.
* When type-1 codebook is configured, counter SAI uses 2 bits.
* PSFCH-to-HARQ\_feedback timing indicator uses bits, where is the number of configured values of the PSFCH to PUCCH gap.

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| **Company** | **Views** |
| Ericsson | Agree |
| Intel | The maximum number of Nprocesses may need to be decided by RAN1  The maximum number of Nconf may need to be decided by RAN1.  Other bullets are fine. |
| Futurewei | Agree with Intel that Nprocesses and Nconf need to be decided by RAN1.  For Nprocesses, our view is that it should be configurable from 0 to 4 bits (like URLLC, as V2X apps have eMBB and URLLC characteristics) |
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## Q2. Contents of DCI format 3\_0. Indication of activation/release for Type-2 CG.

**For activation/release of CG type-2, which of the following options should be used:**

* **Option 1. One bit is included in SCI for explicit activation/release when the UE is configured with SL-CS-RNTI.**
* **Option 2. One combination of values of SCI. Indicate the combination.**

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| **Company** | **Views** |
| Ericsson | We are fine either way as long as scheduling flexibility is not lost. |
| Intel | Option 2, with HARQ ID codepoints indicating activation or release, e.g. all 0 for activation and all 1 for release. We assume that HARQ ID is not used for its purpose during activation and release, only during dynamic ReTX.  Furthermore, for the release many other fields may be set to ‘all 1’ since those are not used after the release. This increases robustness to positive false alarm. |
| Futurewei | Option1 since it is simpler |
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## Q3. Contents of DCI format 3\_0. Define the combination of PSFCH-to-HARQ feedback timing indicator and PUCCH resource indicator used to indicate that PUCCH resource is not provided.

**Do you agree with the following proposal:**

Proposal:

* The combination of all-zero bits for PSFCH-to-HARQ feedback timing indicator and all-zero bits PUCCH resource indicator is used to indicate that PUCCH resource is not provided.

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| **Company** | **Views** |
| Ericsson | Agree |
| Intel | Agree |
| Futurewei | Agree |
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## Q4. Contents of DCI format 3\_0. Whether to include a Resource pool index and, if so, details.

**Regarding the possibility of having a resource pool index field in DCI.**

* **Do you think it is necessary? Why?**
* **What functionality would it provide? What happens if the field is not part of DCI?**
* **What should the size be?**

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| **Company** | **Views** |
| Ericsson | We do not see the need for a pool index. In our understanding, the inclusion of time-frequency allocation information in DCI is everything that is needed. From that allocation, the UE can determine all the necessary pool information. This is the same behaviour as in LTE. |
| Intel | The assumption on overlapping of resource pool configurations needs to be clarified first.  It seems this field is only needed in case of possibility of overlapped in time resource pool configurations.  If resource pools overlap in time but not in frequency or in both time and frequency, there is ambiguity, since frequency resource assignment and starting frequency sub-channel are interpreted within resource pool. |
| Futurewei | Including resource index is beneficial for two reasons: 1) as explained by Intel, and 2) even if not overlapping, the receiving UE could be using a different resource pool than the transmitting UE. In such a case, timeslot indexes, subchannel indexes could be different based on each resource pool is used. Having a resource pool index eliminates any ambiguity. |
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## Q5. Alignment of DCI format 3\_0 with other DCI formats.

In RAN1#99, the following agreement was made:

Agreements:

* Existing DCI size budget is maintained when the UE is configured with SL
* (working assumption): The size of the new DCI format and the size of one of the existing NR DCI formats are aligned.

**Which existing NR DCI format should be used for alignment.**

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| **Company** | **Views** |
| Ericson | DCI format 0\_1 |
| Intel | First, we think a generalized framework of alignment can be defined, not limited to alignment to only one of the formats.  Regardless of the agreed format, we would like to allow zero padding to both the SL format and Uu format for alignment in order to avoid truncation. |
| Futurewei | DCI format 0\_1 |
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## Q6. Other issues.

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| **Company** | **Views** |
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