TSG-RAN WG1#7bis **TSGR1#7(99)e90**
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Source: **Mitsubishi Electric**

Title: **Uplink Compressed Mode Frame Format**

Document for: **Discussion**

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1. Introduction

DL compressed mode for measurements on other frequencies is an alternative to the use of dual receivers.

When in compressed mode, information that is normally transmitted within a 10 ms frame, must be compressed in time. This can be done either by reducing the spreading factor by 2 or by a combination of rate matching and puncturing. Maximum idle gap length is restricted to 7 slots per frame for downlink compressed mode. The transmit power is increased in the compressed frame in order to maintain the target BER.

There are 2 different scenarios for the use of UL compressed mode:

1. simultaneous DL and UL compressed mode
2. UL compressed mode only

Whereas transmission time reduction method, frame format, idle gap position and creation of different idle gap lengths for downlink compressed mode are already described in TS25.212, there is still no description of uplink compressed mode so far. This document discusses aspects which we think are important for the specification of uplink compressed mode.

2. Constraints on UL compressed mode

Several points need to be considered for creation of idle gaps in the UL:

- Unlike DL, where DPCCH and DPDCH are transmitted in time-multiplex, UL DPCCH has always a fixed SF=256 and is transmitted by I/Q-multiplexing with UL DPDCH.
- UE Peak-power limitation for cell border scenarios
- Resumption of closed-loop power-control after the idle gap
- Time-alignment between DL and UL idle gaps in case of simultaneous DL/UL compressed mode
- Transmission of feedback information (TFCI, TPC, FBI) within an UL compressed frame

A change of UL slot formats (e.g. away from I/Q-multiplexed DPDCH and DPCCH) during an UL compressed frame is not an attractive solution. This imposes that TFCI-bits could not be transmitted by puncturing UL DPDCH bits as this is done in DL compressd mode.

UL DPCCH should be spread with SF=256 even within an UL compressed frame. These assumptions would keep the implementation of the UL compressed mode function simple on UE as well as on BTS side.

Similar to DL compressed mode, either SF-reduction method or rate matching/puncturing should be applied as methods for creating idle gaps of different lengths for the UL DPDCH.

Available measurement time per idle gap is already reduced by a synthesizer switching time (500us) and some implementation margin (200us). Mis-alignment of DL and UL idle gaps in case of simultaneous DL/UL compressed mode should be avoided as much as possible. One solution to this constraint would be to have n+1 UL idle slots for n DL idle slots. Another solution would be to have only n UL idle slots, which need to be carefully aligned with the DL idle slots (Figure 1).

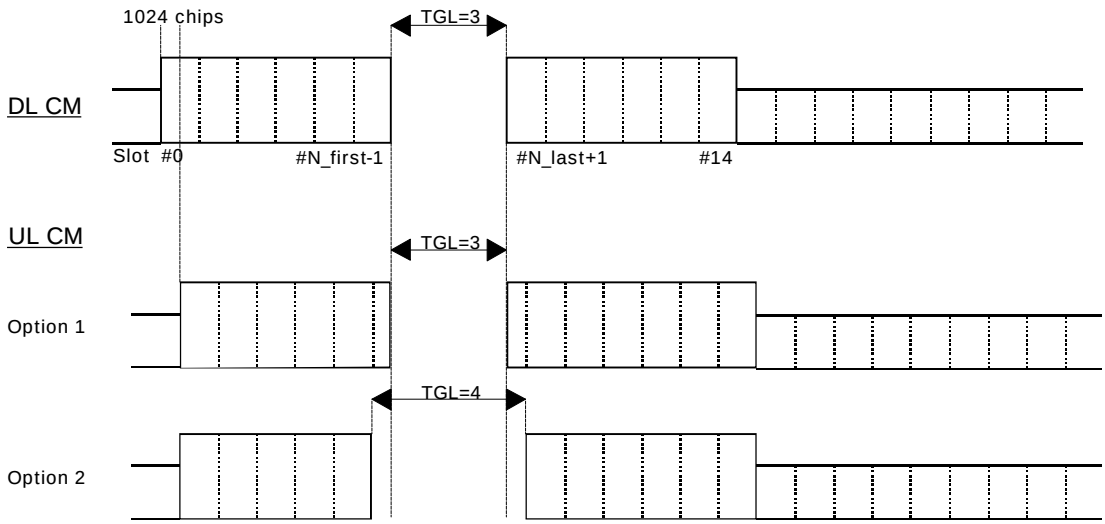


Figure 1: Simultaneous DL/UL compressed mode

Option 2 in Figure 1 is not optimal because the closed-loop power-control loop is interrupted at least one supplementary slot and because 2 more TFCI-bits would be lost compared to option 1. In our understanding, option 1 should be the prefered solution.

3. UL compressed mode frame types

Currently, there are 2 DL compressed mode frame types defined (Figure 2). Using DL frame type A, transmission stops at the slot boundary of slot N_first and resumes with the pilot field of slot N_last. Frame type B transmits the TPC-field of slot N_first (where dummy bits are inserted in the corresponding TFCI and Data1-Fields).

We propose the use of 2 basic UL compressed mode types (Figure 2). UL frame type B could be used in case of UL compressed mode only, whereas UL frame type A would be used in case of simultaneous DL/UL compressed mode.

No special action is taken in case of UL compressed mode only (Figure 3). UL Transmission stops at the end of UL-slot N_first-1 and resumes with the beginning of the pilot field of slot N_last+1.

In case of simultaneous DL/UL compressed mode (Figure 3), perfect time alignment can always be achieved with DL Frame type A for the beginning of the idle gap as (2560 – 1024) = 1536 chips is a multiple of 256. UL DPCCH before the gap can accommodate up to 6 bits which can be split between pilot bits and TFCI-bits.

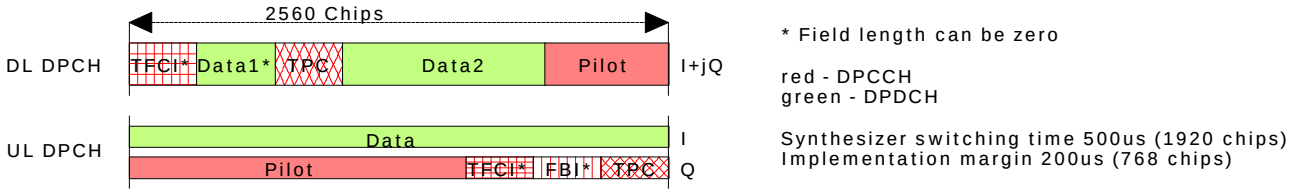
Perfect alignment at the end of the DL and UL idle gap is not possible in the general case as there are DL slot formats with 32…1024 chips for pilot symbols in the DL. But in most cases, we can have between 4 and 6 pilot bits and 2 TPC-bits on UL DPCCH before the following ordinary UL slot.

UL Frame type A for simultaneous DL/UL compressed mode has also the advantage that the closed-loop power-control cycle can resume immediately after the idle gap, as UL transmisssion starts with pilot bits and DL pilots are already available for TPC. For keeping implementation simple and because a supplementary TPC-field does not impact UL when the UL idle gap starts, only DL frame type A should be used when DL and DL idle gaps need to be created simultaneously.

4. Conclusion

We propose the use of 2 frame format types for UL compressed mode. Priority is given to the time-alignment of the DL and UL idle gap and to the resumption of the power-control cycle after the gap.

DL and UL slot structure:

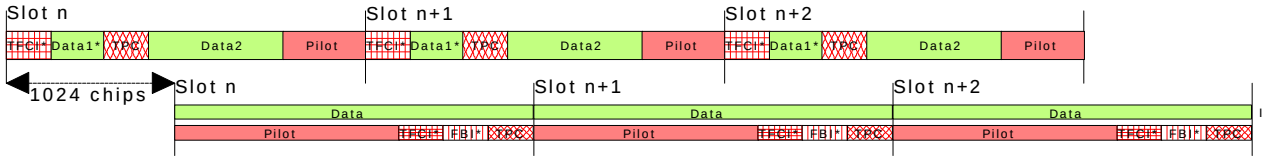


* Field length can be zero

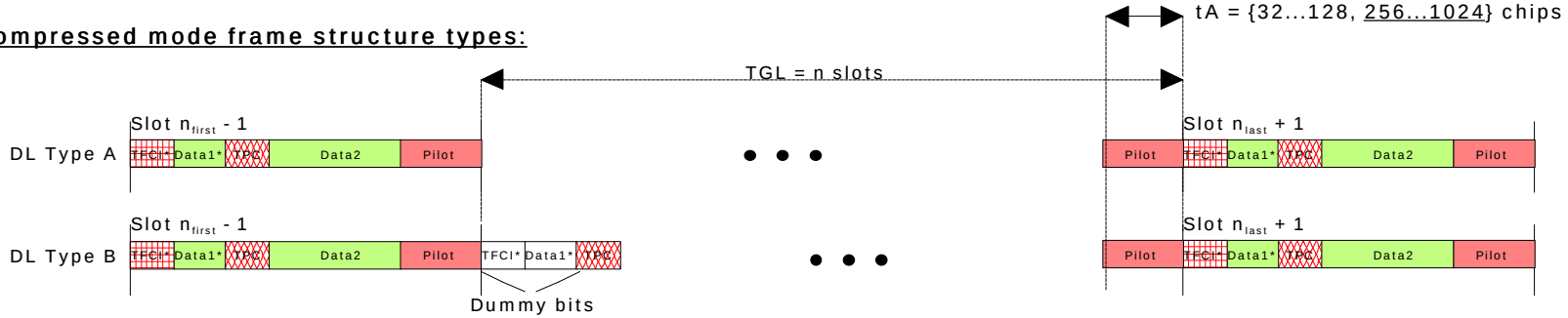
red - DPCCH
green - DPDCH

Synthesizer switching time 500us (1920 chips)
Implementation margin 200us (768 chips)

DL and UL timing:



DL compressed mode frame structure types:



Proposed UL compressed mode frame structures:

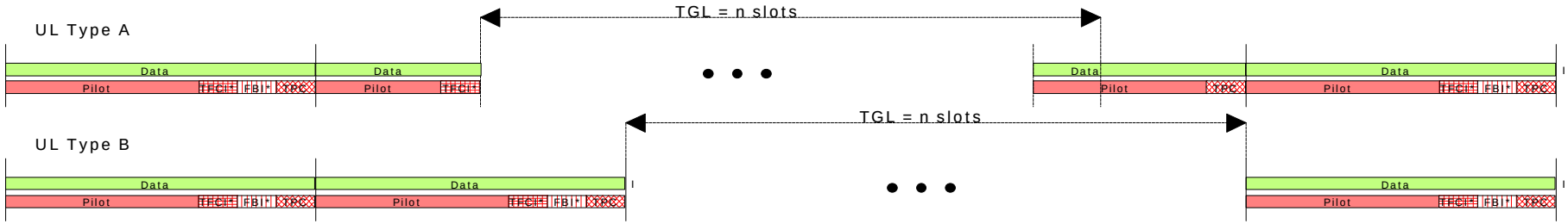
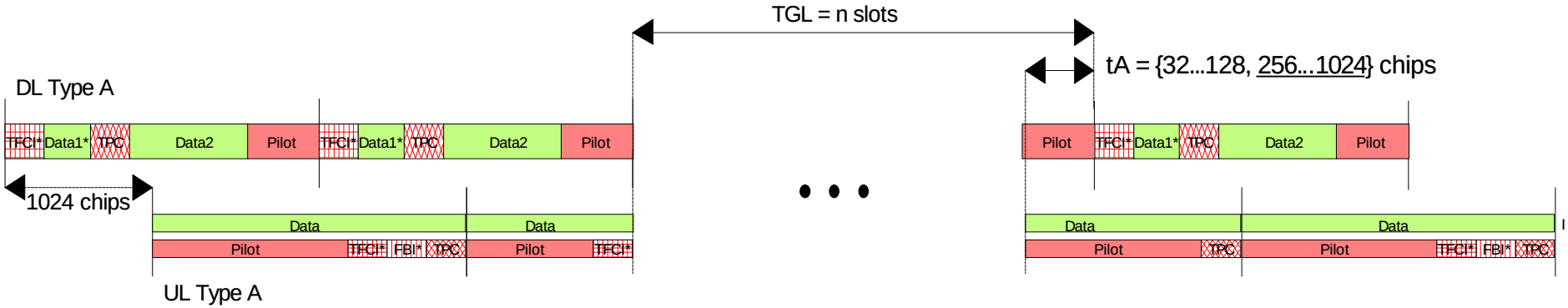


Figure 2: DL and UL compressed mode frame types

Simultaneous DL/UL compressed mode:



UL CM only:

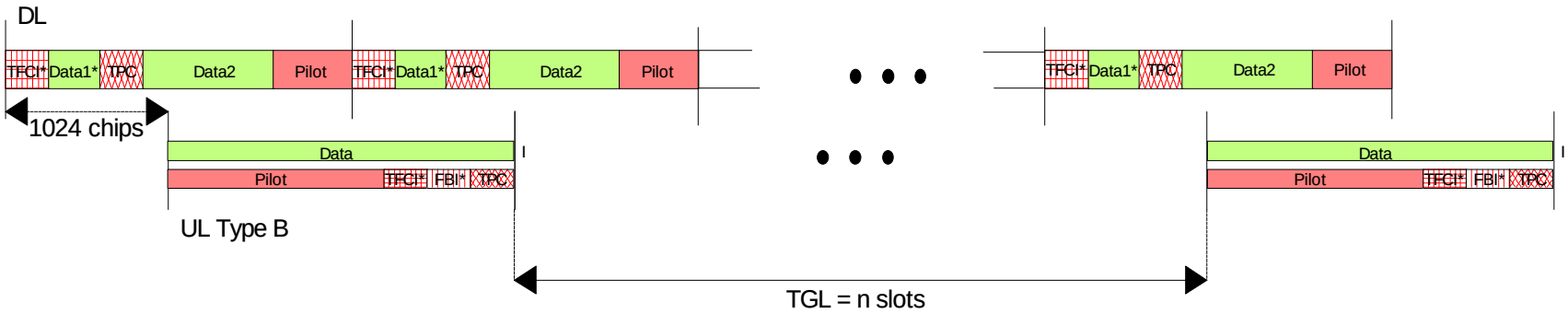


Figure 3: DL and UL idle gap alignment