TSG-RAN Working Group 1 meeting #7bis
Kyongju, South Korea
October 4 – October 5, 1999

TSGR1#7bis(99)e84

Agenda item:

Source: Ericsson

Title: Clarification of physical channel timing

Document for: Decision

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1 Introduction

Currently in TS 25.211 V2.4.0, section 7, there is a reference to TS 25.401 to the timing information that was previously found in TS 25.211. However, WG3 has since then removed that information, so the reference is no longer valid. Hence, nowhere can the timing relation between CPICH/P-CCPCH and S-CCPCH/P-CCPCH be found.

This contribution proposes some text to fix this.

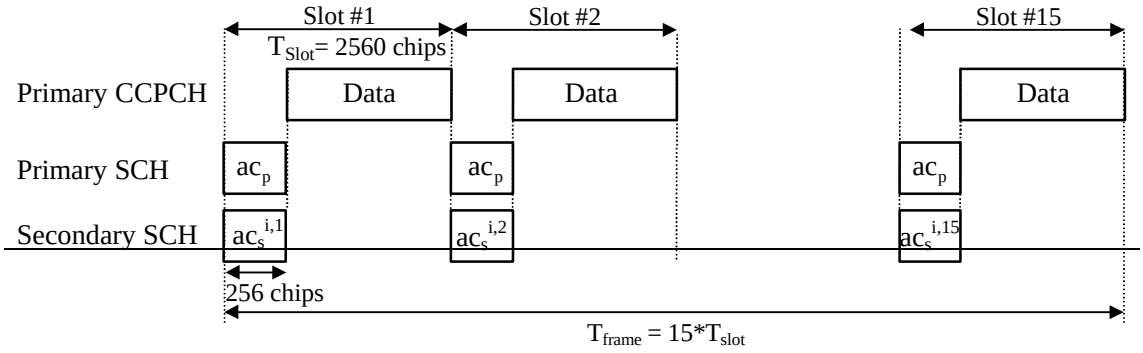
2 Proposed changes to TS 25.211

- The timing relations for all channels are described in section 7, meaning that the information about relative timing in 5.3.3.4 is moved to section 7.
- The paragraph in section 7 contains no information relevant to WG1. In fact, it contains incorrect assumptions, since there is no "Reference System Frame Number" in Node B defined in WG3. The different counters are better left to be defined by WG3 in TS 25.401.
- It is proposed to use the P-CCPCH as timing reference, since it is on the P-CCPCH the system frame number (SFN) is found.
- The CPICH is assumed to have the same frame timing as the P-CCPCH.
- Previously it was assumed in WG1 that the S-CCPCH could be time offset from the P-CCPCH. This assumption is kept. Timing offsets between P-CCPCH and S-CCPCH enables processing load distribution in the network and gives the possibility to distribute DTX periods of different channels.
- The order of the sections are changed to first cover common physical channels, then dedicated.
- The PICH/S-CCPCH and DPCH/PDSCH sections have been rewritten to become more clear.
- The AICH/PRACH section has been rewritten to become more clear. Note that not all of the parameters given in the old description are needed, some can be computed from the other parameters. Further, the section has been updated to take into account the RACH sub-channel concept.
- The AICH/PCPCH section has not been modified (since the author did not fully understand the section), although some updates could be valuable to clarify the timing relations.

3 Text proposal for TS 25.211 V2.4.0

5.3.3.4 Synchronisation Channel

The Synchronisation Channel (SCH) is a downlink signal used for cell search. The SCH consists of two sub channels, the Primary and Secondary SCH. The 10 ms radio frames of the primary and secondary SCH are divided into 15 slots, each of length 2560 chips. Figure 1 illustrates the structure of the SCH radio frame.~~and the transmission timing relationship with the Primary CCPCH:~~



c_p : Primary Synchronization Code
$c_s^{i,k}$: One of 16 possible Secondary Synchronization Codes
($c_s^{i,1}$, $c_s^{i,2}$, ..., $c_s^{i,15}$) encode cell specific long scrambling code group i
a: Modulation on primary and secondary synchronization codes to indicate STTD encoding on PCCPCH

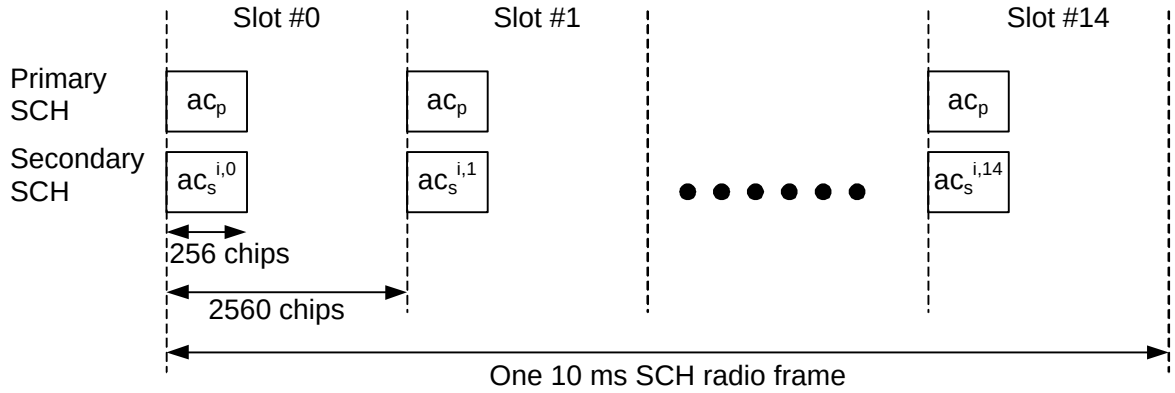


Figure 1: Structure of Synchronisation Channel (SCH).

The Primary SCH consists of a modulated code of length 256 chips, the Primary Synchronisation Code (PSC) denoted c_p in Figure 1, transmitted once every slot. The PSC~~rimary Synchronisation Code~~ is the same for every cell in the system~~ and is transmitted time-aligned with the period where the Primary CCPCH is not transmitted as illustrated in Figure 18~~.

The Secondary SCH consists of repeatedly transmitting a length 15 sequence of modulated codes of length 256 chips, the Secondary Synchronisation Codes (SSC), transmitted in parallel with the Primary SCH~~ynchronisation channel~~. The SSC is denoted $c_s^{i,k}$ in Figure 1, where i = 1, 2, …, 64 is the number of the scrambling code group, and k = 0, 1, …, 14 is the slot number. Each SSC~~econdary Synchronisation code~~ is chosen from a set of 16 different codes of length 256. This sequence on the Secondary SCH indicates which of the~~ 32 different~~ code groups the cell's downlink scrambling code belongs. ~~32 sequences are used to encode the 32 different code groups each containing 16 scrambling codes.~~

The primary and secondary synchronization codes are modulated by the symbol *a* shown in Figure 1, which indicates the presence/-absence of STTD encoding on the P-CCPCH and is given by the following table:

P-CCPCH STTD encoded	a = +1
P-CCPCH not STTD encoded	a = -1

5.3.3.4.1 SCH transmitted by TSTD

Figure 2 illustrates the structure of the SCH transmitted by the TSTD scheme. ~~In this Figure, STTD is applied to the Primary CCPCH~~In even numbered slots both PSC and SSC is transmitted on antenna 1, and in odd numbered slots both PSC and SSC is transmitted on antenna 2.

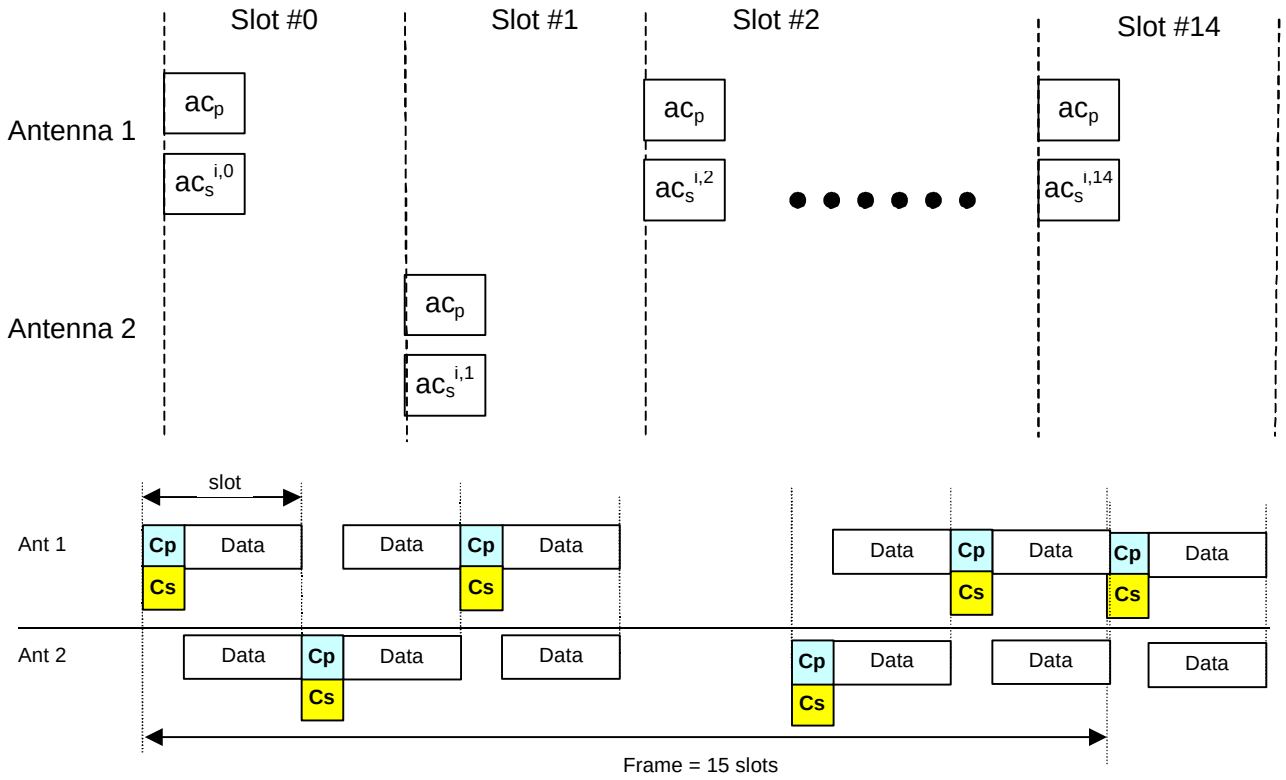


Figure 2: Structure of SCH transmitted by TSTD scheme.

7 Timing relationship between physical channels

7.1 General

The P-CCPCH, on which the cell SFN is transmitted, is used as timing reference for all the physical channels, directly for downlink and indirectly for uplink.

Figure XXX below describes the frame timing of the downlink physical channels. For the AICH the access slot timing is included. Timing for uplink physical channels is given by the downlink timing, as described in the following sections.

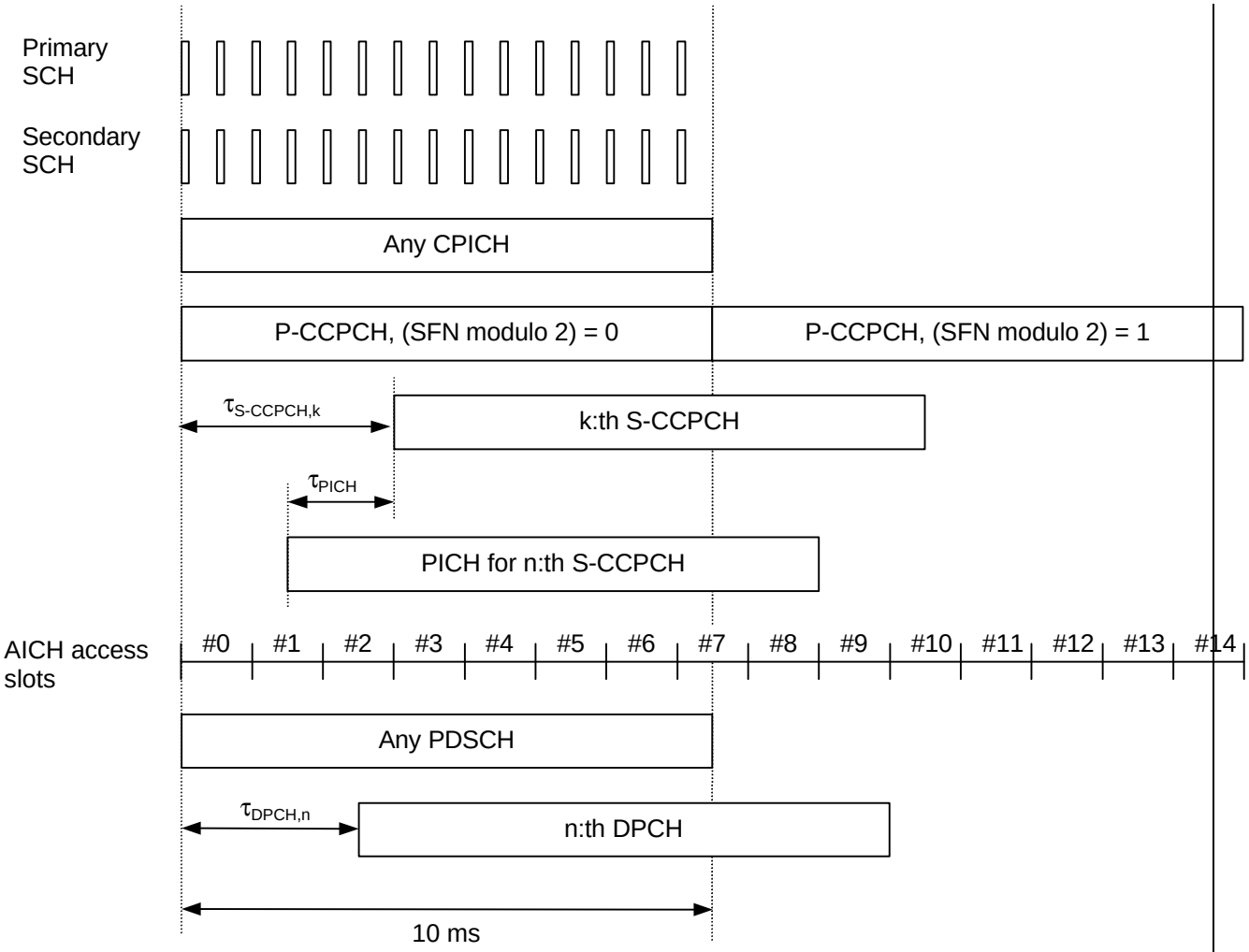


Figure XXX: Frame timing and access slot timing of downlink physical channels.

In the figure above the following applies:

- SCH (primary and secondary), CPICH (primary and secondary), P-CCPCH, and PDSCH have identical frame timings.
- The S-CCPCH timing may be different for different S-CCPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips, i.e. $\tau_{S\text{-}CCPCH,k} = T_k \times 256$ chip, $T_k \in \{0, 1, \ldots, 149\}$.
- The PICH timing is $\tau_{PICH} = 7680$ chips prior to its corresponding S-CCPCH frame timing. The PICH timing relation to the S-CCPCH is described more in section 7.2.
- The AICH access slot #0 starts the same time as a P-CCPCH frame with (SFN modulo 2) = 0. The AICH/PRACH and AICH/PCPCH timing is described in sections 7.3 and 7.4 respectively.
- The PDSCH timing relative the DPCH timing is described in section 7.5.
- The DPCH timing may be different for different DPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips, i.e. $\tau_{DPCH,n} = T_n \times 256$ chip, $T_n \in \{0, 1, \ldots, 149\}$. The DPCH (DPCCH/DPDCH) timing relation with uplink DPCCH/DPDCHs is described in section 7.6.

~~In general, a Node B covers *N* cells, where *N ³1*. Each Node B has a Reference System Frame Number (SFN), which counts from *0* to *M -1* in Radio Frame (10 ms) intervals. *M* is a multiple of the superframe (72), and is TBD. The purpose of the Reference SFN is to make sure that the correct frames are combined at soft handover. Each cell has a Cell SFN, which is broadcast on the BCH.~~

~~The physical channel timing is shown in [13].~~

7.2 PICH/S-CCPCH timing relation

illustrates the timing between a PICH frame and its associated S-CCPCH frame. A paging indicator set in a PICH frame means that the paging message is transmitted on the PCH in the S-CCPCH frame starting τ_{PICH} chips after the transmitted PICH frame. τ_{PICH} is defined in section 7.1.

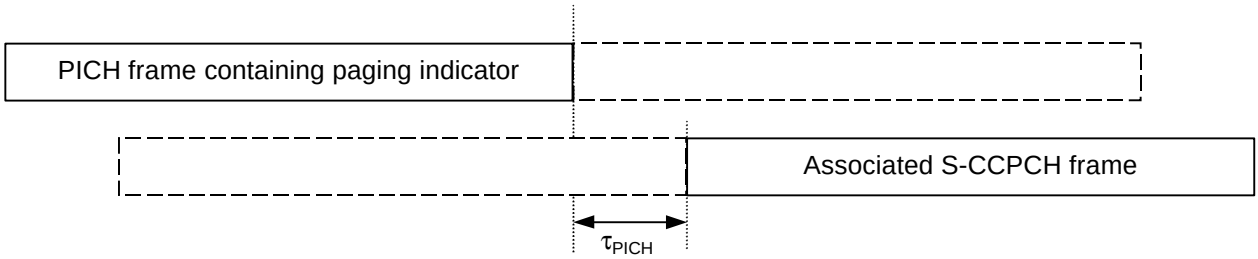


Figure 3: Timing relation between PICH frame and associated S-CCPCH frame.

~~7.1 DPCCH/DPDCH timing relations~~

~~7.1.1 Uplink~~

~~In uplink the DPCCH and all the DPDCHs transmitted from one UE have the same frame timing.~~

~~7.1.2 Downlink~~

~~In downlink, the DPCCH and all the DPDCHs carrying CCTrCHs of dedicated type to one UE have the same frame timing.~~

~~7.1.3 Uplink/downlink timing at UE~~

~~At the UE, the uplink DPCCH/DPDCH frame transmission takes place approximately T_0 chips after the reception of the first significant path of the corresponding downlink DPCCH/DPDCH frame. T_0 is a constant defined to be 1024 chips. More information about the uplink/downlink timing relation and meaning of T_0 can be found in [5] section 4.5.~~

~~7.2 DSCH timing~~

~~The relative timing between a DSCH and DCH is given as follows:~~

~~DSCH timing is identical to the cell primary CCPCH.~~

~~DCH timing is asynchronous with max 1 slot (2560 chips) ahead or max 14 slots (35840 chips) behind. This determines explicitly which frame on DSCH carries the user data based on the TFCI or higher layer signaling on DCH.~~

7.3 PRACH/AICH timing relation~~:~~

The downlink AICH is divided into downlink access slots, each access slot is of length 5120 chips. The downlink access slots are time aligned with the P-CCPCH as described in section 7.1

The uplink PRACH is divided into uplink access slots, each access slot is of length 5120 chips. Uplink access slot number n is transmitted from the UE $\tau_{p\text{-}a}$ chips prior to the reception of downlink access slot number n, n = 0, 1, …, 14.

Transmission of downlink acquisition indicators may only start at the beginning of a downlink access slot. Similarly, transmission of uplink RACH preambles and RACH message parts may only start at the beginning of an uplink access slot.

The PRACH/AICH timing relation is shown in figure QQQ.

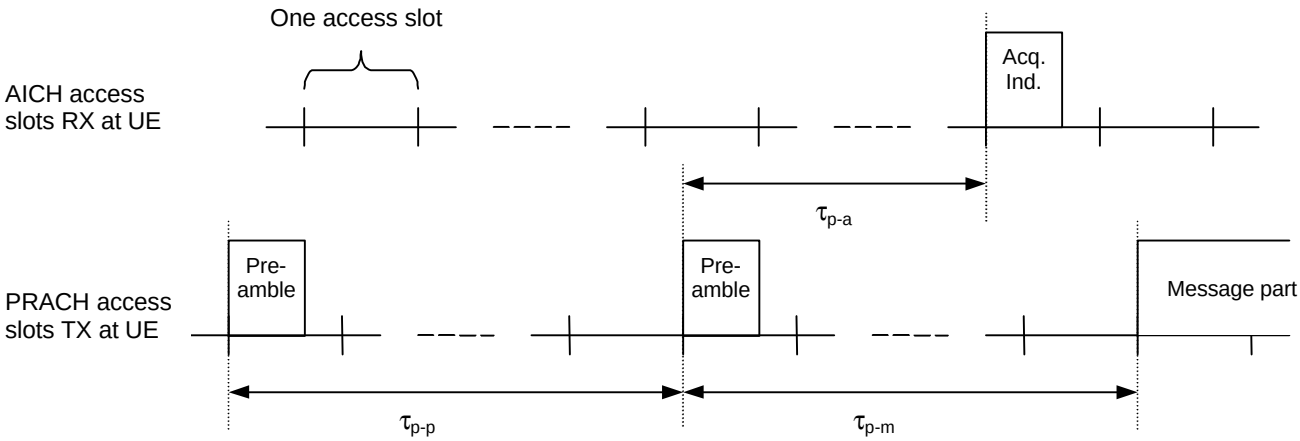


Figure QQQ: Timing relation between PRACH and AICH as seen at the UE.

The preamble-to-preamble distance τ_{p-p} shall be larger than or equal to the minimum preamble-to-preamble distance $\tau_{p-p,min}$, i.e. $\tau_{p-p} \geq \tau_{p-p,min}$.

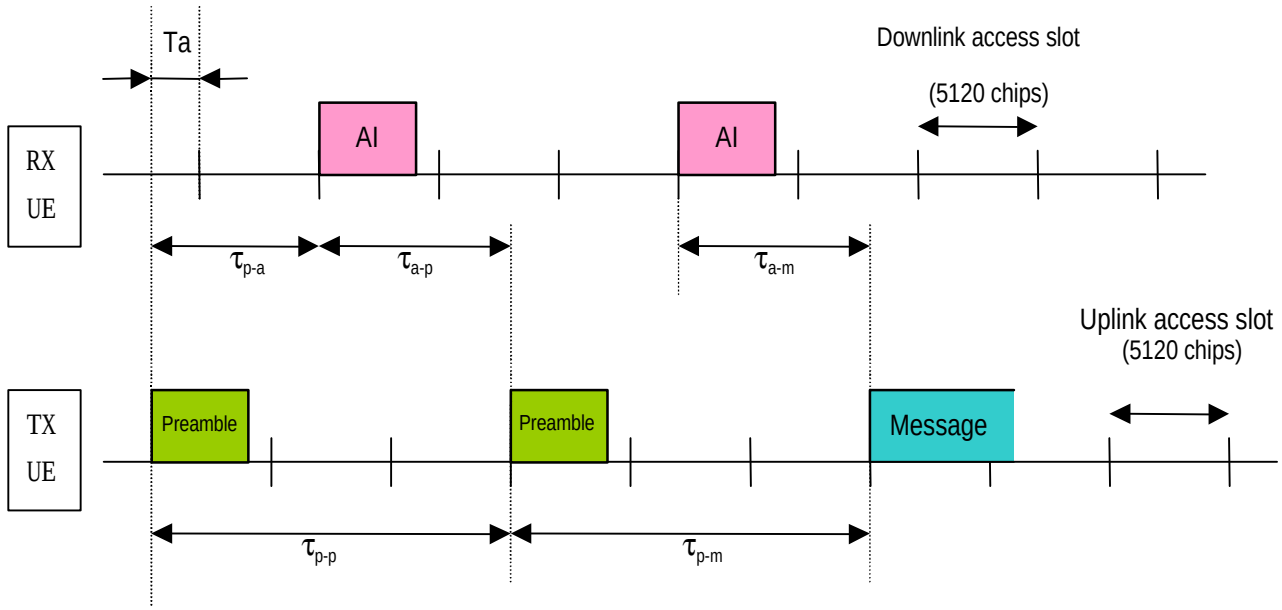
In addition to $\tau_{p-p,min}$, the preamble-to-AI distance τ_{p-a} and preamble-to-message distance τ_{p-a} are defined as follows:

when AICH_Transmission_Timing is set to 0, then

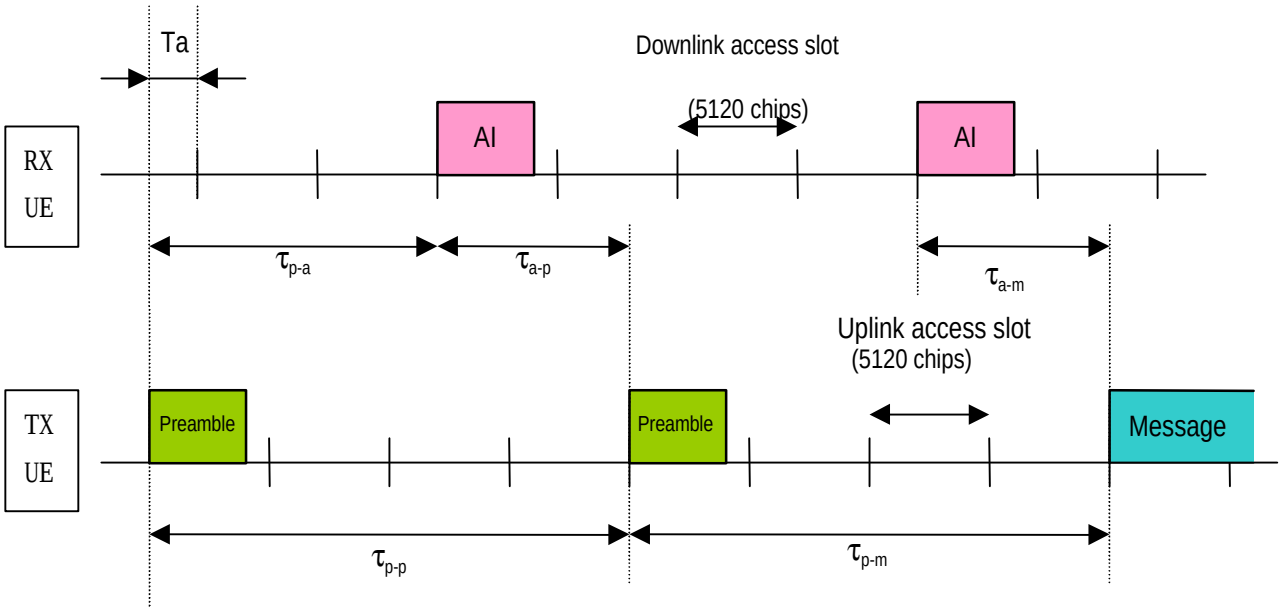
- $\tau_{p-p,min}$ = 15360 chips (3 access slots),
- τ_{p-a} = 7680 chips,
- τ_{p-m} = 15360 chips (3 access slots);

when AICH_Transmission_Timing is set to 1, then

- $\tau_{p-p,min}$ = 20480 chips (4 access slots),
- τ_{p-a} = 12800 chips,
- τ_{p-m} = 20480 chips (4 access slots).



~~**Figure 24: Timing of PRACH and AICH transmission as seen by the UE, with AICH transmission timing set to 0.**~~



~~Figure 25: Timing of PRACH and AICH transmission as seen by the UE, with AICH transmission timing set to 1.~~

~~Figure 24 and Figure 25 illustrate the timing relation between PRACH and AICH as seen by the UE, with AICH transmission timing set to 0 and 1, respectively.~~

~~- Both uplink and downlink access slots of length 5120 chips are defined.~~

~~- For each downlink access slot there is a corresponding uplink access slot.~~

~~- The preambles are to be transmitted time aligned with the uplink access slots.~~

~~-The downlink access slot #0 is transmitted time aligned with the PCCPCH frame boundary with SFN mod 2 = 0.~~

~~- An uplink access slot is transmitted a specified time τ_{p-a} before the corresponding downlink access slot.~~

~~- Subsequent preambles can be transmitted either three or four access slots after the latest transmitted preambles (τ_{p-p} is either 3 or 4 access slots), depending on the AICH transmission timing value.~~

~~- The message can be transmitted either three or four access slots after the latest transmitted preamble (τ_{p-m} is either 3 or 4 access slots), depending on the AICH transmission timing value.~~

~~The timing offset (T_a) between uplink and downlink access slots, as seen by the UE, is the same as 1 slot duration of 2560 chips.~~

~~The timing of preamble to AICH (τ_{p-a}) has two alternative values: 7680 chips or 12800 chips, depending on the AICH transmission timing value.~~

~~The timing of AICH to preamble(τ_{a-p}) has one value: 7680 chips.~~

~~The timing of AICH to message(τ_{a-m}) has one value: 7680 chips.~~

7.4 PCPCH/AICH timing relation

Everything in the previous section [PRACH/AICH] applies to this section as well. The timing relationship between preambles, AICH, and the message is the same as PRACH/AICH. Note that the collision resolution preambles follow the access preambles in PCPCH/AICH. However, the timing relationships between CD-Preamble and CD-AICH is

identical to RACH Preamble and AICH. The timing relationship between CD-AICH and the Power Control Preamble in CPCH is identical to AICH to message in RACH. However, the set of values for T_{cpch} is TBD. As an example, when T_{cpch} is set to zero or one, the following PCPCH/AICH timing values apply:

Note that a1 corresponds to AP-AICH and a2 corresponds to CD-AICH.

$\tau_{p\text{-}p}$ = Time between Access Preamble (AP) to the next AP. is either 3 or 4 access slots, depending on $T_{cpch.}$

$\tau_{p\text{-}a1}$ = Time between Access Preamble and AP-AICH has two alternative values: 7680 chips or 12800 chips, depending on T_{cpch}

$\tau_{a1\text{-}cdp}$ = Time between receipt of AP-AICH and transmission of the CD Preamble has one value: 7680 chips.

$\tau_{p\text{-}cdp}$ = Time between the last AP and CD Preamble. is either 3 or 4 access slots, depending on T_{cpch}

$\tau_{cdp\text{-}a2}$ = Time between the CD Preamble and the CD-AICH has two alternative values: 7680 chips or 12800 chips, depending on T_{cpch}

$\tau_{cdp\text{-}pcp}$= Time between CD Preamble and the start of the Power Control Preamble is either 3 or 4 access slots, depending on $T_{cpch.}$

Error! Reference source not found. shows the timing of the CPCH uplink transmission with the associated DPCCH control channel in the downlink.

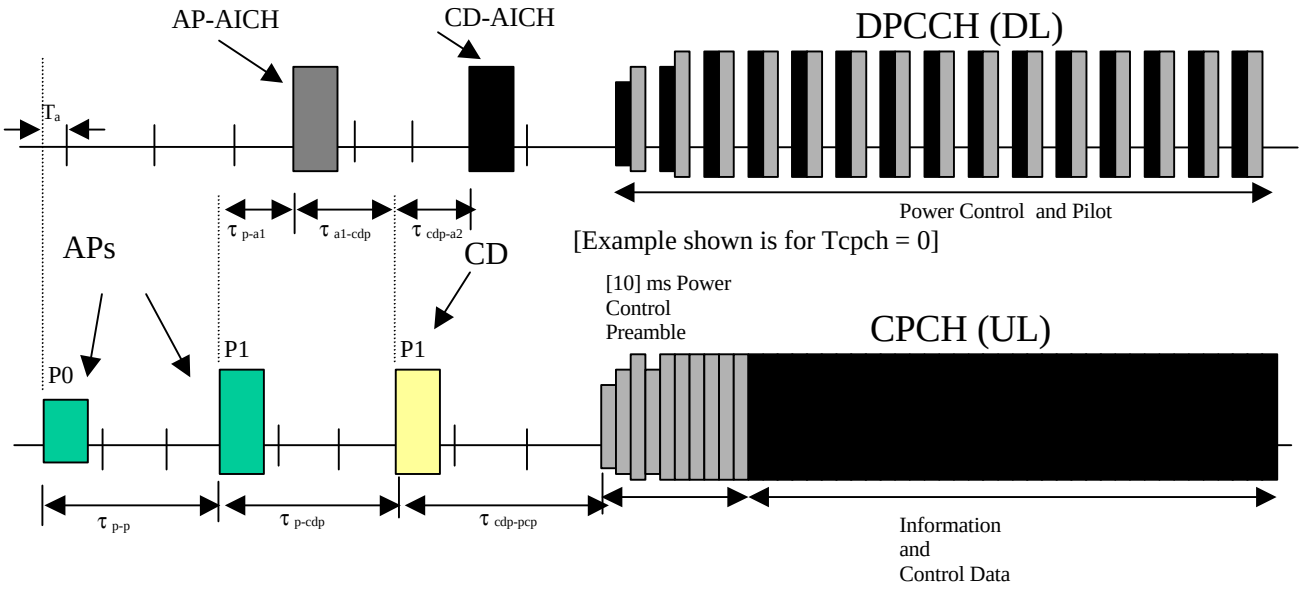


Figure 6: Timing of PCPCH and AICH transmission as seen by the UE, with T_{cpch}= 0.

7.5 DPCH/PDSCH timing

The relative timing between a DPCH frame and the associated PDSCH frame is shown in figure ZZZ.

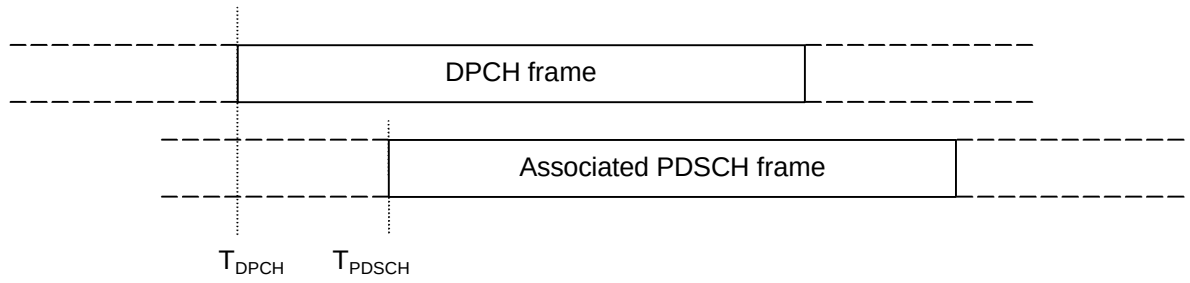


Figure ZZZ: Timing relation between DPCH frame and associated PDSCH frame.

The start of a DPCH frame is denoted T_{DPCH} and the start of the associated PDSCH frame is denoted T_{PDSCH}. Any DPCH frame is associated to one PDSCH frame through the relation -35840 chips < T_{DPCH} - T_{PDSCH} ≤ 2560 chips, i.e. the associated PDSCH frame starts anywhere between 1 slot before or up to 14 slots behind the DPCH.

7.6 DPCCH/DPDCH timing relations

7.1.1 Uplink

In uplink the DPCCH and all the DPDCHs transmitted from one UE have the same frame timing.

7.1.2 Downlink

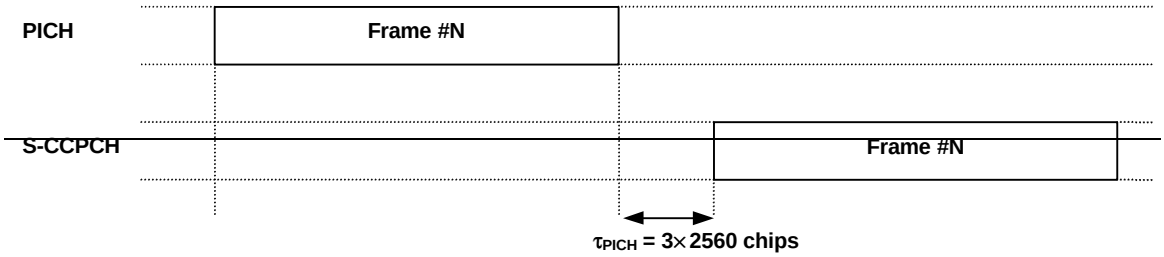
In downlink, the DPCCH and all the DPDCHs carrying CCTrCHs of dedicated type to one UE have the same frame timing.

7.1.3 Uplink/downlink timing at UE

At the UE, the uplink DPCCH/DPDCH frame transmission takes place approximately T_0 chips after the reception of the first significant path of the corresponding downlink DPCCH/DPDCH frame. T_0 is a constant defined to be 1024 chips. More information about the uplink/downlink timing relation and meaning of T_0 can be found in **Error! Reference source not found.** section 4.5.

~~7.5 Paging timing relation~~

~~Figure 27 illustrates the timing between an S-CCPCH frame and the corresponding frame of an associated PICH. The frame of the associated PICH precedes the corresponding S-CCPCH frame by τ_{PICH} = 3×2560 chips.~~



~~Figure 27: Timing between S-CCPCH and associated PICH.~~