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Contents

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Foreword

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The contents of this TS may be subject to continuing work within the 3GPP and may change following formal TSG approval. Should the TSG modify the contents of this TS, it will be re-released with an identifying change of release date and an increase in version number as follows:

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m indicates [major version number]

x the second digit is incremented for all changes of substance, i.e. technical enhancements, corrections, updates, etc.

y the third digit is incremented when editorial only changes have been incorporated into the specification.

1 Scope

The present document describes spreading and modulation for UTRA Physical Layer FDD mode.

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, the latest version applies.
- A non-specific reference to an ETS shall also be taken to refer to later versions published as an EN with the same number.

[<seq>] <doctype> <#>[([up to and including]{yyyy[-mm]|V<a[.b[.c]]>}[onwards])]: "<Title>".

[1] EN 301 234 (V2.1 onwards): "Example 1, using sequence field".

[2] EG 201 568 (V1.3.5): "Example 2, using fixed text".

<doctype> <#>[([up to and including]{yyyy[-mm]|V<a[.b[.c]]>}[onwards])]: "<Title>".

EN 301 234 (V2.1 onwards): "Example 1".

EG 201 568 (V1.3.5): "Example 2".

3 Definitions, symbols and abbreviations

3.1 Definitions

For the purposes of the present document, the following terms and definitions apply.

3.2 Symbols

For the purposes of the present document, the following symbols apply:

<symbol> <Explanation>

3.3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

AP Access Preamble
BCH Broadcast Control Channel
BER Bit Error Rate
BS Base Station
CCPCH Common Control Physical Channel
CD Collision Detection
CPCH Common Packet Channel
DCH Dedicated Channel

DL	Downlink
DPCH	Dedicated Physical Channel
DPCCH	Dedicated Physical Control Channel
DPDCH	Dedicated Physical Data Channel
DS-CDMA	Direct-Sequence Code Division Multiple Access
FACH	Forward Access Channel
FDD	Frequency Division Duplex
Mcps	Mega Chip Per Second
MS	Mobile Station
OVSF	Orthogonal Variable Spreading Factor (codes)
PCH	Paging Channel
PCPCH	Physical Common Packet Channel
PG	Processing Gain
PRACH	Physical Random Access Channel
RACH	Random Access Channel
RX	Receive
SCH	Synchronisation Channel
SF	Spreading Factor
SIR	Signal-to-Interference Ratio
TDD	Time Division Duplex
TFCI	Transport-Format Combination Indicator
TPC	Transmit Power Control
TX	Transmit
UE	User Equipment
UL	Uplink

4 Uplink spreading and modulation

4.1 Overview

Spreading is applied after modulation. It consists of two operations. The first is the channelization operation, which transforms every data symbol into a number of chips, thus increasing the bandwidth of the signal. The number of chips per data symbol is called the Spreading Factor (SF). The second operation is the scrambling operation, where a scrambling code is applied to the spread signal.

With the channelization, data symbol on so-called I- and Q-branches are independently multiplied with an OVSF code. With the scrambling operation, the resultant signals on the I- and Q-branches are further multiplied by complex-valued scrambling code, where I and Q denote real and imaginary parts, respectively. Note that before complex multiplication binary values 0 and 1 are mapped to +1 and -1, respectively.

4.2 Spreading

4.2.1 Uplink Dedicated Physical Channels (uplink DPDCH/DPCCH)

Figure 1 illustrates the spreading and modulation for the case of multiple uplink DPDCHs when total data rate is less than or equal to 1024kbps in the 5MHz band. Note that this figure only shows the principle, and does not necessarily describe an actual implementation. Figure 2 illustrates the case for data rate at 2048kbps in the 5 MHz band. Modulation is dual-channel QPSK (i.e.; separate BPSK on I- and Q-channel), where the uplink DPDCH and DPCCH are mapped to the I and Q branch respectively. The I and Q branches are then spread to the chip rate with two different channelization codes and subsequently complex scrambled by a UE specific complex scrambling code C_{scramb}.

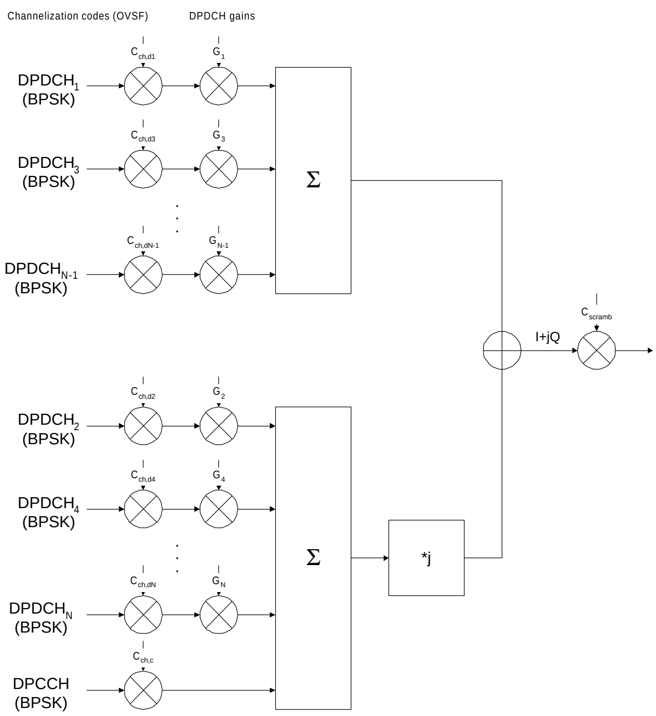

Figure 1 Spreading/modulation for uplink DPDCH/DPCCH for user services less than or equal to 1024kbps in the 5MHz band

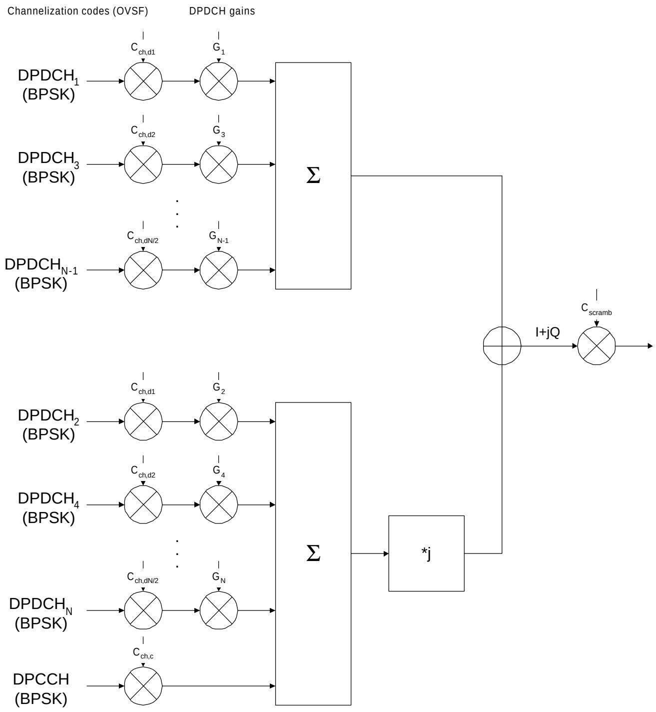

Figure 2. Spreading/modulation for uplink DPDCH/DPCCH for user services at 2048kbps in the 5MHz band

For a single uplink DPDCH transmission, only $DPDCH_1$ and DPCCH are transmitted.

For services less than or equal to 1024kbps in the 5MHz band, the DPCCH is spread by the channelization code $C_{ch,c}$ and each $DPDCH_i$ is spread by a predefined individual channelization codes, $C_{ch,di}$ (di=1,2,…). For 2048kbps rate in the 5MHz band, the DPCCH is spread by the channelization code $C_{ch,c}$ and each pair of $DPDCH_{2di-1}$ and $DPDCH_{2di}$ is spread by a predefined individual channelization codes, $C_{ch,di}$. The data symbols of both the DPDCHs and the DPCCH are BPSK-modulated and the channelization codes are real-valued. The real-valued signals of the I- and Q-branches are then summed and treated as a complex signal. This complex signal is then scrambled by the complex-valued scrambling code, C_{scramb}. The powers of the DPDCHs may be adjusted by gain factors, β_c, β_{di} .

The channel with maximum power has always $b_i \equiv 1.0$ and the others have $b_i \leq 1.0$, where i is in the range 1, 2, .. N, c The β-values are quantized into 4 bits, and the quantization steps are given in Table 1.

	Quantized amplitude ratio (b_{quant})
15	1.0
14	0.9375
13	0.875
12	0.8125
11	0.75
10	0.6875
9	0.625
8	0.5625
7	0.5
6	0.4375
5	0.375
4	0.3125
3	0.25
2	0.1875
1	0.125
0	Switch off

Table 1: The quantization of the gain parameters.

4.2.2 PRACH

The spreading and modulation of the message part of the Random-Access message part is basically the same as for the uplink dedicated physical channels, see Figure 1, where the uplink DPDCH and uplink DPCCH are replaced by the data part and the control part respectively. The scrambling code for the message part is chosen based on the preamble code.

4.3 Code generation and allocation

4.3.1 Channelization codes

The channelization codes of Figure 1 are Orthogonal Variable Spreading Factor (OVSF) codes that preserve the orthogonality between a user's different physical channels. The OVSF codes can be defined using the code tree of Figure 3.

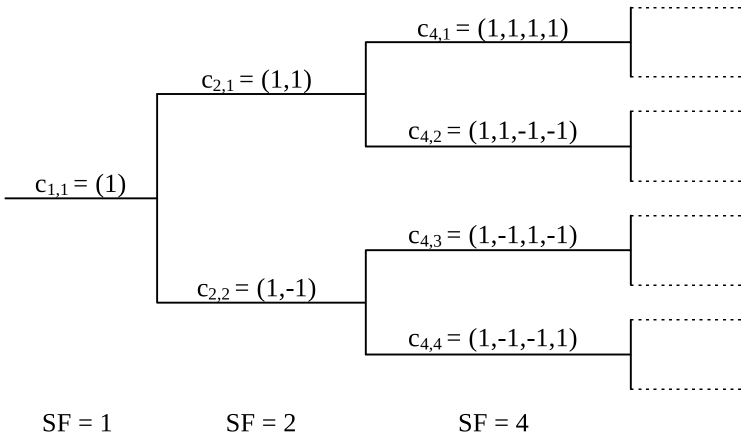

Figure 3. Code-tree for generation of Orthogonal Variable Spreading Factor (OVSF) codes.

In Figure 3, the OVSF code is described as $C_{SF,\text{code number}}$, where $SF_{d,n}$ represents the spreading factor of n^{th} DPDCH. Then the DPCCH is spread by code number 1 with a spreading factor of SF_c.

Each level in the code tree defines channelization codes of length SF, corresponding to a spreading factor of SF in Figure 3. All codes within the code tree cannot be used simultaneously by one mobile station. A code can be used by a UE if and only if no other code on the path from the specific code to the root of the tree or in the sub-tree below the specific code is used by the same mobile station. This means that the number of available channelization codes is not fixed but depends on the rate and spreading factor of each physical channel.

The generation method for the channelization code can also be explained in Figure 4.

$$C_{1,1} = 1$$

$$\begin{bmatrix} C_{2,1} \\ C_{2,2} \end{bmatrix} = \begin{bmatrix} C_{1,1} & C_{1,1} \\ C_{1,1} & \overline{C_{1,1}} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$$

$$\begin{bmatrix} C_{4,1} \\ C_{4,2} \\ C_{4,3} \\ C_{4,4} \end{bmatrix} = \begin{bmatrix} C_{2,1} & C_{2,1} \\ C_{2,1} & \overline{C_{2,1}} \\ C_{2,2} & C_{2,2} \\ C_{2,2} & \overline{C_{2,2}} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & 1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix}$$

: :

$$\begin{bmatrix} C_{2^{n+1},1} \\ C_{2^{n+1},2} \\ C_{2^{n+1},3} \\ C_{2^{n+1},4} \\ \vdots \\ C_{2^{n+1},2^{n+1}-1} \\ C_{2^{n+1},2^{n+1}} \end{bmatrix} = \begin{bmatrix} C_{2^n,1} & C_{2^n,1} \\ C_{2^n,1} & \overline{C_{2^n,1}} \\ C_{2^n,2} & C_{2^n,2} \\ C_{2^n,2} & \overline{C_{2^n,2}} \\ \vdots & \vdots \\ C_{2^n,2^n} & C_{2^n,2^n} \\ C_{2^n,2^n} & \overline{C_{2^n,2^n}} \end{bmatrix}$$

Figure 4. Spreading Code Generation Method

Binary code words are equivalent to the real valued sequences by the transformation ‘0’ -> ‘+1’, ‘1’ -> ‘-1’.

The spreading code cycle is the symbol cycle. Thus, for a given chip rate, the spreading code cycle depends on the symbol rate. Furthermore, the number of codes that can be used also differs according to the symbol rate. The relations between symbol rate, spreading code types, spreading code cycle and number of spreading codes is listed in Table 2.

The spreading code phase synchronises with the modulation/demodulation symbols. In other words, the head chip of the symbol is spreading code phase=0.

Symbol rate (ksps)				spreading code cycle(chip) SF	No. of Spreading codes
Chip rate= [0.96 Mcps]	3.84 Mcps	[7.68 Mcps]	[15.36 Mcps]		
[240]	960	[1920]	[3840]	4	4
[120]	480	[960]	[1920]	8	8
[60]	240	[480]	[960]	16	16
[30]	120	[240]	[480]	32	32
[15]	60	[120]	[240]	64	64
[7.5]	30	[60]	[120]	128	128
-	15	[30]	[60]	256	256
-	[7.5]	[15]	[30]	512	512
-	-	[7.5]	[15]	1024	1024
			[7.5]	2048	2048

Table 2. Correspondence between Symbol Rate and Spreading Code Types

The DPCCH is spread by code number 1 in any code tree as described in Section 4.3.1. The first DPDCH is spread by code number ($SF_{d,1}$ / 4 + 1). Subsequently added DPDCHs for multi-code transmission are spread by codes in ascending order starting from code number 2 excepting the one used for the first DPDCH. However to guarantee the orthogonality between channels, any subtree below the specified node is not used for the channelization code of a DPDCH.

<Editor's Note: The case of OVSF code allocation with multiple DPDCHs with different spreading factors is for further study

4.3.2 Scrambling codes

4.3.2.1 General

There are 2^{24} uplink scrambling codes. Either short or long scrambling codes should be used on the uplink. The short scrambling code is typically used in cells where the base station is equipped with an advanced receiver, such as a multi-user detector or interference canceller. With the short scrambling code the cross-correlation properties between different physical channels and users does not vary in time in the same way as when a long code is used. In cells where there is no gain in implementation complexity using the short scrambling code, the long code is used instead due to its better interference averaging properties. Both short and long scrambling codes are represented with complex-value.

The uplink scrambling generator (either short or long) shall be initialised by a 25 bit value. One bit shall indicate selection of short or long codes (short = 1, long = 0). Twenty four bits shall be loaded into the scrambling generators as shown in sections 4.3.2.2 and 4.3.2.3.

MSB — Initialisation Code Short/Long flag + Value *v* — LSB

short /long	v(23)	v(22)	v(21)	v(20)	v(19)	v(18)	v(17)	v(16)	v(15)	v(14)	v(13)	v(12)	v(11)	v(10)	v(9)	v(8)	v(7)	v(6)	v(5)	v(4)	v(3)	v(2)	v(1)	v(0)

Figure 5 - Initialisation Code for Uplink Scrambling generator

[Alternatively, if the system chooses, RSTS for uplink transmission, the scrambling code is the same as the downlink scrambling code described in 5.2.2. In this case, the same scrambling code is allocated to all dedicated physical channels in the cell.]

Both short and long scrambling codes are formed as follows:

$$C_{scramb} = c_1(w_0 + jc_2'w_1)$$

where w_0 and w_1 are chip rate sequences defined as repetitions of:

$$w_0 = \{1 \quad 1\}$$

$$w_1 = \{1 \quad -1\}$$

Also, c_1 is a real chip rate code, and c_2' is a decimated version of the real chip rate code c_2. The preferred decimation factor is 2, however other decimation factors should be possible in future evolutions of 3GPP if proved desirable.

With a decimation factor 2, c_2' is given as:

$$c_2'(2k) = c_2'(2k+1) = c_2(2k), \quad k=0,1,2\ldots.$$

The constituent codes c_1 and c_2 are formed differently for the short and long scrambling codes as described in Sections 4.3.2.2 and 4.3.2.3.

4.3.2.2 Long scrambling code

The long scrambling codes are formed as described in Section 4.3.2, where c_1 and c_2 are constructed as the position wise modulo 2 sum of 38400 chip segments of two binary *m*-sequences generated by means of two generator polynomials of degree 25. Let *x*, and *y* be the two *m*-sequences respectively. The *x* sequence is constructed using the primitive (over GF(2)) polynomial $X^{25}+X^{3}+1$. The *y* sequence is constructed using the polynomial $X^{25}+X^{3}+X^{2}+X+1$. The resulting sequences thus constitute segments of a set of Gold sequences.

The code, c_2, used in generating the quadrature component of the complex spreading code is a 16,777,232 chip shifted version of the code, c_1, used in generating the in phase component.

The uplink scrambling code word has a period of one radio frame of 10 ms.

Let $n_{23} \ldots n_0$ be the 24 bit binary representation of the scrambling code number *n* (decimal) with n_0 being the least significant bit. The *x* sequence depends on the chosen scrambling code number *n* and is denoted x_n, in the sequel. Furthermore, let $x_n(i)$ and $y(i)$ denote the *i*:th symbol of the sequence x_n and *y*, respectively

The *m*-sequences x_n and *y* are constructed as:

Initial conditions:

$x_n(0)=n_0$, $x_n(1)= n_1$, … $=x_n(22)= n_{22}$,$x_n(23)= n_{23}$, $x_n(24)=1$

$y(0)=y(1)= \ldots =y(23)= y(24)=1$

Recursive definition of subsequent symbols:

$x_n(i+25) =x_n(i+3) + x_n(i) \text{ modulo } 2, i=0,\ldots, 2^{25}-27,$

$y(i+25) = y(i+3)+y(i+2) +y(i+1) +y(i) \text{ modulo } 2, i=0,\ldots, 2^{25}-27.$

The definition of the *n*:th scrambling code word for the in phase and quadrature components follows as (the left most index correspond to the chip scrambled first in each radio frame):

$c_{1,n} = < x_n(0)+y(0), x_n(1)+y(1), \ldots,x_n(N-1)+y(N-1) >,$

$c_{2,n} = < x_n(M)+y(M), x_n(M+1)+y(M+1), \ldots, x_n(M+N-1) + y(M+N-1) >,$

again all sums being modulo 2 additions.

Where N is the period in chips and M = 16,777,232.

These binary code words are converted to real valued sequences by the transformation ‘0’ -> ‘+1’, ‘1’ -> ‘-1’.

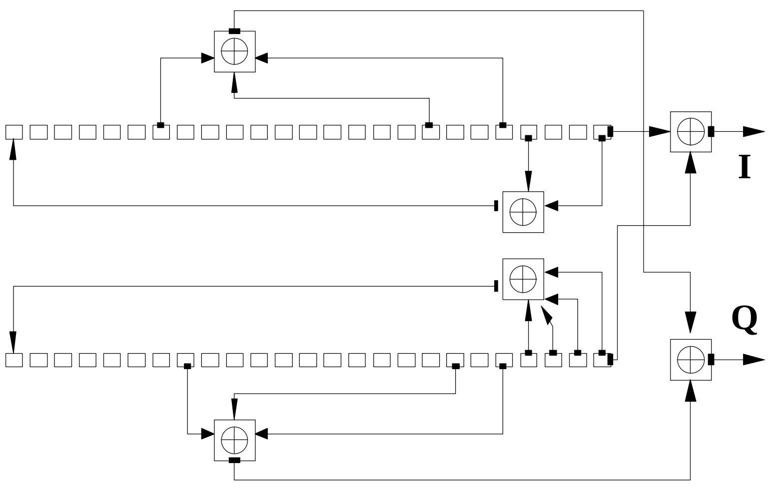

Figure 6. Configuration of uplink scrambling code generator

4.3.2.3 Short scrambling code

The short scrambling codes are formed as described in Section 4.3.2.1,where c1 and c2 are the real and imaginary components of the complex spreading code from the family of periodically extended S(2) codes.

The uplink short codes $S_v(n)$, n=0,1,…255, of length 256 chips are obtained by one chip periodic extension of S(2) sequences of length 255. It means that the first chip ($S_v(0)$) and the last chip ($S_v(255)$) of any uplink short scrambling code are the same.

The quaternary S(2) sequence $z_v(n)$, $0 \le v \le 16{,}777{,}216$, of length 255 is obtained by modulo 4 addition of three sequences, a quaternary sequence $a_r(n)$ and two binary sequences $b_s(n)$ and $c_t(n)$, according to the following relation:

$$z_v(n) = a_r(n) + 2 \cdot b_s(n) + 2 \cdot c_t(n) \quad (mod\ 4)\ , \quad n = 0, 1, \ldots, 254.$$

The user index v determines the indexes r, s, and t of the constituent sequences in the following way:

$$v = t \cdot 2^{16} + s \cdot 2^{8} + r\ ,$$

$r = 0, 1, 2, \ldots, 255,$

$s = 0, 1, 2, \ldots, 255,$

$t = 0, 1, 2, \ldots, 255.$

The quaternary sequence $a_r(n)$ is generated by the recursive generator G_0 defined by the polynomial

$g_0(x)= x^8+x^5+3x^3+x^2+2x+1$ as

$$a_r(n)= 3.a_r(n-3) +1.a_r(n-5) + 3.a_r(n-6) +2.a_r(n-7) + 3.a_r(n-8) \ (mod\ 4).$$

$n = 8 \ldots 254.$

The binary sequence $b_s(n)$ is generated by the recursive generator G_1 defined by the polynomial

$g_1(x)= x^8+x^7+x^5+x+1$ as

$$b_s(n)= b_s(n-1)+ b_s(n-3)+ b_s(n-7)+ b_s(n-8) \ (mod\ 2).$$

The binary sequence $c_t(n)$ is generated by the recursive generator G_2 defined by the polynomial

$g_2(x)= x^8+x^7+x^5+x^4+1$ as

$$c_t(n)= c_t(n-1)+ c_t(n-3)+ c_t(n-4)+ c_t(n-8) \ (mod\ 2).$$

An implementation of the short scrambling code generator is shown in Figure 7. The initial states for the binary generators G_1 and G_2 are the two 8-bit words representing the indexes s and t in the 24-bit binary representation of the user index v, as it is shown in Figure 8.

The initial state for the quaternary generator G_0 is according to Figure 8 obtained after the transformation of 8-bit word representing the index r. This transformation is given by

$a_r(0) = 2v(0)+1 \ \ (mod\ 4), \quad a_r(n) = 2v(n) \ \ (mod\ 4), \quad n = 1,\ldots,7.$

The complex quadriphase sequence $S_v(n)$ is obtained from quaternary sequence $z_v(n)$ by the mapping function given in Table 3.

The Re{Sv(n)} and Im{Sv(n)} of the S(2) code are the pair of two binary sequences corresponding to input binary sequences c_1 and c_2 respectively described in 4.3.2.

zv(n)	Sv(n)
0	+1 + j1
1	-1 + j1
2	-1 - j1
3	+1 - j1

Table 3. Mapping between $S_v(n)$ and $z_v(n)$

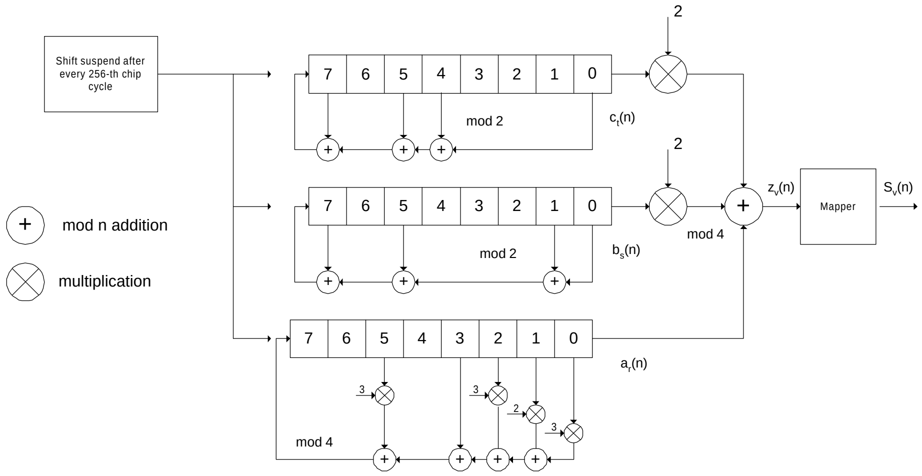

Figure 7. Uplink short scrambling code generator

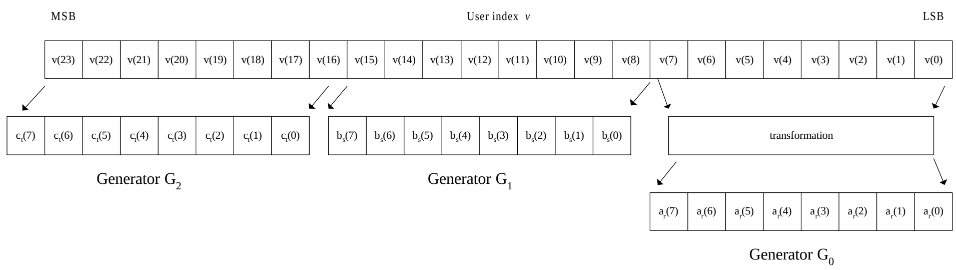

Figure 8. Uplink short scrambling code generator state initialisation

The short scrambling code may, in rare cases, be changed during a connection.

4.3.3 Random access codes

4.3.3.1 Preamble scrambling code

The scrambling code for the preamble part is as follows.

The code generating method is the same as for the real part of the long codes on dedicated channels. Only the first 4096 chips of the code are used for preamble spreading with the chip rate of 3.84 Mchip/s. The long code c1 for the in-phase component is used directly on both in phase and quadrature branches without offset between branches. The preamble scrambling code is defined as the position wise modulo 2 sum of 4096 chips segments of two binary m-sequences generated by means of two generator polynomials of degree 25. Let x and y be the two m-sequences respectively. The x sequence is constructed using the primitive (over GF(2)) polynomial $X^{25}+X^3+1$. The y sequence is constructed using the polynomial $X^{25}+X^3+X^2+X+1$. The resulting sequences thus constitute segments of a set of Gold sequences.

Let $n_7 \ldots n_0$ be the binary representation of the code number *n* (decimal) with n_0 being the least significant bit. The *m*-sequences x_n and *y* are constructed as:

Initial conditions:

$x_n(0)=n_0$, $x_n(1)= n_1$, $\ldots =x_n(6)= n_6$, $x_n(7)= n_7$, $x_n(8)= 0$,…, $x_n(22)= 0$,$x_n(23)= 1$, $x_n(24)=0$

$y(0)=y(1)= \ldots =y(23)= y(24)=1$

Recursive definition of subsequent symbols:

$x_n(i+25) =x_n(i+3) + x_n(i)$ *modulo 2, i=0,…,* 4070,

$y(i+25) = y(i+3)+y(i+2) +y(i+1) +y(i)$ *modulo 2, i=0,…,* 4070.

The definition of the *n*:th code word follows (the left most index correspond to the chip transmitted first in each slot):

$C_{RACH,n} = \langle x_n(0)+y(0), x_n(1)+y(1), \ldots, x_n(4095)+y(4095) \rangle$,

All sums of symbols are taken modulo 2.

The preamble spreading code is described in Figure 9.

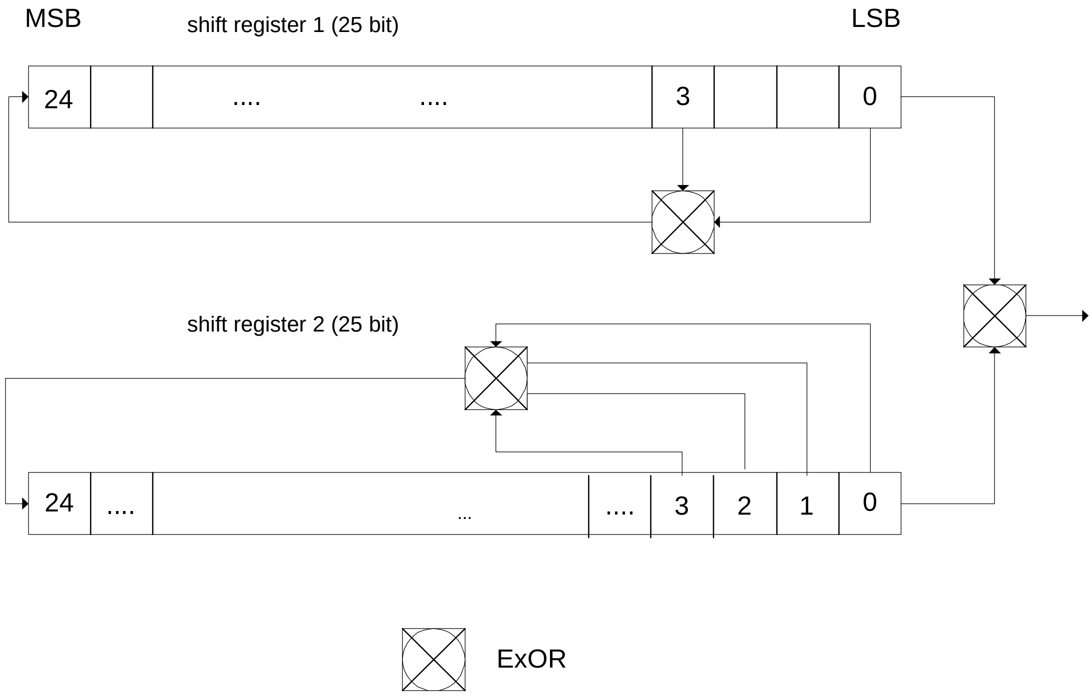

Figure 9. Preamble scrambling code generator

Before transmission these binary code words are converted to real valued sequences by the transformation ‘0’ -> ‘+1’,

Note: WG1 has accepted the 4096 chip long code scrambling as a working assumption.

4.3.3.2 Preamble signature

The preamble part consists of 256 repetitions of a length 16 signature,<P_0,P_1,…,P_{15}>. Before scrambling the preamble is therefore

$$P_0, P_1, \cdots, P_{15}, P_0, P_1, \cdots, P_{15}, \cdots\cdots, P_0, P_1, \cdots, P_{15}$$

The signature is from the set of 16 Hadamard codes of length 16. These are listed in Table 5

	Preamble symbols															
Signature	P_0	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P_8	P_9	P_{10}	P_{11}	P_{12}	P_{13}	P_{14}	P_{15}
1	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
2	A	-A	A	-A	A	-A	A	-A	A	-A	A	-A	A	-A	A	-A
3	A	A	-A	-A	A	A	-A	-A	A	A	-A	-A	A	A	-A	-A
4	A	-A	-A	A	A	-A	-A	A	A	-A	-A	A	A	-A	-A	A
5	A	A	A	A	-A	-A	-A	-A	A	A	A	A	-A	-A	-A	-A
6	A	-A	A	-A	-A	A	-A	A	A	-A	A	-A	-A	A	-A	A
7	A	A	-A	-A	-A	-A	A	A	A	A	-A	-A	-A	-A	A	A
8	A	-A	-A	A	-A	A	A	-A	A	-A	-A	A	-A	A	A	-A
9	A	A	A	A	A	A	A	A	-A	-A	-A	-A	-A	-A	-A	-A
10	A	-A	A	-A	A	-A	A	-A	-A	A	-A	A	-A	A	-A	A
11	A	A	-A	-A	A	A	-A	-A	-A	-A	A	A	-A	-A	A	A
12	A	-A	-A	A	A	-A	-A	A	-A	A	A	-A	-A	A	A	-A
13	A	A	A	A	-A	-A	-A	-A	-A	-A	-A	-A	A	A	A	A
14	A	-A	A	-A	-A	A	-A	A	-A	A	-A	A	A	-A	A	-A
15	A	A	-A	-A	-A	-A	A	A	-A	-A	A	A	A	A	-A	-A
16	A	-A	-A	A	-A	A	A	-A	-A	A	A	-A	A	-A	-A	A

Table 4. Preamble signatures

The value of A = +1 in bipolar representation which is equivalent to 0 in boolean representation.

Note: the Hadamard signatures are a working assumption.

4.3.3.3 Preamble PAPR reduction

In order to reduce the PAPR during RACH preamble transmission the following technique is used.

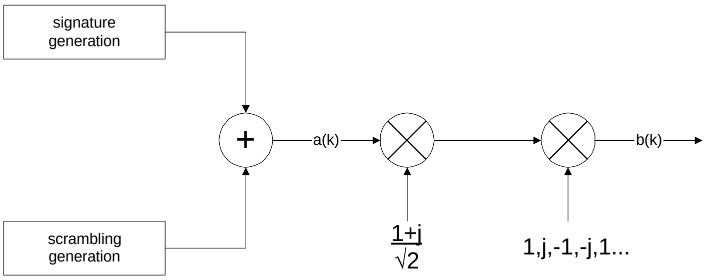

Figure 10 - Baseband modulator for RACH preamble.

The binary preamble $a(k)$ is modulated to get the complex valued preamble $b(k)$,

$$b(k) = a(k)\ e^{j(\frac{\pi}{4}+\frac{\pi}{2}k)},\ k = 0, 1, 2, 3, \ldots, 4095.$$

Note: this is a working assumption.

4.3.3.4 Channelization codes for the message part

The signature in the preamble specifies one of the 16 nodes in the code-tree that corresponds to channelization codes of length 16, as shown in Figure 11. The sub-tree below the specified node is used for spreading of the message part. The control (Q-branch) is spread with the channelization code of spreading factor 256 in the lowest branch of the sub-tree. The data part (I-branch) can use any of the channelization codes from spreading factor 32 to 256 in the upper-most branch of the sub-tree.

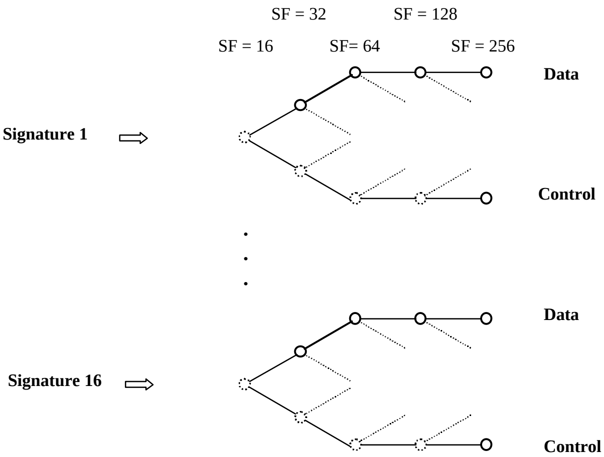

Figure 11. Channelization codes for the random access message part.

4.3.3.5 Scrambling code for the message part

In addition to spreading, the message part is also subject to scrambling with a 10 ms complex code. The scrambling code is cell-specific and has a one-to-one correspondence to the spreading code used for the preamble part.

The scrambling codes used are from the same set of codes as is used for the other dedicated uplink channels when the long scrambling codes are used for these channels. The first 256 of the long scrambling codes are used for the random access channel. The phases 4096..42496 of the codes are used for the message part (phases 0..4095 of c_1 are used in preamble spreading) with the chip rate of 3.84 Mchips/s.

The generation of these codes is explained in Section 4.3.2.2. The mapping of these codes to provide a complex scrambling code is also the same as for the other dedicated uplink channels and is described in Section 4.3.2.

Note: the 4096 long code scrambling is a working assumption.

4.3.4 Common packet channel codes

<to be defined>

4.3.4.1 Access Preamble scrambling code

<to be defined>

4.3.4.2 CD preamble spreading code

<to be defined>

4.3.4.3 CPCH preamble signatures <to be defined>

4.3.4.4 Channelization codes for the CD message part

<to be defined>

4.3.4.5 Scrambling code for the CD message part

<to be defined>

4.4 Modulation

4.4.1 Modulating chip rate

The modulating chip rate is 3.84 Mcps. This basic chip rate can be extended to [0.96,] 7.68 or 15.36 Mcps.

4.4.2 Modulation

In the uplink, the modulation of both DPCCH and DPDCH is BPSK. The modulated DPCCH is mapped to the Q-branch, while the first DPDCH is mapped to the I-branch. Subsequently added DPDCHs are mapped alternatively to the I or Q-branches.

5 Downlink spreading and modulation

5.1 Spreading

Figure 12 illustrates the spreading and modulation for the downlink DPCH. Data modulation is QPSK where each pair of two bits are serial-to-parallel converted and mapped to the I and Q branch respectively. The I and Q branch are then spread to the chip rate with the same channelization code c_{ch} (real spreading) and subsequently scrambled by the scrambling code C_{scramb} (complex scrambling).

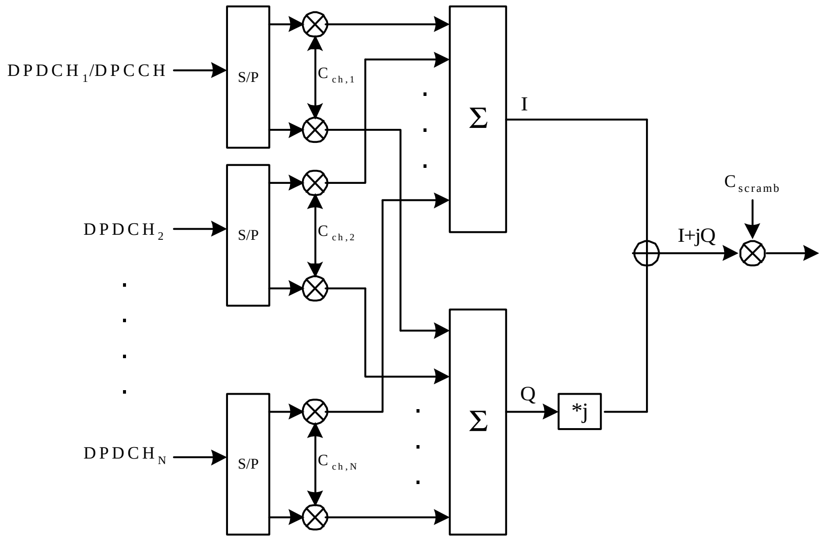

Figure 12. Spreading/modulation for downlink DPCH.

Spreading/modulation of the Secondary CCPCH, PSCCCH, PDSCH, PICH and AICH is done in an identical way as for the downlink DPCH.

Spreading/modulation of the Primary CCPCH is done in an identical way as for the downlink DPCH, except that the Primary CCPCH is time multiplexed after spreading. As illustrated in Figure 13. Primary SCH and Secondary SCH are code multiplexed and transmitted simultaneously during the 1st 256 chips of each slot. The transmission power of SCH can be adjusted by a gain factor $G_{P\text{-}SCH}$ and $G_{S\text{-}SCH}$, respectively, independent of transmission power of P-CCPCH. The SCH is *non-orthogonal* to the other downlink physical channels.

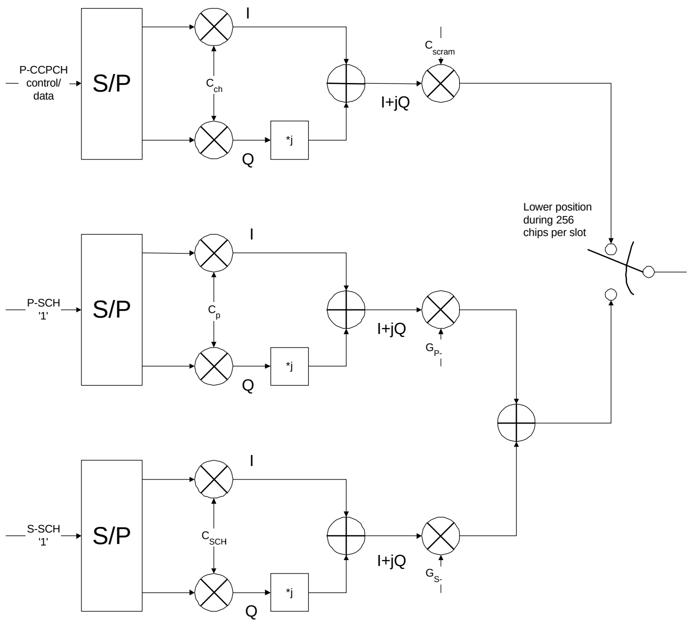

Figure 13. Spreading and modulation for SCH and P-CCPCH

5.2 Code generation and allocation

5.2.1 Channelization codes

The channelization codes of Figure 12 and Figure 13 are the same codes as used in the uplink, namely Orthogonal Variable Spreading Factor (OVSF) codes that preserve the orthogonality between downlink channels of different rates and spreading factors. The OVSF codes are defined in Figure 3 in Section 4.3.1. The same restriction on code allocation applies as for the uplink, but for a cell and not a UE as in the uplink. Hence, in the downlink, a specific combination of channelization code and scrambling code can be used in a cell if and only if no other channelization code on the path from the specific code to the root of the tree or in the sub-tree below the specific code is used in the same cell with the same scrambling code.

The channelization code for the BCH is a predefined code which is the same for all cells within the system.

The channelization code(s) used for the Secondary Common Control Physical Channel is broadcast on the BCH.

<Editor's note: the above sentence may not be within the scope of this document.>

5.2.2 Scrambling code

There are a total 512*512 = 262,144 scrambling codes, numbered 0…262,143. The scrambling codes are divided into 512 sets each of a primary scrambling code and 511 secondary scrambling codes.

The primary scrambling codes consist of scrambling codes i=0…511. The i:th set of secondary scrambling codes consists of scrambling codes i+k*512, where k=1…511.

There is a one-to-one mapping between each primary scrambling code and 511 secondary scrambling codes in a set such that i:th primary scrambling code corresponds to i:th set of scrambling codes.

The set of primary scrambling codes is further divided into 32 scrambling code groups, each consisting of 16 primary scrambling codes. The j:th scrambling code group consists of scrambling codes j*16, …, j*16+15, where j=0, …, 31.

Each cell is allocated one and only one primary scrambling code. The primary CCPCH is always transmitted using the primary scrambling code. The other downlink physical channels can be transmitted with either the primary scrambling code or a secondary scrambling code from the set associated with the primary scrambling code of the cell.

<Editor's note: There may be a need to limit the actual number of codes used in each set of secondary scrambling codes, in order to limit the signalling requriements. >

<Editor's note: it is not standardised how many scrambling codes a UE must decode in parallel.>

The scrambling code sequences are constructed by combining two real sequences into a complex sequence. Each of the two real sequences are constructed as the position wise modulo 2 sum of [38400 chip segments of] two binary *m*-sequences generated by means of two generator polynomials of degree 18. The resulting sequences thus constitute segments of a set of Gold sequences. The scrambling codes are repeated for every 10 ms radio frame. Let *x* and *y* be the two sequences respectively. The *x* sequence is constructed using the primitive (over GF(2)) polynomial $1+X^7+X^{18}$. The y sequence is constructed using the polynomial $1+X^5+X^7+X^{10}+X^{18}$.

<Editor's note: [ ] is due to the fact that only 3.84Mcps is an agreement. 0.96, 7.68, and 15.36Mcps are ffs.>

Let $n_{17} \ldots n_0$ be the binary representation of the scrambling code number *n* (decimal) with n_0 being the least significant bit. The *x* sequence depends on the chosen scrambling code number *n* and is denoted x_n, in the sequel. Furthermore, let $x_n(i)$ and $y(i)$ denote the *i*:th symbol of the sequence x_n and *y*, respectively

The *m*-sequences x_n and *y* are constructed as:

Initial conditions:

$x_n(0)=n_0$, $x_n(1)= n_1$, … $=x_n(16)= n_{16}$, $x_n(17)= n_{17}$

$y(0)=y(1)= \ldots =y(16)= y(17)=1$

Recursive definition of subsequent symbols:

$x_n(i+18) =x_n(i+7) + x_n(i) \text{ modulo } 2,\ i=0,\ldots,2^{18}-20,$

$y(i+18) = y(i+10)+y(i+7)+y(i+5)+y(i) \text{ modulo } 2,\ i=0,\ldots, 2^{18}-20.$

The n:th Gold code sequence z_n is then defined as

$z_n(i) = x_n(i) + y(i) \text{ modulo } 2,\ i=0,\ldots, 2^{18}-2.$

These binary code words are converted to real valued sequences by the transformation ‘0’ -> ‘+1’, ‘1’ -> ‘-1’.

Finally, the n:th complex scrambling code sequence C_{scramb} is defined as (the lowest index corresponding to the chip scrambled first in each radio frame): (where N is the period in chips and M is 131,072)

$C_{scramb}(i) = z_n(i) + j\, z_n(i+M),\ i=0,1,\ldots,N-1.$
<Editor’s note: the values 38400 is based on an assumption of a chip rate of 3.84 Mcps.>

Note that the pattern from phase 0 up to the phase of 38399 is repeated.

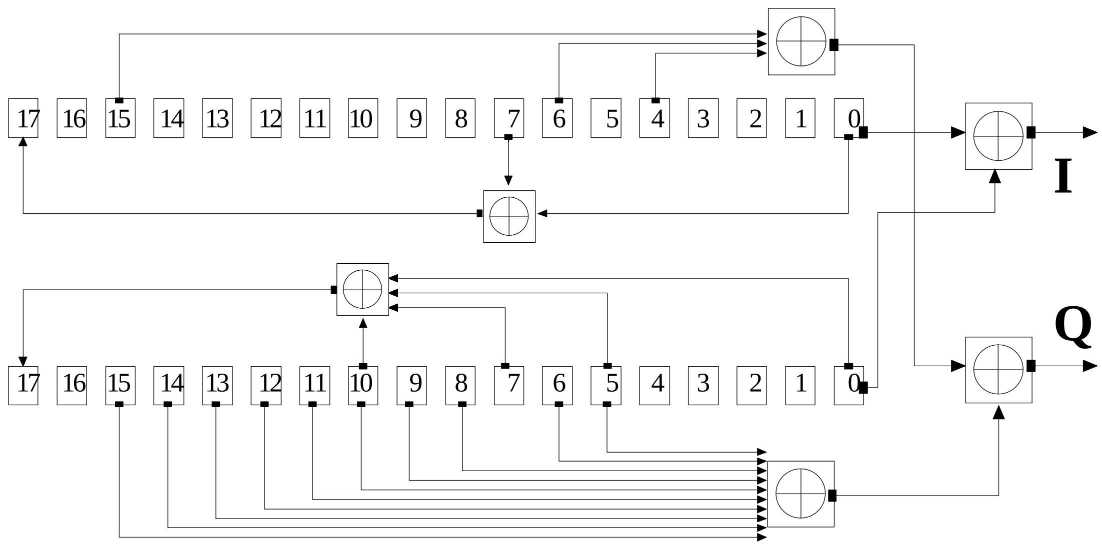

Figure 14. Configuration of downlink scrambling code generator

5.2.3 Synchronisation codes

5.2.3.1 Code Generation

The Primary code sequence, C_p is constructed as a so-called generalised hierarchical Golay sequence. The Primary SCH is furthermore chosen to have good aperiodic auto correlation properties.

Letting a = $<x_1, x_2, x_3, \ldots, x_{16}>$ = <0, 0, 0, 0, 0, 0, 1, 1, 0, 1, 0, 1, 0, 1, 1, 0> and

$$b =< x_1, x_2,.., x_8, \bar{x}_9, \bar{x}_{10},.., \bar{x}_{16} >$$

The PSC code is generated by repeating sequence ‘a’ modulated by a Golay complementary sequence.

Letting $y =< a, a, a, \bar{a}, \bar{a}, a, \bar{a}, \bar{a}, a, a, a, \bar{a}, a, \bar{a}, a, a >$

The definition of the PSC code word C_p follows (the left most index corresponds to the chip transmitted first in each time slot):

C_p=<y(0),y(1),y(2),...,y(255)>.

Let the sequence $Z = \{b,b,b,\bar{b},b,b,\bar{b},\bar{b},b,\bar{b},b,\bar{b},\bar{b},\bar{b},\bar{b},\bar{b}\}$. Then the Secondary Synchronization code words, $\{C_1,\ldots,C_{16}\}$ are constructed as the position wise addition modulo 2 of a Hadamard sequence and the sequence *z*.
The Hadamard sequences are obtained as the rows in a matrix H_8 constructed recursively by:

$$H_0 = (0)$$
$$H_k = \begin{pmatrix} H_{k-1} & H_{k-1} \\ H_{k-1} & \overline{H_{k-1}} \end{pmatrix}, \quad k \geq 1$$

The rows are numbered from the top starting with row *0* (the all zeros sequence).

The Hadamard sequence *h* depends on the chosen code number *n* and is denoted h_n in the sequel.

This code word is chosen from every 16^{th} row of the matrix H_8 implying 16 possible code words given by n =0,16,32,48,64,80,96,112,128,144,160,176,192,208,224,240.

Furthermore, let $h_n(i)$ and $z(i)$ denote the *i:*th symbol of the sequence h_n and *z*, respectively.

The definition of the *n*:th SCH code word follows (the left most index correspond to the chip transmitted first in each slot):

$C_{SCH,n} = \langle h_n(0)+z(0), h_n(1)+z(1), h_n(2)+z(2), \ldots, h_n(255)+z(255) \rangle$,

All sums of symbols are taken modulo 2.

These PSC and SSC binary code words are converted to real valued sequences by the transformation ‘0’ -> ‘+1’, ‘1’ ->

The Secondary SCH code words are defined in terms of $C_{SCH,n}$ and the definition of $\{C_1,\ldots,C_{16}\}$ now follows as:
$C_i = C_{SCH,i}$, i=1,…,16

5.2.3.2 Code Allocation

The 32 sequences are constructed such that their cyclic-shifts are unique, i.e., a non-zero cyclic shift less than 15 of any of the 32 sequences is not equivalent to some cyclic shift of any other of the 32 sequences. Also, a non-zero cyclic shift less than 15 of any of the sequences is not equivalent to itself with any other cyclic shift less than 15. The following sequences are used to encode the 32 different scrambling code groups (note that c_i indicates the i’th Secondary Short code of the 16 codes). Note that a Secondary Short code can be different from one time slot to another and that the sequence pattern can be different from one cell to another, depending on Scrambling Code Group the cell uses

Scrambling Code Groups	Slot Number														
	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14	#15
Group1	C_1	C_1	C_2	C_8	C_9	C_{10}	C_{15}	C_8	C_{10}	C_{16}	C_2	C_7	C_{15}	C_7	C_{16}
Group2	C_1	C_2	C_5	C_2	C_3	C_7	C_7	C_1	C_8	C_4	C_6	C_5	C_8	C_6	C_3
Group 3	C_1	C_3	C_{12}	C_{12}	C_{16}	C_5	C_{14}	C_{10}	C_7	C_5	C_{10}	C_3	C_{16}	C_1	C_7
Group 4	C_1	C_5	C_7	C_{13}	C_7	C_1	C_9	C_9	C_5	C_{11}	C_3	C_{15}	C_{13}	C_{11}	C_{15}
Group 5	C_1	C_9	C_{16}	C_3	C_8	C_9	C_3	C_{11}	C_1	C_6	C_8	C_6	C_{11}	C_{14}	C_{14}
Group 6	C_1	C_4	C_{15}	C_{14}	C_6	C_{12}	C_6	C_{15}	C_9	C_9	C_{14}	C_1	C_7	C_4	C_{12}
Group 7	C_1	C_7	C_{13}	C_1	C_2	C_{14}	C_{12}	C_7	C_{12}	C_2	C_{11}	C_{11}	C_{14}	C_{13}	C_8

Group 8	C_{1}	C_{13}	C_{9}	C_{10}	C_{10}	C_{2}	C_{5}	C_{6}	C_{14}	C_{1}	C_{5}	C_{14}	C_{9}	C_{2}	C_{13}
Group 9	C_{1}	C_{12}	C_{1}	C_{9}	C_{11}	C_{11}	C_{10}	C_{4}	C_{2}	C_{3}	C_{12}	C_{4}	C_{3}	C_{9}	C_{10}
Group 10	C_{1}	C_{6}	C_{4}	C_{11}	C_{13}	C_{16}	C_{1}	C_{16}	C_{11}	C_{7}	C_{7}	C_{13}	C_{6}	C_{10}	C_{4}
Group 11	C_{1}	C_{11}	C_{6}	C_{15}	C_{1}	C_{6}	C_{2}	C_{5}	C_{16}	C_{15}	C_{16}	C_{2}	C_{12}	C_{12}	C_{5}
Group 12	C_{1}	C_{8}	C_{10}	C_{7}	C_{12}	C_{3}	C_{4}	C_{2}	C_{6}	C_{14}	C_{15}	C_{9}	C_{5}	C_{16}	C_{11}
Group 13	C_{1}	C_{15}	C_{3}	C_{6}	C_{15}	C_{13}	C_{8}	C_{12}	C_{3}	C_{12}	C_{13}	C_{10}	C_{10}	C_{8}	C_{6}
Group 14	C_{1}	C_{16}	C_{8}	C_{4}	C_{5}	C_{4}	C_{16}	C_{13}	C_{13}	C_{8}	C_{9}	C_{12}	C_{1}	C_{5}	C_{9}
Group 15	C_{1}	C_{14}	C_{14}	C_{16}	C_{4}	C_{15}	C_{13}	C_{3}	C_{4}	C_{13}	C_{1}	C_{16}	C_{2}	C_{3}	C_{2}
Group 16	C_{1}	C_{10}	C_{11}	C_{5}	C_{14}	C_{8}	C_{11}	C_{14}	C_{15}	C_{10}	C_{4}	C_{8}	C_{4}	C_{15}	C_{1}
Group 17	C_{2}	C_{6}	C_{8}	C_{14}	C_{8}	C_{2}	C_{10}	C_{10}	C_{6}	C_{12}	C_{4}	C_{16}	C_{14}	C_{12}	C_{16}
Group 18	C_{2}	C_{5}	C_{3}	C_{12}	C_{14}	C_{15}	C_{2}	C_{15}	C_{12}	C_{8}	C_{8}	C_{14}	C_{5}	C_{9}	C_{3}
Group 19	C_{2}	C_{8}	C_{14}	C_{2}	C_{1}	C_{13}	C_{11}	C_{8}	C_{11}	C_{1}	C_{12}	C_{12}	C_{13}	C_{14}	C_{7}
Group 20	C_{2}	C_{2}	C_{1}	C_{7}	C_{10}	C_{9}	C_{16}	C_{7}	C_{9}	C_{15}	C_{1}	C_{8}	C_{16}	C_{8}	C_{15}
Group 21	C_{2}	C_{14}	C_{10}	C_{9}	C_{9}	C_{1}	C_{6}	C_{5}	C_{13}	C_{2}	C_{6}	C_{13}	C_{10}	C_{1}	C_{14}
Group 22	C_{2}	C_{7}	C_{9}	C_{8}	C_{11}	C_{4}	C_{3}	C_{1}	C_{5}	C_{13}	C_{16}	C_{10}	C_{6}	C_{15}	C_{12}
Group 23	C_{2}	C_{4}	C_{11}	C_{11}	C_{15}	C_{6}	C_{13}	C_{9}	C_{8}	C_{6}	C_{9}	C_{4}	C_{15}	C_{2}	C_{8}
Group 24	C_{2}	C_{10}	C_{15}	C_{4}	C_{7}	C_{10}	C_{4}	C_{12}	C_{2}	C_{5}	C_{7}	C_{5}	C_{12}	C_{13}	C_{13}
Group 25	C_{2}	C_{15}	C_{7}	C_{3}	C_{6}	C_{3}	C_{15}	C_{14}	C_{14}	C_{7}	C_{10}	C_{11}	C_{2}	C_{6}	C_{10}
Group 26	C_{2}	C_{1}	C_{6}	C_{1}	C_{4}	C_{8}	C_{8}	C_{2}	C_{7}	C_{3}	C_{5}	C_{6}	C_{7}	C_{5}	C_{4}
Group 27	C_{2}	C_{16}	C_{4}	C_{5}	C_{16}	C_{14}	C_{7}	C_{11}	C_{4}	C_{11}	C_{14}	C_{9}	C_{9}	C_{7}	C_{5}
Group 28	C_{2}	C_{3}	C_{16}	C_{13}	C_{5}	C_{11}	C_{5}	C_{16}	C_{10}	C_{10}	C_{13}	C_{2}	C_{8}	C_{3}	C_{11}
Group 29	C_{2}	C_{12}	C_{5}	C_{16}	C_{2}	C_{5}	C_{1}	C_{6}	C_{15}	C_{16}	C_{15}	C_{1}	C_{11}	C_{11}	C_{6}
Group 30	C_{2}	C_{11}	C_{2}	C_{10}	C_{12}	C_{12}	C_{9}	C_{3}	C_{1}	C_{4}	C_{11}	C_{3}	C_{4}	C_{10}	C_{9}
Group 31	C_{2}	C_{9}	C_{12}	C_{6}	C_{13}	C_{7}	C_{12}	C_{13}	C_{16}	C_{9}	C_{3}	C_{7}	C_{3}	C_{16}	C_{2}
Group 32	C_{2}	C_{13}	C_{13}	C_{15}	C_{3}	C_{16}	C_{14}	C_{4}	C_{3}	C_{14}	C_{2}	C_{15}	C_{1}	C_{4}	C_{1}
[SyncBTS]	C_{3}	C_{11}	C_{14}	C_{1}	C_{6}	C_{11}	C_{1}	C_{9}	C_{3}	C_{8}	C_{6}	C_{8}	C_{9}	C_{16}	C_{16}

Table 9 Spreading Code allocation for Secondary SCH Code

5.3 Modulation

5.3.1 Modulating chip rate

The modulating chip rate is 3.84 Mcps. This basic chip rate can be extended to [0.96,] 7.68 or 15.36 Mcps.

5.3.2 Modulation

QPSK modulation is used.

Annex A Generalised Hierarchical Golay Sequences

A.1 Alternative generation

The generalised hierarchical Golay sequences for the PSC described in 5.2.3.1 may be also viewed as generated (in real valued representation) by the following methods:

Method 1.

The sequence y is constructed from two constituent sequences x_1 and x_2 of length n_1 and n_2 respectively using the following formula:

$y(i) = x_2(i \bmod n_2) * x_1(i \operatorname{div} n_2),\ i = 0 \ldots (n_1 * n_2) - 1$

The constituent sequences x_1 and x_2 are chosen to be the following length 16 (i.e. $n_1 = n_2 = 16$) sequences:

- x_1 is defined to be the length 16 ($N^{(1)}=4$) Golay complementary sequence obtained by the delay matrix $D^{(1)} = [8, 4, 1, 2]$ and weight matrix $W^{(1)} = [1, -1, 1, 1]$.

- x_2 is a generalised hierarchical sequence using the following formula, selecting s=2 and using the two Golay complementary sequences x_3 and x_4 as constituent sequences. The length of the sequence x_3 and x_4 is called n_3 respectively n_4.

  $x_2(i) = x_4(i \bmod s + s*(i \operatorname{div} sn_3)) * x_3((i \operatorname{div} s) \bmod n_3),\ i = 0 \ldots (n_3 * n_4) - 1$

  x_3 and x_4 are defined to be identical and the length 4 ($N^{(3)}= N^{(4)}=2$) Golay complementary sequence obtained by the delay matrix $D^{(3)} = D^{(4)} = [1, 2]$ and weight matrix $W^{(3)} = W^{(4)} = [1, 1]$.

The Golay complementary sequences x_1,x_3 and x_4 are defined using the following recursive relation:

$a_0(k) = \delta(k)$ and $b_0(k) = \delta(k)$

$a_n(k) = a_{n-1}(k) + W^{(j)}_n \cdot b_{n-1}(k-D^{(j)}_n)$,

$b_n(k) = a_{n-1}(k) - W^{(j)}_n \cdot b_{n-1}(k-D^{(j)}_n)$,

$k = 0, 1, 2, \ldots, 2^{**}N^{(j)} -1$,

$n = 1, 2, \ldots, N^{(j)}$.

The wanted Golay complementary sequence x_j is defined by a_n assuming $n=N^{(j)}$. The Kronecker delta function is described by δ, k,j and n are integers.

Method 2

The sequence y can be viewed as a pruned Golay complementary sequence and generated using the following parameters which apply to the generator equations for a and b above:

(a) Let $j = 0$, $N^{(0)} = 8$

(b) $[D_1^0,D_2^0,D_3^0,D_4^0,D_5^0,D_6^0,D_7^0,D_8^0] = [128, 64, 16, 32, 8, 1, 4, 2]$

(c) $[W_1^0,W_2^0,W_3^0,W_4^0,W_5^0,W_6^0,W_7^0,W_8^0] = [1, -1, 1, 1, 1, 1, 1, 1]$

(d) For $n = 4, 6$, set $b_4(k) = a_4(k)$, $b_6(k) = a_6(k)$.

6 History

Document history		
draft	1999-02-12	New document merged from ETSI XX.05 and ARIB 3.2.4 sources.
0.0.1	1999-02-12	Corrected typo in table2.
0.0.2	1999-02-16	Added sec. SCH code table, option for HPSK on S(2) codes, scale on SCH.
0.0.3	1999-02-18	Reflected decision made on SCH multiplexing (see document titled 'Report from Ad Hoc #2 SCH multiplexing'.) and additional description on the use of S(2) for uplink short scrambling code.
0.1.0	1999-02-28	Raised to 0.1.0 after TSG RAN WG1#2 meeting (Yokohama).
1.0.0	1999-03-12	Raised to 1.0.0 when presented to TSG RAN.
1.0.1	1999-03-17	Raised to 1.0.1 incorporated Ad Hoc changes and errata from e-mail.
1.0.2	1999-03-23	Raised to 1.0.2 incorporated reports from Ad Hocs plus editorial matters.
1.0.3	1999-03-24	Raised to 1.0.3 incorporated actions from WG1#3 plenary..
1.1.0	1999-03-26	Raised to 1.1.0 changed as result of text proposal, Tdoc 298.
1.1.1	1999-04-12	Raised to 1.1.1 by incorporating 3GPP template and adding editor's note.
1.1.2	1999-04-12	Raised to 1.1.2 by entering editorial changes with revision marks.
1.1.3	1999-04-19	Rasied to 1.1.3 by Tdocs 347, 385 at WG1#4 meeting (Yokohama)
1.1.4	1999-04-20	Raised to 1.1.4 by Tdoc 397 at WG1#4 meeting (Yokohama)
2.0.0	1999-04-20	Raised to 2.0.0 at WG1#4 (Yokohama) for presentation to RSG RAN.
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