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Agenda item :
Source : CSELT[1]
Title : BER on power control bits
Document for : decision

Rationale

Performance of power control commands is evaluated in order to estimate their reliability in uplink and downlink. Simulations have been carried out for the 144 kbit/s LCD data service.

Recommendations

The reliability of TPC bits in downlink (with high data rate services) has to be improved with respect to the current assumptions (2 TPC bits independently of the DPDCH bit rate).
Possible solutions are to adopt a power offset for different DPCCH fields or to increase the number of power control bits.
Suitable DPCCH configuration for downlink in case of spreading factor lower or equal than 16 are (case without offset on DPCCH fields):

Pilot bits	TPC bits	TFCI bits
16	8	8
24	8	0

Further investigations may be required for low data rate services.

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Introduction

The BER on power control bits has been evaluated by simulation in case of high data rate services. In this document results obtained with the 144 kbit/s LCD data service are considered.

The BER performance is given as a function of the Eb/No ratio (Eb=energy per information bits, No=noise power spectral density) measured at the receiver side on DPDCH bits. The Eb/No includes all the transmission overheads (Pilot, TPC, TFI, tail bits, coding, rate matching, etc.) and the possible offset introduced by the closed loop power control on the received power.

The simulation parameters are listed in Tab. 1. Note that the error probability on power control commands (in the link not under evaluation) is considered fixed during the simulation. This is a simplified model, but we think it is sufficiently accurate for the purpose of this paper (evaluation of DPCCH bits performance in the examined link). A turbo coding scheme with 8 states, polynomial generators 13_8 and 15_8 and 5120 bits MIL internal interleaver has been adopted.

Downlink results

Performance of downlink has been evaluated with different conditions relevant to DPCCH overhead. Fig. 1 shows a comparison between performance of 144 kbit/s LCD service based on the ITU assumptions (as presented in the ITU evaluation report) and based on a more precise propagation model (CSELT assumptions). Other differences between the two simulation models are the number of pilot bits per slot and the error probability on TPC bits. The differences between the two assumptions are listed in Tab. 2, while Tabs. 3 and 4 give the different channel model.

With both models it can be seen that the performance of TPC bits is quite poor. Curves are very flat and at the operating point for the DPDCH we obtain a TPC BER of about $8 \cdot 10^{-2}$ with two TPC bits and a TPC BER greater than 10^{-1} with 1 TPC bit. As a consequence, some improvement is needed. Two possible solutions (equivalent from a performance point of view) are to increase the power of the TPC field or to increase the number of TPC bits to be transmitted in downlink.

The following results have been obtained with the complete (6 taps) channel.

Fig. 2 shows the performance obtained with different power offsets for the downlink TPC field (0, +3 and +6 dB). This figure has been obtained by using 16 pilot bits and an error probability on power control commands in the uplink equal to 0.1% (see uplink results). This figure shows that to achieve a BER on downlink TPC commands in the range 1-2% a power offset equal to 6 dB (or an increase from 2 to 8 in the number of TPC bits) is required. Note that this has a very small impact (negligible) on DPDCH performance, as shown also in Fig. 2, where the BER curves are given after the first iteration of the turbo code.

Finally, Fig. 3 evaluates the impact of different DPCCH overheads on the DPDCH performance. As it can be seen, the case with 16 pilots, 2 TPC bits and 0 TFCI bits presents performance practically equivalent to the case with 24 pilots, 8 TPC and 8 TFCI bits.

Conclusions

From simulation results, it comes out that the current assumption to use 2 TPC bits to carry power control commands in downlink implies a low reliability of TPC bits in case of high bit rate services. The results show that an error rate on the order of $8 \cdot 10^{-2}$

is achieved with two TPC bits at the working point for data. Error rates greater than 10^{-1} are achieved in case only one TPC bit is transmitted in downlink (this can happen if TPC bits are punctured to allow transmission of other fields).
TPC commands error rate can be improved by increasing the available energy. Possible (equivalent from a link level point of view) solutions are to increase the transmission power of the TPC field or to increase the number of TPC bits in downlink. With a power offset of +6 dB (i.e., by transmitting 8 TPC bits) the error rate on power control commands is on the order of 1-2%. The increase of power dedicated to TPC bits has a negligible impact on DPDCH performance. Simulations carried out as a function of the DPCCH overhead confirm this result.
Suitable DPCCH configuration for downlink in case of spreading factor lower or equal than 16 are (case without offset on DPCCH fields):

Pilot bits	TPC bits	TFCI bits
16	8	8

To maintain the same DPCCH overhead, in case no TFCI bits are transmitted, the proposed solution becomes:

Pilot bits	TPC bits	TFCI bits
24	8	0

Uplink results

Taking into account the results obtained in downlink, BER figures have been derived also in uplink. The main impact of downlink simulation on uplink results is the error probability on power control commands sent in downlink to vary the transmisison power of the terminal. On the basis of previous results, the error probability on downlink power control commands has been set equal to 10%.
Fig. 4 gives the uplink performance as a function of the power ratio between DPCCH and DPDCH. From the figure it comes out that the optimal ratio is –6 dB. In this condition the error rate on uplink TPC commands (2 TPC bits) is on the order of 0.1-0.3%. with only 1 TPC bit the error rate for uplink TPC commands becomes on the order of 1-2%.
The power control performance can be improved by increasing the DPCCH power at the expenses of DPDCH performance (about 0.5 dB loss).

Conclusion

In the uplink (high data rate case) the high spreading factor on DPCCH (SF=256) permits to achieve a low TPC BER in case an optimal power ratio between DPCCH and DPDCH is used. More in general, a further degree of flexibility to increase DPCCH performance in uplink is to vary the power ratio between the two physical channels.
Note that the difference on the DPDCH performance between uplink and downlink can be explained by:

- No antenna diversity is adopted in downlink
- The channel estimation is less reliable in downlink (the pilot filed has a shorter duration in time with respect to the uplink and the pilot symbols have a lower bit energy)

arameter	Downlink	Uplink
	LCD 144 kbit/s data service	LCD 144 kbit/s data service
ation bits per sub-block	120 (12 sub-blocks of 120 bits=1440 bits)	120 (12 sub-blocks of 120 bits=1440 bits)
nd tail bits	8+0	8+0
	rate 1/3, 8 states	rate 1/3, 8 states
	MIL 5120 bits	MIL 5120 bits
ation	Internal	Internal
tors (octal)	13, 15	13, 15
gorithm	Max-Log MAP	Max-log MAP
	N.A.	9 -> 10
r	20 ms (96x96 bit)	20 ms (128x80 bit)
	16	16
he DPCCH	See figures	6/2/2
nsmission (DTX)	apllied	N.A.
he DPDCH per each slot	640	320
DPDCH)	8	8
DPDCH)	28.4	28.4
DPCCH)	8	256
h respect to DPDCH [dB]	N.A.	See figure
	QPSK	QPSK
	4.096 MHz	4.096 MHz
	Raised cosine (roll-off 0.22)	Raised cosine (roll-off 0.22)
	Ideal	Ideal
y on TPC bits	See figures	See figures
	1 slot (0.625 ms)	1 slot (0.625 ms)
amic	unlimited	unlimited
	± 0.5 dB	± 0.5 dB
	2 GHz	2 GHz
nel	Vehicular A	Vehicular A
	120 km/h	120 km/h
gers	3	3
	no	yes
timation	Linear interpolation on two consecutive time slots	

Tab. 1 Parameters of the simulated radio chain (144 kbit/s LCD data)

Parameter	CSELT	ITU
odel	Vehicular A standard (6 rays)	Vehicular A simplified (4 rays with delay multiple of the chip period)
Rake's fingers	3	4
-TFI	8+2+0	16+2+0
	342 bit per slot	334 bits per slot
C bits	5%	1%

Tab. 2 Differences between CSELT and ITU simulation parameters

Vehicular A channel (standard)			
Tap	**Relative delay [ns]**	**Average power [dB]**	**Doppler spectrum**
1	0	0.0	CLASSIC
2	310	-1.0	CLASSIC
3	710	-9.0	CLASSIC
4	1090	-10.0	CLASSIC
5	1730	-15.0	CLASSIC
6	2510	-20.0	CLASSIC

Tab. 3 – Vehicular A channel model (standard) – CSELT assumption

Vehicular A channel (simplified)			
Tap	**Relative delay [ns]**	**Average power [dB]**	**Doppler spectrum**
1	0	0.0	CLASSIC
2	Tc	-2.37	CLASSIC
3	2·Tc	-6.46	CLASSIC
4	3·Tc	-9.42	CLASSIC

Tab. 4 – Vehicular A channel model (simplified) - ITU assumption

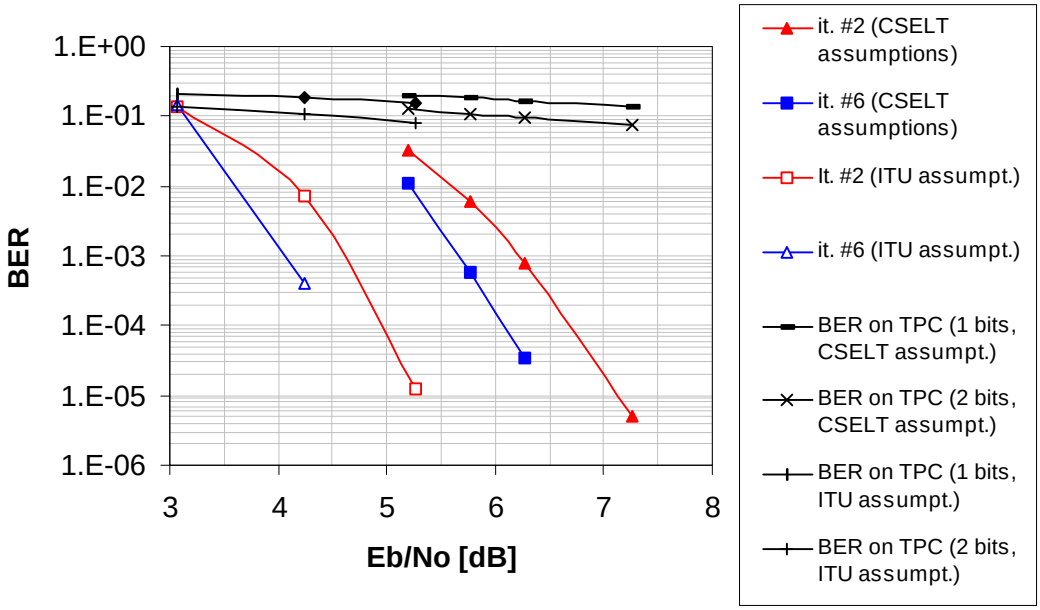

Fig. 1 LCD 144 kbit/s data service, downlink (it. # X=BER on DPDCH after X turbo iterations). Simulation assumptions are indicated in Tabs. 1 and 2.

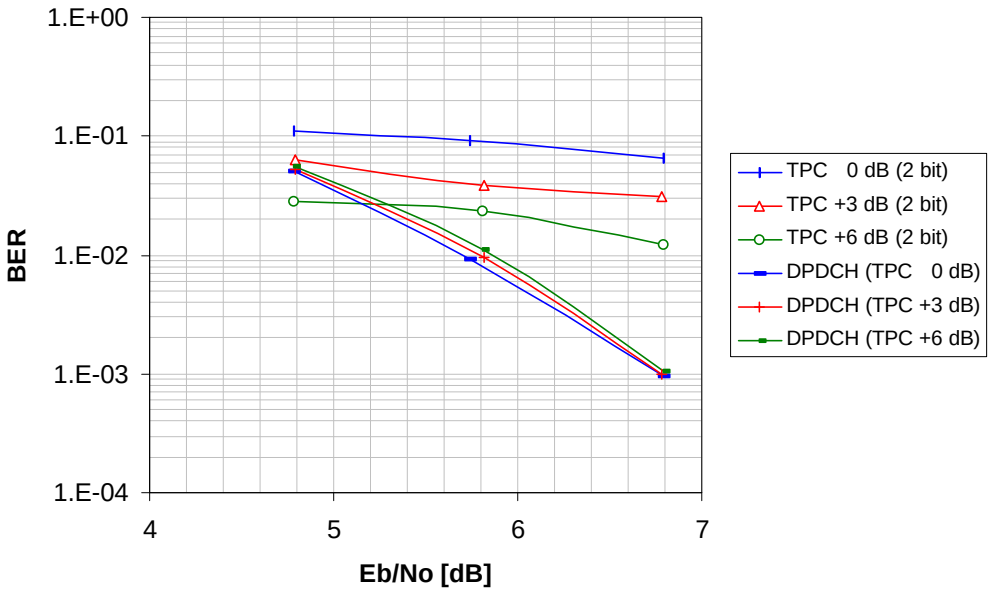

Fig. 2 LCD 144 kbit/s data service, downlink. TPC and DPDCH bit error rate as a function of the power offset in the TPC field. DPDCH figures are given after the first iteration of the turbo decoder. Error probability for uplink power control commands: 0.1% - DPCCH fields: pilot/TPC/TFCI: 16/2/0.

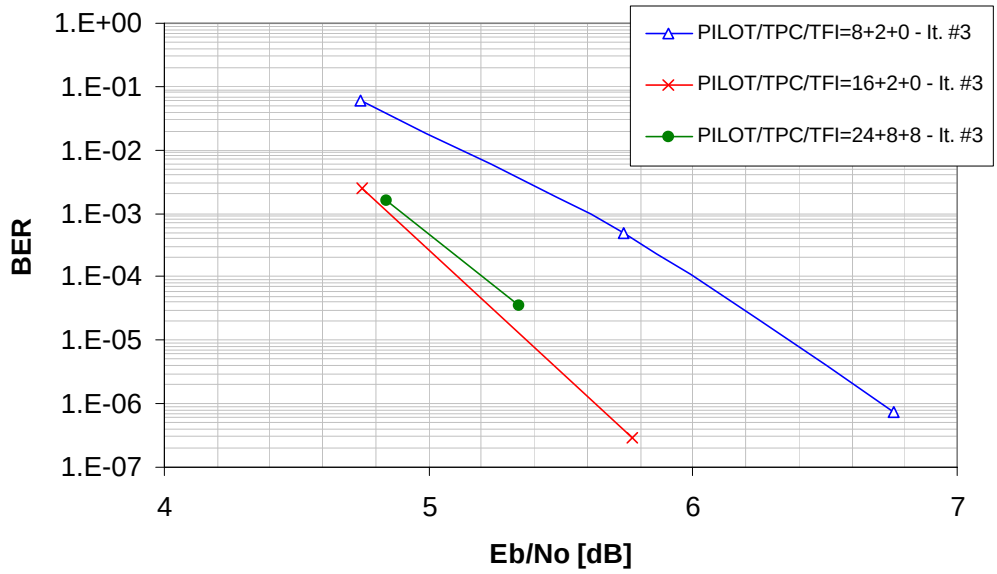

Fig. 3 LCD 144 kbit/s data service, downlink. DPDCH bit error rate (after iteration #3)as a function of different DPCCH overheads. Error probability for uplink power control commands: 0.1%.

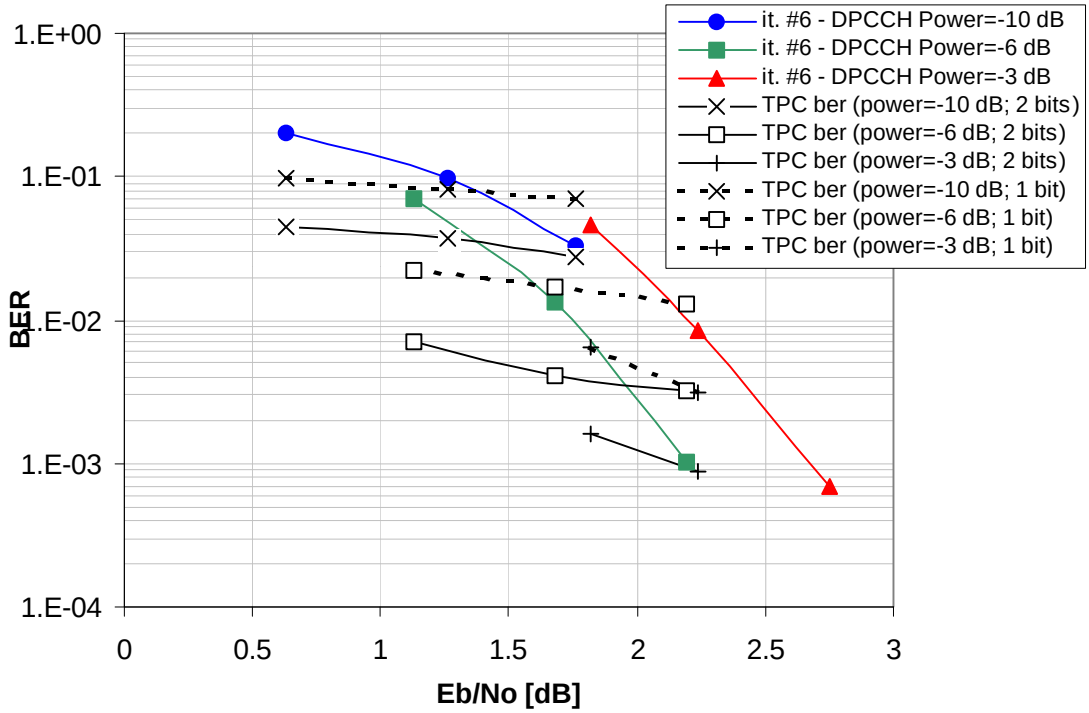

Fig. 4 LCD 144 kbit/s data service, uplink. DPDCH bit error rate (after iteration #6)as a function of the power ratio between DPCCH and DPDCH. Error probability for downlink power control commands: 10%.