TSG-RAN Working Group 1 meeting #3 **TSGR1 #3(99) 167**
Nynäshamn/Stockholm, Sweden; 22.-26. March 1999

Agenda Item:

Source: Siemens

Title: Monitoring for Handover from TDD to GSM

Document for: Handover Preparation

Monitoring for Handover from TDD to GSM

The intention of this document is an explanation of the TDD resources necessary for the handover from TDD to GSM. In the current specification S1.25 concerning high data rate traffic it is proposed to consider 2 consecutive TDD timeslots for a dual synthesizer terminal as sufficient to detect the FCCH.
The following article will show that at least 3 consecutive TDD timeslots must be used for monitoring to guarantee an FCCH detection. Furthermore some simulation results for average and the maximum synchronisation time will be presented explaining that with monitoring every TDD frame the maximum synchronisation time cannot exceed 660ms.

1. FCCH burst positions in a TDD frame

As depicted in fig.1 the GSM multiframe consists of 51 GSM frames (=periods of 60ms/13 which are divided in 8 slots: slot 0 ... slot 7) and the FCCH bursts necessary for the synchronisation is slot 0 of frame 0, 10, 20, 30 and 40.

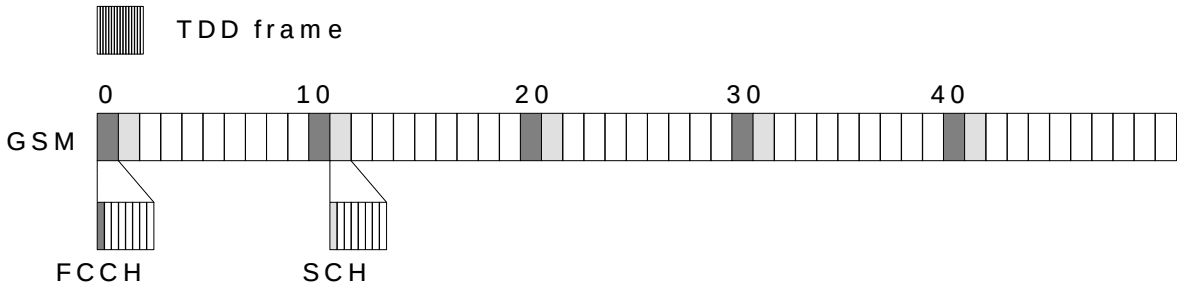

figure 1 TDD frame and GSM multiframe structure

In this article we only consider the FCCH burst as necessary for the synchronisation procedure since the SCH burst follows exactly one frame after the FCCH. Nevertheless, for a parallel tracking of FCCH and SCH bursts the SCH detection has the same TDD timeslot requirements, since the SCH and the FCCH burst have the same width. Furthermore, we assume that the UE has no knowledge available about the relative timing of the TDD cell and the neighbouring GSM cells and that a detection is only successful when a complete FCCH burst is captured.
The GSM 51-multiframe is repeated all the time and it is the task of the UE (dual or more mode terminal) to detect one of the GSM FCCH bursts. For that purpose the UE can use the idle TDD slots. That means those slots of the 16 slots of a TDD frame (=10ms) which are neither used for uplink nor for downlink transmissions.
In these idle periods the synthesizer of the UE receiver has to switch from the TDD frequency band to the GSM frequency band which should be monitored (and after the monitoring vice versa).
In the simulations published up to now this synthesizer switching time t_{synth} varies from 0ms (for UEs with two synthesizers) over 0.5ms (most popular value for single synthesizer UEs) up to 0.8ms for low cost single synthesizer UEs. (The actual value depends on frequency interval over which the synthesizer switch has to be carried out)
Before we enter the discussion of simulation results it is worth to consider the following analytical approach:

The time difference between two FCCH bursts is either 10 GSM frames or 11 GSM frames (frame 40 to frame 0 of the next GSM multiframe).

Error! Bookmark not defined.

(1)

Error! Bookmark not defined.

(2)

At first, express these time periods in multiples of TDD frames, see equations (1) and (2). Now consider one TDD frame as a circle of 10ms circumference. Assuming an arbitrary timing between the TDD and the GSM system we can choose an arbitrary point on the TDD circle from which we begin winding the GSM multiframe around the TDD circle.
As illustrated in figure 2, independent from the starting point we will always get 13 FCCH burst positions around the TDD circle. This is obvious from equations (1) and (2) because apart from the multiples of TDD frames (4 for the 10 GSM frame step and 5 for the 11 GSM frame step) we have always an offset of 8/13 or 1/13 of a TDD frame.
Different alignments of the GSM multiframe and the TDD frame can be taken into account if you turn the TDD circle against the FCCH burst circle.

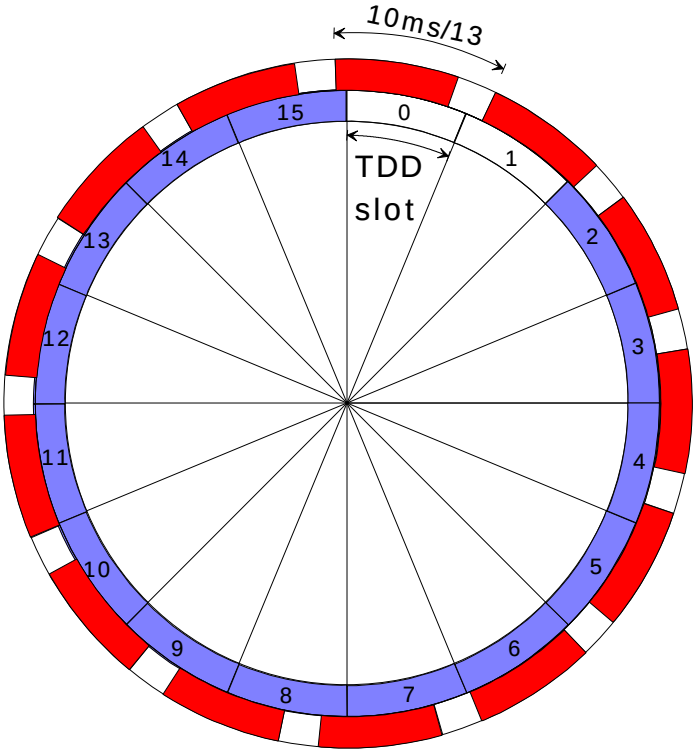

figure 2 Example for a TDD to GSM alignment where only 2 idle TDD slots for monitoring (slot 0 and 1) are not sufficient to detect a complete FCCH burst (dark periods on the outer circle)

In figure 2 it is also shown that with only two idle TDD slots per frame (here slot 0 and 1) there are alignments where no complete FCCH burst falls in the idle period (the synthesizer switching is neglected here, as it is done in the specification S1.25). What does that mean in practice? In reality that has the consequence that a UE which is not properly aligned with the GSM system will infinitely try to find a complete FCCH burst on these 2 slots.

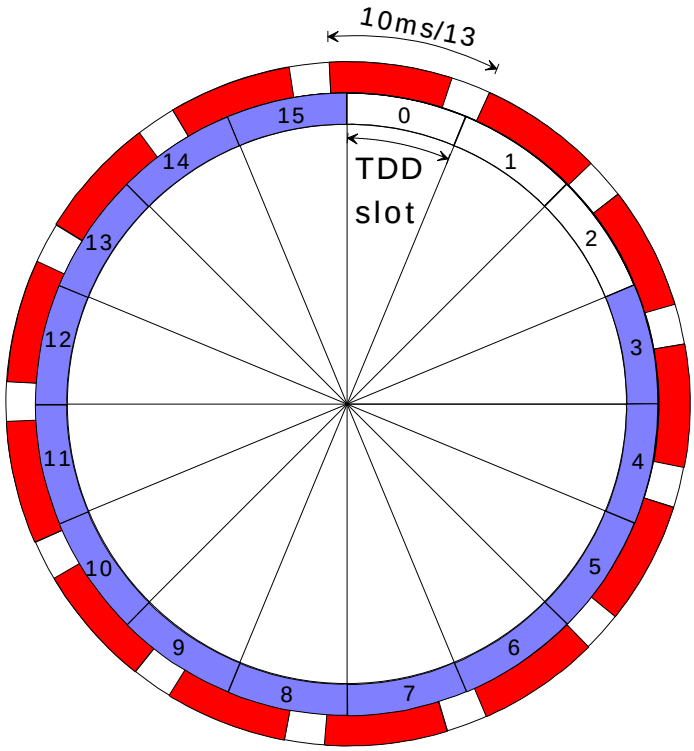

figure 3 Example for a TDDtoGSM alignment with 3 idle TDD timeslots (slot 0, 1, 2) which can be used for monitoring GSM

In contrast to that, figure 3 explains that with 3 consecutive idle TDD slots a dual synthesizer UE will always detect a complete FCCH burst, whatever the alignment between TDD and GSM may be.
In general, the minimum period which must be covered by consecutive idle slots to guarantee the FCCH (or alternatively SCH) detection for all alignments can be formulated by equation (3). (This consideration assumes that the monitoring period is for all TDD frames at the same position. With this assumption the rule can also be applied to FDD).

$$t_{\min,\ guaranteed} = 2 \times t_{synth} + t_{FCCH} + \frac{10\text{ms}}{13} = 2 \times t_{synth} + \frac{35\text{ms}}{26} \qquad (3)$$

Now to the question of the maximum synchronisation time, i. e. the maximum time to capture one FCCH burst. Here it is useful to consider the sequence in which the 13 possible FCCH positions are addressed. Let us assume we start with FCCH burst position 0 (you can choose an arbitrary position for that, since only relative aspects are important here) with the first FCCH burst in a GSM multiframe. The next burst will be 4 TDD frames and 8/13 TDD frames later which we call FCCH position 8. The next but one FCCH burst will also have an offset of 8/13 and due to the modulo 13 consideration we call that position 3 (instead of 16). You can continue in that way for 19 GSM multiframes and you will get table 1.
From this table you can find two important points:
On the one hand, the whole sequence of FCCH positions repeats after 13 multiframes (=3060ms). Therefore this is one upper limit for the maximum synchronisation time.
On the other hand, it is obvious that whereever you start with the first FCCH burst position, after a maximum of 14 FCCH bursts all 13 FCCH positions will be touched. That means for the worst case, adding 11 times a 10

GSM frame period and 3 times an 11 GSM frame period, you will get 660ms for the maximum synchronisation time.
That has to say, if you monitor GSM every TDD frame (or analogous every FDD frame) with a constant arrangement of idle periods you will detect the FCCH burst before 660ms or you will **NEVER** detect it.
(Therefore the specification should be updated to prevent misunderstandings!)
Greater maximums are only possible if monitor only every nth TDD frame or if you change the idle period arrangement.

table 1 Numbering of FCCH bursts on the TDD frame circle depending on time

Concerning dynamic changes of the idle period arrangement it should be noticed that they always increase the maximum synchronisation time in comparison to the 660ms limit. Their possible advantage is to achieve comparable average synchronisation times with less or smaller idle periods.
Nevertheless, one should be aware that at the end of such a dynamic change there must be a method which guarantees FCCH detection, otherwise the worst case of an UE which is not able to hand over can not be excluded.

2. Simulation Results

In the next 4 tables the simulation results are depicted to detect a complete FCCH burst of GSM using an allocation of busy slots which is constant for all the TDD frames (a parallel SCH search is not considered in these simulations). Busy means that the slot can be an uplink or a downlink slot. For each number of busy slots N there are 16!/((16-N)!*N!) possible cases of TDD slot allocations. For each case 1000 possible start positions of the TDD frame in the GSM 51-multiframe are considered, so that in regard of that stepsize almost all alignments of the TDD and the GSM frame structure are included. If only one or more of these 1000 alignments does not allow

a detection of a complete FCCH then this case is considered as ‚not successful' and all alignments of this case are excluded from the averaging process and the maximum determination.

The simulation results confirm the explainations made before: For a dual synthesizer approach 3 consecutive idle TDD timeslots are necessary to guarantee FCCH detection. For a single synthesizer approach with a synthesizer switching time of 0.3 or 0.5ms 4 timeslots are necessary. For a low cost UE with 0.8ms 5 timeslots are necessary.

busy slots	cases	not successful cases	FCCH detection time in ms	
			average	maximum
2	120	0	36.85	189.17
3	560	0	45.53	327.59
4	1820	0	56.21	419.41
5	4368	0	69.68	567.63
6	8008	0	87.01	658.78
7	11440	16	109.55	659.96
8	12870	226	137.83	659.96
9	11440	1104	168.78	659.96
10	8008	2432	195.37	659.96
11	4368	2608	214.77	659.96
12	1820	1540	226.78	659.96
13	560	544	228.68	659.96
14	120	120	-	-
15	16	16	-	-

table 2 Simulation results for monitoring GSM from TDD with a synthesizer switching time of 0ms (dual synthesizer)

busy slots	cases	not successful cases	FCCH detection time in ms	
			average	maximum
2	120	0	44.79	189.17
3	560	0	60.51	470.45
4	1820	0	82.24	562.74
5	4368	16	112.52	659.90
6	8008	600	144.92	659.96
7	11440	3040	170.71	659.96
8	12870	6646	189.16	659.96
9	11440	8432	201.92	659.96
10	8008	7072	211.02	659.90
11	4368	4192	218.26	659.72
12	1820	1804	224.66	659.72
13	560	560	-	-
14	120	120	-	-
15	16	16	-	-

table 3 Simulation results for monitoring GSM from TDD with a synthesizer switching time of 300ms

busy slots	cases	not successful cases	FCCH detection time in ms	
			average	maximum
2	120	0	50.36	189.17
3	560	0	72.82	470.69

4	1820	0	106.74	659.96
5	4368	208	148.01	659.96
6	8008	1456	186.18	659.96
7	11440	4384	216.56	659.96
8	12870	7646	239.68	659.96
9	11440	8800	256.94	659.96
10	8008	7128	269.81	659.96
11	4368	4192	279.85	659.96
12	1820	1804	288.91	659.96
13	560	560	-	-
14	120	120	-	-
15	16	16	-	-

table 4 Simulation results for monitoring GSM from TDD with a synthesizer switching time of 500ms

busy slots	cases	not successful cases	FCCH detection time in ms	
			average	maximum
2	120	0	59.98	235.34
3	560	0	100.43	659.96
4	1820	140	148.71	659.96
5	4368	1168	187.57	659.96
6	8008	4016	215.88	659.96
7	11440	8080	236.33	659.96
8	12870	10950	251.67	659.96
9	11440	10720	264.13	659.96
10	8008	7848	275.12	659.96
11	4368	4352	284.90	659.96
12	1820	1820	-	-
13	560	560	-	-
14	120	120	-	-
15	16	16	-	-

table 5 Simulation results for monitoring GSM from TDD with a synthesizer switching time of 800ms

3. Proposal for Modification of S1.25 respectively S1.31

6.1.5.3 High data rate traffic.

~~6.1.5.3.1 High-end dual synthesisers terminals~~

In case of high data traffic using a dual synthesizer UE, a monitoring period of at least ~~two~~ three TDD timeslots is ~~desirable~~ necessary to guarantee a detection of the FCCH burst of GSM (same is valid for detecting only the SCH, since it has also a length of one GSM timeslot) as shown by the simulation results appearing on the table 2 below.

busy slots= 16-idle slots	cases	FCCH detection time in ms	
		Average	maximum
2	120	36.85	189.17
3	560	45.53	327.59
4	1820	56.21	419.41
5	4368	69.68	567.63
6	8008	87.01	658.78
7	11440	109.55	659.96
8	12870	137.83	659.96

9	11440	168.78	659.96
10	8008	195.37	659.96
11	4368	214.77	659.96
12	1820	226.78	659.96
13	560	228.68	659.96
14	120	-	-
15	16	-	-

~~Number of consecutive TS per frame available for monitoring~~	~~Average synchronisation time (s)~~	~~Maximum synchronisation time (s)~~
~~3~~	~~0,23~~	~~0,65~~
~~2~~	~~0,4~~	~~1,9~~
~~1~~	~~7,2~~	~~23,2~~

Table 2: FCCH detection time avering over arbitrary alignments between the TDD and the GSM frame structure considering a dual synthesizer UE and all possible cases of slot allocations

~~**synchronisation time for a monitoring period of one, two or three consecutive time slot per frame.**~~

For single synthesizer UEs the synthesizer switching time t_{synth} from the TDD band to the GSM band and vice versa have to be taken into account. The minimum time for a guaranteed FCCH detection can be calculated as follows (t_{FCCH} = one GSM slot):

Error! Bookmark not defined.

(e.g for t_{synth} =0,3ms: 4 TDD consecutive idle timeslots needed, for t_{synth} =0,5ms: 4 slots, for t_{synth} =0,8ms: 5 slots)
For detecting SCH instead of FCCH (for a parallel search) the same equation applies.
~~The number of consecutive Time Slots needed to obtain an effective monitoring period of two Time Slots depends on the synthesiser characteristics that can be better for the high-end high-date-rate capable terminal than for the low cost terminal considered in section 9.2.2.2. The switching time could for instance be considered as being one or one half of a TS for one-way, resulting in the effective monitoring period indicated in the table 3 below.~~
For even better performance, a dual synthesiser terminal could be considered: this would allow a negligible switching time between UMTS and GSM frequencies. When the first synthesiser is used, the frequency jump for monitoring is performed by the second synthesiser.

One-way switching time for the synthesiser	Number of free consecutive TSs needed in the frame for a~~n~~ guaranteed FCCH detection ~~effective monitoring period of 2 TSs~~
1 TS (= 625µs)	5 ~~4~~
0.5 TS (=312µs)	4 ~~3~~
0 (dual synthesiser)	3 ~~2~~

Table3: link between the synthesiser performance and the number of free consecutive TSs for a guaranteed FCCH detection ~~a monitoring period of two TSs,~~ needed for GSM monitoring.