**3GPP TSG-RAN WG4 Meeting #96-e R4-200xxxx**

**Electronic Meeting, 17th –28th Aug., 2020**

**Agenda item: 7.13.1.3, 7.13.1.4**

**Source:** Intel Corporation

**Title:** [96e][221] NR\_RRM\_Enh\_RRM\_Part\_1

**Document for:** Information

# Introduction

The email discussion is intended to cover topics in AI 7.13.1.3 (BWP switching on multiple CCs), 7.13.1.4 (UL spatial relation info switching).

In last meeting, there is agreed WF in R4-2008675 for BWP switching on multiple CCs which are as follows:

**Delay requirements for DCI/timer based BWP switch**

*;* N: Number of CCs with simultaneous BWP switch; K is number of CCs that can be processed simultaneously; D is incremental delay for BWP switch processing on additional CCs

Value of D:

* + Define new UE capabilities for BWP switching on multiple CCs
  + Type 1: D = 100us, 200us
  + Type 2: D = 400us, 800us, 1000us
  + Same capabilities apply for FR1 and FR2

Definition of N :

* + Option 1: N is the number of CCs with simultaneous BWP switch.
  + Option 2: For DCI and timer-based BWP switch on multiple CCs, for UE which is capable of per-FR gap, and no BWP switch involves SCS change, N is the number of simultaneous BWP switching on CCs within the same frequency range; For UE which is not capable of per-FR gap, N is the number of simultaneous BWP switching on both FR

**Delay requirements for RRC based BWP switch**

;

Where DRRC is FFS.

* Option 1: DRRC = 0ms
* Option 2: DRRC = D (agreed value for DCI/timer based BWP switch)

Option 3: if N<=3, re-use the existing requirement. if N>3, DRRC =D. where N is the total number of CCs.

**when SCS changes**

* The simultaneous BWP switch on multiple CCs case, if the BWP switch on multiple CCs results in the change of the SCS on any CC among involved CCs, TBWPswitchDelay should be based on the smallest SCS among all SCS values of all involved CCs.

**Conditions when requirements for partial overlap BWP switch are defined**

* + DCI and RRC based BWP switch with partial overlap are defined for FR1+FR2 in NR-DC operation, when BWP switch doesn’t involve SCS change and UE supports per-FR gap.

**Delay requirements for Timer based BWP switch**

**Sub1:** if UE is capable of per-FR gap and the timer based BWP switch happens in two frequency range, whether UE handled timer-based BWP switch in parallel or sequentially

* Option 1: in parallel
* Option 2: sequentially

**Sub2:** Delay requirement for timer based BWP switch

* Option 1: Don’t differentiate UE capability of per-FR gap
* Option 2: Dependent on the UE capability of per-FR gap

**Delay requirements for RRC based BWP switch**

**Sub1:** Whether RRC processing time is equal to BWP switch time in RAN2 (In case the RRC procedure triggers BWP switching, the RRC procedure delay is the value defined in the following table (Table 12.1-1 in TS 38.331) plus the BWP switching delay defined in TS 38.133 [14], clause 8.6.3.)

* Option 1: Yes
* Option 2: No

**Sub2:** Delay requirement for RRC based BWP switch

* Option 1:upper bounded by the multiple BWP switch time in CG1.
* Option 2:upper bounded by the RRC processing time in the 1st CG.
* Option 3:No need to introduce the waiting time for RRC based partial overlap BWP switching on multiple CCs, and the delay requirements for simultaneous BWP switch on multiple CCs shall be reused

# Topic #1: BWP Switching on multiple CCs

## Companies’ contributions summary

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| **T-doc number** | **Company** | **Proposals / Observations** |
| [R4-2009607](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_95_e/Docs/R4-2006203.zip) | Apple | For simultaneous triggering  **Proposal #1: Define N as the number of CCs with simultaneous BWP switch**  **Proposal #2: Define DRRC = D for RRC based simultaneous BWP switch.**  For partial overlap triggering  **Proposal #3: Define requirements based on sequential processing for overlapped timer based switch for all cases and do not differentiate between UE capability of per-FR gap.**  **Proposal #4: Define timer based partial overlap BWP switch as TBWPSwitchDelayPartialOverlapTimer = TDelayTimer + TBWPSwitchDelayTimer**  **Proposal #5: The delay on processing 2nd BWP switch is upper bounded by the multiple BWP switch delay on CG1**  **Proposal #6: Define RRC based partial overlap delay as TBWPSwitchDelayPartialOverlapRRC = TDelayRRC + TBWPSwitchDelayRRC’** |
| [R4-2009745](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2009745.zip) | Intel | ***Proposal 1: For delay requirement for DCI/timer based BWP switch, the definition of N is as follows:***   * + ***for UE which is capable of per-FR gap, and no BWP switch involves SCS change, N is the number of simultaneous BWP switching on CCs within the same frequency range; For UE which is not capable of per-FR gap, N is the number of simultaneous BWP switching on both FR.***   ***Proposal 2: For RRC based multiple BWP switch, if N<=3, DRRC =0. if N>3, DRRC =D. where N is the total number of CCs.***  ***Proposal 3: For timer based partially overlapped multiple BWP switch, if UE is capable of per-FR gap and the BWP switch happens in two frequency ranges where no SCS changes, UE handles timer-based BWP switch in parallel.***  ***Proposal 4: If UE is not capable of per-FR gap or BWP switch involves SCS change,*** ***the timer based partially overlapped delay time is:***  **TBWPSwitchDelayPartialOverlapTimer = TDelay + TBWPSwitchDelayTimer**  ***where TDelay is the time delayed by ongoing BWP switching on single or simultaneously triggered multiple CCs. TBWPSwitchDelayTimer is the timer-based BWP switch delay on the later-coming*** ***single CC or simultaneously triggered multiple CCs. The TDelay is upper bounded by the ongoing BWP switching time on single or simultaneously triggered multiple CCs.***  ***Proposal 5: For RRC based partial overlap triggered BWP switching, the delay time is upper bounded by the multiple BWP switch delay in the first CG.*** |
| [R4-2009769](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2009769.zip) | Xiaomi Technology | **Proposal 1: For DCI and timer-based BWP switch on multiple CCs, for UE which is capable of per-FR gap, and no BWP switch involves SCS change, N is the number of simultaneous BWP switching on CCs within the same frequency range; For UE which is not capable of per-FR gap, N is the number of simultaneous BWP switching on both FR.**  **Proposal 2: The extended delay for RRC based BWP switch (DRRC) shall be the same as that for DCI/timer based BWP switch.**  **Proposal 3: If UE is capable of per-FR gap and the timer based BWP switching happens in two frequency range, the UE is assumed to change timer-based BWP switch in sequentially.**  **Proposal 4: the delay requirement for partial overlap timer based BWP switching is defined as TBWPSwitchDelayPartialOverlapTimer = TDelay + TBWPSwitchDelayTimer ,**  **Where TDelay is the time delayed by ongoing BWP switching on other single or multiple CCs, which can be N\* TBWPSwitchDelayTimer (N is the number of ongoing BWP switch on CCs);**  **TBWPSwitchDelayTimer is the timer-based BWP switch delay on current single CC or multiple CCs.**  **Proposal 5: RRC processing time is equal to BWP switch time in RAN2 (In case the RRC procedure triggers BWP switching, the RRC procedure delay is the value defined in the following table (Table 12.1-1 in TS 38.331) plus the BWP switching delay defined in TS 38.133 [14], clause 8.6.3.)**  **Proposal 6: For the delay requirement for partial overlap RRC based BWP switching, the upper bounded by the multiple BWP switch time in CG1 shall be considered.** |
| [R4-2009980](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2009980.zip) | Qualcomm | **Observation 1:** For a UE that supports per FR gap, BWP switch in one FR does not impact the timeline of BWP switching in the other FR.  **Observation 2:** The agreement of the last meeting did not focus on the scenario of per-FR gap capable UEs where BWP switch involves SCS change.   * According to 38.133, UE can cause interruption of up to X slots to other active serving cells in both FR if any BWP switch involves SCS change.   **Observation 3:** If UE requires very close to 16 ms to switch one single BWP based on RRC command, option 1 and option 3 will simply not work for the UE because it will obviously need additional time to switch additional number of BWPs based on the RRC command.  **Observation 4:** RAN2 spec clearly shows that the RRC procedure delay that is triggered by BWP switch is equal to the total BWP switch delay.  **Observation 5:** Current text regarding the timeline of DCI/timer based simultaneous BWP switch does not clarify the value of TBWPSwitchDelay where BWP change does not change SCS on any CC but the SCSes are different among CCs.  **Proposal 1:** RAN4 supports option 2 regarding the definition of N in DCI/timer based simultaneous BWP switch.   * For DCI and timer-based BWP switch on multiple CCs, for UE which is capable of per-FR gap, and no BWP switch involves SCS change, N is the number of simultaneous BWP switching on CCs within the same frequency range; * For DCI and timer-based BWP switch on multiple CCs, for UE which is capable of per-FR gap, and any BWP switch involves SCS change, N is the number of simultaneous BWP switching on both FR. * For UE which is not capable of per-FR gap, N is the number of simultaneous BWP switching on both FR.   **Proposal 2:** RAN4 supports option 2 regarding the delay for RRC based simultaneous BWP switch.   * ;   + Where DRRC = D (agreed value for DCI/timer-based BWP switch).   **Proposal 3:** If UE is capable of per-FR gap and the timer-based BWP switch happens in two frequency range, UE handles timer-based BWP switch in parallel across two frequency ranges.  **Proposal 4:** The delay requirements for timer-based BWP switch with partial overlap are dependent on the UE capability of per-FR gap.   * For UE capable of per-FR gap:   + TBWPSwitchDelayPartialOverlapTimer = TDelay + TBWPSwitchDelayTimer , where TDelay is the time delayed by ongoing BWP switching on other single or simultaneously triggered multiple CCs within the same frequency range. TBWPSwitchDelayTimer is the timer-based BWP switch delay on current single CC or simultaneously triggered multiple CCs. * For UE not capable of per-FR gap:   + TBWPSwitchDelayPartialOverlapTimer = TDelay + TBWPSwitchDelayTimer , where TDelay is the time delayed by ongoing BWP switching on other single or simultaneously triggered multiple CCs across all frequency ranges. TBWPSwitchDelayTimer is the timer-based BWP switch delay on current single CC or simultaneously triggered multiple CCs.   **Proposal 5:** Delay requirement for RRC based BWP switch is upper bounded by the multiple BWP switch time in CG1; where multiple BWP switch time is simply equal to the summation of each individual BWP switch time in CG1.  **Proposal 6:** The value of TBWPSwitchDelay should be based on the smallest SCS among all SCS values of all involved CCs even where BWP change does not change SCS on any CC.   * RAN4 supports the following TP. |
| [R4-2010042](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2010042.zip) | MediaTek inc. | ***Proposal 1: Send LS to RAN1 to clarify whether currently RAN4’s agreement for multiple BWP switch is applied for HARQ processing timeline design in dormancy SCell.***   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 1. **Overall Description:**   RAN4 had defined the DCI-based simultaneous multiple BWP switch delay as follow.  *;* N: Number of CCs with simultaneous BWP switch; D is incremental delay for BWP switch processing on additional CCs.   * Value of D:   + Define new UE capabilities for BWP switching on multiple CCs   + Type 1: D = 100us, 200us   + Type 2: D = 400us, 800us, 1000us   + Same capabilities apply for FR1 and FR2   The overall activation delay for dormancy SCell(N=7) based on RAN4’s agreements is shown as the table below.   |  |  |  |  | | --- | --- | --- | --- | | **SCS(KHz)** | **Single BWP switch delay(ms)** | **Multiple BWP extension D for Type2 UE(ms)** | **Multiple dormancy SCell activation delay(N=7) (ms)** | | 15 | 3 | 0.4 | 5.4 | | 0.8 | 7.8 | | 1 | 9 | | 30 | 2.5 | 0.4 | 4.9 | | 0.8 | 7.3 | | 1 | 8.5 | | 60 | 2.25 | 0.4 | 4.65 | | 0.8 | 7.05 | | 1 | 8.25 | | 120 | 2.25 | 0.4 | 4.65 | | 0.8 | 7.05 | | 1 | 8.25 |   **2. Actions:**  **To RAN1.**  **ACTION:** RAN4 kindly asks RAN1 whether current RAN4’s agreement on multiple BWP switch will be applied for HARQ processing timeline in dormancy SCell’s design. |   ***Proposal 2: Add additional D=200us for type 2 UE in simultaneous DCI-based BWP switching.***  ***Proposal 3: N is the number of simultaneous BWP switching CCs within the same FR for the UE supporting per-FR gap.***  ***Proposal 4: For simultaneous RRC-based BWP switch, the agreed D for DCI/timer based BWP switch can be reused with additional D=200us for type 2 UE.***  ***Proposal 5: UE should be allowed to conduct the BWP switch sequentially for non-simultaneous timer-based BWP switch in NR-DC whatever UE supports per-FR gap.***  ***Proposal 6: The total RRC processing time equals RRC procedure delay plus BWP switch time.***  ***Proposal 7: Delay requirement for non-simultaneous RRC based BWP switch is upper bounded by the multiple BWP switch delay of the 1st CG.*** |
| [R4-2010361](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2010361.zip) | vivo | **Proposal 1: Use option 2 DRRC = D for simultaneously RRC based BWP switch.**  **Proposal 2: An upper bound Nbound on N could be defined and the total switch delay will not further increase when N is larger than Nbound.**  **Proposal 3: For issue 1, option 2 is preferred, i.e., UE handled timer-based BWP switch sequentially. For issue 2, option 1 should be selected if option 2 is used for issue 1, i.e., delay requirement is not differentiated when a UE is per-FR gap capable or not.**  **Proposal 4: Use option 1 for both issue 1 and issue 2.** |
| [R4-2010668](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2010668.zip) | Ericsson | The following proposals are made regarding simultaneously triggered BWP switching:  **Proposal 1:** For simultaneously triggered DCI or timer-based BWP switching of multiple carriers, and under the condition that neither of the BWP switchings entails a change in SCS, the value of N is determined per frequency range for UE with per-FR gap capability, and as summation over all frequency ranges for UE with per-UE gap capability. This corresponds to Option 2 in the WF.  **Proposal 2:** For simultaneously triggered RRC-based BWP switching on multiple CCs, the incremental time for switching of each additional CC is DRRC for switching on N≤3 CCs, otherwise DRRC = D as reported by UE for DCI and timer-based BWP switching. This corresponds to Option 3 in the WF.  The following proposals are made regarding partially overlapping BWP switching:  **Proposal 3:** Timer-based BWP switch on all CCs including across the two CGs are performed sequentially.  **Proposal 4:** Define one set of requirements for timer-based BWP switch on multiple CCs regardless of whether the UE supports per FR measurement gaps or not.  **Proposal 5:** The partially overlap timer-based BWP switch delay (TMultipleBWPSwitchDelayTimer) for a CC (CC1) can be expressed as follows:  TMultipleBWPSwitchDelayTimer = (1+M)\*TBWPSwitchDelayTimer  where:   * M=0 when the timer-based BWP switch is triggered on CC1, no timer-based BWP switch is ongoing on any other CC. * M> 0 if the timer-based BWP switch is triggered on CC1 and a timer-based BWP switch is ongoing on another CC (CC2). * (M-1) is the number of CCs on which the timer-based BWP switch is triggered before the triggering of the timer-based BWP switch on CC1 but while the timer-based BWP is ongoing on CC2.   **Proposal 6:** The RRC processing time for RRC-based BWP switch includes RRC procedure delay in Table 12.1-1, 38.331 and RRC based BWP switching delay in section 8.6.3, 38.133.  **Proposal 7:** Delay requirement for RRC based BWP switch for CG2 is upper bounded by the multiple BWP switch time in CG1. |
| [R4-2010711](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2010711.zip) | OPPO | **Proposal 1: For UE which is capable of per-FR gap, N is the number of simultaneous BWP switching on CCs within the same frequency range. Otherwise N is the number of simultaneous BWP switching on both FR(s).**  **Proposal 2: Support option 2, DRRC = D as agreed for DCI/timer based BWP switch.**  **Proposal 3: Consider sequential processing of timer-based BWP switch with partial overlap regardless of UE capable of per-FR gap.**  **Proposal 4: Define waiting time for RRC-based partial overlap BWP switch, which is upper bounded by the RRC processing time in the 1st CG.** |
| [R4-2010759](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2010759.zip) | NEC | **Proposal 1: When DCI and timer based BWP switch do not involves SCS change, definition of N for DCI and timer-based BWP switch on multiple CCs:**   * **For UE which is capable of per-FR gap: N is the number of simultaneous BWP switching on CCs within the same frequency range;** * **For UE which is not capable of per-FR gap: N is the number of simultaneous BWP switching on both FR**   **Proposal 2: RRC based BWP switch delay on multiple CC with simultaneous trigger is given by  where DRRC=0;**  **Proposal 3a: RAN4 to agree that UE process timer based BWP sequentially irrespective of per-FR capability of UE.**  **Proposal 3b: Delay requirement for timer based partially overlapped triggering is given by TBWPSwitchDelayPartialOverlapTimer = TDelay + TBWPSwitchDelayTimer; Where,**   * **TDelay is the time delayed by ongoing BWP switching on other single or simultaneously triggered multiple CCs within the same frequency range.** * **TBWPSwitchDelayTimer is the timer-based BWP switch delay on current single CC or simultaneously triggered multiple CCs.**   **Proposal 4: RAN4 to agree that wait time for RRC based non-simultaneous BWP switchshould be upper bounded by RRC processing time in 1st CG.** |
| [R4-2011070](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2011070.zip) | Huawei, Hisilicon | **Observation 1: There is no impact between FRs when the UE is capable of per-FR gap and the BWP switch does not involve SCS changes.**  **Proposal 1: For UE which is capable of per-FR gap, and no BWP switch involves SCS change, N is the number of simultaneous BWP switching on CCs within the same frequency range; For UE which is not capable of per-FR gap, or the BWP switches on multiple CCs involves SCS changing, N is the number of simultaneous BWP switching on both FR.**  **Proposal 2: TBWPswitchDelay shall also be based on the smallest SCS among all SCS values of all involved CCs regardless of SCS changes.**  **Proposal 3: For RRC-based simultaneous BWP switching on multiple CCs, the delay shall be same as single CC (𝑇𝑅𝑅𝐶𝑝𝑟𝑜𝑐𝑒𝑠𝑠𝑖𝑛𝑔+𝑇𝐵𝑊𝑃𝑠𝑤𝑖𝑡𝑐ℎ𝐷𝑒𝑙𝑎) without extension.**  **Observation 2: If UE is capable of per-FR gap, the timer based BWP switch happens in two frequency range are performed in parallel if the BWP switch doesn’t involve SCS change.**  **Observation 3: Delaying the timer-based BWP switch for BWP switch on both FRs is not consist with RAN1’s spec.**  **Proposal 4: Timer-based partial overlapping BWP switch requirements are defined when BWP switch does not involve SCS changing.**  **Proposal 5:**  **For UE capable of per-FR gap:**  **TMultipleBWPswitchDelayTotal = TDelay + TMultipleBWPswitchDelay , where TDelay is the time delayed by ongoing BWP switching on other single or simultaneously triggered multiple CCs within the same frequency range. TMultipleBWPswitchDelay is the timer-based BWP switch delay on current single CC or simultaneously triggered on multiple CCs.**  **For UE not capable of per-FR gap:**  **TMultipleBWPswitchDelayTotal = TDelay + TMultipleBWPswitchDelay*,* where *TDelay*is the time delayed by ongoing timer-based BWP switching with in the same frequency range; TMultipleBWPswitchDelayis TBWPSwitchDelay*+* D(N-1), N is the number of timer-based BWP switch on CCs in the other FR of which the time periods of BWP switching delay are overlapped with TMultipleBWPswitchDelay, and D is the incremental delay, which is same as that of simultaneous BWP switch on multiple CCs**  **Observation 4: The intention to introduce the waiting time raised from the description in RAN2’s spec to guarantee that UE could process the RRC messages in order.**  **Observation 5: Under the limited conditions (FR1+FR2 NR-DC without SCS changes and UE is capable of per-FR gap), option 1 means the RRC message processing in one CG has to be delayed until UE is ready for UL grant reception in the other CG, which is not reasonable.**  **Observation 6: if we use the RRC procedure delay defined in clause 12 to interpret the description at the beginning of clause 5, it means UE shall not decode the second RRC message when the 1st one has been processed and the BWP switch is ongoing.**  **Proposal 6: The waiting time is upper bounded by the RRC processing time (10ms) in the 1st CG.**  **Observation 7: For the requirements for the BWP switch on a single CC, the cross carrier scheduling is not considered.**  **Observation 8: The cross carrier scheduling is not considered for BWP switch on multiple CCs.**  **Proposal 7: The cross carrier scheduled DCI-based BWP switch on single CC/multiple CCs shall be considered in Rel-16.**  **Proposal 8:**  **The requirements for BWP switch on multiple CCs in Rel-16 apply to following 2 cases: 1) the BWP switch on each CC is scheduled by a separate DCI which is received in the same CC; 2) All CCs involved in the simultaneous BWP switch on multiple CCs are scheduled by a single DCI.**  **Observation 9: The reference CC to define the starting and end point of cross carrier scheduled BWP switch shall be carefully considered.**  **Proposal: 9**  **Define the starting point of the cross carrier BWP switch as the slot of the scheduling CC where UE receives the DCI and TBWPSwitchDelay ­shall be determined by the smaller SCS of all involved CC.**  **Proposal 10:**  **For cross carrier scheduling, when the SCS of the scheduled CC is larger than or equal to that of the scheduling CC, one additional slot of the scheduled CC is allowed; when the SCS of the scheduling CC is larger than that of the scheduled CC, there is no need to introduce extra delay.** |
| [R4-2011428](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2011428.zip) | Nokia, Nokia Shanghai Bell | 1. DRRC = 0ms in the Delay requirement for RRC-based simultaneous BWP switch on multiple CCs. 2. Extra waiting time in the delay requirement for RRC-based partial overlap BWP switch on multiple CCs could be upper bounded by the RRC processing time defined in the 38.331. |

## Open issues summary and companies view’s collection

*Before e-Meeting, moderators shall summarize list of open issues, candidate options and possible WF (if applicable) based on companies’ contributions.*

### Sub-topic 1-1: Simultaneous BWP switch on multiple CCs

**Issue 1-1-1: Delay requirements for DCI/timer based BWP switch**

; N: Number of CCs with simultaneous BWP switch; D is incremental delay for BWP switch processing on additional CCs;

* Value of D:
  + Option 1(MediaTek): Add additional D=200us for type 2 UE in simultaneous DCI-based BWP switching
* FFS on definition of N.
  + Option 1(Apple): N is the number of CCs with simultaneous BWP switch.
  + Option 2(Intel, Xiaomi, Ericsson, OPPO, NEC, MediaTek): For DCI and timer-based BWP switch on multiple CCs, for UE which is capable of per-FR gap, and no BWP switch involves SCS change, N is the number of simultaneous BWP switching on CCs within the same frequency range; For UE which is not capable of per-FR gap, N is the number of simultaneous BWP switching on both FR
  + Option 2a(Huawei,):For UE which is capable of per-FR gap, and no BWP switch involves SCS change, N is the number of simultaneous BWP switching on CCs within the same frequency range; For UE which is not capable of per-FR gap, or the BWP switches on multiple CCs involves SCS changing, N is the number of simultaneous BWP switching on both FR.
  + Option 3 (Qualcomm)
    - Introduce a new UE feature (mentioned as 9-12 in RAN4 UE feature list parameter set).
    - For UEs that support this capability and no BWP involves SCS change, N is the number of simultaneous BWP switching on CCs within the same frequency range; For UEs that do not support this feature, or the BWP switches on multiple CCs involves SCS changing, N is the number of simultaneous BWP switching on both FR.
* Recommended WF:
  + Definition of N: For UE which is capable of per-FR gap, and no BWP switch involves SCS change, N is the number of simultaneous BWP switching on CCs within the same frequency range; For UE which is not capable of per-FR gap, or the BWP switches on multiple CCs involves SCS changing, N is the number of simultaneous BWP switching on both FR.

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| **Company** | **Comments** |
| Qualcomm | We are adding a new option (option 3) for this issue. We did not add it to the summary on Friday because this option was not part of our BWP switching contribution. However, we proposed it to UE feature list session..  We support option 3.  The per FR gap capability was originally intended to be used for L3 mobility measurements. But this proposal ties that feature to UE’s capability of performing BWP processing, in parallel, in two different FRs. The per FR gap feature should not be stretched to cover this parallel BWP processing capability in FR1 and FR2 and a new feature should be introduced.  Also, if BWP switching on any of the CCs involves SCS change, UE should be able to cause interruption to other FRs. And N would be the number of simultaneous BWP switching on both FR, in this case. |
| MTK | D:  Option 1.  When 7 dormancy SCells are activated simultaneously, the activation delay will be larger than HARQ scheduling limitation defined in RAN1 based on current agreed values for type 2 UE in FR2. Thus, it should add D=200ms to permit some type 2 UEs can activated max 7 dormancy SCells simultaneously.  N:  Option 2 and no requirement if BWP switch involves SCS changing.  In last meeting, it agreed only define requirement when BWP switch doesn’t involve SCS change for **DCI based BWP switch with partial overlap**. We suggest to apply the same rule in simultaneous DCI-based BWP switch.  For QC’s option 3, in R15, we had already defined BWP switch requirement based on per-FR gap capability. Thus, we think it’s natural to re-use the same concept in R16 multiple BWP switch. Actually, RAN4 nearly agreed all the scenarios based on per-FR gap capability in multiple BWP switch. It’s unnecessary to re-discuss all the scenarios with another UE’s capability. |
| vivo | For the value of N, support option 2 |
| Ericsson | For definition of N, support option 2a. “or the BWP switches on multiple CCs involves SCS changing” was missing in the WF and thus in our original proposal. |
| NEC | D: we are OK with option 1.  N: We support option 2. |
| OPPO | Agree with the recommended WF |
| Apple | Definition of N.  We cannot agree with the recommended WF. We prefer option 1 as UE support of per FR gap doesn’t ensure that UE can process BWP switch on different FR simultaneously. We are also fine with Option 3. Also, with option 2/2a, it is unclear what the delay equation will be when there are N1 CCs in FR1 and N2 CCs in FR2 and the suggested conditions are met.  To MTK: The reason to have the condition on DCI based partial overlap switch is to ensure that the DCI command on 2nd CC is received without being interrupted.  For D=200ms, we already have D=200 ms in Type 1, what is the reason for introducing it in Type 2? If UE is capable of incremental delay of 200ms, shouldn’t it declare Type 1? |
| Xiaomi | Definition of N:  Support option 2, and also fine with option 2a. |
| Huawei | For the definition of N, we support option 2a.  It RAN4’s common understanding that for UE which is capable of per-FR gap and without SCS changes, there is no impact between FR1 and FR2, which could be observed in the interruption requirements of BWP switch. The BWP switch on multiple CC in R16 is to enable faster BWP switch to improve the performance and decrease the latency. We cannot see the reason to revert the fundamental assumption from R15 and introduce unnecessary latency which is not needed.  Thus we share the similar views as MTK that there is no need to introduce a new capability. Also we think it is confusing to introduce this capability to indicate whether UE could perform BWP switch in parallel as it is mostly related to UE implementation. It is also complex for NW to combine this capability and the capability of D to figure out the actual BWP switching delay.  To Apple’s question. When there are N1 CCs in FR1 and N2 CCs in FR2, if there is no SCS changes on all involved CCs, the BWP switching delay for the CCs in FR1/FR2 will be calculated by N1/N2 respective. When there is SCS changes on any CC(s), the BWP switching delay will be calculated using the equation with N=N1+N2. |
| Nokia | Value of D: we are fine with option 1.  Definition of N: we are fine with option 2. |
| Huawei | Further comments:  To Qualcomm:  Some questions to the option 3 about the feature mentioned since we didn’t find the corresponding discussion about this capability in the R16 feature discussion.  Does it only related to the definition N in the DCI-based BWP switch?  Does it mean it could happen that a UE which is capable of performing BWP switch in different FRs in parallel but the interruption should be considered in both FR2 since the UE may not support per-FR gap? |
| Intel | Definition of N:  Support option 2. if UE is capable of per-FR gap and no SCS changing is involved, UE can process the DCI/timer based BWP switch on FR1 and FR2 independently. N is the number of simultaneous BWP switching on CCs within the same frequency range.  By the way, this issue has relationship with Issue 1-2-2. A unified behavior of UE for simultaneous DCI/timer based BWP switch and partial overlap DCI/timer based BWP switch is expected. For timer based partial overlap BWP switch in Issue 1-2-2, the delay requirement will be defined considering UE capability of per-FR gap as well. |

**Issue 1-1-2: Delay requirements for RRC based BWP switch**

; Where DRRC is FFS

extended delay for RRC based BWP switching on multiple CCs is needed.

* Where DRRC is FFS.
  + Option 1(NEC, Huawei, Nokia): DRRC = 0ms
  + Option 2 (Apple, Xiaomi, Qualcomm, Vivo, OPPO): DRRC = D
  + Option 2a(MediaTek): DRRC = D. For simultaneous RRC-based BWP switch, the agreed D for DCI/timer based BWP switch can be reused with additional D=200us for type 2 UE.
  + Option 3 (Intel, Ericsson): if N<=3, re-use the existing requirement. if N>3, DRRC =D. where N is the total number of CCs.
  + Option 4 (Vivo): An upper bound Nbound on N could be defined and the total switch delay will not further increase when N is larger than Nbound
* Recommended WF:
  + Further discussion

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| **Company** | **Comments** |
| Qualcomm | We support option 2.  Same incremental delay should be used for both DCI and RRC based simultaneous BWP switch. |
| MTK | Option 2a.  For RRC-based BWP switching, we agree to follow the same extension D values in DCI-based BWP switch but with additional D=200us. |
| vivo | Option 2. Option 4 could be considered if the total delay is quite long with the increase of N. |
| Ericsson | Our preferrence is Option 3. We can also consider Option 2 but think there is some margin in the RRC-based switching delay for single CC that can absorb the switching delay on a few carriers. We do however think that Option 1 might be a little too optimistic in how many can be absorbed. To us, Option 4 would imply that there is some unnecessary margin when switching is carried out on fewer than N\_bound carriers, so we do not immediately see the merit of that proposal. |
| NEC | Our preference is option 1. To make progress we can consider option 3 also. |
| OPPO | Prefer Option 2. |
| Apple | Option 2  The incremental processing delay for RRC based switch is the same as DCI/timer based. |
| Xiaomi | Support option 2, similar to DCI based simultaneous BWP switching, the incremental processing delay shall be defined for RRC based case. |
| Huawei | As analyzed in our paper, we should not enable the new feature by introducing a quite long delay for all CCs involved. To make progress considering the timeline, we agree that it may related to UE implementation. Thus we propose that for type 1 UE, DRRC = 0ms; For type 2 UE, DRRC = D. |
| Nokia | We support option 1. We have very relaxed requirement for UE to perform BWP switch which is 6ms in Rel-15 for single CC, this value is for the worst situation and also considered the impact of switching on multiple CCs. No extra delay is needed for simultaneous RRC-based BWP switch on multiple CCs. |
| Intel | support option 3. We can compromise to option 2 either. |

**Issue 1-1-3: whether send LS to RAN1 about whether multiple BWP switch can apply for HARQ design in dormancy SCell**

* Option 1(MediaTek): Send LS to RAN1 to clarify whether currently RAN4’s agreement for multiple BWP switch is applied for HARQ processing timeline design in dormancy SCell
* Recommended WF:
  + Further discussion

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| **Company** | **Comments** |
| Qualcomm | We agree with the principle of option 1. We also think that RAN4 should send a LS to RAN1 regarding the agreements related to simultaneous BWP switch. However, the LS does not have to be solely for HARQ design in dormancy SCell. RAN4 agreements may allow RAN1 to rethink about allowed gap between PDCCH and PDSCH. The LS can simply mention all relevant RAN4 agreements. RAN1 can decide these agreements will be applied.  Also, RAN4 should send the LS after finalizing the definition of N. |
| MTK | Option 1  Currently, RAN4 made an agreements for DCI-based BWP switch delay. And also RAN4 had a common understanding on dormancy SCell’s activation delay will re-use DCI-based BWP switch length.  As we mentioned before, when 7 dormancy SCells will be activated in FR2, the total delay will be larger than HARQ scheduling timeline.  But RAN1 already agreed the HARQ feedback time ‘*slotoffset*’ in DCI scheduling shall be larger than BWP switch delay in R15. Thus, we suggested RAN4 to notice RAN1 that we had agreed some larger delay values for multiple BWP switch to avoid the possible mismatch between RAN1 and RAN4.  Otherwise, when RAN1 finalizes their design in dormancy SCell and follows the same logic in R15 BWP switch, RAN4 will face the spec.’s contradiction. RAN4 had to re-open the discussion on this issue again. |
| vivo | We agree that a LS could be sent to RAN1 to inform RAN1 about possible issue. Agree with QC that such LS should be sent after finishing the discussion regarding N. |
| Ericsson | We are fine with Option 1 |
| OPPO | Similar view as QC’s |
| Apple | We support sending LS to RAN1, also agree with Qualcomm’s proposal to wait until definition of N is finalized. |
| Huawei | We share the similar views as Qualcomm. The extended DCI-based BWP switching delay on multiple CC will not only impact the HARQ timeline for dormancy SCell. It will also impact the PDSCH and PUSCH scheduling (k0 and k1) in multi-CC BWP switching. |
| Intel | Fine with option 1. Sending LS to RAN1 about the current RAN4 agreement about DCI-based BWP switch on multiple CCs after the definition of N is finalized. |

**Issue 1-1-4: TBWPSwitchDelay based on the smallest SCS**

* Option 1(Qualcom): The value of TBWPSwitchDelay should be based on the smallest SCS among all SCS values of all involved CCs even where BWP change does not change SCS on any CC
* Option 1a(Huawei):TBWPswitchDelay shall also be based on the smallest SCS among all SCS values of all involved CCs regardless of SCS changes.
* Recommended WF:
  + TBWPswitchDelay shall also be based on the smallest SCS among all SCS values of all involved CCs regardless of SCS changes.

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| **Company** | **Comments** |
| Qualcomm | We support the recommended WF. |
| MTK | Support recommended WF. |
| vivo | Support recommended WF. |
| Ericsson | We support the recommended WF. |
| OPPO | Support the recommended WF. |
| Apple | We support the recommended WF. |
| Xiaomi | Support the recommended WF. |
| Huawei | We support the recommended WF. |
| Nokia | We support the recommended WF. |
| Intel | We support the recommended WF. |

### Sub-topic 1-2: Partial overlap BWP switch on multiple CCs

*Sub-topic description : Requirements for partial overlap BWP switch on multiple CCs*

*Open issues and candidate options before e-meeting:*

**Issue 1-2-1: Condition when define requirement for timer based partial overlap BWP switch**

* Option 1 (Huawei): Timer-based partial overlapping BWP switch requirements are defined when BWP switch does not involve SCS changing.
* Recommended WF:
  + Further discussion

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| **Company** | **Comments** |
| Qualcomm | We agree with option 1. |
| MTK | We agree with option 1. |
| vivo | Ok with option 1. |
| Ericsson | We propose sequential approach regardless of whether UE is capable of per FR gap or not, hence we do not see the need for restriction according to Option 1. |
| Apple | We would like to simplify the requirements for timer based partial overlap switch requirements and define requirements based on sequential processing for all cases. Hence option1 need not be discussed in our opinion. But we are fine with not defining requirements for this case if that is majority view. |
| Xiaomi | OK with option 1 |
| Huawei | We agree with option 1. |
| Intel | we are fine with option 1. |

**Issue 1-2-2: Delay requirements for Timer based BWP switch**

**Sub1:** if UE is capable of per-FR gap and the timer based BWP switch happens in two frequency range, whether UE handled timer-based BWP switch in parallel or sequentially

* Option 1(Huawei, Intel, Qualcomm): If UE is capable of per-FR gap, the timer based BWP switch happens in two frequency range are performed in parallel if the BWP switch doesn’t involve SCS change.
* Option 2(Apple, Xiaomi, MediaTek, Vivo, Ericsson, OPPO, NEC): sequentially

**Sub2:** Delay requirement for timer based BWP switch

* Option 1(Vivo, Ericsson, Apple, Xiaomi, NEC): Don’t differentiate UE capability of per-FR gap

TBWPSwitchDelayPartialOverlapTimer = TDelayTimer + TBWPSwitchDelayTimer

* Option 1a (Ericsson):

TMultipleBWPSwitchDelayTimer = (1+M)\*TBWPSwitchDelayTimer

where:

* M=0 when the timer-based BWP switch is triggered on CC1, no timer-based BWP switch is ongoing on any other CC.
* M> 0 if the timer-based BWP switch is triggered on CC1 and a timer-based BWP switch is ongoing on another CC (CC2).

(M-1) is the number of CCs on which the timer-based BWP switch is triggered before the triggering of the timer-based BWP switch on CC1 but while the timer-based BWP is ongoing on CC2.

* Option 2: (Qualcomm, Intel, Huawei) Dependent on the UE capability of per-FR gap
* For UE capable of per-FR gap:
  + Option 2a (Qualcomm): TBWPSwitchDelayPartialOverlapTimer = TDelay + TBWPSwitchDelayTimer , where TDelay is the time delayed by ongoing BWP switching on other single or simultaneously triggered multiple CCs within the same frequency range. TBWPSwitchDelayTimer is the timer-based BWP switch delay on current single CC or simultaneously triggered multiple CCs.
  + Option 2b (Huawei): TMultipleBWPswitchDelayTotal = TDelay + TMultipleBWPswitchDelay, where TDelay is the time delayed by ongoing BWP switching within the same frequency range. TMultipleBWPswitchDelay is the timer-based BWP switch delay on current single CC or simultaneously triggered on multiple CCs.
* For UE not capable of per-FR gap:
  + Option 2a (Qualcomm): TBWPSwitchDelayPartialOverlapTimer = TDelay + TBWPSwitchDelayTimer , where TDelay is the time delayed by ongoing BWP switching on other single or simultaneously triggered multiple CCs across all frequency ranges. TBWPSwitchDelayTimer is the timer-based BWP switch delay on current single CC or simultaneously triggered multiple CCs.
  + Option 2b (Huawei): TMultipleBWPswitchDelayTotal = TDelay + TMultipleBWPswitchDelay*,* where *TDelay*is the time delayed by ongoing timer-based BWP switching with in the same frequency range; TMultipleBWPswitchDelayis TBWPSwitchDelay*+* D(N-1), N is the number of timer-based BWP switch on CCs in the other FR of which the time periods of BWP switching delay are overlapped with TMultipleBWPswitchDelay, and D is the incremental delay, which is same as that of simultaneous BWP switch on multiple CCs
* Recommended WF:
  + Further discussion

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| **Company** | **Comments** |
| Qualcomm | Sub 1: We are OK with option 2, i.e., sequential processing.  Sub 2: We are OK with option 1.The delay can be defined as:  TBWPSwitchDelayPartialOverlapTimer = TDelay + TBWPSwitchDelayTimer , where TDelay is the time delayed by ongoing BWP switching on other single or simultaneously triggered multiple CCs across all frequency ranges. TBWPSwitchDelayTimer is the timer-based BWP switch delay on current single CC or simultaneously triggered multiple CCs. |
| MTK | Sub 1 – option 2  Timer-based BWP switch is triggered when UE cannot detect any PDCCH for a certain period of time. It means UE is now in a very low traffic mode. Thus, it’s reasonable to follow RAN1’s design rule to allow UE to conduct the BWP switch sequentially also between FRs.  Sub 2 – option 1 |
| vivo | Sub 1: prefer option 2 for simplicity reason. Sub 2: support option 1 providing option 2 is used for sub 1. |
| Ericsson | Sub 1: Prefer Option 2. Sub 2: Prefer Option 1a. |
| NEC | Sub 1: OK with option 2; Sub 2: Prefer option 1 |
| OPPO | Sub 1: support option 2. Consider sequential processing of timer-based BWP switch with partial overlap regardless of UE capable of per-FR gap.  Sub 2:Prefer option 1. |
| Apple | Sub1: Option 2- Sequential processing irrespective of UE capability of per-FR gap in order to simplify requirements for this case  Sub 2: Option 1. This covers all cases without additional conditions on UE capability of per FR gap/ SCS change. |
| Xiaomi | Sub1: Option 2, allow UE to have more time to process BWP switch for this case from UE implementation point of view.  Sub2: prefer option 1. |
| Huawei | Sub 1- option1  Sub 2- option 2b  We agree with that timer-based BWP switch is triggered when UE is in low traffic load, and it may not as time-critical as DCI-based BWP switch. However, as we have defined the same delay requirement as DCI-based case for single CC, we support not to relax the requirement for multiple CCs. Also option 1 is not exactly aligned with RAN1’s spec which only allow UE to delay the timer-based BWP switch by ongoing BWP switch within the same FR. |
| Intel | Sub: Option 1.  Sub2: Option 2.  As explained in Issue 1-1-1, a unified UE behavior is expected for simultaneous BWP switch and partial overlap BWP switch. if UE is capable of per-FR gap and no SCS changing is involved, UE can process the timer based BWP switch on FR1 and FR2 independently. |

**Issue 1-2-3: Delay requirements for RRC based BWP switch**

**Sub1:** Whether RRC processing time is equal to BWP switch time in RAN2 (In case the RRC procedure triggers BWP switching, the RRC procedure delay is the value defined in the following table (Table 12.1-1 in TS 38.331) plus the BWP switching delay defined in TS 38.133 [14], clause 8.6.3.)

* Option 1(Xiaomi, Vivo): Yes
* Option 2(MediaTek, Ericsson, NEC): No.

**Sub2:** Additional waiting timefor RRC based BWP switch

* Option 1 (Apple, Intel, Xiaomi, MediaTek, Vivo, Ericsson): upper bounded by the multiple BWP switch time in CG1
* Option 2(OPPO, Nokia, NEC): upper bounded by the RRC processing time in the 1st CG.

Option 2a(Huawei): The waiting time is upper bounded by the RRC processing time (10ms) in the 1st CG

* Recommended WF:
  + Further discussion

**Issue 1-2-4: Delay requirements for RRC based BWP switch**

* Option 1(Apple): TBWPSwitchDelayPartialOverlapRRC = TDelayRRC + TBWPSwitchDelayRRC’
* Recommended WF:
* Further discussion.

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| **Company** | **Comments** |
| Qualcomm | Issue 1-2-3:  Sub 2: We support option 1.  RAN2 spec clearly shows that the RRC procedure delay, that is triggered by BWP switch, is equal to the total BWP switch delay. Hence, we support option 1. We think that option 1 should be further clarified to the following: “Delay requirement for RRC based BWP switch is upper bounded by the multiple BWP switch time in CG1; where multiple BWP switch time is simply equal to the summation of each individual BWP switch time in CG1.”  Issue 1-2-4:  The equation shown in option 1 is not very clear. The parameters need to be clarified and described, in details. Overall, the total delay of partially overlapped BWP switch should capture the clarified description that we mentioned above. |
| MTK | Sub 1.  In RAN2 spec, it clearly captured that RRC procedure delay = RRC reconfiguration time + BWP switching delay.  In RAN4, we agreed to define total BWP switch delay = RRC reconfiguration time + BWP switching delay.  Thus, RRC procedure delay in RAN2 = total BWP switch delay in RAN4.  Sub 2. – Option 1.  In RAN2, it clearly captured the RRC procedure shall be processed sequentially and the RRC procedure delay should include RRC reconfiguration time and BWP switch delay. |
| vivo | Sub 1: option 1; Sub 2: option 1; |
| Ericsson | Issue 1-2-3:  Sub1: Prefer Option 2  Sub2: Prefer Option 1 |
| NEC | Sub 1: Our view is option 2. RRC procedure delay for BWP switching is RRC message processing delay + RAN 4 defined BWP switch delay. That means RRC processing time is equal to RRC message processing delay.  Sub 2: Our view is Option 2.  Our understanding is for some scenarios there may not be any additional wait time is required and some scenarios may require additional wait time. However, if we further split up the scenarios, requirements may be complicated. Hence we are fine to define additional wait time.  Since RRC processing finishes in 10ms, UE can start process other RRC message immediately after 10ms. There is no need for UE to wait for BWP switch delay. |
| OPPO | Issue 1-2-3：  Sub 1：Share the similar view as MTK’s. RRC procedure delay in RAN2 = RRC reconfiguration time + BWP switching delay  Sub 2: No strong opinion on additional waiting time. Either option 1 or 2 is fine. |
| Apple | Issue 1-2-3  Sub1: Option 1. RAN2 spec clearly captures that RRC procedure delay in case of BWP switch includes BWP switching delay  Sub 2: Option 1.  Issue 1-2-4  Option 1 |
| Xiaomi | Issue 1-2-3:  Sub 1: option 1, follow RAN2 spec  Sub 2: option 1. |
| Huawei | Sub2 option 2/2a  RAN2 spec in clause 12 is to define the performance requirement where the end point is that UE is ready for reception of UL grant, and this is why the BWP switching time is included.  However, the issues raised from clause 5 that UE should process the message in order.  “process the received messages in order of reception by RRC, i.e. the processing of a message shall be completed before starting the processing of a subsequent message;”  We don't think companies have consistent understanding about RRC procedure delay/RRC processing delay and also we cannot understand the link between the definition in clause 12 in TS38.331 and the UE behaviour for RRC-based BWP switch in 2 CGs.  Under the scenarios RAN4 has defined (FR1 + FR2 NR-DC without SCS changes and UE is capable of Per-FR change), can proponents of option 1 explain why the 2nd RRC message cannot be processed until BWP switch is completed in the 1st CG?  Also from NW’s perspective, there could be no coordination between MN and SN, for option 1, it means the RRC-triggered BWP switch in the 2nd RRC messages may experience an unexpected long waiting time, which could be worse if the BWP switching is extended for multiple CC.  In summary, we support option 2 and we think it is aligned with RAN2’s spec that the RRC message should be processed in order. For option 1 we didn't see the need and benefit to delay the 2nd RRC message processing until the UE complete the 1st RRC-triggered BWP switch expect for the wording about the performance requirement defined in clause 12 in TS 38.133 which we think is not related here. Also from NW’s perspective, option2 will introduce unexpected delay which could be extremely long and will not bring any benefits under the scenario RAN4 has defined. |
| Nokia | UE processes a single RRC command at a time and there is only one RRC entity. Hence, we can assume that there is ongoing RRC based BWP switching, the other one should wait until UE has completed the RRC process. The extra waiting time will be needed for this case, and the maximum extra waiting time should be RRC processing time. The RRC processing time is the RRC procedure delay is the value defined in the following table (Table 12.1-1 in TS 38.331)  Sub 1: we support option 2.  Sub 2: we support option 2. |
| Intel | Sub1: Option 2  In RAN2 spec, it specified that RRC procedure delay is RRC message processing delay + RAN 4 defined BWP switch delay.  Sub2: Option 1  In partially overlapped case, it’s up to UE implementation whether UE can process the second RRC message after BWP switch or not. One example is that UE will process the second RRC processing only after UE finish the BWP switch of the first CG. It’s also possible that there can be some overlapping between the BWP switch of the first CG and the RRC processing of the second CG. Considering the worst case and this is not typical scenario, it’s better to assume the delay time is upper bounded by the multiple BWP switch delay of the first CG. |

### Sub-topic 1-3: Cross carrier scheduling DCI-based BWP switch

**Issue 1-3-1: whether cross carrier scheduled DCI-based BWP switch on single/multiple CCs is considered in Rel-16**

* Option 1(Huawei): Yes
* Recommended WF:
  + Further discussion

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| **Company** | **Comments** |
| Qualcomm | We think that both sub-topic 3-1 and 3-2 are more relevant for dormant SCell discussion and these topics should be discussed in that session; not in BWP switching session. |
| MTK | Option 1.  We support to consider cross carrier scheduling in R16, otherwise dormancy SCell application scenario will be limited.  Since this is a new issue, do we plan to discuss it in R16 maintenance part? |
| vivo | Support to consider this issue in R16 however we can discuss it at SCell dormancy session. There are few tdoc discuss this issue at Scell dormancy session. |
| Ericsson | Support Option 1. Cross carrier scheduling is essential for SCell dormancy, where triggering normally will be via spCell. As pointed out by Qualcomm and vivo, there are a few contributions in thread 213 about this. |
| Apple | Since this is last meeting to complete this WI, we should probably not be discussing new issues at this stage. If this is already discussed in SCell dormancy session, we prefer not to discuss it here. |
| Huawei | We agree with companies’ comment to issue 1-3-1 and 1-3-2 that the some discussions are only related to dormancy SCell. We are fine to discussion the issue in dormancy SCell topic and only consider the self-scheduling case in BWP switching requirement in R16. |
| Intel | Due to the limited time, prefer not to discuss it here. |

**Issue 1-3-2: Requirements for cross carrier BWP switch on multiple CCs in Rel-16**

* Option 1(Huawei):
* The requirements for BWP switch on multiple CCs in Rel-16 apply to following 2 cases: 1) the BWP switch on each CC is scheduled by a separate DCI which is received in the same CC; 2) All CCs involved in the simultaneous BWP switch on multiple CCs are scheduled by a single DCI.
* Define the starting point of the cross carrier BWP switch as the slot of the scheduling CC where UE receives the DCI and TBWPSwitchDelay ­shall be determined by the smaller SCS of all involved CC.
* For cross carrier scheduling, when the SCS of the scheduled CC is larger than or equal to that of the scheduling CC, one additional slot of the scheduled CC is allowed; when the SCS of the scheduling CC is larger than that of the scheduled CC, there is no need to introduce extra delay.
* Recommended WF:
  + Further discussion

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| **Company** | **Comments** |
| Qualcomm | In Rel-16, the scenario “All CCs involved in the simultaneous BWP switch on multiple CCs are scheduled by a single DCI” is only applicable for dormant SCells. We don’t think that this scenario is applicable for BWP switching in non-dormant SCells.  Hence, both 3-1 and 3-2 should be discussed in dormant SCells session. |
| MTK | We support 1st bullet  But for the 2nd and 3rd bullets in HW’s proposal, we have some questions need further clarifications.  To HW,   1. Do you mean always adding 1 slot for both type 1 and type 2 UEs, Or Type 1 only? 2. If the scheduling CC aligns with scheduled CC, do we still need to add 1 slot if scheduled CC is larger than or equal to that of the scheduling CC? For example, in scheduling CC’s slot n+8 from your figure. |
| vivo | As before, suppor the principles. However it is not necessary to discuss the same issue at two different places and suggest to discuss it at scell dormancy session. Agree with QC’s comments. |
| Ericsson | Agree with Qualcomm and vivo on that we can discuss it in the context of SCell dormancy. |
| OPPO | Agree with QC and Ericsson to discuss this in [213] |
| Apple | Since this is last meeting to complete this WI, we should probably not be discussing new issues at this stage. If this is already discussed in SCell dormancy session, we prefer not to discuss it here. |
| Huawei | For the 1st bullet.  We agree that the 2nd scenario is only applicable for dormancy SCell. We could focus on 1st scenarios for BWP switching requirements (the BWP switch on each CC is scheduled by a separate DCI which is received in the same CC)  Reply to MTK: 1. We think it is necessary at least for type 1 when the SCS of the scheduling CC is smaller. For example the SCS of the scheduling CC is 15 KHz and the SCS of the scheduled CC is 120 KHz, as shown in the fig below, the symbol length of 15 KHz is much larger than that of 120KHz, and it could take almost 2 slot for the 120 KHz to receive the DCI. The MRTD should also be considered between the scheduling and scheduled CC. Thus the existing requirements my no longer applicable.    2.There is no need to add 1 slot when the SCS of scheduling CC is larger even it is not aligned as the starting point of the cross carrier BWP switch is defined as the slot of the scheduling CC (2nd bullet). |
| Intel | Agree to discuss this in dormancy SCell. |

### Sub-topic 1-4: test case design for multiple BWP switch

Moderator note: core part discussion should be prioritized in this meeting. however, it could be good for companies to share views on performance part as well. Comments on this clause are welcome.

**Issue 1-4-1: Test scenarios for simultaneous BWP switching (DCI/timer/RRC based):**

* Option 1(Intel):
* EN-DC with intra-band FR1 CA
* EN-DC with intra-band FR2 CA
* SA with intra-band FR1 CA
* SA with intra-band FR2 CA
* Recommended WF:
  + Further discussion

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| **Company** | **Comments** |
| Qualcomm | We thank Intel for sharing their views. Could the moderator please clarify that the performance related issues will be decided in the next meeting and this meeting’s discussion regarding these topics is only intended for information sharing? |
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**Issue 1-4-2: Number of CCs for simultaneous BWP switching in the test case**

* Option 1(Intel):
* Number of CC will be further discussed since it has dependency on the conclusion of current RRC based BWP switch discussion
* Recommended WF:
* Further discussion

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| **Company** | **Comments** |
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**Issue 1-4-3: Test case for partial overlap BWP switching**

* Option 1(Intel):
* Test scenario for delay requirements for RRC based partial overlap BWP switch is NR-DC FR1+FR2.
* Don’t need to define test case for delay requirement of DCI based partial overlap BWP switch.
* Recommended WF:
* Further discussion

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| **Company** | **Comments** |
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### CRs/TPs comments collection

*Major close-to-finalize WIs and Rel-15 maintenance, comments collections can be arranged for TPs and CRs. For Rel-16 on-going Wis, suggest to focus on open issues discussion on 1st round.*

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| **CR/TP number** | **Comments collection** |
| R4-2011069  Huawei | Qualcomm: Almost all changes mentioned in this CR depend on the conclusion of the open issues. Hence, this and all other relevant CRs can be considered only after deciding the open issues. |
| Ericsson: N is not clearly defined in section 8.6.2A.1, should be “number of CCs on which simultaneous BWP switching occurs” rather than “number of simultaneous BWP switchings on CCs”. For non-simultaneous BWP switching, we have a different view, so a conclusion has to be reached before we can agree on this CR. |
| Apple: Most of the issues being discussed need to be resolved before discussing the CR. |
| Nokia: CR could be treated after we have conclusion of the open issues. |
| R4-2009864  Intel | Qualcomm: We have the same comment that we previously mentioned for R4-2011069. |
| Ericsson: In our view the definition of simultaneous needs to be corrected; it should be when the UE receives BWP switch for CCs in the same RRC msg. Non-simultaneous case is missing. |
| Apple: Most of the issues being discussed need to be resolved before discussing the CR. |
| Nokia: CR could be treated after we have conclusion of the open issues. |
| R4-2011248  Ericsson | Qualcomm: We mostly agree with the proposed changes in “non-simultaneous timer based BWP switch” and “simultaneous RRC based BWP switch” Regarding “non-simultaneous RRC based BWP switch” part, the proposed equation is valid if only two RRC based BWP switches are partially overlapped with each other. However, if multiple RRC based BWP switches are partially overlapped with each other, then TBWPswitchDelayRRC should capture the BWP processing time of previous N-1 switches. |
| Ericsson: Regarding QC’s comments on “multiple RRC based BWP switches are partially overlapped with each other….”, the BWP switch delay due to (N-1) CCs of the second CG (CG2) is covered by factor Drrc \*(N-1). There is a factor T\_Delay which includes the BWP processing time of previous BWP switches in the first CG (CG1 i.e. where BWP switch was on going when UE receives RRC for CG2). T\_Delay is not elaborated but it can be defined as: T\_Delay= TBWPswitchDelayRRC + Drrc \*(M-1); where M is the number of CCs in CG2 on which BWP switch is performed before starting BWP switch on CCs on CG2. Is this ok? |
| Apple: We are fine with most of the proposed changes, except for timer based partial overlap case. This is still under discussion |
| R4-2010197  Apple | Qualcomm: We agree with the CR. |
| Ericsson: OK |
| Nokia: OK |
| R4-2010362  Vivo | Qualcomm: We agree with the CR. |
| Ericsson: Seems a normalization with slot length is missing. Non-simultaneous case is missing. |
| Apple: We are fine with the CR. Normalization by slot length is missing. |
| Nokia: CR could be treated after we have conclusion of the open issues. |

## Summary for 1st round

### Open issues

*Moderator tries to summarize discussion status for 1st round, list all the identified open issues and tentative agreements or candidate options and suggestion for 2nd round i.e. WF assignment.*

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|  | **Status summary** |
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*Recommendations on WF/LS assignment*

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|  | **WF/LS t-doc Title** | **Assigned Company,**  **WF or LS lead** |
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### CRs/TPs

*Moderator tries to summarize discussion status for 1st round and provides recommendation on CRs/TPs Status update*

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| **CR/TP number** | **CRs/TPs Status update recommendation** |
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## Discussion on 2nd round (if applicable)

### Sub-topic 1-1: Simultaneous BWP switch on multiple CCs

### Sub-topic 1-2: Partial overlap BWP switch on multiple CCs

## Summary on 2nd round (if applicable)

*Moderator tries to summarize discussion status for 2nd round and provided recommendation on CRs/TPs/WFs/LSs Status update suggestion*

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# Topic #2: UL Spatial Relation Info Switching

## Companies’ contributions summary

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| **T-doc number** | **Company** | **Proposals / Observations** |
| [R4-2009608](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2009608.zip) | Apple | **Proposal #1: DL time tracking shall not be considered when associated DL-RS is known or unknown for UL spatial relation switch.**  **Proposal #2: For MAC CE based uplink spatial relation info switch associated with DL-RS the requirements are defined as: THARQ + 3ms; for known spatial relation and THARQ + 3ms + TL1-RSRP; for unknown spatial relation.**  **Proposal #3: For RRC based uplink spatial relation info switch associated with DL-RS the requirements are defined as: TRRC-processing; for known spatial relation and TRRC-processing + TL1-RSRP; for unknown spatial relation.** |
| [R4-2009708](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2009708.zip) | NTT DOCOMO, INC. | **Observation 1: Transmit timing other than initial case such as first transmission in a DRX cycle or PRACH transmission can be tracked by normal TA procedure.**  **Proposal 1: No initial timing accuracy requirements are needed for UL spatial relation info switch.**  **Observation 2: Timing tracking is performed upon TCI state change procedure if needed.**  **Observation 3: If the source RS of new TCI state is unknown, it must be known after TCI state switching since UE perform L1-RSRP measurement.**  **Proposal 2: Timing tracking shall not be required for sub1 and no requirement shall be defined for sub2.**  **Proposal 3: UE shall use previous TX beam or drop the corresponding UL transmission when the UL signal has spatial relation to an unknown TCI-state.**  **Proposal 4: Delay requirement for UE which only supports BC Bit-0 shall be same as that of BC Bit-1 UE.**  **Proposal 5: Delay requirement for known spatial relation but the DL RS is not in the active TCI list shall be THARQ +3ms and for unknown spatial relation shall be THARQ + 3ms+ TL1-RSRP**  **Proposal 6: Delay requirement for known spatial relation but the DL RS is not in the active TCI list shall be TRRCprocessing and for unknown spatial relation shall be TRRCprocessing + TL1-RSRP** |
| [R4-2009752](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2009752.zip) | Intel Corporation | ***Proposal 1: When UL transmission is configured with spatial relation info associated with DL RS and the TCI state of the DL RS is unknown, don’t define requirement.***  ***Observation 1:*** ***If the UL transmission with UL spatial info switch satisfies the transmission condition defined in timing accuracy requirement, UL timing accuracy requirement need to be satisfied.***  ***Proposal 2: There is no need for UE to define new initial transmit timing accuracy test case to verify timing error after UL spatial relation switch.***  ***Proposal 3: When QCLed DL-RS is in tracking list, don’t need to consider DL tracking time. When QCLed DL-RS is not in tracking list, don’t define delay requirement.***  ***Proposal 4:*** ***Delay requirement for MAC CE based spatial relation info switching associated with DL-RS for PUCCH could be defined as:***  ***If the spatial relation associated DL-RS is in the active TCI state list: Tdelay = THARQ +3ms/NR slot length***  ***If the spatial relation associated DL-RS is not in the active TCI state list or unknown, no requirement is defined.***  ***Proposal 5:*** ***Delay requirement for RRC spatial relation info switching associated with DL-RS for P-SRS could be defined as:***  ***If the spatial relation associated DL-RS is in the active TCI state list: Tdelay = TRRCprocessing***  ***If the spatial relation associated DL-RS is not in the active TCI state list or unknown, no requirement is defined.***  ***Proposal 6:*** ***For Bit-0 UE, the same delay requirement as Bit-1 UE can be defined.*** |
| [R4-2009987](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2009987.zip) | Qualcomm | **Observation 1: 38.214 proposes UE to switch its spatial relation corresponding to a RS immediately after 3 ms. This requirement does not depend on whether the RS is known or unknown.**   * **Adoption of option 1 will lead to mismatch between 38.214 and 38.133 and one of these two specs will have to be clarified regarding this issue.**   **Observation 2: RAN plenary has not listed UL TX timing accuracy after UL spatial relation change as an open issue for Rel-16; which means that no related requirement will be defined for the UE in Rel-16.**   * **This means, it is not essential for the UE during the tests to get additional time for time tracking in Rel-16.**   **Proposal 1: When the UL signal has spatial relation to an unknown DL RS,**   * **UE’s selection of spatial relation during the delay period is up to its implementation and it does not need to be specified.**   **Proposal 2: Down-select between option 1 and 2 of the last meeting regarding whether to consider timing tracking when associated DL-RS is known or unknown.**  **Proposal 3: Down-select between option 1 and 2 of the last meeting regarding delay requirements for both MAC-CE and RRC based known and unknown spatial relations.** |
| [R4-2010043](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2010043.zip) | MediaTek inc. | ***Proposal 1: Do not define UE’s requirement in unknown spatial relation condition.***  ***Proposal 2: Only define the requirement when DL RS is in the active TCI list.***  ***Proposal 3: Fine timing tracking isn’t needed when the DL RS has already added in the active TCI state list.***  ***Proposal 4: The MAC CE based spatial relation switching associated with DL-RS for PUCCH and semi-persistent SRS is THARQ +3ms when the target spatial relation associated to DL RS is known and the DL RS is in the active TCI list.***  ***Proposal 5: The RRC based spatial relation info switching associated with DL-RS for P-SRS is TRRCprocessing when the target spatial relation associated to DL RS is known and the DL RS is in the active TCI list.*** |
| [R4-2010364](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2010364.zip) | vivo | **Proposal 1: Use option 1 for sub1 and option 3 for sub 2**  **Proposal 2: For MAC CE based spatial relation info switching associated with DL-RS for PUCCH,**  **Use option 1 for the switch delay when DL RS spatial relation is known but the DL RS is not in the active TCI list**  **Use option 3 when the DL RS spatial relation is unknown**  **Proposal 3: For RRC based spatial relation info switching associated with DL-RS for P-SRS,**  **Use option 1 for the switch delay when DL RS spatial relation is known but the DL RS is not in the active TCI list**  **Use option 3 when the DL RS spatial relation is unknown**  **Proposal 4: When the UL signal has spatial relation to an unknown DL RS using option** **3, i.e., up to UE implementation and no need to be specified.** |
| [R4-2010573](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2010573.zip) | Nokia, Nokia Shanghai Bell | Proposal 1: When the UL signal has spatial relation to an unknown DL RS the UE drop UL transmission until TCI state is known.  Proposal 2: For bit-0 UE not indicating *beamCorrespondenceWithoutUL-BeamSweeping* is allowed delay for UL SRS sweep. |
| [R4-2010666](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2010666.zip) | Ericsson | **Proposal 1:** The UE shall meet the initial transmit timing accuracy requirement after UL spatial relation switching. This corresponds to Option 2 in the WF.  **Proposal 2:** No time tracking shall be considered for the case where associated downlink reference is known but QCL-ed with a different qcl-Type1 RS. This corresponds to Option 1 in the WF.  **Proposal 3:** For the case where the DL RS is unknown to the UE, additional time for beam sweeping shall be granted. During the beam sweeping, the UE shall detect the DL RS and determine its timing. No additioanl time for time tracking shall be considered. This corresponds to Option 1 in the WF.  **Proposal 4:** The UE behaviour when UL signal has a spatial relation to an unknown DL RS shall be well defined. With reference to the options in the WF, either Option 1 or Option 2 shall be specified.  **Proposal 5:** A UE that is reporting BC bit-0 capability shall fulfill spatial relation switching delay requirements associated with SRS. Hence any such requirements explicitly defined by RAN4 shall apply for UEs reporting BC bit-0 and BC bit-1, respectively. With reference to the options in the WF, this would correspond to Option 1.  **Proposal 6:** Delay requirementMAC CE-based spatial relation switching for PUCCH with associated known DL-RS not in the active TCI state list shall be: THARQ +3ms. This corresponds to Option 1 in the WF.  **Proposal 7:** Delay requirementMAC CE-based spatial relation switching for PUCCH with associated unknown DL-RS shall be: THARQ +(3ms+ TL1-RSRP), i.e., it shall be assumed that DL RS timing is determined during beam sweeping and no additional time for time tracking would be needed. This corresponds to Option 1 in the WF.    **Proposal 8:** Delay requirementfor RRC-based spatial relation switching for P-SRS with associated known DL-RS not in the active TCI state list shall be: TRRCprocessing. This corresponds to Option 1 in the WF.  **Proposal 9:** Delay requirementfor RRC-based spatial relation switching for P-SRS with associated unknown DL-RS shall be: TRRCprocessing + TL1-RSRP ), i.e., it shall be assumed that DL RS timing is determined during beam sweeping and no additional time for time tracking would be needed. This corresponds to Option 1 in the WF. |
| [R4-2011126](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2011126.zip) | Huawei, Hisilicon | **Proposal 1: No timing tracking is considered when associated DL-RS is known but QCLed with a different qcl-Type1 RS.**  ***Proposal 2: Whether to consider timing tracking when associated DL-RS is an unknown DL RS?***   * + - ***Option 1: No***     - ***Option 3: No requirement will be defined***   ***Prefer option3, otherwise option 1 is acceptable.***  ***Proposal 3: when PUCCH-SpatialRelationInfo is provided, upon receiving MAC-CE activation command indicating a value of pucch-SpatialRelationInfoId in slot n,***   * ***If the spatial relation associated downlink RS is known, UE shall be able to transmit a PUCCH with target spatial relation at slot n+ THARQ +3 ms/ NR slot length.*** * ***If the spatial relation associated downlink RS is unknown, there are no requirements.***   ***Proposal 4: Periodic SRS spatial relation switching delay is specified as below,***   * ***If the spatial relation associated downlink RS is known, the periodic SRS spatial relation switching delay is TRRC\_processing;*** * ***If the spatial relation associated downlink RS is unknown, no requirement is defined.***   ***Proposal 5: Semi-persisitent SRS spatial relation switching delay can be specified as below,***  ***Upon receiving MAC-CE activation command indicating triggering a new semi-persistent SRS in slot n,***   * ***If the spatial relation associated downlink RS is known, UE shall be able to transmit a Semi-persisitent SRS with target spatial relation at slot n+ THARQ +3 ms/ NR slot length.*** * ***If the spatial relation associated downlink RS is unknown, no requirement is defined.*** |

## Open issues summary and companies view’s collection

*Before e-Meeting, moderators shall summarize list of open issues, candidate options and possible WF (if applicable) based on companies’ contributions.*

### Sub-topic 2-1: General

*Sub-topic description: Requirements for general*

*Open issues and candidate options before e-meeting:*

**Issue 2-1-1: When the UL signal has spatial relation to an unknown DL RS**

* Option 1 (Ericsson, NTT DOCOMO): UE transmits using previous TX beam
* Option 2 (NTT DOCOMO, Nokia, Ericsson): Drop UL transmission until spatial relation info is known
* Option 3 (Intel, Qualcomm, Vivo, MediaTek): Up to UE implementation and no requirement is needed to be specified
* Recommended WF:
  + Further discussion.

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| **Company** | **Comments** |
| MTK | Option 3.  RAN1 already agreed to switch to new spatial relation after T\_HARQ+3ms. Thus, it’s better to follow RAN1’s spec and follow the same logic used in TCI state switch. |
| vivo | Option 3. Within this 3ms network does not expect any particular UE behavior hence it is not necessary to fix a particular UE behavior. |
| Ericsson | Option 1 or Option 2. If the DL RS from which the UE is to deduce the spatial transmission filter is unknown, why should the UE transmit at all? Why is there a need for different UE implementations with respect to this? What benefit does it bring to a UE implementation? What benefit does it bring on a system level? |
| OPPO | Support option 3. |
| NTT DOCOMO, INC. | We can compromise option 3.  Although option 1 or 3 is better, the objective scenario can be avoided by operation. |
| Huawei | Support option 3. This issue is similar as TCI state switching (DL) we discussed during last meeting. As RAN1 had its conclusion, it is better RAN4 not to make conflict with RAN1. Then the proper way is left to UE implementation. |
| Qualcomm | We support option 3.  38.214 proposes UE to switch its spatial relation corresponding to a RS immediately after 3 ms. Adoption of option 1 will lead to mismatch between 38.214 and 38.133 and one of these two specs will have to clarify this issue. Hence, a better option would be leaving this issue up to UE implementation. |
| Nokia | We would like to understand what option 3 and ‘no UE requirements need to be specified’ means?  Our concern here is that the UE is transmitting in UL using the wrong UL beam and hence can cause unwanted interference. There would have been a reason for the network to change the settings of the UE to utilize a new UL Tx beam. There may be various reasons for this depending on implementation. One could be that the UE should not use the old Tx beam. Leaving this to UE implementation is from network point of view a worse solution than having the UE not transmitting in UL at all (old and/or new Tx beam).  Option 2 is preferred based on the negative impact on network side from option 3. Option 1 can be compromised. |
| Intel | For option 3, from our understanding, no requirement means that there is no delay requirement if UL transmission is associated with DL-RS whose spatial info is unknown. There is no restriction about UE behaviour. |
| Samsung | Option 3.  For Option 2, it will have impact on existing gNB implementation, which may not have the mechanism to avoid UE scheduling before spatial relation info is known. We don’t prefer introducing new UE requirement but have impact on existing network implementation. |

**Issue 2-1-2: Whether to consider DL timing tracking when associated DL-RS**

Whether to consider timing tracking when associated DL-RS?

* Sub1. Whether to consider timing tracking when associated DL-RS is known but QCLed with a different qcl-Type1 RS?
  + Option 1 (Apple, NTT DOCOMO, Vivo, Ericsson, Huawei): No
  + Option 2: Yes
  + Option 3 (Nokia): No requirement will be defined.
  + Option 4 (MediaTek, Intel): Only define the requirement when DL RS is in the active TCI list; Fine timing tracking isn’t needed when the DL RS has already added in the active TCI state list
* Sub2. Whether to consider timing tracking when associated DL-RS is an unknown DL RS?
  + Option 1(Apple, Ericsson, Huawei, NTT DOCOMO): No
  + Option 2 (Nokia): Yes
  + Option 3 (MediaTek, Vivo, Huawei, Intel): No requirement will be defined for unknown DL RS
* Recommended WF:
  + Further discussion.

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| **Company** | **Comments** |
| MTK | Option 4.  We think spatial relation switch shall be triggered after TCI state switch in downlink.  If the DL RS isn’t in the active TCI list, whether UE will track timing depends on UE itself. A reasonable DL-RS configuration should be included in the active TCI list to guarantee the uplink performance from network side. Thus, if the configured DL-RS isn’t in the active TCI list, it’s up to UE to choose either additional timing tracking duration or unguaranteed uplink transmission performance.  Option 3.  Uplink spatial relation switch will follow the configured DL RS due to beam correspondence. It’s reasonable to only ask UE to trigger uplink spatial relation switch when the configured DL RS has been measured and indicated in TCI state switch. |
| vivo | Sub 1: support option 1; Sub 2: option 3; |
| Ericsson | Sub 1: support Option 1; Sub 2: support Option 1 (timing shall be established as part of the L1-RSRP measurement). For Sub 1 Option 4 we see an issue since previously UE/chipset vendors have indicated that the capabilities with respect to supported number of tracked TCI states will be highly limited. |
| OPPO | Sub 1: support option 4 ; Sub 2: option 3; |
| Apple | Sub 1: Option 1 In our understanding, additional time for tracking is not needed, the UE should use DL serving cell timing in case of UL spatial relation switch. In case the UL timing does need to change with UL spatial relation, the timing from DL measurements should be sufficient and additional time for tracking should not be required.  Sub2: Option 1. |
| NTT DOCOMO, INC. | Sub 1: support option 1.  Sub 2: support option 1. |
| Huawei | Sub1: option 1. When UE switches from associated DL RS0 to DL RS1 whose QCL-TypeA is different with DL RS0, the downlink timing reference is kept unchanged, and UE just switches its uplink transmission beam to a new beam when UE receives PUCCH-SpatialRelationInfo.  Sub2: both option 1 and option 3 are fine and option 3 is more preferred. It is a strange case that network configures an unknown DL RS to UE. As this associated DL RS is unknown to UE, UE has not report any information to network ever, how network know this uplink beam is suitable to this UE? This is a blind decision for network and UE. We don’t think This case is typical in real network. |
| Qualcomm | Sub 1: Option 1.  Sub 2: option 1.  If UL TX timing is not tested after UL spatial relation switch, we wonder why UE needs timing tracking. |
| Nokia | We prefer to have some defined UE requirements. Hence, for Sub 2 we do not prefer option 3. As for Sub 1 we could then compromise to option 1 to have some defined UE requirements. |
| Intel | Sub1. We can compromise to option 1.  Sub2. Option 3. We don’t think it’s proper for NW to configure UL transmission with an unknown DL-RS. It’s better not define requirement for this case. |
| Samsung | Sub 1: support option 1.  Sub 2: support option 1. |

### Sub-topic 2-2: MAC CE based spatial relation info switch

*Sub-topic description: Requirements for MAC CE based spatial relation switch*

*Open issues and candidate options before e-meeting:*

**Issue 2-2-1: Delay requirement for MAC CE based spatial relation info switching associated with DL-RS for PUCCH**

* For known spatial relation switch
* Option 1: No DL timing tracking is needed:
  + Option 1a (NTT DOCOMO, Apple, Vivo, Nokia, Ericsson): THARQ +3ms
  + Option 1b (Huawei): THARQ +3ms/NR slot length
  + Option 1c (MediaTek, Intel):
* If the spatial relation associated downlink RS is in the active TCI state list, UE shall be able to transmit a PUCCH with target spatial relation at slot n+ THARQ +3 ms
* If the spatial relation associated downlink RS is not in the active TCI state list, no requirement is defined.
* Option 2: DL timing tracking is needed.
* For unknown spatial relation switch
* Option 1(Apple, NTT DOCOMO, Ericsson): No DL timing tracking is needed: THARQ + 3ms + TL1-RSRP
* Option 2 (Nokia): DL timing tracking is needed: THARQ + 3ms + ‘time for tracking’
* Option 3(Huawei, MediaTek, Vivo, Intel): No requirement
* Recommended WF
  + Further discussion

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| **Company** | **Comments** | |
| MTK | For known spatial relation switch  Option 1c.  The same reason as we discussed in 2-1-2.  For unknown spatial relation switch  Option 3.  The same reason as we discussed in 2-1-2. | |
| vivo | For known spatial relation switch  Option 1a.  For unknown spatial relation switch  Option 3. | |
| Ericsson | For switching to known SR: Option 1a/1b  For switching to unknown SR: Option 1 (and potentially normalization with slot length is needed too) | |
| vivo | For known spatial relation switch: Option 1c.  For unknown spatial relation switch: Option 3. | |
| Apple | For known spatial relation: Option 1a  For unknown spatial relation: Option 1 | |
| NTT DOCOMO, INC. | For known spatial relation switch, support option 1a/1b  For unknown spatial relation switch, support option 1 | |
| Huawei | For known spatial relation: in essence, option 1a and 1b is similar, while option 1b is more accurate as the unit of THARQ is slot, 3ms is ms level.  For unknown spatial relation: Option 3. The reason is the same as issue 2-1-2. | |
| Qualcomm | | Issue 2-2-1:  We support option 1a. We think that option 1a and 1b are equivalent.  Regarding option 1c, a UE may support as low as one DL RS in its active TCI state. If option 1c is selected, network will have to always change active TCI state before changing UL spatial relation. This will limit network’s flexibility to change UL spatial relation quickly, especially when network has to change UL spatial relation immediately after receiving L1-RSRP report due to UL demand.  For unknown spatial relation switch:  we support option 1. |
| Nokia | | For known spatial relation switch:  Option 1a and 1b seems to end similar accounting time in slots. Option 1a/1b.  For unknown spatial relation switch:  Option 1. |
| Intel | | For known spatial relation: Option 1a or 1b  For unknown spatial relation: Option 3. The same reason in Issue 2-2-1. |
| Samsung | | For known spatial relation switch  Option 1a or 1b depending on time unit.  For unknown spatial relation switch  Option 3. Don’t see the necessity to define requirement like this case. |

### Sub-topic 2-3: RRC based spatial relation info switch

*Sub-topic description: Requirements for RRC based spatial relation switch for DL-RS and SRS*

*Open issues and candidate options before e-meeting:*

**Issue 2-3-1: Delay requirement for RRC based spatial relation info switching associated with DL-RS for P-SRS**

* For known spatial relation switch
* Option 1: No DL timing tracking is needed.
  + Option 1a (Apple, NTT DOCOMO, Vivo, Nokia, Ericsson, Huawei): TRRCprocessing
  + Option 1b (MediaTek, Intel):
* The RRC based spatial relation info switching associated with DL-RS for P-SRS is TRRCprocessing when the target spatial relation associated to DL RS is known and the DL RS is in the active TCI list
* If the spatial relation associated downlink RS is not in the active TCI state list, no requirement is defined.
* Option 2: DL timing tracking is needed.
* For unknown spatial relation switch
* Option 1(Apple, NTT DOCOMO, Ericsson): No DL timing tracking is needed: TRRCprocessing + TL1-RSRP
* Option 2(Nokia): DL timing tracking is needed : TRRCprocessing + TL1-RSRP + time for time tracking if applicable
* Option 3(Huawei, Vivo, Intel, MediaTek): No requirement.
* Recommended WF
  + Further discussion

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| **Company** | **Comments** |
| MTK | The same reason as 2-2-1 |
| vivo | For known spatial relation switch: Option 1a  For unknown spatial relation switch : Option 3 |
| Ericsson | For switching to known SR: Option 1a  For switching to unknown SR: Option 1 |
| Ericsson | For switching to known SR: Option 1b  For switching to unknown SR: Option 3 |
| Apple | For known spatial relation: Option 1a  For unknown spatial relation: Option 1 |
| NTT DOCOMO, INC. | For known spatial relation switch, support option 1a  For unknown spatial relation switch, support option 1 |
| Huawei | For known spatial relation switch: Option 1a.  For unknown spatial relation switch: Option 3. The reason is the same as issue 2-1-2. |
| Qualcomm | Issue 2-3-1:  We support option 1a.  Our motivation is the same as the one that we mentioned in issue 2-2-1.  For unknown spatial relation switch:  we support option 1. |
| Nokia | For known spatial relation switch:  Option 1a  For unknown spatial relation switch:  Option 1. |
| Intel | For known spatial relation switch, support option 1a  For unknown spatial relation switch, support option 3 |
| Samsung | For known spatial relation switch, support option 1b  For unknown spatial relation switch, support option 3 |

### Sub-topic 2-4: test case scenario for UL spatial relation info switching

Moderator note: core part discussion should be prioritized in this meeting. however, it could be good for companies to share views on performance part as well. Comments on this clause are welcome.

**Issue 2-4-1: test case scenario for UL spatial relation info switching**

* Option 1(Intel):
* EN-DC FR2 MAC CE based spatial relation info switching for PUCCH associated with DL-RS in known state
* EN-DC FR2 MAC CE based spatial relation info switching for SP-SRS associated with DL-RS in known state
* EN-DC FR2 RRC based spatial relation info switching for P-SRS associated with DL-RS in known state
* EN-DC FR2 DCI based spatial relation info switching for A-SRS associated with DL-RS in known state
* SA FR2 MAC CE based spatial relation info switching for PUCCH associated with DL-RS in known state
* SA FR2 MAC CE based spatial relation info switching for SP-SRS associated with DL-RS in known state
* SA FR2 RRC based spatial relation info switching for P-SRS associated with DL-RS in known state
* SA FR2 DCI based spatial relation info switching for A-SRS associated with DL-RS in known state
* Recommended WF
  + Further discussion

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| **Company** | **Comments** |
| Apple | We propose the following tests:   * EN-DC FR2 MAC CE based spatial relation info switching for PUCCH associated with DL-RS in known state * EN-DC FR2 RRC based spatial relation info switching for P-SRS associated with DL-RS in known state * SA FR2 MAC CE based spatial relation info switching for PUCCH associated with DL-RS in known state * SA FR2 RRC based spatial relation info switching for P-SRS associated with DL-RS in known state |
| Qualcomm | We thank Intel for sharing their views. Could the moderator please clarify that the performance related issues will be decided in the next meeting and this meeting’s discussion regarding these topics is only intended for information sharing? |
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### CRs/TPs comments collection

*Major close to finalize WIs and Rel-15 maintenance, comments collections can be arranged for TPs and CRs. For Rel-16 on-going WIs, suggest to focus on open issues discussion on 1st round.*

|  |  |
| --- | --- |
| **CR/TP number** | **Comments collection** |
| [R4-2009865](http://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_96_e/Docs/R4-2009865.zip)  Intel | MTK: We think current spec. is enough. |
| Ericsson: We do not agree to this change – particularly regarding DL RS that may be known but not in the active TCI state list. |
| Apple: The current requirements are clearly defined for known spatial relation in active TCI state list. The change is not needed, even if we agree not to define requirements for unknown spatial relation or DL-RS not in active TCI state list. |
| Nokia: Based on the discussion we do not agree to this change. Current specification already covers when the requirements apply. |

## Summary for 1st round

### Open issues

*Moderator tries to summarize discussion status for 1st round, list all the identified open issues and tentative agreements or candidate options and suggestion for 2nd round i.e. WF assignment.*

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|  | **Status summary** |
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*Suggestion on WF/LS assignment*

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| --- | --- | --- |
|  | **WF/LS t-doc Title** | **Assigned Company,**  **WF or LS lead** |
|  |  |  |

### CRs/TPs

*Moderator tries to summarize discussion status for 1st round and provided recommendation on CRs/TPs Status update suggestion*

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| **CR/TP number** | **CRs/TPs Status update recommendation** |
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## Discussion on 2nd round (if applicable)

### Sub-topic 2-1: General

### Sub-topic 2-2: MAC CE based spatial relation info switch

### Sub-topic 2-3: RRC based spatial relation info switch

## Summary on 2nd round (if applicable)

*Moderator tries to summarize discussion status for 2nd round and provided recommendation on CRs/TPs/WFs/LSs Status update suggestion*

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|  | **Status summary** | |
| **CR/TP/LS/WF number** | | **T-doc Status update recommendation** |
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