3GPP TSG-RAN WG2 Meeting #118 Electronic R2-220xxxx

Online Meeting, May 9th – 20th 2022

**Agenda item: 6.11.1**

**Source: CATT**

**Title:**  **[AT118-e][626][POS] LS on TEG framework (CATT)**

**WID/SID: NR\_pos\_enh-Core**

**Document for: Discussion and Agreement**

# 1 Introduction

This document is to kick off the following email discussion:

* [AT118-e][626][POS] LS on TEG framework (CATT)

 Scope: Handle the LS in R2-2204478, determine a way forward, and draft a reply.

 Intended outcome: Approved LS (without CB if possible)

 Deadline: Friday 2022-05-13 1800 UTC

This email discussion will determine a way forward on the LS in R2-2204478, and discuss the possible content for the Reply LS.

# 2 Contact Information

Respondents to the email discussion are kindly asked to fill in the following table.

|  |  |
| --- | --- |
| Company | Contact: Name (E-mail) |
| Intel | Yi.guo@intel.com |
| Huawei, HiSilicon | yinghaoguo@huawei.com |
| ZTE | pan.yu24@zte.com.cn |
| vivo | panxiang@vivo.com |
| Spreadtrum Communications | Huifang.Fan@unisoc.com |
| CATT | lijianxiang@catt.cn |
| Samsung  | June77.hwang@samsung.com |
| OPPO | liuyangbj@oppo.com |
| Ericsson | Ritesh.shreevastav@ericsson.com |
|  |  |

# 3 References

1. R2-2204139 LS on the UE/TRP TEG framework LS in Rel-17 NR\_pos\_enh-Core To: RAN1, RAN2
2. R2-2205829 LPP Updates Qualcomm Incorporated draftCR Rel-17 37.355 17.0.0 F NR\_pos\_enh-Core
3. R2-2204688 Reply LS on the UE/TRP TEG framework (R4-2206998; contact: CATT) CATT LS out Rel-17 To:RAN4 Cc:RAN1,RAN3
4. R2-2204705 Discussion on the LS on the framework of UE/TRP Rx TEG CATT discussion Rel-17

# 4 Discussion

## 4.1 Analysis on the UE/TRP TEG framework in RAN4 LS

RAN2 received an LS [1] from RAN4, with the following agreements:

|  |
| --- |
| * The framework of UE/TRP Rx TEG:
	+ Define multiple candidate timing error margin values {TE1, TE2, …, TEN} in the spec.
		- The number of candidate values (i.e. N) and the exact values of {TE1, TE2, …, TEN} will be decided in Perf part.
	+ UE/TRP selects one value M from {TE1, TE2, …, TEN} based on its implementation and indicate to LMF.
	+ For UE that supports multiple Rx TEGs (TEG#1, TEG#2, …), the associated timing error margin value of each Rx TEG is M, which means the timing error difference between the measurements within the same Rx TEG is within the margin M.
	+ The applicability of reported UE Rx TEG is limited to the measurements contained within the measurement report in which the Rx TEG information is provided, and only to measurements that are tagged with the corresponding TEG ID.
	+ The RRM accuracy requirements corresponding to the candidate timing error margin values {TE1, TE2, …, TEN} will be defined in Perf part.
* The framework of UE/TRP Rx TEG can be also applied for UE/TRP RxTx TEG
	+ Note: if additional issues are identified based on RAN1/2 progress, then this agreement can be revised.
 |

RAN4 kindly asks RAN1/2 to take the above information into account in the following work on NR positioning enhancements, and design the necessary signalling support for the TEG framework. RAN4 kindly asks RAN1/2 to provide feedback if any issues are identified.

‘

According to the first agreement as below,

* + Define multiple candidate timing error margin values {TE1, TE2, …, TEN} in the spec.
		- The number of candidate values (i.e. N) and the exact values of {TE1, TE2, …, TEN} will be decided in Perf part.

RAN2 need to add a field of UE Rx TEG value, corresponding to one of the candidate timing error margin values {TE1, TE2, …, TEN}. Examples of error margin on RxTEG have been captured in the existing LPP draft CR [2] (except RxTxTEG) as below:

#1: RxTEG error margin report in DL-TDOA

NR-DL-TDOA-SignalMeasurementInformation-r16 ::= SEQUENCE {

 dl-PRS-ReferenceInfo-r16 DL-PRS-ID-Info-r16,

 nr-DL-TDOA-MeasList-r16 NR-DL-TDOA-MeasList-r16,

 ...,

 [[

 ue-Rx-TEG-ErrorMarginList-r17 SEQUENCE (SIZE(1..maxNumOfRxTEGs-r17)) OF

 UE-Rx-TEG-ErrorMarginElement-r17 OPTIONAL

 ]]

}

UE-Rx-TEG-ErrorMarginElement-r17 ::= SEQUENCE {

 nr-UE-Rx-TEG-ID-r17 INTEGER (0..maxNumOfRxTEGs-1-r17),

 timingErrorMargin-r17 INTEGER (1..FFS),

 ...

}

#2: RxTEG error margin report in Multi-RTT

NR-Multi-RTT-SignalMeasurementInformation-r16 ::= SEQUENCE {

 nr-Multi-RTT-MeasList-r16 NR-Multi-RTT-MeasList-r16,

 nr-NTA-Offset-r16 ENUMERATED { nTA1, nTA2, nTA3, nTA4, ... } OPTIONAL,

 ...,

 [[

 nr-SRS-TxTEG-Set-r17 SEQUENCE (SIZE(1..maxTxTEG-Sets-r17)) OF

 NR-SRS-TxTEG-Element-r17 OPTIONAL,

 -- Cond Case2-3

 ue-Rx-TEG-ErrorMarginList-r17 SEQUENCE (SIZE(1..maxNumOfRxTEGs-r17)) OF

UE-Rx-TEG-ErrorMarginElement-r17 OPTIONAL -- Cond Case3

 ]]

}

UE-Rx-TEG-ErrorMarginElement-r17 ::= SEQUENCE {

 nr-UE-Rx-TEG-ID-r17 INTEGER (0..maxNumOfRxTEGs-1-r17),

 timingErrorMargin-r17 INTEGER (1..FFS),

 ...

}

Since RAN4 has not determined the exact values, the field with value is FFS, and RAN2 waits for further reply from RAN4 on the exact value. Similarly, a field of UE RxTx TEG value also need to be further informed by RAN4.

To notice that RAN2 taking the UE/TRP TEG framework into account and waiting for further LS from RAN4, RAN2 reply an LS to RAN4 as response to [1].

**Question 1: Do you agree that RAN2 reply an LS to RAN4 to notice that RAN2 waits for more information about exact TEG value? If you want to take some further actions, please also comment in the table.**

|  |  |  |
| --- | --- | --- |
| Company |  Yes/ No | Comments |
| Intel | No | “The number of candidate values (i.e. N) and the exact values of {TE1, TE2, …, TEN} will be decided in Perf part.”RAN4 indicated that the value will be decided in perf part, that means they will provide value when discussing performance part that will be the quite late stage. Do not see the need to tell them, we are waiting since it is normal process procedure.But then the problem is that the late value will impact ASN.1 if we capture the structure for now, i.e. non-backward compatibility change cannot be avoided. RAN2 need to decide whether it is allowed or not after ASN.1 frozen. If not, we cannot capture the structure in this meeting and leaving value open, i.e. we have to wait until RAN4 finish all the work.  |
| Huawei, HiSilicon | No | Same view as intel that they are under the performance part and we only need to wait for the R4’s final conclusion |
| ZTE | No | Agree with Intel and HW the LS is not needed for now;In addition, RAN4’s LS indicates ‘The framework of UE/TRP Rx TEG can be also applied for UE/TRP RxTx TEG’, so if the structure is agreed to capture in LPP, RxTx TEG should also be included. |
| Apple | No | We don’t see how sending an LS helps, we need to wait for RAN4. |
| Qualcomm | No | No need for an LS. This is like other open issues, such as RAN1 capability list. The current LPP draft implemented also the FFS items (using yellow highlight), but if no update is received from RAN1/RAN4 it must be deleted and probably introduced later. From ASN.1 point of view, it should be possible to add this backwards compatible. Thanks for pointing out the RxTx TEG; I missed this in the LPP drafting.[ |
| Intel1 |  | For values with FFS, our thinking is, we should not leave any FFS after this meeting, therefore either to remove the filed at all as mentioned by Sven, or we introduce value range large enough. Of course both of them are not perfect.  |
| Vivo | No | No need to reply the LS as RAN4 has planned to decide it in Perf part and there is no extra essential information that RAN2 can provided to RAN4. Besides, we are not convinced about the structure. As described in the LS, the UE/TRP selects one value M from {TE1, TE2, …, TEN} based on its implementation and indicate to LMF. In our understanding, only one value is needed instead of a list. Thus, we prefer to add the field after RAN4 provides final conclusion. |
| Spreadtrum | No | No need for an LS. We are inclined to remove the structure in this meeting and wait until RAN4 finish all the work. |
| CATT |  | RAN4 should be aware of that RAN2 is waiting for the values of TxTEG/RxTEG/RxTxTEG and RAN4 should take the issue as higher priority. But we are fine not to send the LS if there is no majority support. And suggest deleting the TEG-ErrorMarginList in the existing LPP update in case of possible NBC issue. |
| Xiaomi | No | Agree with CATT. |
| Samsung  | No  | Same view with Intel. |
| OPPO | No | Agree with CATT |
| Ericsson | Yes | No harm in sending LS. There is no need for deleting the existing structure.  |

**Summary:**

12 companies provided feedback. 10/12 companies answered ‘No’ for “RAN2 reply an LS to RAN4 to notice that RAN2 waits for more information about exact TEG value”, 1/12 company think there is no harm in sending LS, 1/12 company think they are fine not to send the LS if there is no majority support. Therefore, to follow the views of majority, rapporteur proposes for RAN2 to agree the following proposal:

**Proposal 1: RAN2 wait for the TEG value from RAN4 without replying an LS.**

Further, considering the error margin on RxTEG have been captured in the existing LPP draft CR [2], the concerns of non-backward compatibility was raised in the comment field. There are three views to be considered:

* Option 1: In case of possible non-backward compatibility issue, RAN2 delete the TEG-ErrorMarginList in the existing LPP update and wait until RAN4 finish all the work.

**Supported by Intel, QC, vivo, Spreadtrum, CATT, Xiaomi, Samsung, OPPO**

* Option 2: Value with FFS should not be allowed after this meeting. RAN2 can keep the existing structure and introduce value range large enough. **Supported by Intel**, **Samsung**
* Option 3: There is no need to delete the existing structure, and the framework of UE/TRP RxTx TEG should be also added. **Supported by** **Ericsson**

There is overwhelming majority on whether and how to capture the error margins on Rx TEG and RxTx TEG in LPP CR supporting Option1. So we proposed:

**Proposal 2: In case of possible non-backward compatibility issue, RAN2 to delete the timingErrorMargin in the existing LPP and wait until RAN4 finish all the work.**

## 4.2 Discussion about draft Reply LS

Based on the previous discussion, we draft the following contents of the Reply LS to RAN4 and CC RAN1 and RAN3：

**1. Overall Description:**

RAN2 thanks RAN4 for their LS on the UE/TRP TEG framework. RAN2 would like to wait for further notice from RAN4 and then capture the info of values of Rx TEG and RxTx TEG.

**2. Actions:**

**To WG RAN4:**

RAN2 would like to wait for further notice on the values of Rx TEG and RxTx TEG from RAN4.

**3. Date of Next TSG-RAN2 Meetings:**

TSG-RAN2 Meeting #119 22 - 26 August 2022 Toulouse, FR

**Question 2: Do you agree with the above contents？Please share your comments in the table.**

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| --- | --- | --- |
| Company | Yes/ No | Comments |
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**Summary:**

No action.

# 5 Conclusion

Based on the discussion in section 3 we propose the following:

**Proposal 1: RAN2 wait for the TEG value from RAN4 without replying an LS.**

**Proposal 2: In case of possible non-backward compatibility issue, RAN2 to delete the timingErrorMargin in the existing LPP and wait until RAN4 finish all the work.**