3GPP TSG-RAN WG2 Meeting #118 electronic R2-220

Online, May 9 – 20, 2022

Agenda Item: 6.17.3.1

Source: Ericsson

Title: [AT118-e][053][feMIMO] Discussion on H060

Document for: Discussion, Decision

# Introduction

# Contact Information

Respondents to the email discussion are kindly asked to fill in the following table.

|  |  |  |
| --- | --- | --- |
| Company | Name | Email Address |
| Ericsson | Helka-Liina Määttänen | Helka-liina.maattanen@ericsson.com |
| MediaTek | Li-Chuan TSENG | li-chuan.tseng@mediatek.com |
| LGE | SungHoon Jung | Sunghoon.jung@lge.com |
| Samsung | Seungri Jin | seungri.jin@samsung.com |
| ZTE | Fei Dong | Dong.fei@zte.com.cn |
| Huawei, HiSilicon | David Lecompte | david.lecompte@huawei.com |
| Vivo | Chenli | Chenli5g@vivo.com |
| CATT | Erlin Zeng | erlin.zeng@catt.cn |
| Apple | Fangli XU | fangli\_xu@apple.com |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

# PCI in resources in CSI-SSB-ResourceSet (H060)

The below contributions discuss the PCI associated to SSB indexes in same CSI-SSB-ResourceSet:

R2-2205916 M [H060] Inter-cell beam measurement configuration Huawei, HiSilicon

R2-2204599 M Discussion on RILs:F001, F002, V101,V102,H059,H060, I105,V112,V109,I115,Z095 OPPO

The corresponding LS text is as follows:

**Question 1.13:** Should it be possible for different SSB indexes in the same *CSI-SSB-ResourceSet* to be associated with different *additionalPCI*?

**Answer 1.13:**

Yes, it should be possible that different SSB indexes in the same CSI-SSB-ResourceSet are associated with different additionalPCI.

The LS response says quite clearly that the different SSB indexes can be associated with different additionalPCI. The additionalPCI does not include serving cell PCI by definition.

***additionalPCI***

PCI of the additional SSB different from serving cell PCI.

Hence there is contradiction between RAN1 response to Ran2 and what RAN1 has specified in TS 38.214 refferred to in R2-2205916.

***TS 38.214 V17.1.0, Clause 5.2.1.4.2***

If the UE is configured with the higher layer parameter [*NumberOfAdditionalPCI*], the UE is allowed to report in a single reporting instance up to four SSBRIs for each report setting, where SSB resources are associated with PCI indices referring to the PCI of the serving cell and PCI(s) different from the PCI of the serving cell within the set of PCIs configured.

Hence RAN2 should discuss what to do. R2-2205916 suggests TP as copied also in Annex of this document to make changes according to TS 38.214 while R2-2204599 suggests not to agree on this TP.

**Q2: Please give your view whether**

1. **RAN2 should agree on TP in R2-2205916(also in Annex here)**
2. **LS to RAN1 is needed and what should be the content**

|  |  |  |
| --- | --- | --- |
| Company | 1. Agree the TP | 1. Views whether LS to RAN1 is needed and what should be the content |
| Ericsson | TP is not necessary | To inform RAN1 RAN2 has specified the feature according to information received from RAN1 |
| Intel | Intention of TP is ok. But think that we can still make serving cell ID absent by changing structure of servingAdditionalPCIList-r17 ? | Our RAN1 believes that there is no restriction discussed in RAN1 for SSB and thus, it should be possible to associate with serving cell ID. If majority of companies are not confident, we would be ok to send LS to RAN1. |
| MediaTek | The intention of TP is correct. But currently the value of AdditionalPCIIndex-r17 starts from 1, does this already imply that the value ‘0’ means the serving cell? | We may inform RAN1 that current structure can support the case mentioned. |
| LGE | We agree with the intention of TP, and Intel’s suggestion is also fine.  So, we can either take a) the TP or b) change the structure of additionalPCIList-r17 to make absence of the field mean a serving cell.  No strong preference between them. | We can simply inform both the current structure and alternative and ask their preference, so that we can just take the RAN1 preference. |
| Samsung | Same vie with Intel and LG | Same view with MediaTek, if RAN1 have concerns on the LS we think RAN1 will point out the view on our structure. |
| ZTE | WE agree with the intention of TP.  Just have a suggestion on ‘ServingAdditionalPCIIndex-r17’ in the TP.  In the TP, the value 0 of the servingAdditionalPCIIndex-r17 is to represent the serving cell the CSI-SSB-ResourceSet belong to,and other values are to represent the indicated non-serving cell. That’s why we also need change the value range of the additionalPCIIndex in SSB-MTC from {0, maxNrofAdditionalPCI-r17-1} to {1, maxNrofAdditionalPCI-r17}  For minimizing the impact from the correction, we suggest to use the value maxNrofAdditionalPCI-r17 of servingAdditionalPCIIndex-r17 to represent the serving cell the CSI-SSB-ResourceSet belong to, then the *additionalPCIIndex* can be kept as it is. | We are not sure whether the LS is needed since the change is caused by the answer from a question we asked them. If companies think we still have two interpretations as we discussed during online, we can send it to RAN1 for confirmation. Otherwise, there is no need for us to send the LS. |
| Huawei, HiSilicon | Yes (proponent).  With respect to Intel's suggestion: we need a way to know which PCI (serving cell PCI or additional PCI) corresponds to which entry in csi-SSB-ResourceList.  One way is to have the same number of entries, which is what is done in the TP.  If we want to indicate the additionalPCI only for entries that don't use the serving cell PCI, we need to have a list of (entry number, AdditionalPCIIndex).  Both work, we have no preference.  With respect to ZTE's suggestion: if the number of additional PCI would need to be extended in a later release, using maxNrofAdditionalPCI-r17 to mean the serving cell PCI seems not a great idea. | We don't see the need for a LS to RAN1 but can send one if that is the general preference.  If we send a LS to RAN1, the LS should describe the feature in an English sentence (not rely on an ASN.1 TP which is not RAN1's expertise).  So the LS could say: "RAN2 assume that a CSI SSB resource set can include CSI SSB resources associated with the serving cell PCI and CSI SSB resources associated with additional PCIs. Please indicate if this is not RAN1's intention." |
| vivo | We agree with the intention of TP, and also the Intel’s suggestion. What we understand is it should be possible to associate with serving cell. | It is better to send LS to RAN1 to confirm our understanding.  If companies donot agree with the TP, we are also fine to check with RAN1 which is the correct understanding. |
| CATT | We agree with the intention of the TP. | We agree with HW’s TP. If R2 could agree on this, then no need to send LS to R1.  Besides, we do not see any inconsistence btw the previous R1 reply LS and R1 agreemeent/spec.  **Question 1.13:** Should it be possible for different SSB indexes in the same *CSI-SSB-ResourceSet* to be associated with different *additionalPCI*?  **Answer 1.13:**  Yes, it should be possible that different SSB indexes in the same CSI-SSB-ResourceSet are associated with different additionalPCI.  The R1 answer in 1.13 is only talking about “different *additionalPCI*” because the question was formulated that way. |
| Apple | Agree with the intention and fine with the TP. | It’s no need to send LS to RAN1, since the change is just based on RAN1 feedback. |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

# Conclusion

In the previous sections we made the following observations:

1. Annex: Text Proposal to TS 38.331

- CSI-SSB-ResourceSet

The IE *CSI-SSB-ResourceSet* is used to configure one SS/PBCH block resource set which refers to SS/PBCH as indicated in *ServingCellConfigCommon* and *ServingCellConfig*.

*CSI-SSB-ResourceSet* information element

-- ASN1START

-- TAG-CSI-SSB-RESOURCESET-START

CSI-SSB-ResourceSet ::= SEQUENCE {

csi-SSB-ResourceSetId CSI-SSB-ResourceSetId,

csi-SSB-ResourceList SEQUENCE (SIZE(1..maxNrofCSI-SSB-ResourcePerSet)) OF SSB-Index,

...,

[[

servingAdditionalPCIList-r17 SEQUENCE (SIZE(1..maxNrofCSI-SSB-ResourcePerSet)) OF ServingAdditionalPCIIndex-r17 OPTIONAL -- Need R

]]

}

ServingAdditionalPCIIndex-r17 ::= INTEGER(0..maxNrofAdditionalPCI-r17)

-- TAG-CSI-SSB-RESOURCESET-STOP

-- ASN1STOP

|  |
| --- |
| *CSI-SSB-ResourceSet* field descriptions |
| ***servingAdditionalPCIList***  Indicates the physical cell IDs (PCI) of the SSBs in the csi-SSB-ResourceList. If present, the list has the same number of entries as csi-SSB-ResourceList and the first entry of this list indicates the value of the PCI for the first entry of *csi-SSB-ResourceList*, the second entry of this list indicates the value of the PCI for the second entry of *csi-SSB-ResourceList*, and so on.  For each entry;  - if the value is zero, the PCI is the PCI of the serving cell in which this *CSI-SSB-ResourceSet* is defined;  - otherwise, the value is *additionalPCIIndex-r17* of an *SSB-MTC-AdditionalPCI-r17* in the *additionalPCIList-r17* in *ServingCellConfig*, and the PCI is the *additionalPCI-r17* in this *SSB-MTC-AdditionalPCI-r17*. |

– *SSB-MTC*

The IE *SSB-MTC* is used to configure measurement timing configurations, i.e., timing occasions at which the UE measures SSBs.

***SSB-MTC* information element**

-- ASN1START

-- TAG-SSB-MTC-START

SSB-MTC ::= SEQUENCE {

periodicityAndOffset CHOICE {

sf5 INTEGER (0..4),

sf10 INTEGER (0..9),

sf20 INTEGER (0..19),

sf40 INTEGER (0..39),

sf80 INTEGER (0..79),

sf160 INTEGER (0..159)

},

duration ENUMERATED { sf1, sf2, sf3, sf4, sf5 }

}

SSB-MTC2 ::= SEQUENCE {

pci-List SEQUENCE (SIZE (1..maxNrofPCIsPerSMTC)) OF PhysCellId OPTIONAL, -- Need M

periodicity ENUMERATED {sf5, sf10, sf20, sf40, sf80, spare3, spare2, spare1}

}

SSB-MTC2-LP-r16 ::= SEQUENCE {

pci-List SEQUENCE (SIZE (1..maxNrofPCIsPerSMTC)) OF PhysCellId OPTIONAL, -- Need R

periodicity ENUMERATED {sf10, sf20, sf40, sf80, sf160, spare3, spare2, spare1}

}

SSB-MTC3-r16 ::= SEQUENCE {

periodicityAndOffset-r16 CHOICE {

sf5-r16 INTEGER (0..4),

sf10-r16 INTEGER (0..9),

sf20-r16 INTEGER (0..19),

sf40-r16 INTEGER (0..39),

sf80-r16 INTEGER (0..79),

sf160-r16 INTEGER (0..159),

sf320-r16 INTEGER (0..319),

sf640-r16 INTEGER (0..639),

sf1280-r16 INTEGER (0..1279)

},

duration-r16 ENUMERATED {sf1, sf2, sf3, sf4, sf5},

pci-List-r16 SEQUENCE (SIZE (1..maxNrofPCIsPerSMTC)) OF PhysCellId OPTIONAL, -- Need M

ssb-ToMeasure-r16 SetupRelease { SSB-ToMeasure } OPTIONAL -- Need M

}

SSB-MTC4-r17 ::= SEQUENCE {

pci-List-r17 SEQUENCE (SIZE (1..maxNrofPCIsPerSMTC)) OF PhysCellId OPTIONAL, -- Need R

offset-r17 INTEGER (0..159)

}

-- Editor's note: UE assistance information for SMTC/MG could be captured, and the content is FFS

SSB-MTC-AdditionalPCI-r17 ::= SEQUENCE {

additionalPCIIndex-r17 AdditionalPCIIndex-r17,

additionalPCI-r17 PhysCellId,

periodicity-r17 ENUMERATED { ms5, ms10, ms20, ms40, ms80, ms160, spare2, spare1 } OPTIONAL, -- Need S

ssb-PositionsInBurst-r17 CHOICE {

shortBitmap BIT STRING (SIZE (4)),

mediumBitmap BIT STRING (SIZE (8)),

longBitmap BIT STRING (SIZE (64))

},

ss-PBCH-BlockPower-r17 INTEGER (-60..50)

}

--Editor's note: more RAN1 input may be coming for this IE

AdditionalPCIIndex-r17 ::= INTEGER(1..maxNrofAdditionalPCI-r17)

-- TAG-SSB-MTC-STOP

-- ASN1STOP