**3GPP TSG-RAN WG2 Meeting #116 electronic** [**R2-2111311**](https://www.3gpp.org/ftp/TSG_RAN/WG2_RL2/TSGR2_116-e/Docs/R2-2111311.zip)

**Online, Nov. 1st – Nov. 12th, 2021**

**Agenda Item: 8.2.4**

**Source: OPPO**

**Title: [AT116-e][220][R17 DCCA] TRS-based Scell activation details (OPPO)**

**Document for: Discussion and decision**

# Introduction

This paper is to trigger the following email discussion of TRS based SCell activation in RAN2#116e.

* [AT116-e][220][R17 DCCA] TRS-based Scell activation details (OPPO)

Scope:

* + - Discuss remaining RAN2 aspects on of TRS-based SCell activation based on online discussion.

Intended outcome:

* + - Discussion summary in [R2-2111311](https://www.3gpp.org/ftp/TSG_RAN/WG2_RL2/TSGR2_116-e/Docs/R2-2111311.zip) (by email rapporteur).

Deadline for providing comments, for rapporteur inputs, conclusions and CR finalization:

* + - Initial deadline (for company feedback): 1st week Fri, UTC 0900
    - Initial deadline (for rapporteur summary): 2nd week Mon, UTC 1000

The following agreements for TRS based SCell activation are listed below:

* 1: For TRS based SCell activation, RAN2 finalizes the MAC CE based SCell activation case first and come back on RRC case if time allows.
* 2: The TRS can be activated for fast SCell activation, only when all following conditions are met:
* (a) The TRS for SCell activation is configured for this SCell;
* (b) The SCell is activated from deactivated state by New SCell A/D MAC CE;
* (c) The BWP indicated by firstActiveDownlinkBWP-Id is not dormant BWP;
* FFS how we handle the case when some Scells use TRS and some don't
* RAN2 will not specify UE behaviour for the case when new MAC CE is used but a)+c) are not fulfilled for the SCell that uses TRS
* 3: One new MAC CE for to trigger both SCell activation and corresponding temporary RS.
* 4: Define 2 eLCIDs for new MAC CEs with “one octet” SCell activation indication and with “four octet” SCell activation indication respectively.
* Discuss MAC CE structure in offline [220] (OPPO) based on concrete TPs. Should try to converge to a RAN2 proposal. Can discuss if we need to send LS to RAN4 on RAN2 decisions on TRS-based SCell activation.
* Wait for RAN1 input on RRC parameters and capabilities

**Contact Information**

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# Discussion

Based on RAN1 agreements in RAN1#106bis-e, there are two alternatives to define the MAC CE for TRS activation part.

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| Alt 1: Bitmap approach in MAC-CE   * Every Z-bit block in the bitmap corresponds to a SCell, Z>=0 * A Z-bit block indicates the temporary RS [configuration index], and a value zero indicated by the bit block means no RS resource transmitted. * The to-be-activated SCell is indicated via the C values in the legacy SCell activation/de-activation MAC CE or in the new MAC-CE   Alt 2: Reuse A-TRS triggering framework   * A trigger state is indicated by the MAC-CE explicitly * The association between a trigger state and temporary RS for one or multiple SCells is configured by RRC according Rel-16 A-TRS triggering framework * FFS: The value zero of the MAC-CE indication means no temporary RS is triggered by the MAC-CE for all to-be-activated SCells |

According to RAN1 discussion, a list of TRS configuration will be configured per SCell in both Alt1 an Alt2 [1]. For Alt2, the extra TRS trigger state list will be configured [1].

For Alt2, it is not clear how many IEs can be resued and how many IEs expecially madataory IEs will be ignored by TRS. It is not one hundred percent resue from RRC signalling point of view. The MAC CE, i.e. Aperiodic CSI Trigger State Subselection MAC CE, is used to do sub-selection from RRC configured Aperiodic CSI Trigger State, e.g. at most 8 states will be activated via MAC CE, and the DCI will indicate the last triggered Aperiodic CSI Trigger State. However, the new MAC CE for TRS activation will only include one activated state for TRS activation. So the MAC CE is also not same as legacy.

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| 6.1.3.13 Aperiodic CSI Trigger State Subselection MAC CE The Aperiodic CSI Trigger State Subselection MAC CE is identified by a MAC subheader with LCID as specified in Table 6.2.1-1. It has a variable size consisting of following fields:  ===omit some text==== |

RAN2 agreed to use new MAC CE for both SCell activation/deactivation and corresponding TRS activation. RAN2 futher defined two eLCID for new MAC CE with “one octet” SCell activation indication and with “four octet” SCell activation indication respectively.

In [1][4][5][6][7], companies provide the opinion for the Alt1 VS Alt2. The observations are summarized based on the 4 company papers.

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| **Alternatives** | **Comments** | **Observations** |
| Alt 1: Bitmap approach in MAC-CE | The MAC CE will include temporary RS index for each SCell.   * The MAC CE size is variable up to the number of SCell with TRS activation in one MAC CE. | * No need of pre-configuration for TRS trigger state list in RRC signaling. * The signaling overhead of MAC CE is variable and is low usually depends on the number of SCell with TRS activation (i.e. the SCell is configured with TRS and the SCell is activated from deactivation) in one MAC CE. * The SCell activation/deactivation part is bitmap style and the TRS acativation also use bitmap style to align with SCell A/D part in one MAC CE. |
| Alt 2: Reuse A-TRS triggering framework | The MAC CE will include temporary RS trigger state index for UE, and the temporary RS trigger state index refers to the entry number in list of TRS trigger state configuration. Each state will contain each SCell’s TRS trigger state and which TRS is triggered.   * The TRS trigger state index will be included according to RRC configuration. | * The RRC needs to configure the list of temporary RS trigger state. The network should ensure to configure all possible case of TRS trigger of each SCell and each TRS in one Scell，otherwise, the flexibility for TRS configuration for SCell and TRS activation will be lost. The RRC signaling overhead is huge. * the temporary RS trigger state index will be bigger no matter the number of SCell with TRS activation in one MAC CE. The MAC CE size will be always high even if there is only one SCell is activated with TRS activation. * RAN1 should be involved to decide the field size of temporary RS trigger state index and RAN1 did not discuss it yet. * The style of TRS activatation is not aligned with SCell A/D part in one MAC CE. |

**Q1: Which Alternative do companies prefer for TRS activation part in the new MAC CE?**

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| Company | Alt 1/2? | Comments |
| OPPO | Alt1 | For Alt 1, the size of TRS activation in MAC CE is variable, e.g. there are 7 SCells configured for UE and 2 bits for TRS index. If the number of SCells with TRS activation <=4, then one octet is enough for TRS activation. If the number of SCells with TRS activation >4, then at most two octets are enough for TRS activation. E.g. only the SCell is activated from deactivated state and configured with TRS, its TRS index will be present in MAC CE.  For Alt2, first RRC signaling will configure each TRS trigger state index with possible SCell activation and possible TRS activation for each SCell, e.g. there are 7 SCell and 4 TRS in each SCell. The number of possible cases will be 78124, then 17bit (3 octets) will be needed in MAC CE. Alt 2 will use more octet than Alt 1. Even if there is only one SCell’ TRS activation, the TRS activation will always use 3 octets, the field size of TRS trigger state index is based on RRC configuration.  Some companies may argue that not all possibilities will be configured. If so, my question is which possibility will be omitted and then the flexibility for TRS configuration for SCell and TRS activation will be lost. Furthermore, we consider MAC overhead and should also consider RRC overhead. It is obvious that the overhead in RRC for Alt2 is huge and it is complex for both network and UE.  If RAN2 choose Alt 2, RAN1 should be involved to decide the field size of temporary RS trigger state index in MAC CE and this is not discussed in RAN1 yet. Alt 2 leaves more open issues in RAN1 than Alt1.  RAN2 should also note that SCell activation part in new MAC CE is based on bitmap style and it is straightforward to design TRS activation part based on bitmap style in new MAC CE also. |
| vivo | Alt 1 | Above all, we prefer variable-sized new MAC CE for the case.  With variable-sized new MAC CE, the network is able to configure all possible cases for all SCell activation/deactivation without causing much burden in the MAC CE, since it is likely that network will activate TRS for only a few to-be-activated SCells for which the network configures TRS. Therefore, alt 1 is not necessarily deteriorating heavily in the MAC CE size compared to alt 2.  The only good performance scheme for alt 2 is introducing only 1 octet for TRS activation part, which can only indicate 256 possible combinations at most. We do not think this can satisfy the actual need for flexible TRS configuration. If more than 1 octet is used for TRS activation part for alt 2, e.g. 2 octets, the network needs to configure at most 65536 entries in the TRS trigger state configuration list. In this case, though network flexibility might be guaranteed, but the additional burden introduced in RRC configuration does not seem to compensate the gain in saving bits for the new MAC CE.  Besides, if there is any possible case that is not included in the configured TRS trigger state configuration list for alt 2, the network needs to update the configuration. This leads to potential network signalling burden.  In conclusion, variable-sized MAC CE design for alt 1 is a better choice. |
| Jarkko | Alt2 | Firstly RRC signaling should not be deciding factor as ASN.1 is simple. Then To us it seems main difference between options is that do we signal index per SCell or common index for all cells.  It seems obvious that common index for all cells is most optimal way to signal the index as if we have index per SCell then there will always be unused codepoints in each SCell but with common index there will only be unused codepoints in on index.  So it seem obvious that alt2 is much more optimal.  In the OPPOs comment one only has 4 options per SCell but if one would need more for any one cell then one would need more index values for all the cells? Or is this correct understanding? If the index length is variable then definitely we should go for al2 to get something out of this WI. |
| ZTE | Alt2 | Why proponents of Alt 1 think network would like to configure 65536 combinations...128 is already an amazing number!  We support Alt 2 because: (same comments are provided during POST email disc)   1. Alt 2 needs less specification effort, because it reuses the existing A-TRS trigger state mechanism, so the defined parameters can be reused mostly (e.g. CSI-AperiodicTriggerStateList).   Alt 1 causes more signalling overhead in MAC CE, because each SCell will be mapped to Z-bits. But Alt 2 only requires few bits in MAC CE (e.g. 7 bits can represent 128 trigger states) |
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Based on RAN1#106e agreements, RAN1 agreed that following parameters are configured for temporary RS in RRC signanling.

* The number of temporary RS bursts;
* gap length between the RS bursts;
* The candidate value(s) of triggering offset(s);
* A list of temporary RS;

According RAN1 discussion and conlusion (refer to the figure 1 and 2), it is common understanding that the above parameters are per TRS configured and a list of TRS configuration is configured per SCell. It is also common understanding that only TRS index for one SCell will be included in new MAC CE. RAN1 also agreed that TRX index 0 will indecate no TRS activation even if the SCell is configured with TRS and the SCell is also activated from deactivated state, e.g. there is SSB nearby and no need to trigger TRS.

In RAN2 online discussion, there is FFS:

*FFS how we handle the case when some Scells use TRS and some don't.*

In my understanding, the SCell is optionally configured with TRS. If the TRS is configured, then the TRS may be triggered when SCell is activated from deactivation state in new MAC CE, e.g. there is SSB nearby. If the TRS is not triggetred the network will set TRS index 0. If the SCell is not configured with TRS or the TRS is nsot activated for this SCe, then the UE will follow the legacy behavior for this SCell.

**Rapporteur’s understanding for Alt1:**

* **Only when the SCell is configured with TRS and the SCell is activated from deactivated state, the corresponding TRS index of this SCell will be present in new MAC CE.**
* **Only when the SCell is configured with TRS and the SCell is activated from deactivated state, the TRS may be activated in new MAC CE (i.e. TRS index 0 indicate TRS is not activated, otherwise TRS is activated.).**
* **The TRS index of each SCell is ascending order of the SCell index.**
* **If the TRS of one SCell is not activated or the SCell is not configured with TRS, the UE follow legacy behavior as recevei leagay SCell A/D MAC CE.**

**Q2: Do companies agree the rapporteur’s understanding for Alt1?**

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| Company | Yes/No? | Comments |
| OPPO | Yes |  |
| vivo | Yes with comments | There is some wording ambitugity, so we suggest to clarify the understanding as following:  **Rapporteur’s understanding for Alt1:**   * **Only when the SCell is configured with TRS and the SCell is activated from deactivated state, the corresponding TRS index field of this SCell will be present in new MAC CE.** * **Only when the SCell is configured with TRS and the SCell is activated from deactivated state, the TRS may be activated in new MAC CE (i.e. TRS index field value ‘0’ indicate TRS is not activated, otherwise TRS is activated.).** * **The TRS index field of each SCell is in ascending order of the SCell index field.** * **If the TRS of one SCell is not activated or the SCell is not configured with TRS, i.e. the corresponding TRS index field is absent of this SCell in new MAC CE, the UE follow legacy behavior as receiving legacy SCell A/D MAC CE.** |
| Nokia | Question | If the SCell is configured in RRC with TRS but network does not want to activate TRS for that SCell then how the MAC CE looks like? Is ther index codepoint for the SCell indicating no TRS is activated? |
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For Alt2, a list of TRS trigger state will be pre-configured in RRC siganlling. And only one TRS state id will be included in MAC CE for all SCells. However, it is not clear how to define the field size of TRS trigger state in new MAC CE.

**Rapporteur’s understanding for Alt1:**

* **Only one TRS trigger state id is included for all SCells.**
* **The field size will be up to RAN1 and others open issues is up to RAN1 to identify.**

**Q3: Do companies agree the rapporteur’s understanding for Alt2?**

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| Company | Yes/No? | Comments |
| OPPO | Yes |  |
| vivo | Yes |  |
| Nokia | No | Why would the size be up to RAN1? Isn’t this RAN2 aspects to discuss? RAN1 needs to indicate fields and value ranges and RAN2 should have sufficient amount of index value(s) which should be naturally sized so that MAC CE is octet aligned (could be even RRC configurable) |
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**Q4: Any other open issues need to confirm?**

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RAN4 will define the requirement for TRS based SCell activation, e.g. the timeline of the new MAC CE. So it is necessary to let RAN4 know RAN2 decision about TRS based SCell activation. For RAN1, the size of TRS index is up to RAN1 to decide if Alt1 is chosen and the field size of TRS trigger state id is up to RAN1 to decide if Alt2 is chosen.

**Q5: Do companies agree to send LS to RAN4/1 to include the following agrements and questions from RSN2 side?**

* **RAN2 agree to define one new MAC CE for both SCell A/D and corresponding TRS activation indiction. After the reception of the new MAC CE, UE will follow legacy behaviour for some SCells (i.e. without TRS activation)and UE will follow new behaviouir defined in 38.321CR for other SCells (with TRS activtion).**
* **For TRS activation part, RAN2 decide to use Alt1/2(TBD) and ask RAN1 to define the RRC parameters for TRS based SCell actiovation, i.e. the parameters and corresponding value scope.**

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| Company | Yes/No? | Comments |
| OPPO | Yes | For RAN4, the LS will help RAN4 to start their work.  For RAN1, the LS will help RAN1 to focus the part RAN1 should decide. |
| vivo | Yes, and | We suggest to send LS to RAN1/4 to discuss and determine the maximum number of Temporary RS Configurations that is actually needed for one SCell.  For alt 1, this will only affect the size of the MAC CE.  For alt 2, more issue may arise, e.g., if there are too many possible TRS configurations for one SCell, it seems alt 2 cannot work well with enough flexibility due to limited size of the TRS trigger state configuration list. |
| Nokia | Not sure (likely yes) | MAC CE should be able to activate SCells without activating TRS for some and activating it for some SCells. Why would we need any LS to RAN1. Isn’t it obvious that RAN2 defines solution? |
| ZTE | Prefer no | For the first bullet, when RAN4 specifies the UE requirements, we think they does not care whether old or new MAC CE is used. And the case that some SCells are activated, some are not in one MAC CE is RAN2 issue, we think RAN4 does not need to capture this scenario in their spec.  For the second bullet, if the intention is to ask RAN1 to define RRC parameters, maybe there is no needed, anyway, RAN1 will send required parameters list to RAN2, and they will check the progress in RAN2 if needed. |
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# Conclusions

Based on the discussion above, we propose:

# Reference

[1] R2-2109472 Discussion on TRS activation for fast SCell activation OPPO discussion Rel-17 LTE\_NR\_DC\_enh2-Core

[2] R2-2109473 Email report of [Post115-e][218][R17 DCCA] TRS-based SCell activation (OPPO) OPPO discussion Rel-17 LTE\_NR\_DC\_enh2-Core

[3] R2-2109657 Introduction of TRS based SCell activation OPPO CR Rel-17 38.321 16.6.0 1164 - B LTE\_NR\_DC\_enh2-Core

[4] R2-2110556 Temporary RS activation Nokia, Nokia Shanghai Bell discussion Rel-17 LTE\_NR\_DC\_enh2-Core

[5] R2-2110875 Temporary RS based fast SCell activation Huawei, HiSilicon discussion LTE\_NR\_DC\_enh2-Core

[6] R2-2110910 Discussion on support of Temporary RS for SCell activation Futurewei discussion Rel-17 LTE\_NR\_DC\_enh2-Core

[7]R2-2111201 Discussion on Temporary RS activation for fast SCell activation vivo discussion Rel-17 LTE\_NR\_DC\_enh2-Core R2-2110505