3GPP TSG-RAN WG2 #114-e electronic R2-210xxxx

Electronic Meeting, 19th – 27th May, 2021

Agenda Item: 8.17.1

Source: Intel Corporation

Title: [AT114-e][035][feMIMO] TCI states indication for PDCCH (Intel)

Document for: Discussion, Decision

# 1 Introduction

This contribution summarizes the following discussion:

* [AT114-e][035][feMIMO] TCI states indication for PDCCH (Intel)

      Scope: Treat R2-2104712 and the related submitted tdocs.

      Discuss the topic, attempt to make some basic agreements, e.g. agree to have the requested MAC CE, and potentially identify FFS.

      Intended outcome: Report

      Deadline: Monday May 24 for on-line CB

Contact person(s) for each participating company:

|  |  |  |
| --- | --- | --- |
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# 2 Discussion

RAN1 sent an LS [1] to inform RAN1 agreement on PDCCH enhancement. In this LS, RAN1 agreed to introduce enhanced MAC CE ignalling for PDCCH activating two TCI states for SFN-based PDCCH transmission.

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| --- |
| **Agreement**   * Introduce enhanced MAC CE signaling for PDCCH activating two TCI states for SFN-based PDCCH transmission   + The corresponding MAC CE includes at least the following fields     - Serving cell ID     - CORESET ID     - Two TCI state IDs   + FFS whether for CA scenario additionally support RRC configured set of the serving cells which can be addressed by a single MAC CE   + FFS whether or not enhanced MAC CE signaling is applicable to a CORESET configured with CORESETPoolindex |

All contributions [2-5] seem to agree that the existing TCI State Indication for UE-specific PDCCH MAC CE is not enough.

**Q1: Do you agree that the exsiting MAC CE is not sufficient to support Rel-17 PDCCH enhancement and therefore we should introduce enhanced MAC CE?**

|  |  |  |
| --- | --- | --- |
| Company | Yes/No | Comments |
| Intel | Yes |  |
| ZTE | Yes | The current MAC CE carry only one TCI state information for the PDCCH. |
| LG | Yes |  |
| Xiaomi | Yes |  |
| Lenovo&MM | Yes |  |
| OPPO | Yes |  |
| CATT | Yes |  |

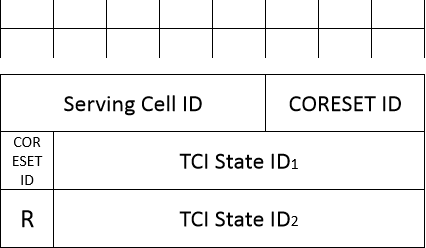
RAN1 requested to include the following fields 1) serving cell ID, 2) CORESET ID, 3) Two TCI state IDs.

**Q2: Do you agree that the enhanced MAC CE should include the following fields 1) serving cell ID, 2) CORESET ID and 3) Two TCI state IDs?**

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| --- | --- | --- |
| Company | Yes/No | Comments |
| Intel | Yes |  |
| ZTE | Yes |  |
| LG | Yes |  |
| Xiaomi | Yes |  |
| Lenovo&MM | Yes |  |
| OPPO | Yes |  |
| CATT | Yes |  |

Three companies provide the possible enhanced MAC CE structure. Two of them ([2,4]) are the same format, while the other [5] is slightly different. However, there seems no big difference. Is there any preference between two formats?

**Q3: Which MAC CE strcture is preferred?**

Option 1 [2,4] Option 2 [5]

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| --- | --- | --- |
| Company | Preference | Comments |
| Intel | Either one is ok. |  |
| ZTE | Either one is Okay |  |
| LG | Option 1 | We think both options work, but we prefer to simply add 1byte of new field after the existing format. |
| Xiaomi | Either one is ok | Although we are the proponent of Option 2, Option 1 is also acceptable to us. With the R bit at the beginning of the MAC CE, the MAC CE would be more future extentable. |
| Lenovo&MM | Either one is fine. | If more TCI state should be added e.g. 3 TCI state, option 1 is easy to extend. |
| OPPO | Either one is Ok. |  |
| CATT | Either one is ok. |  |

There are some views that RAN2 should ask RAN1 on some questions to clarify [4,5].

1. Whether the enhanced TCI state indication for UE specific PDCCH MAC CE can be applied to a set of serving cells configured in simultaneousTCI-UpdateList1 or simultaneousTCI-UpdateList2? [4]
2. Which CORESET can be indicated with two TCI states ? [5]
3. How many TCI states (i.e. maximum number) can be configured for the CORESET indicated with two TCI states? [5]
4. Anything else?

**Q4: Do you agree to send LS to aks RAN1 some questions? If yes, are the above question A-C reasonable to ask? Companies are also invited to provide more questions if deemed useful.**

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| --- | --- | --- |
| Company | Yes/No | Comments |
| Intel | No | Question A: This issue is currently captured as FFS bullet in RAN1 LS [1].  Question B: we understand that it should not be applicable to CORESET 0 similar to Rel-15 MAC CE design.  Question C: There is no proposal in RAN1 to increase the number of TCI states to larger value comparing to Rel-15. |
| ZTE | No | Question A: Agree with Intel  Question B: Regarding the comments from Intel, it seems CORESET0 is supported by this MAC CE as shown below  - CORESET ID: This field indicates a Control Resource Set identified with *ControlResourceSetId* as specified in TS 38.331 [5], for which the TCI State is being indicated. In case the value of the field is 0, the field refers to the Control Resource Set configured by *controlResourceSetZero* as specified in TS 38.331 [5]. The length of the field is 4 bits;  In our understanding, all the CORESET including CORESET0 can be indicated by this MAC CE as Rel15, no need to ask the question.  Question C: Agree with Intel  In addition to above three questions, we think there is one question D is supposed to be asked to RAN1:  In rel-15, the first 64 entries of the tci-States-ToAddModList can be applied to CORESET 0 while up to 128 entries of the tci-States-ToAddModList can be applied to the CORESET other than CORESET 0. we would like to ask whether this rule is still available for the newly introduced MAC CE? |
| LG | No | We have same understanding with Intel on Question A.  Regarding Question B and C, if there is no additional request from RAN1, we think that RAN2 can go with same way as legacy. |
| Xiaomi | B. C. | Question A is already part of the RAN1 feMIMO discussion.  For Question B and C, we think that which CORESET can be configured should be up to RAN1 to decided. Even though companies consider that we should allow CORESET#0 as legacy, the RRC configuration of TCI state for CORESET#0 still needs to be provided by RAN1. We just hope companies can keep this in mind that the CORESET configuration details should be up to RAN1 to decided, RAN2 should not make any assumption based on the old MAC CE. |
| Lenovo&MM | No | Question A: RAN1 is discussins this.  Question B: RAN1 will discuss whether two TCI states are applied to CORESET 0.  Question C: Ageee with Intel. |
| OPPO | No | Question A: The discussion on whether to support group-based TCI state indication for UE specific PDCCH is ongoing in RAN1, we can wait for their agreement on that.  Question B: Agree with ZTE. TCI states indication for coreset 0 by MAC CE is supported in legacy spec, that is, all of the coresets can be indicated with two TCI states.  Question C: Agree with Intel, the number of TCI states shall keep as legacy. |
| CATT | No |  |

**Q5: Is there any aspect that RAN2 needs to discuss?**

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| Company | Comments |
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# 3 Conclusion

To be updated.

# 4 References

1. R2-2104712 LS on TCI states indication for PDCCH (R1-2104064; contact: Intel) RAN1 LS in Rel-17 NR\_feMIMO-Core To:RAN2
2. R2-2105027 Enhanced MAC CE for PDCCH in multi-TRP deployment Intel Corporation discussion Rel-17 NR\_feMIMO
3. R2-2105907 On the LS about Activating two TCI states with a MAC CE Ericsson discussion NR\_feMIMO-Core
4. R2-2105858 Consideration on the enhanced TCI state indication MAC CE for PDCCH ZTE, Sanechips discussion Rel-17 NR\_feMIMO-Core
5. R2-2105731 Enhanced TCI State Indication for UE-specific PDCCH MAC CE Xiaomi Communications discussion Rel-17 NR\_feMIMO-Core