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Title: **Discussion on timing relation of HSDPA**

Document for: **Discussion**

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1. Introduction

This document discusses the timing relation of HSDPA. We compared four combinations of the way of transmitting TFCI information and TTI length. From the result, we propose following.

1. UE always receive TFCI shared channel [1]. This is said one step approach. Although this increase UE power consumption, this can increase UE processing time and NodeB scheduler processing time.

2. We propose 1 slot TTI length. This makes processing time longer. This can also decrease UE power consumption when UE receive HS-DSCH channel by FHT despreading [2].

We think to have enough processing time to NodeB and UE is essential to realize HSDPA system.

2. Timing relation comparison

We compared four combinations in following conditions.

- The time between first transmission and second transmission is 18 slots. This timing relation comes from 3 slots TTI and 6 sub-channels SAW [3]

- DPCH and HS-DSCH has a flexible timing offset i.e. slot boundary is not aligned each other.

- Uplink ACK/NACK is transmitted on uplink DPCH. This is transmitted in one slot length.

- If shared channel for TFCI is used, this information is transmitted over one slot length.

- Node B scheduler are worked based on HS-DSCH timing.

Table 1 shows the four combinations.

Table 1 Condition of four methods.

	TFCI is sent on	Is UE signalled on existence of TFCI shared channel?	HS-DSCH TTI
Combination1	Shared	Yes. UE always receive only DPCH. DPCH tells UE to receive shared TFCI channel. (2 step approach)	3slot
Combination2	Shared	No. UE always receive DPCH and shared TFCI channel. (1 step approach)	3slot
Combination3	Dedicated	-	3slot
Combination4	Shared	No. UE always receive DPCH and shared TFCI channel. (1 step approach)	1slot

Table 2 compares four processing time of each combination. UE and NodeB processing time can adjust by such way of that UE get one more slot, NodeB lost one slot of processing time. We assigned each processing time based our assumption of each complexity. Annex shows timing relation figures.

Table 2 Processing time comparisons of four combinations

	UE HSDSCH decoding time	NodeB scheduler processing time	UE DPCH flag decoding time	UE TFCI decoding time
Combination1	4 slot	2 slot - Tprop	2 slot	2 slot
Combination2	6 slot	3 slot - Tprop	-	3 slot
Combination3	5 slot	3 slot - Tprop	-	3 slot
Combination4	7 slot	4 slot - Tprop	-	3 slot

Tprop is the propagation time.

Discussion

- Two-step approach cannot assign enough time in 18 slot timing relation. We think 4slot for UE decoding is too short and the other processing is only two slots is too short. This comes from UE DPCH flag decoding time and following DPCH and HS-DSCH timing relation.

- Timing flexibility between DPCH and HS-DSCH tighten UE and NodeB processing time. One-step approach is not related with downlink DPCH timing. This can change Node B processing time minimum 3 slots to always 3 slots. We assigned this margin for UE processing time.

- To change 3 slot TTI to 1 slot TTI give another two slots margin. We assigned this margin for UE processing time and NodeB scheduler time in above table. As discussed in [1], WHT can reduce the multi code complexity and despread all the codes at the same time. One slot approach fit this method for keeping data granularity small. Another possibility of using two-slot margin in one slot TTI is to reduce the time for retransmission to one frame length. If UE processing time reduces to 5 slot and Node B scheduler processing time reduce to (3slot - Tprop), time required for the retransmission is 15-slot length. This may simplify the relation between release 99 function but this requires further study.

3. Conclusion

We propose following.

1. UE always receive TFCI shared channel. This is said one step approach. This can increase UE processing time and NodeB scheduler processing time.

2. We propose 1 slot TTI length. This also makes processing time longer.

4. Reference

[1] RAN 1 RAN 2 Joint Ad-Hoc Meeting on HSDPA, 12A010029, Discussion on TFCI for E-DSCH, Panasonic

[2] RAN1#20, R1-01-0499, Discussion on UE capability of HSDPA, Panasonic

[3] RAN 1 RAN 2 Joint Ad-Hoc Meeting on HSDPA, 12A010003, Further buffer complexity and processing time considerations on HARQ, Nokia

A. Annex

Following are the timing relation figures of each combination.

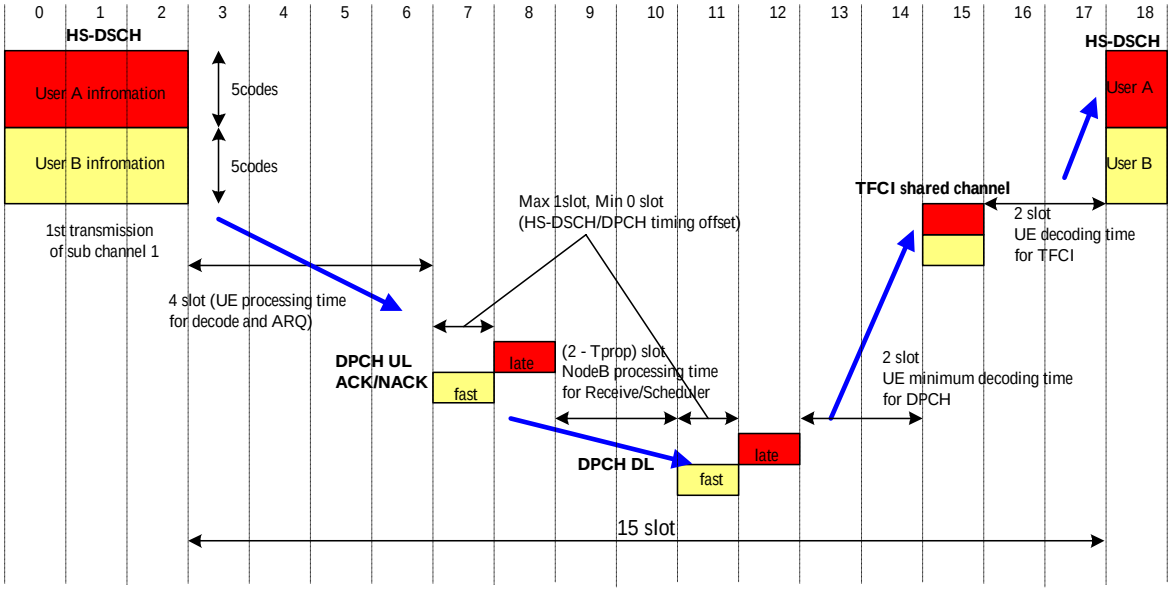

Figure 1. Combination 1

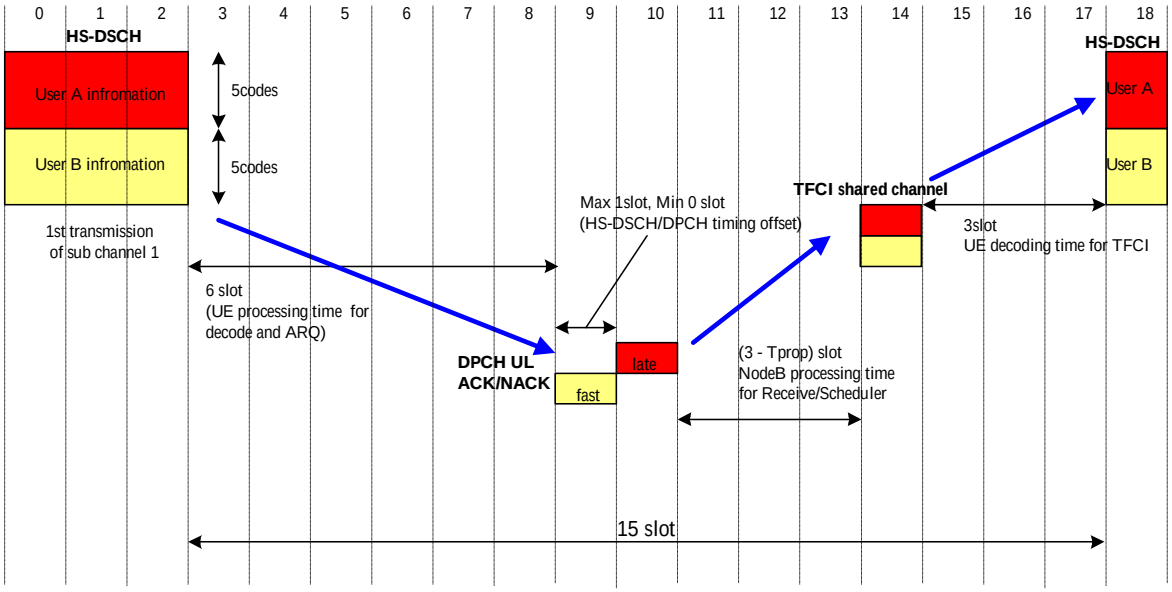

Figure 2. Combination 2

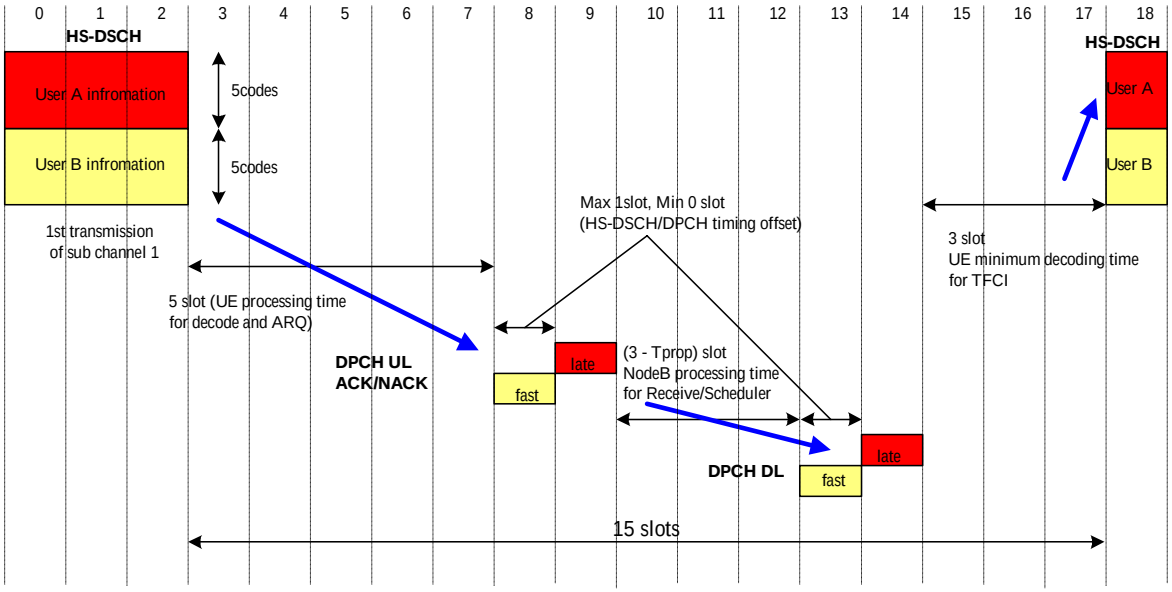

Figure 3. Combination 3

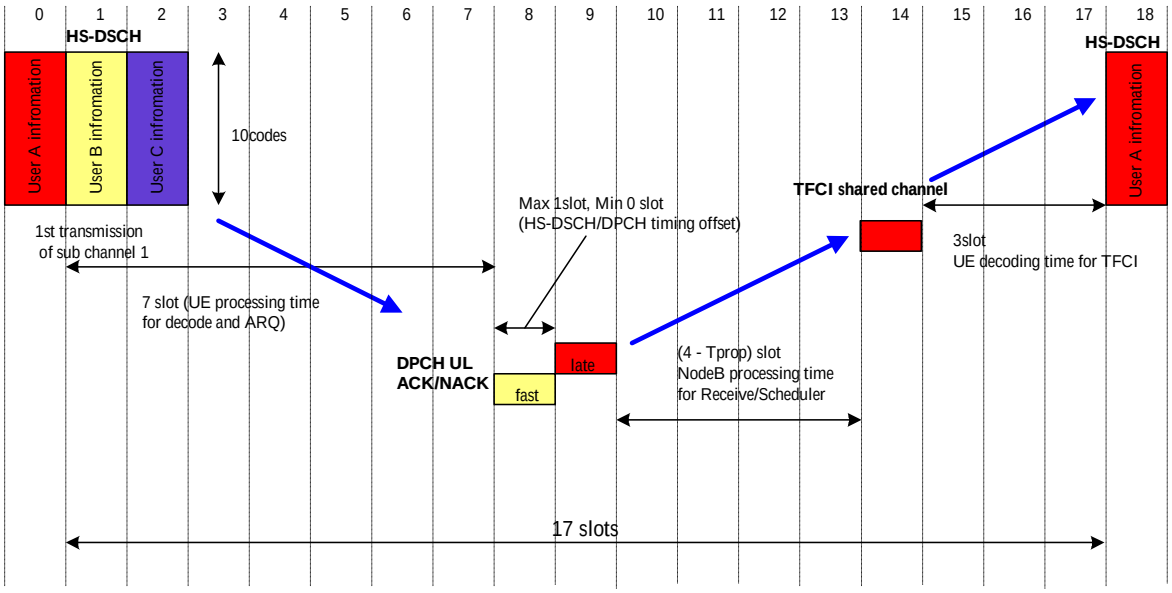

Figure 4. Combination 4