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CHANGE REQUEST

✍ **25.221** CR **43** ✍ rev **1** ✍ Current version: **3.5.0** ✍

*For **HELP** on using this form, see bottom of this page or look at the pop-up text over the ✍ symbols.*

Proposed change affects: ✍ (U)SIM ☐ ME/UE **X** Radio Access Network **X** Core Network ☐

Title: ✍	Inclusion of 1.28Mcps TDD in TS 25.221	
Source: ✍	Siemens, CWTS, CATT	
Work item code: ✍ LCRTDD		***Date:*** ✍ 28.02.2001
Category: ✍ **B**		***Release:*** ✍ REL-4

Use *one* of the following categories:
   F *(essential correction)*
   A *(corresponds to a correction in an earlier release)*
   B *(Addition of feature),*
   C *(Functional modification of feature)*
   D *(Editorial modification)*
Detailed explanations of the above categories can
be found in 3GPP TR 21.900.

Use *one* of the following releases:
   2   (GSM Phase 2)
   R96 (Release 1996)
   R97 (Release 1997)
   R98 (Release 1998)
   R99 (Release 1999)
   REL-4 (Release 4)
   REL-5 (Release 5)

Reason for change: ✍	Inclusion of 1.28 Mcps TDD
Summary of change: ✍	?? The basis for this document was CR0043, R1-01-0221 ?? inclusion of contributions approved at WG1#19
Consequences if not approved: ✍	

Clauses affected: ✍	3, 5, new section 6, 7, new section 8, new Annex B, new Annex D, new Annex G, new Annex H
Other specs Affected: ✍	**X** Other core specifications ✍ 25.201, 25.222, 25.223, 25.224, 25.225 ☐ Test specifications ☐ O&M Specifications
Other comments: ✍	

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3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

BCH	Broadcast Channel
CCPCH	Common Control Physical Channel
CCTrCH	Coded Composite Transport Channel
CDMA	Code Division Multiple Access
DPCH	Dedicated Physical Channel
DRX	Discontinuous Reception
DSCH	Downlink Shared Channel
DwPCH	Downlink Pilot Channel
DwPTS	Downlink Pilot Time Slot
FACH	Forward Access Channel
FDD	Frequency Division Duplex
FEC	Forward Error Correction
GP	Guard Period
GSM	Global System for Mobile Communication
MIB	Master Information Block
NRT	Non-Real Time
OVSF	Orthogonal Variable Spreading Factor
P-CCPCH	Primary CCPCH
PCH	Paging Channel
PDSCH	Physical Downlink Shared Channel
PI	Paging Indicator (value calculated by higher layers)
PICH	Page Indicator Channel
P_q	Paging Indicator (indicator set by physical layer)
PRACH	Physical Random Access Channel
PUSCH	Physical Uplink Shared Channel
RACH	Random Access Channel
RF	Radio Frame
RT	Real Time
S-CCPCH	Secondary CCPCH
SCH	Synchronisation Channel
SFN	Cell System Frame Number
TCH	Traffic Channel
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
TrCH	Transport Channel
UE	User Equipment
UpPTS	Uplink Pilot Time Slot
UpPCH	Uplink Pilot Channel
USCH	Uplink Shared Channel

5 Physical channels for the 3.84 Mcps option

5.6.1.2.2 Common Midamble

The use of the common midamble allocation scheme is signalled to the UE by higher layers as a part of the physical channel configuration. A common midamble may be assigned by layer 1 to all physical channels in one DL time slot, if:

- a single UE uses all physical channels in one DL time slot (as in the case of high rate service);

or

- multiple UEs use the physical channels in one DL time slot; and

- no beamforming is applied to any of these DL physical channels; and

- no closed loop TxDiversity is applied to any of these DL physical channels; and

- midambles are not used for PDSCH physical layer signalling.

The number of channelisation codes currently employed in the DL time slot is associated with the use of a particular common midamble. Different associations apply for different burst types and cell configurations with respect to the maximum number of midambles, see annex BC.

6 Physical channels for the 1.28 Mcps option

All physical channels take three-layer structure with respect to timeslots, radio frames and system frame numbering (SFN), see [14]. Depending on the resource allocation, the configuration of radio frames or timeslots becomes different. All physical channels need guard symbols in every timeslot. The time slots are used in the sense of a TDMA component to separate different user signals in the time and the code domain. The physical channel signal format for 1.28Mcps TDD is presented in figure [19].

A physical channel in TDD is a burst, which is transmitted in a particular timeslot within allocated Radio Frames. The allocation can be continuous, i.e. the time slot in every frame is allocated to the physical channel or discontinuous, i.e. the time slot in a subset of all frames is allocated only. A burst is the combination of a data part, a midamble and a guard period. The duration of a burst is one time slot. Several bursts can be transmitted at the same time from one transmitter. In this case, the data part must use different OVSF channelisation codes, but the same scrambling code. The midamble part has to use the same basic midamble code, but can use different midambles.
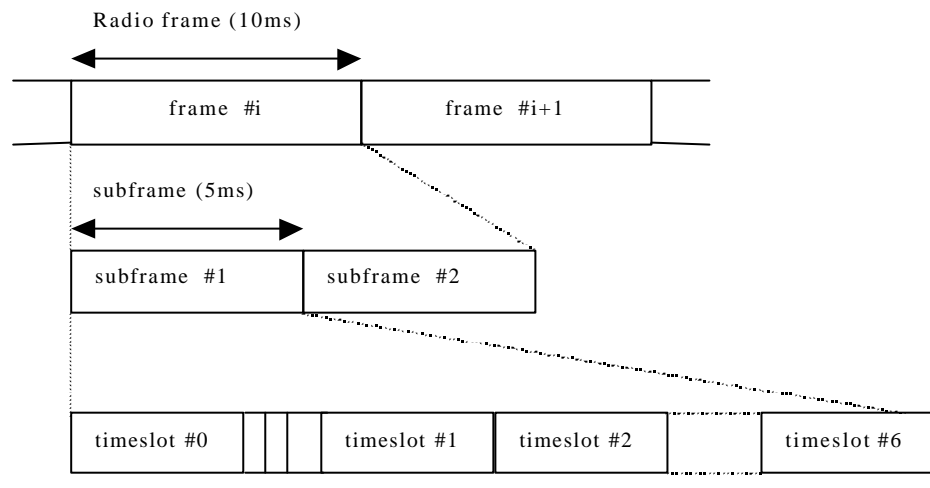

Figure [19]: Physical channel signal format for 1.28Mcps TDD option

The data part of the burst is spread with a combination of channelisation code and scrambling code. The channelisation code is a OVSF code, that can have a spreading factor of 1, 2, 4, 8, or 16. The data rate of the physical channel is depending on the used spreading factor of the used OVSF code.

So a physical channel is defined by frequency, timeslot, channelisation code, burst type and Radio Frame allocation The scrambling code and the basic midamble code are broadcast and may be constant within a cell. When a physical channel is established, a start frame is given. The physical channels can either be of infinite duration, or a duration for the allocation can be defined.

6.1 Frame structure

The TDMA frame has a duration of 10 ms and is divided into 2 sub-frames of 5ms. The frame structure for each sub-frame in the 10ms frame length is the same.
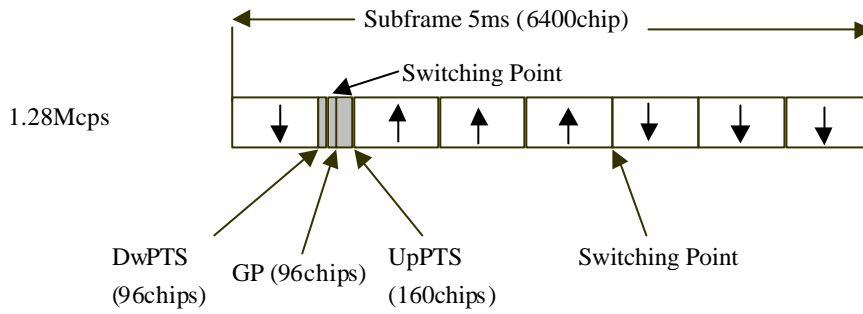
Figure [20]: Structure of the sub-frame for 1.28Mcps TDD option

Time slot#n (n from 0 to 6): the nth traffic time slot, 864 chips duration;
DwPTS: downlink pilot time slot, 96 chips duration;
UpPTS: uplink pilot time slot, 160 chips duration;
GP: main guard period for TDD operation, 96 chips duration;

In Figure [20], the total number of traffic time slots for uplink and downlink is 7, and the length for each traffic time slot is 864 chips duration. Among the 7 traffic time slots, time slot#0 is always allocated as downlink while time slot#1 is always allocated as uplink. The time slots for the uplink and the downlink are separated by switching points. Between the downlink time slots and uplink time slots, the special period is the switching point to separate the uplink and downlink. In each sub-frame of 5ms for 1.28Mcps option, there are two switching points (uplink to downlink and vice versa).

Using the above frame structure, the 1.28Mcps TDD option can operate on both symmetric and asymmetric mode by properly configuring the number of downlink and uplink time slots. In any configuration at least one time slot (time slot#0) has to be allocated for the downlink and at least one time slot has to be allocated for the uplink (time slot#1).

Examples for symmetric and asymmetric UL/DL allocations are given in figure [21].
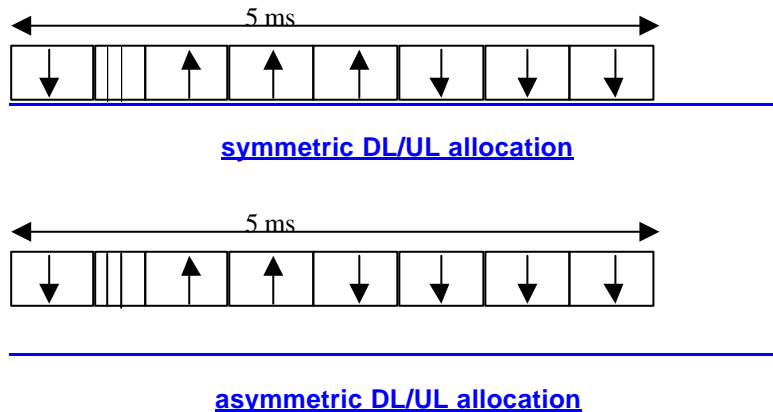

symmetric DL/UL allocation

asymmetric DL/UL allocation

Figure [21]: 1.28Mcps TDD sub-frame structure examples

6.2 Dedicated physical channel (DPCH)

The DCH as described in subclause 4.1 'Dedicated transport channels' is mapped onto the dedicated physical channel.

6.2.1 Spreading

The spreading of physical channels is the same as in 3.84 Mcps TDD (cf. 5.2.1 'Spreading').

6.2.2 Burst Format

A traffic burst consists of two data symbol fields, a midamble of 144 chips and a guard period. The data fields of the burst are 352 chips long. The corresponding number of symbols depends on the spreading factor, as indicated in table 10 below. The guard period is 16 chip periods long.

The burst format is shown in Figure 22. The contents of the traffic burst fields is described in table 11.

Table 10: number of symbols per data field in a traffic burst

Spreading factor (Q)	Number of symbols (N) per data field in Burst
1	352
2	176
4	88
8	44
16	22

Table 11: The contents of the traffic burst format fields

Chip number (CN)	Length of field in chips	Length of field in symbols	Contents of field
0-351	352	cf table 10	Data symbols
352-495	144	-	Midamble
496-847	352	cf table 10	Data symbols
848-863	16	-	Guard period

Data symbols 352 chips	Midamble 144 chips	Data symbols 352 chips	GP 16 CP

$$864*T_c$$
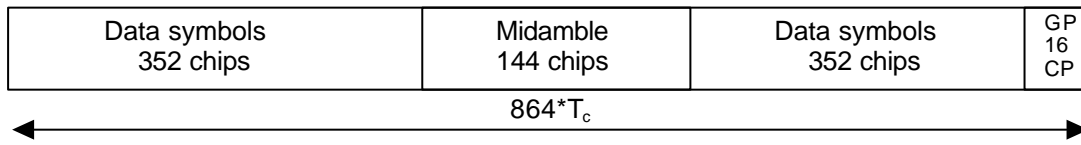
Figure 22: Burst structure of the traffic burst format (GP denotes the guard period and CP the chip periods)

6.2.2.1 Transmission of TFCI

The traffic burst format provides the possibility for transmission of TFCI in uplink and downlink.

The transmission of TFCI is negotiated at call setup and can be re-negotiated during the call. For each CCTrCH it is indicated by higher layer signalling, which TFCI format is applied. Additionally for each allocated timeslot it is signalled individually whether that timeslot carries the TFCI or not. If a time slot contains the TFCI, then it is always transmitted using the first allocated channelisation code in the timeslot, according to the order in the higher layer allocation message.

The transmission of TFCI is done in the data parts of the respective physical channel, this means TFCI and data bits are subject to the same spreading procedure as depicted in [8]. Hence the midamble structure and length is not changed.

The encoded TFCI symbols are equally distributed between the two subframes and the respective data fields. The TFCI information is to be transmitted possibly either directly adjacent to the midamble or after the SS and TPC symbols. Figure [23] shows the position of the TFCI in a traffic burst, if neither SS nor TPC are transmitted. Figure [24] shows the position of the TFCI in a traffic burst , if SS and TPC are transmitted.
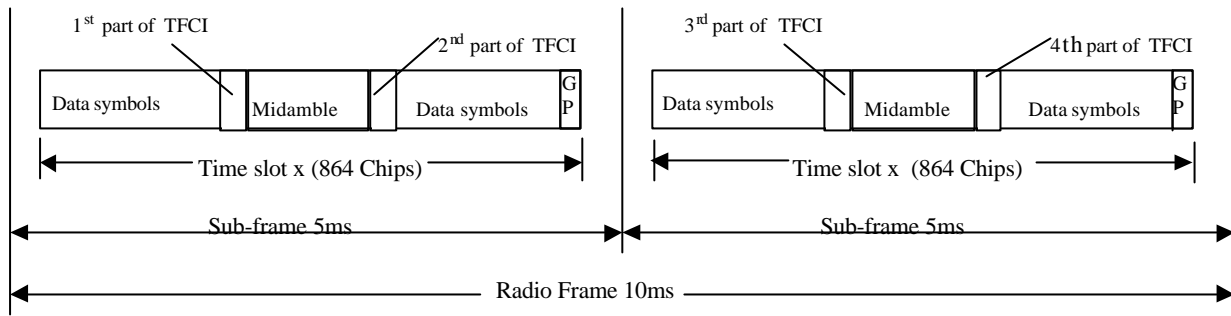
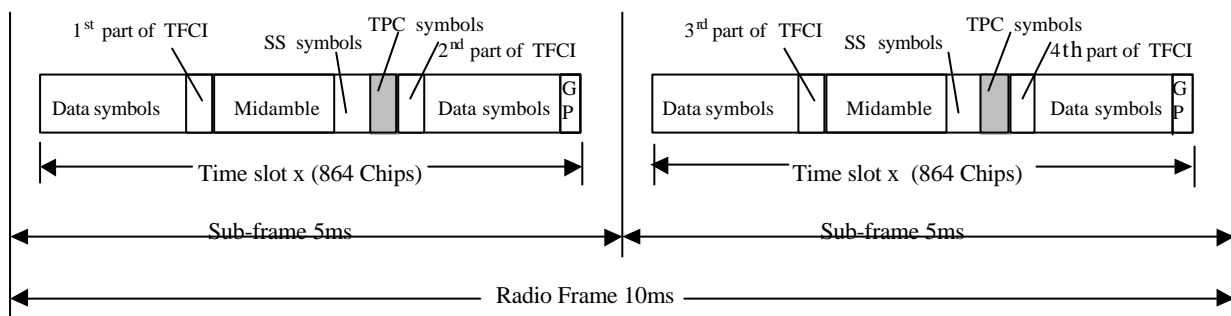**Figure 23: Position of TFCI information in the traffic burst in case of no TPC and SS in 1.28 Mcps TDD**

Figure 24:Position of TFCI information in the traffic burst in case of TPC and SS in 1.28 Mcps TDD

6.2.2.2 Transmission of TPC

The burst type for dedicated channels provides the possibility for transmission of TPC in uplink and downlink.

The transmission of TPC is done in the data parts of the traffic burst. Hence the midamble structure and length is not changed. The TPC information is to be transmitted directly after the SS information, which is transmitted after the midamble. Figure 25 shows the position of the TPC command in a traffic burst.

For every user the TPC information is to be transmitted at least once per 5ms sub-frame. If applied, transmission of TPC is done in the data parts of the traffic burst and it can be transmitted using the first allocated channelisation code and the first allocated timeslot (according to the order in the higher layer allocation message). Other allocations (more than one TPC transmission in one sub-frame) of TPC are also possible. The TPC is spread with the same spreading factor (SF) and spreading code as the data parts of the respective physical channel.
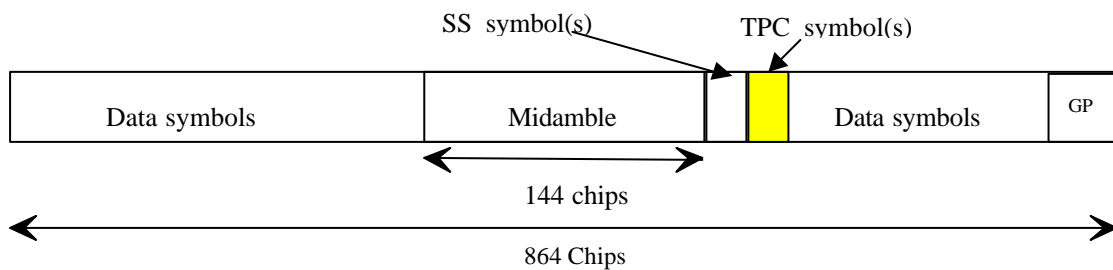
Figure 25: Position of TPC information in the traffic burst in downlink and uplink

For the number of layer 1 symbols per channelisation code there are 3 possibilities for each channelisation code, configured by higher layers:

1) one SS and one TPC symbol
2) no SS and no TPC symbols
3) 16/SF SS and 16/SF TPC symbols

So, in case 3), when SF=1, there are 16 TPC symbols which correspond to 32 bits (for QPSK) and 48 bits (for 8PSK).

In the following the uplink is described only. For the description of the downlink, downlink (DL) and uplink (UL) have to be interchanged.

Each of the TPC symbols for uplink power control in the DL will be associated with an UL time slot and an UL CCTrCH pair. This association varies with

?? the number of allocated UL time slots and UL CCTrCHs on these time slots (time slot and CCTrCH pair) and

?? the allocated TPC symbols in the DL.

In case a UE has

✍ more than one channelisation code

and/or

✍ channelisation codes being of lower spreading factor than 16 and using 16/SF SS and 16/SF TPC symbols,

the TPC commands for each ULtime slot CCTrCH pair (all channelisation codes on that time slot belonging to the same time slot and CCTrCH pair have the same TPC command) will be distributed to the following rules:

1. The ULtime slots and CCTrCH pairs the TPC commands are intended for will be numbered form the first to the last ULtime slot and CCTrCH pair allocated to the regarded UE (starting with 0). The number of a time slot and CCTrCH pair is smaller then the number of another time slot and CCTrCH pair within the same time slot if its spreading code with the lowest SC number according to the following table has a lower SC number then the spreading code with the lowest SC number of the other time slot and CCTrCH pair.

2. The commanding TPC symbols on all DLCCTrCHs allocated to one UE are numbered consecutively starting with zero according to the following rules:

   a) The numbers of the TPC commands of a regarded DL time slot are lower than those of DL time slots being transmitted after that time slot

   b) Within a DL time slot the numbers of the TPC commands of a regarded channelisation code are lower than those of channelisation codes having a higher spreading code number

   The spreading code number is defined by the following table (see[8]):

SC number	SF (Q)	Walsh code number (k)
0	16	$c_{Q=16}^{(k=1)}$
	...	
15	16	$c_{Q=16}^{(k=16)}$
16	8	$c_{Q=8}^{(k=1)}$
	...	
23	8	$c_{Q=8}^{(k=8)}$

24	4	$\mathbf{c}_{Q?4}^{(k?1)}$
	...	
27	4	$\mathbf{c}_{Q?4}^{(k?4)}$
28	2	$\mathbf{c}_{Q?2}^{(k?1)}$
29	2	$\mathbf{c}_{Q?2}^{(k?2)}$
30	1	$\mathbf{c}_{Q?1}^{(k?1)}$

Note: Spreading factors 2-8 are not used in DL

c) Within a channelisation code numbers of the TPC commands are lower than those of TPC commands being transmitted after that time

The following equation is used to determine the UL time slot which is controlled by the regarded TPC symbol in the DL:

$$UL_{pos} ? (SFN'' N_{UL\_TPCsymbols} ? TPC_{DLpos}) \mod(N_{ULslot})$$

where

UL_{pos} is the number of the controlled uplink time slot and CCTrCH pairs.

SFN' is the system frame number counting the sub-frames. The system frame number of the radio frames (SFN) can be derived from SFN' by

SFN=SFN' div 2, where div is the reminder free division operation.

$N_{UL\_PCsymbols}$ is the number of UL TPC symbols in a sub-frame.

TPC_{DLpos} is the number of the regarded UL TPC symbol in the DL within the sub-frame.

N_{ULslot} is the number of UL slots and CCTrCH pairs in a frame.

In Annex G two examples of the association of TPC commands to time slots and CCTrCH pairs are shown.

Coding of TPC:

The relationship between the TPC Bits and the transmitter power control command for QPSK is the same as in the 3.84Mcps TDD cf. [5.2.2.5 'Transmission of TPC'].

The relationship between the TPC Bits and the transmitter power control command for 8PSK is given in table [12]

Table 12: TPC Bit Pattern for 8PSK

TPC Bits	TPC command	Meaning
000	'Down'	Decrease Tx Power
110	'Up'	Increase Tx Power

6.2.2.3 Transmission of SS

The burst type for dedicated channels provides the possibility for transmission of uplink synchronisation control (ULSC).

The transmission of ULSC is done in the data parts of the traffic burst. Hence the midamble structure and length is not changed. The ULSC information is to be transmitted directly after the midamble. Figure 26 shows the position of the SS command in a traffic burst.

For every user the ULSC information shall be transmitted at least once per transmitted sub-frame. By default the following rules apply:

1. If TFCI is applied for a CCTrCH, the SS command(s) shall be transmitted using the same channelisation code and the same timeslots as the TFCI.

2. If no TFCI is applied for a CCTrCH, the SS command(s) shall be transmitted using the first allocated channelisation code and the first allocated timeslot, according to the order in the higher layer allocation message.

Apart from the default rules other allocations of SS commands are possible according higher layer signalling – e.g. the transmission of more then one SS command (on more than one time slot).

The SS command is spread with the same spreading factor (SF) and spreading code as the data parts of the respective physical channel.

The SS is utilised to command a timing adjustment by (k/8) Tc each M sub-frames, where Tc is the chip period. The default k and M values are signalled by the network by means of system information that is broadcast in the cell. The SS, as one of L1 signals, is to be transmitted once per 5ms sub-frame.

M (1-8) and k (1-8) can be adjusted during call setup or readjusted during the call.

Note: The smallest step for the SS signalled by the UTRAN is 1/8 Tc. For the UE capabilities regarding the SS adjustment of the UE it is suggested to set the tolerance for the executed command to be [1/9;1/7] Tc.
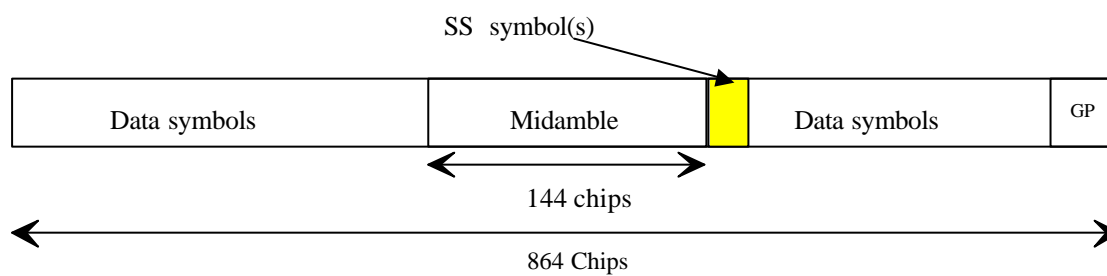

Figure 26: Position of ULSC information in the traffic burst (downlink and uplink)

*Note that for the uplink where there's no SS symbol used, the SS symbol space is reserved for future use. This can keep UL and DL slots the same structure.

For the number of layer 1 symbols there are 3 possibilities configurable for each channelisation code during the call setup:
?? one SS symbol
?? no SS symbol
?? 16/SF SS symbols

So, in case 3, when SF=1, there are 16 SS symbols which correspond to 32 bits (for QPSK) and 48 bits (for 8PSK).

Each of the SS symbols in the DL will be associated with an UL time slot depending on the allocated UL time slots and the allocated SS symbols in the DL.

Note: Even though the different time slots of the UE are controlled with independent SS commands, the UE is not in need to execute SS commands leading to a deviation of more than [3] chip with respect to the average timing advance applied by the UE.

The synchronisation shift commands for each UL time slot (all channelisation codes on that time slot have the same SS command) will be distributed to the following rules:

1. The UL time slots the SS commands are intended for will be numbered form the first to the last UL time slot occupied by the regarded UE (starting with 0) considering all CCTrCHs allocated to that UE.

2. The commanding SS symbols on all downlink CCTrCHs allocated to one UE are numbered consecutively starting with zero according to the following rules:

a) The numbers of the SS commands of a regarded DL time slot are lower than those of DL time slots being transmitted after that time slot

b) Within a DL time slot the numbers of the SS commands of a regarded channelisation code are lower than those of channelisation codes having a bigger spreading code number

The spreading code number is defined by the following table: (see TS 25.223)

Spreading code number	SF (Q)	Walsh code number (k)
0	16	$c_{Q?16}^{(k?1)}$
	...	
15	16	$c_{Q?16}^{(k?16)}$
	Spreading factors 2-8 are nor used in DL	
30	1	$c_{Q?1}^{(k?1)}$

c) Within a channelisation code numbers of the SS commands are lower than those of SS commands being transmitted after that time

The following equation is used to determine the UL time slot which is controlled by the regarded SS symbol:

$$UL_{pos} ? (SFN'?N_{SSsymbols} ? SS_{pos}) \mod(N_{ULslot}).$$

where

UL_{pos} is the number of the controlled uplink time slot.

SFN' is the system frame number counting the sub-frames. The system frame number of the radio frames (SFN) can be derived from SFN' by

SFN=SFN' div 2, where div is the reminder free division operation.

$N_{SSsymbols}$ is the number of SS symbols in a frame.

SS_{pos} is the number of the regarded SS symbol within the sub-frame.

N_{ULslot} is the number of UL slots in a frame.

The relationship between the SS Bits and the SS command for QPSK is the given in table 13:

Table 13: Coding of the SS for QPSK

SS Bits	SS command	Meaning
00	'Down'	Decrease synchronisation shift by k/8 Tc
11	'Up'	Increase synchronisation shift by k/8 Tc
01	'Do nothing'	No change

The relationship between the SS Bits and the SS command for 8PSK is given in table [14]:

Table 14: Coding of the SS for 8PSK

SS Bits	SS command	Meaning
000	'Down'	Decrease synchronisation shift by k/8 Tc
110	'Up'	Increase synchronisation shift by k/8 Tc
011	'Do nothing'	No change

6.2.2.4　　Timeslot formats

The timeslot format depends on the spreading factor, the number of the TFCI bits, the number of SS and TPC symbols and the applied modulation scheme (QPSK/8PSK) as depicted in the following tables.

6.2.2.4.1　　Timeslot formats for QPSK

6.2.2.4.1.1　　Downlink timeslot formats

Table 15 : Time slot formats for the Downlink

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} (bits)	N_{SS} & N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
0	16	144	0	0 & 0	88	88	44	44
1	16	144	4	0 & 0	88	86	42	44
2	16	144	8	0 & 0	88	84	42	42
3	16	144	16	0 & 0	88	80	40	40
4	16	144	32	0 & 0	88	72	36	36
5	16	144	0	2 & 2	88	84	44	40
6	16	144	4	2 & 2	88	82	42	40
7	16	144	8	2 & 2	88	80	42	38
8	16	144	16	2 & 2	88	76	40	36

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} (bits)	N_{SS} & N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
9	16	144	32	2 & 2	88	68	36	32
10	1	144	0	0 & 0	1408	1408	704	704
11	1	144	4	0 & 0	1408	1406	702	704
12	1	144	8	0 & 0	1408	1404	702	702
13	1	144	16	0 & 0	1408	1400	700	700
14	1	144	32	0 & 0	1408	1392	696	696
15	1	144	0	2 & 2	1408	1404	704	700
16	1	144	4	2 & 2	1408	1402	702	700
17	1	144	8	2 & 2	1408	1400	702	698
18	1	144	16	2 & 2	1408	1396	700	696
19	1	144	32	2 & 2	1408	1388	696	692
20	1	144	0	32 & 32	1408	1344	704	640
21	1	144	4	32 & 32	1408	1342	702	640
22	1	144	8	32 & 32	1408	1340	702	638
23	1	144	16	32 & 32	1408	1336	700	636
24	1	144	32	32 & 32	1408	1328	696	632

6.2.2.4.1.2 Uplink timeslot formats

Table 16 : Time slot formats for the Uplink

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} (bits)	N_{SS} & N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
0	16	144	0	0 & 0	88	88	44	44
1	16	144	4	0 & 0	88	86	42	44
2	16	144	8	0 & 0	88	84	42	42
3	16	144	16	0 & 0	88	80	40	40
4	16	144	32	0 & 0	88	72	36	36
5	16	144	0	2 & 2	88	84	44	40
6	16	144	4	2 & 2	88	82	42	40
7	16	144	8	2 & 2	88	80	42	38
8	16	144	16	2 & 2	88	76	40	36
9	16	144	32	2 & 2	88	68	36	32
10	8	144	0	0 & 0	176	176	88	88
11	8	144	4	0 & 0	176	174	86	88
12	8	144	8	0 & 0	176	172	86	86
13	8	144	16	0 & 0	176	168	84	84
14	8	144	32	0 & 0	176	160	80	80

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} (bits)	N_{SS} & N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
15	8	144	0	2 & 2	176	172	88	84
16	8	144	4	2 & 2	176	170	86	84
17	8	144	8	2 & 2	176	168	86	82
18	8	144	16	2 & 2	176	164	84	80
19	8	144	32	2 & 2	176	156	80	76
20	8	144	0	4 & 4	176	168	88	80
21	8	144	4	4 & 4	176	166	86	80
22	8	144	8	4 & 4	176	164	86	78
23	8	144	16	4 & 4	176	160	84	76
24	8	144	32	4 & 4	176	152	80	72
25	4	144	0	0 & 0	352	352	176	176
26	4	144	4	0 & 0	352	350	174	176
27	4	144	8	0 & 0	352	348	174	174
28	4	144	16	0 & 0	352	344	172	172
29	4	144	32	0 & 0	352	336	168	168
30	4	144	0	2 & 2	352	348	176	172
31	4	144	4	2 & 2	352	346	174	172

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} (bits)	N_{SS} & N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
32	4	144	8	2 & 2	352	344	174	170
33	4	144	16	2 & 2	352	340	172	168
34	4	144	32	2 & 2	352	332	168	164
35	4	144	0	8 & 8	352	336	176	160
36	4	144	4	8 & 8	352	334	174	160
37	4	144	8	8 & 8	352	332	174	158
38	4	144	16	8 & 8	352	328	172	156
39	4	144	32	8 & 8	352	320	168	152
40	2	144	0	0 & 0	704	704	352	352
41	2	144	4	0 & 0	704	702	350	352
42	2	144	8	0 & 0	704	700	350	350
43	2	144	16	0 & 0	704	696	348	348
44	2	144	32	0 & 0	704	688	344	344
45	2	144	0	2 & 2	704	700	352	348
46	2	144	4	2 & 2	704	698	350	348
47	2	144	8	2 & 2	704	696	350	346
48	2	144	16	2 & 2	704	692	348	344

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} (bits)	N_{SS} & N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
49	2	144	32	2 & 2	704	684	344	340
50	2	144	0	16 & 16	704	672	352	320
51	2	144	4	16 & 16	704	670	350	320
52	2	144	8	16 & 16	704	668	350	318
53	2	144	16	16 & 16	704	664	348	316
54	2	144	32	16 & 16	704	656	344	312
55	1	144	0	0 & 0	1408	1408	704	704
56	1	144	4	0 & 0	1408	1406	702	704
57	1	144	8	0 & 0	1408	1404	702	702
58	1	144	16	0 & 0	1408	1400	700	700
59	1	144	32	0 & 0	1408	1392	696	696
60	1	144	0	2 & 2	1408	1404	704	700
61	1	144	4	2 & 2	1408	1402	702	700
62	1	144	8	2 & 2	1408	1400	702	698
63	1	144	16	2 & 2	1408	1396	700	696
64	1	144	32	2 & 2	1408	1388	696	692
65	1	144	0	32 & 32	1408	1344	704	640
66	1	144	4	32 & 32	1408	1342	702	640

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} (bits)	N_{SS} & N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
67	1	144	8	32 & 32	1408	1340	702	638
68	1	144	16	32 & 32	1408	1336	700	636
69	1	144	32	32 & 32	1408	1328	696	632

6.2.2.4.2   Time slot formats for 8PSK

The Downlink and the Uplink timeslot formats are described together in the following table.

Table 17: Timeslot formats for 8PSK modulation

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} (bits)	N_{SS} & N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
0	1	144	0	0 & 0	2112	2112	1056	1056
1	1	144	6	0 & 0	2112	2109	1053	1056
2	1	144	12	0 & 0	2112	2106	1053	1053
3	1	144	24	0 & 0	2112	2100	1050	1050
4	1	144	48	0 & 0	2112	2088	1044	1044
5	1	144	0	3 & 3	2112	2106	1056	1050
6	1	144	6	3 & 3	2112	2103	1053	1050
7	1	144	12	3 & 3	2112	2100	1053	1047

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} (bits)	N_{SS} & N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
8	1	144	24	3 & 3	2112	2094	1050	1044
9	1	144	48	3 & 3	2112	2082	1044	1038
10	1	144	0	48 & 48	2112	2016	1056	960
11	1	144	6	48 & 48	2112	2013	1053	960
12	1	144	12	48 & 48	2112	2010	1053	957
13	1	144	24	48 & 48	2112	2004	1050	954
14	1	144	48	48 & 48	2112	1992	1044	948
15	16	144	0	0 & 0	132	132	66	66
16	16	144	6	0 & 0	132	129	63	66
17	16	144	12	0 & 0	132	126	63	63
18	16	144	24	0 & 0	132	120	60	60
19	16	144	48	0 & 0	132	108	54	54
20	16	144	0	3 & 3	132	126	66	60
21	16	144	6	3 & 3	132	123	63	60
22	16	144	12	3 & 3	132	120	63	57
23	16	144	24	3 & 3	132	114	60	54
24	16	144	48	3 & 3	132	102	54	48

6.2.3   Training sequences for spread bursts

In this subclause, the training sequences for usage as midambles are defined. The training sequences, i.e. midambles, of different users active in the same cell and same time slot are cyclically shifted versions of one single basic midamble code. The applicable basic midamble codes are given in Annex B.1.

The basic midamble codes in Annex B.1 are listed in hexadecimal notation. The binary form of the basic midamble code shall be derived according to table [18] below.

Table [18]: Mapping of 4 binary elements m_i on a single hexadecimal digit:

4 binary elements m_i	Mapped on hexadecimal digit
-1 -1 -1 -1	0
-1 -1 -1 1	1
-1 -1 1 –1	2
-1 -1 1 1	3
-1 1 -1 –1	4
-1 1 -1 1	5
-1 1 1 –1	6
-1 1 1 1	7
1 -1 -1 –1	8
1 -1 -1 1	9
1 -1 1 –1	A
1 -1 1 1	B
1 1 -1 –1	C
1 1 -1 1	D
1 1 1 –1	E
1 1 1 1	F

For each particular basic midamble code, its binary representation can be written as a vector $\mathbf{m}_P$:

$$\mathbf{m}_P \ ? \ ?m_1, m_2, ..., m_P ? \tag{1}$$

According to Annex B.1, the size of this vector $\mathbf{m}_P$ is P=128. As QPSK modulation is used, the training sequences are transformed into a complex form, denoted as the complex vector $\underline{\mathbf{m}}_P$:

$$\underline{\mathbf{m}}_P \ ? \ ?\underline{m}_1, \underline{m}_2, ..., \underline{m}_P ? \tag{2}$$

The elements $\underline{m}_i$ of $\underline{\mathbf{m}}_P$ are derived from elements m_i of $\mathbf{m}_P$ using equation (3):

$$\underline{m}_i \ ? \ (j)^i \ ?m_i \ \text{for all} \ i \ ? \ 1, ..., P \tag{3}$$

Hence, the elements $\underline{m}_i$ of the complex basic midamble code are alternating real and imaginary.

To derive the required training sequences, this vector $\underline{\mathbf{m}}_P$ is periodically extended to the size:

$$i_{max} \ ? \ L_m \ ? \ (K \ ? \ 1)W \tag{4}$$

Notes on equation (4):

K and W are taken from Annex B.1

So we obtain a new vector $\underline{\mathbf{m}}$ containing the periodic basic midamble sequence:

$$\underline{\mathbf{m}} = \left(\underline{m}_1, \underline{m}_2, ..., \underline{m}_{i_{\max}} \right) = \left(\underline{m}_1, \underline{m}_2, ..., \underline{m}_{L_m + (K-1)W} \right) \qquad (5)$$

The first P elements of this vector $\underline{\mathbf{m}}$ are the same ones as in vector $\underline{\mathbf{m}}_P$, the following elements repeat the beginning:

$$\underline{m}_i = \underline{m}_{i-P} \text{ for the subset } i = (P+1),...,i_{\max} \qquad (6)$$

Using this periodic basic midamble sequence $\underline{\mathbf{m}}$ for each user k a midamble $\underline{\mathbf{m}}^{(k)}$ of length L_m is derived, which can be written as a user specific vector:

$$\underline{\mathbf{m}}^{(k)} = \left(\underline{m}_1^{(k)}, \underline{m}_2^{(k)}, ..., \underline{m}_{L_m}^{(k)} \right) \qquad (7)$$

The L_m midamble elements $\underline{m}_i^{(k)}$ are generated for each midamble of the k users (k = 1,...,K) based on:

$$\underline{m}_i^{(k)} = \underline{m}_{i+(K-k)W} \text{ with } i = 1,...,L_m \text{ and } k = 1,...,K \qquad (8)$$

The midamble sequences derived according to equations (7) to (8) have complex values and are not subject to channelisation or scrambling process, i.e. the elements $\underline{m}_i^{(k)}$ represent complex chips for usage in the pulse shaping process at modulation.

The term 'a midamble code set' or 'a midamble code family' denotes K specific midamble codes $\underline{\mathbf{m}}^{(k)}$; k=1,...,K, based on a single basic midamble code $\mathbf{m}_P$ according to (1).

6.2.4 Beamforming

Beamforming is same as that of the 3.84Mcps TDD, cf. [5.2.4 Beamforming].

6.3 Common physical channels

6.3.1 Primary common control physical channel (P-CCPCH)

The BCH as described in section 4.1.2 'Common Transport Channels' is mapped onto the Primary Common Control Physical Channels (P-CCPCH1 and P-CCPCH2). The position (time slot / code) of the P-CCPCHs is fixed in the 1.28Mcps TDD. The P-CCPCHs are mapped onto the first two code channels of timeslot#0 with spreading factor of 16. The P-CCPCH is always transmitted with an antenna pattern configuration that provides whole cell coverage.

6.3.1.1 P-CCPCH Spreading

The P-CCPCH uses fixed spreading with a spreading factor SF = 16. The P-CCPCH1 and P-CCPCH2 always use channelisation code $c_{Q=16}^{(k=1)}$ and $c_{Q=16}^{(k=2)}$ respectively.

6.3.1.2 P-CCPCH Burst Format

The burst format as described in section 6.2.2 is used for the P-CCPCH. No TFCI is applied for the P-CCPCH.

6.3.1.3   P-CCPCH Training sequences

The training sequences, i.e. midambles, as described in subclause 6.2.3 are used for the P-CCPCH. For timeslots#0 in which the P-CCPCH is transmitted, the midambles $m^{(1)}$ and $m^{(2)}$ are reserved for P-CCPCH in order to support Block STTD antenna diversity and the beacon function, see 6.4 and 6.5. The use of midambles depends on whether Block STTD is applied to the P-CCPCH:

- If no antenna diversity is applied to P-CCPCH, $m^{(1)}$ is used and $m^{(2)}$ is left unused.

- If Block STTD antenna diversity is applied to P-CCPCH, $m^{(1)}$ is used for the first antenna and $m^{(2)}$ is used for the diversity antenna.

6.3.2   Secondary common control physical channel (S-CCPCH)

PCH and FACH as described in subclause 4.1.2 are mapped onto one or more secondary common control physical channels (S-CCPCH). In this way the capacity of PCH and FACH can be adapted to the different requirements. The time slot and codes used for the S-CCPCH are broadcast on the BCH.

6.3.2.1   S-CCPCH Spreading

The S-CCPCH uses fixed spreading with a spreading factor SF = 16. The S-CCPCHs (S-CCPCH 1 and S-CCPCH 2) are always used in pairs, mapped onto two code channels with spreading factor 16. There can be more than one pair of S-CCPCHs in use in one cell.

6.3.2.2   S-CCPCH Burst Format

The burst format as described in section 6.2.2 is used for the S-CCPCH. TFCI may be applied for S-CCPCHs.

6.3.2.3   S-CCPCH Training sequences

The training sequences, i.e. midambles, as described in the subclause 6.2.3 are also used for the S-CCPCH.

6.3.3   Fast Physical Access CHannel (FPACH)

The Fast Physical Access CHannel (FPACH) is used by the Node B to carry, in a single burst, the acknowledgement of a detected signature with timing and power level adjustment indication to a user equipment. FPACH makes use of one resource unit only at spreading factor 16, so that its burst is composed by 44 symbols. The spreading code, training sequence and time slot position are configured by the network and signalled on the BCH.

6.3.3.1   FPACH burst

The FPACH burst contains 32 information bits. Table 19 reports the content description of the FPACH information bits and their priority order:

Table 19:   FPACH information bits description

Information field	Length (in bits)
Signature Reference Number	3 (MSB)
Relative Sub-Frame Number	2
Received starting position of the UpPCH ($UpPCH_{POS}$)	11
Transmit Power Level Command for RACH message	7

Reserved bits (default value: 0)	9 (LSB)

In the use and generation of the information fields is explained in [9].

6.3.3.1.1 Signature Reference Number

The reported number corresponds to the numbering principle for the cell signatures as described in [8].

The Signature Reference Number value range is 0 – 7 coded in 3 bits such that:

bit sequence(0 0 0) corresponds to the first signature of the cell; …; bit sequence (1 1 1) corresponds to the 8th signature of the cell.

6.3.3.1.2 Relative Sub-Frame Number

The Relative Sub-Frame Number value range is 0 – 3 coded such that:

bit sequence (0 0) indicates one sub-frame difference; …; bit sequence (1 1) indicates 4 sub-frame difference.

6.3.3.1.3 Received starting position of the UpPCH (UpPCH$_{POS}$)

The received starting position of the UpPCH value range is 0 – 2047 coded such that:

bit sequence (0 0 … 0 0 0) indicates the received starting position zero chip; …; bit sequence (1 1 … 1 1 1) indicates the received starting position 2047*1/8 chip.

6.3.3.1.4 Transmit Power Level Command for the RACH message

The transmit power level command is transmitted in 7 bits.

6.3.3.2 FPACH Spreading

The FPACH uses only spreading factor SF=16 as described in subclause 6.3.3. The set of admissible spreading codes for use on the FPACH is broadcast on the BCH.

6.3.3.2 FPACH Burst Format

The burst format as described in section 6.2.2 is used for the FPACH.

6.3.3.3 FPACH Training sequences

The training sequences, i.e. midambles, as described in subclause 6.2.3 are used for FPACH.

6.3.3.4 FPACH timeslot formats

The FPACH uses slot format #0 of the DL time slot formats given in subclause 6.2.2.4.1.1.

6.3.4 The physical random access channel (PRACH)

The RACH as described in subclause 4.1.2 is mapped onto one or more uplink physical random access channels (PRACH). In such a way the capacity of RACH can be flexibly scaled depending on the operators need.

6.3.4.1 PRACH Spreading

The uplink PRACH uses either spreading factor SF=16, SF=8 or SF=4 as described in subclause 6.2.1. The set of admissible spreading codes for use on the PRACH and the associated spreading factors are broadcast on the BCH (within the RACH configuration parameters on the BCH).

6.3.4.2 PRACH Burst Format

The burst format as described in section 6.2.2 is used for the PRACH.

6.3.4.3 PRACH Training sequences

The training sequences, i.e. midambles, of different users active in the same time slot are time shifted versions of a single periodic basic code. The basic midamble codes as described in subclause 6.2.3 are used for PRACH.

6.3.4.4 PRACH timeslot formats

The PRACH uses the following time slot formats taken from the uplink timeslot formats described in sub-clause 6.2.2.4.1.2:

Spreading Factor	Slot Format #
16	0
8	10
4	25

6.3.4.5 Association between Training Sequences and Channelisation Codes

The association between training sequences and channelisation codes of PRACH in the 1.28McpsTDD is same as that of the DPCH.

6.3.5 The synchronisation channels (DwPCH, UpPCH)

There are two dedicated physical synchronisation channels —DwPCH and UpPCH in each 5ms sub-frame of the 1.28Mcps TDD. The DwPCH is used for the down link synchronisation and the UpPCH is used for the uplink synchronisation.

The position and the contents of the DwPCH are equal to the DwPTS as described in the subclause 6.1., while the position and the contents of the UpPCH are equal to the UpPTS.

The DwPCH is transmitted at each sub-frame with an antenna pattern configuration which provides whole cell coverage. Furthermore it is transmitted with a constant power level which is signalled by higher layers.

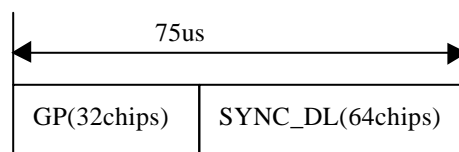The burst structure of the DwPCH (DwPTS) is described in the figure 27.

Figure 27: burst structure of the DwPCH (DwPTS)

Note:' GP' for 'Guard Period'

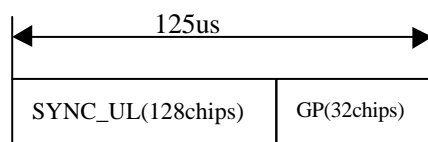The burst structure of the UpPCH (UpPTS) is described in the figure 28.

Figure 28: burst structure of the UpPCH (UpPTS)

The SYNC-DL code in DwPCH and the SYNC-UL code in UpPCH are not spreaded. The details about the SYNC-DL and SYNC-UL code are described in the corresponding subclause and annex in [8].

6.3.6   Physical Uplink Shared Channel (PUSCH)

For Physical Uplink Shared Channel (PUSCH) the burst structure of DPCH as described in subclause 6.2 shall be used. User specific physical layer parameters like power control, timing advance or directive antenna settings are derived from the associated channel (FACH or DCH). PUSCH provides the possibility for transmission of TFCI in uplink.

6.3.7   Physical Downlink Shared Channel (PDSCH)

For Physical Downlink Shared Channel (PDSCH) the burst structure of DPCH as described in subclause 6.2 shall be used. User specific physical layer parameters like power control or directive antenna settings are derived from the associated channel (FACH or DCH). PDSCH provides the possibility for transmission of TFCI in downlink.

To indicate to the UE that there is data to decode on the DSCH, three signalling methods are available:

   1) using the TFCI field of the associated channel or PDSCH;

   2) using on the DSCH user specific midamble derived from the set of midambles used for that cell;

   3) using higher layer signalling.

When the midamble based method is used, the UE shall decode the PDSCH if the PDSCH was transmitted with the midamble assigned to the UE by UTRAN, see 6.6.1.1.2 . For this method no other physical channels may use the same time slot as the PDSCH and only one UE may share the PDSCH time slot at the same time.

6.3.8   The Page Indicator Channel (PICH)

The Paging Indicator Channel (PICH) is a physical channel used to carry the paging indicators.

6.3.8.1   Mapping of Paging Indicators to the PICH bits

Figure 28 depicts the structure of a PICH transmission and the numbering of the bits within the bursts. The burst type as described in [6.2.2 'Burst Format'] is used for the PICH. N_{PIB} bits are used to carry the paging indicators, where $N_{PIB}=352$.
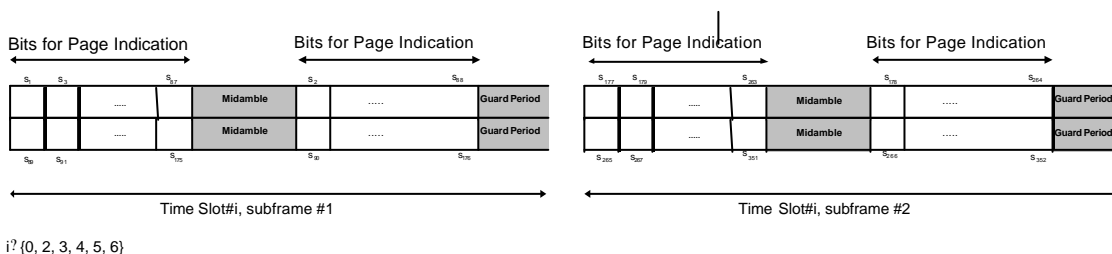

Figure 28: Transmission and numbering of paging indicator carrying bits in the PICH bursts

Each paging indicator P_q (where P_q, $q = 0, ..., N_{PI}-1$, $P_q ? \{0, 1\}$) in one radio frame is mapped to the bits $\{s_{2L_{PI}*q+1}, ..., s_{2L_{PI}*(q+1)}\}$ in subframe #1 or subframe #2. There are $N_{PIB} = 2*N_{PI}*L_{PI}$ bits used for the paging indicator transmission in one radio frame. The mapping of the paging indicators to the bits s_i, $i = 1, ..., N_{PIB}$ is shown in table 20.

Table 20: Mapping of the paging indicator

P_q	Bits $\{s_{2L_{PI}*q+1}, s_{2L_{PI}*q+2}, ..., s_{2L_{PI}*(q+1)}\}$	Meaning
0	{0, 0, ..., 0}	There is no necessity to receive the PCH
1	{1, 1, ..., 1}	There is the necessity to receive the PCH

The bits s_k, $k = 1, ..., S$ are then transmitted over the air as shown in [7].

In each radio frame, N_{PI} paging indicators are transmitted, using $L_{PI}=2$, $L_{PI}=4$ or $L_{PI}=8$ symbols. In table 21 this number is shown for the different possibilities of paging indicator lengths.

Table 21: Number N_{PI} of paging indicators per radio frame for different paging indicator lengths L_{PI}

	$L_{PI}=2$	$L_{PI}=4$	$L_{PI}=8$
N_{PI} per radio frame	88	44	22

6.3.8.2 Structure of the PICH over multiple radio frames

The structure of the PICH over multiple radio frames is common with 3.84 Mcps TDD, cf. [5.3.7.2 Structure of the PICH over multiple radio frames]

6.4 Transmit Diversity for DL Physical Channels

Table 22 summarizes the different transmit diversity schemes for different downlink physical channel types in 1.28Mcps TDD that are described in [9].

Table 22: Application of Tx diversity schemes on downlink physical channel types in 1.28Mcps TDD "X" – can be applied, "–" – must not be applied

Physical channel type	Open loop TxDiversity		Closed loop TxDiversity
	TSTD	Block STTD	
P-CCPCH	X	X	–
DwPCH	X	–	–
DPCH	X	–	X

6.5 Beacon **characteristics** of physical channels

For the purpose of measurements, physical channels at particular locations (time slot, code) shall have particular physical characteristics, called beacon characteristics. Physical channels with beacon characteristics are called beacon channels. The location of the beacon channels is called beacon location. The beacon channels shall provide the beacon function, i.e. a reference power level at the beacon location, regularly existing in each subframe. Thus, beacon channels must be present in each subframe.

6.5.1 Location of beacon channels

The beacon location is described as follows :

The beacon function shall be provided by the physical channels that are allocated to channelisation code $c_{Q?16}^{(k?1)}$ and $c_{Q?16}^{(k?2)}$ in Timeslot#0.

Note that by this definition the P-CCPCH always has beacon characteristics.

6.5.2 Physical characteristics of the beacon function

The beacon channels shall have the following physical characteristics.

They:

- are transmitted with reference power;

- are transmitted without beamforming;

- use midamble $m^{(1)}$ and $m^{(2)}$ exclusively in this time slot

The reference power corresponds to the sum of the power allocated to both midambles $m^{(1)}$ and $m^{(2)}$. Two possibilities exist:

- If no Block STTD antenna diversity is applied to P-CCPCH, all the reference power of any beacon channel is allocated to $m^{(1)}$.

- If Block STTD antenna diversity is applied to P-CCPCH, for any beacon channel midambles $m^{(1)}$ and $m^{(2)}$ are each allocated half of the reference power. Midamble $m^{(1)}$ is used for the first antenna and $m^{(2)}$ is used for the diversity antenna. Block STTD encoding is used for the data in P-CCPCH, see [9]; for all other beacon channels identical data sequences are transmitted on both antennas.

6.6 Midamble Allocation for Physical Channels

The midamble allocation schemes for physical channels are the same as in the 3.84Mcps TDD option. The associations between channelisation codes and midambles for the default and common midamble allocation differ from the 3.84 Mcps TDD option. The associations are given in Annex B.2 [Association between Midambles and channelisation Codes] and D [Signalling of the number of channelisation codes for the DL common midamble case for 1.28Mcps TDD] respectively

6.6.1 Midamble Allocation for DL Physical Channels

Beacon channels shall always use the reserved midambles $m^{(1)}$ and $m^{(2)}$, see 6.5. For the other DL physical channels that are located in timeslot #0, midambles shall be allocated based on the default midamble allocation scheme, using the association for K=8 midambles. For all other DL physical channels, the midamble is explicitly assigned by higher layers or allocated by layer 1.

6.6.1.1 Midamble Allocation by signalling from higher layers

The midamble allocation by signalling is the same like in the 3.84 Mcps TDD cf. [5.6.1.1 Midamble allocation by signalling from higher layers]

6.6.1.2 Midamble Allocation by layer 1

6.6.1.2.1 Default midamble

The default midamble allocation by layer 1 is the same like in the 3.84 Mcps TDD cf. [5.6.1.2.1 Default midamble]. The associations between midambles and channelisation codes are given in Annex B.2 [Association between Midambles and channelisation Codes].

6.6.1.2.2 Common Midamble

The common midamb le allocation by layer 1 is the same like in the 3.84 Mcps TDD cf. [5.6.1.2.2 Common midamble]. The respective associations are given in Annex D [Signalling of the number of channelisation codes for the DL common midamble case for 1.28 Mcps TDD].

6.6.2 Midamble Allocation for UL Physical Channels

The midamble allocation for UL Physical Channels is the same as in the 3.84 Mcps TDD cf. [5.6.2 Midamble allocation for UL Physical Channels]

6.7 Midamble Transmit Power

The setting of the midamble transmit power is done as in the 3.84 Mcps TDD option cf. 5.7 'Midamble Transmit Power'

67 Mapping of transport channels to physical channels for the 3.84 Mcps option

8 Mapping of transport channels to physical channels for the 1.28 Mcps option

This clause describes the way in which the transport channels are mapped onto physical resources, see figure 29.

Transport channels	Physical channels
DCH	Dedicated Physical Channel (DPCH)
BCH	Primary Common Control Physical Channels (P-CCPCH)
PCH	Secondary Common Control Physical Channels(S-CCPCH)
FACH	Secondary Common Control Physical Channels(S-CCPCH)
	PICH
RACH	Physical Random Access Channel (PRACH)
USCH	Physical Uplink Shared Channel (PUSCH)
DSCH	Physical Downlink Shared Channel (PDSCH)
	Down link Pilot Channel (DwPCH)
	Up link Pilot Channel (UpPCH)
	FPACH

Figure 29: Transport channel to physical channel mapping for 1.28Mcps TDD

8.1 Dedicated Transport Channels

The mapping of transport blocks to physical bearers is in principle the same as in 3.84 Mcps TDD but due to the subframe structure the coded bits are mapped onto each of the subframes within the given TTI.
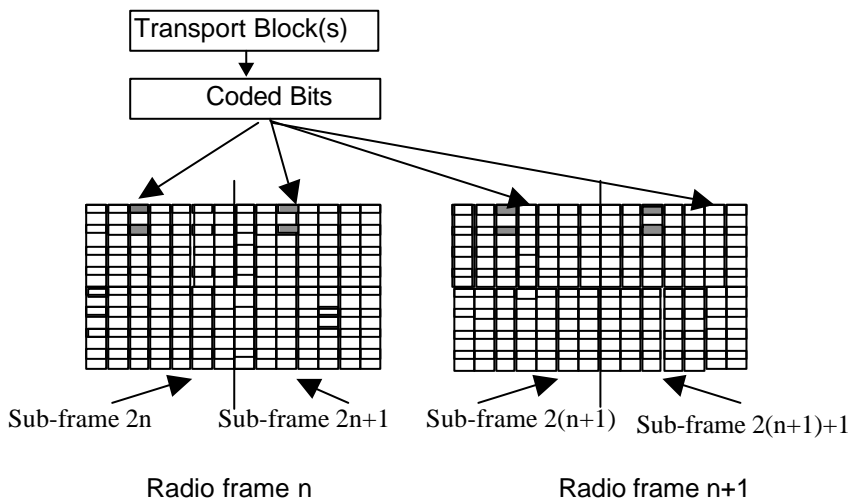

Figure 30 : Mapping of Transport Blocks onto the physical bearer (TTI= 20ms)

8.2 Common Transport Channels

8.2.1 The Broadcast Channel (BCH)

There are two P-CCPCHs, P-CCPCH 1 and P-CCPCH 2 which are mapped onto timeslot#0 using the channelisation codes $c_{Q?16}^{(k?1)}$ and $c_{Q?16}^{(k?2)}$ with spreading factor 16. The BCH is mapped onto the P-CCPCH1+P-CCPCH2.

The position of the P-CCPCHs is indicated by the relative phases of the bursts in the DwPTS with respect to the P-CCPCHs midamble sequences , see [8]. One special combination of the phase differences of the burst in the DwPTS with respect to the P-CCPCH midamble indicates the position of the P-CCPCH in the multi-frame and the start position of the interleaving period.

8.2.2 The Paging Channel (PCH)

The mapping of Paging Channels onto S-CCPCHs and the association between PCHs and Paging Indicator Channels is the same as in the 3.84 Mcps TDD option, cf. 6.2.2 'The paging Channel' and 6.2.2.1 'PCH/PICH Association' respectively.

8.2.3 The Forward Channel (FACH)

The FACH is mapped onto one or several S-CCPCHs. The location of the FACH is indicated on the BCH and both, capacity and location can be changed, if required. FACH may or may not be power controlled.

8.2.4 The Random Access Channel (RACH)

The RACH has intraslot interleaving only and is mapped onto PRACH. More than one slot per frame may be administered for the PRACH. The location of slots allocated to PRACH is broadcast on the BCH. The uplink sync codes (SYNC-UL sequences) used by the UEs for UL synchronisation have a well known association with the P-RACHs, as broadcast on the BCH. On the PRACH, both power control and uplink synchronisation control are used.

8.2.5 The Uplink Shared Channel (USCH)

The uplink shared channel is mapped onto one or several PUSCH, see subclause 6.3.6 'Physical Uplink Shared Channel (PUSCH)'

8.2.6 The Downlink Shared Channel (DSCH)

The downlink shared channel is mapped onto one or several PDSCH, see subclause 6.3.7 'Physical Downlink Shared Channel (PDSCH)'

Annex A (normative):
Basic Midamble Codes for the 3.84 Mcps option

Annex B (normative): Basic Midamble Codes for the 1.28 Mcps option

B.1 Basic Midamble Codes

The midamble has a length of $L_m = 144$, which is corresponding to:

$$K = 2, 4, 6, 8, 10, 12, 14, 16, \qquad W ? \left\lfloor \frac{P}{K} \right\rfloor, P = 128$$

Note: that $\lfloor x \rfloor$ denotes the largest integer number less or equal to x.

Depending on the possible delay spread cells are configured to use midambles which are generated from the Basic Midamble Codes (see table B.1). The cell configuration is broadcast on BCH.

The mapping of these Basic Midamble Codes to Cell Parameters is shown in [8].

Table B.1: Basic Midamble Codes m_p according to equation (5) from subclause 6.2.3

Code ID	Basic Midamble Codes m_P of length P=128
m_{P0}	B2AC420F7C8DEBFA69505981BCD028C3
m_{P1}	0C2E988E0DBA046643F57B0EA6A435E2
m_{P2}	D5CEC680C36A4454135F86DD37043962
m_{P3}	E150D08CAC2A00FF9B32592A631CF85B
m_{P4}	E0A9C3A8F6E40329B2F2943246003D44
m_{P5}	FE22658100A3A683EA759018739BD690
m_{P6}	B46062F89BB2A1139D76A1EF32450DA0
m_{P7}	EE63D75CC099092579400D956A90C3E0
m_{P8}	D9C0E040756D427A2611DAA35E6CD614
m_{P9}	EB56D03A498EC4FEC98AE220BC390450
m_{P10}	F598703DB0838112ED0BABB98642B665
m_{P11}	A0BC26A992D4558B9918986C14861EFF
m_{P12}	541350D109F1DD68099796637B824F88
m_{P13}	892D344A962314662F01F9455F7BC302
m_{P14}	49F270E29CCD742A40480DD4215E1632
m_{P15}	6A5C0410C6C39AA04E77423C355926DE
m_{P16}	7976615538203103D4DBCC219B16A9E1
m_{P17}	A6C3C3175845400BD2B738C43EE2645F
m_{P18}	A0FD56258D228642C6F641851C3751ED
m_{P19}	EFA48C3FC84AC625783C6C9510A2269A
m_{P20}	62A8EB1A420334B23396E8D76BC19740
m_{P21}	9E96235699D5D41C9816C921023BC741
m_{P22}	4362AE4CAE0DCC32D60A3FED1341A848
m_{P23}	454C068E6C4F190942E0904B95D61DFB
m_{P24}	607FEEA6E2E99206718A49C0D6A25034
m_{P25}	E1D1BCDA39A09095B5C81645103A077C
m_{P26}	994B445E558344DE211C8286DDD3D1A3
m_{P27}	C15233273581417638906ADB61FDCA3C
m_{P28}	8B79A274D542F096FB1388098230F8A1
m_{P29}	DF58AC1C5F44B2A40266385CE1DA5640
m_{P30}	B5949A1CC69962C464401D05FF5C1A7A
m_{P31}	85AC489841ED3EAA2D83BBB0039CC707

m_{P32}	AE371CC144BC95923CA8108D8B49FE82
m_{P33}	7F188484A649D1C22BDA1F09D49B5117
m_{P34}	ADAA3C657089DEF7C0284903A491C9B0
m_{P35}	C3F96893C7504DC3B51488604AF64F4C
m_{P36}	B4002F5AE0CE8623AC979D368E9148C1
m_{P37}	0EEBCC0C795C02A106C24ABB36D08C6E
m_{P38}	4B0F537E384A893F58971580D9894433
m_{P39}	08E0035AB29B7ECC53C15DAA0687CC8F
m_{P40}	8611ACBC4C82781D77654EE862506D60
m_{P41}	63315261A8F1CB02549802DBFD197C07
m_{P42}	9A2609A434F43E7DCADC0E22B2EF4012
m_{P43}	F4C9F0A127A88461209ABF8C69CE4D00
m_{P44}	C79124EE3FFC28C5C4524D2B01670D42
m_{P45}	C91985C4FED53D09361914354BA80E79
m_{P46}	82AA517260779ECFF26212C1A10BDC29
m_{P47}	561DE2040ACB458E0DBD354E43E111D9
m_{P48}	2E58C7202D17392BC1235782CEFABB09
m_{P49}	C4FAA121C698047650F6503126A577C1
m_{P50}	E7B75206A9B410E44346E0DAE842A23C
m_{P51}	3F8B1C32682B28D098D3805ED130EA7F
m_{P52}	8D5FC2C1C6715F824B401434C8D4BB82
m_{P53}	0B2A43453ACC028FE6EB6E1CB0740B59
m_{P54}	BC56948FC700BA4883262EE73E12D82A
m_{P55}	558D136710272912FA4F183D1189A7FD
m_{P56}	5709E7F82DC6500B7B12A3072D182645
m_{P57}	86D4F161C844AE5E20EE39FD5493B044
m_{P58}	8729B6EDC382B152185885F013DAE222
m_{P59}	154C45B50720F4C362C14C77FE8335A1
m_{P60}	C6A0962890351F4EB802DE43A7662C9E
m_{P61}	D19D69D6B380B4B22457CB80033519F0
m_{P62}	C7D89509FB0DAE9255998E0A00C2B262
m_{P63}	DFD481C652C0C905D61D66F1732C4AA2
m_{P64}	06C848619AF1D6C910A8EAC4B622FC06
m_{P65}	0635E29D4E7AC8ABC189890241F45ECA
m_{P66}	B272B020586AAD7B093AC2F459076638
m_{P67}	B608ACE46E1A6BC96181EEDD88B54140
m_{P68}	0A516092B3ED7849B168AFE223B8670E
m_{P69}	D1A658C5009E04D0D7D5E9205EE663E8
m_{P70}	AC316DC39B91EB60B1AABD8280740432
m_{P71}	E3F06825476A026CD287625E514519FC
m_{P72}	A56D092080DDE8994F387C175CC56833
m_{P73}	15EA799DE587C506D0CD99A408217B05
m_{P74}	A59C020BAB9AF6D3F813C391CA244CD2
m_{P75}	74B0101EB9F3167434B94BABC8378882
m_{P76}	CE752975C8DA9B0100386DB82A8C3D20
m_{P77}	BBB38DCDB1E9118570AC147DC05241A4
m_{P78}	944ABBF0866098101F6971731AB2E986
m_{P79}	2BB147B2A30C68B4853F90481A166EB6
m_{P80}	444840ACCF3F23C45B56D7704BF18283
m_{P81}	87604F7450D1AD188C452981A5C7FC9B
m_{P82}	8C3842EBC948A65BC4C8B387F11B7090
m_{P83}	10B4767D071CF5DB2288E4029576135A
m_{P84}	6F07AAB697CD0089572C6B062E2018E4
m_{P85}	D3D65B442057E613A8655060C8D29E27
m_{P86}	5EDA330514C604BF4E0894E09EC57A74
m_{P87}	B0899CD094060724DED82AE85F18A43A
m_{P88}	B2D999B86DF902BC25015CAE3A0823C4
m_{P89}	C23CD40F04242B92D46EED82CD9A9A18

m_{P90}	D22DDCC5CB82960125DD24655F3C8788
m_{P91}	54987218FBD99AE4340FD4C9458E9850
m_{P92}	BE4341822997A7B11EA1E8A1A2767005
m_{P93}	255200FBA6EE48E6DE0A82B0461B8D0F
m_{P94}	6FBD58A663932423503690CF9C171701
m_{P95}	D215033A4AA87EC1C232BAC7EDA09370
m_{P96}	CA0959B01AE48E80204F1E4A3F29CE55
m_{P97}	582043413B9B825903E3A3545ED59463
m_{P98}	5016541922971C703D16E284CBDF633B
m_{P99}	7347EF160A1733CA98D43608A83A920B
m_{P100}	908B22AD433CCA00B3FD47C691F1A290
m_{P101}	BB22A272FC6923DF1B43BA4118806570
m_{P102}	0FA75C87474836B47DC7624D61193802
m_{P103}	A22EBA0658A4D0FF1E9CA5030A65CC06
m_{P104}	6C9C51CA15F1F4981F4C46180A6A6697
m_{P105}	4C847ACF8BC15359C405322851C9BDE2
m_{P106}	C1D29499C0082C9DE473ED15B14D63E0
m_{P107}	7E85ECC98AC761005076C5572869A431
m_{P108}	D8F11121595B8F49F78A7039E44126A0
m_{P109}	1A0BC814445FD71C8E5B1A9163ED2059
m_{P110}	A7591F27F8B0C00C68CC41697954FA04
m_{P111}	6CA2CE595E7406D79C4840183D41B9D0
m_{P112}	C093D3CC701FC20E66F5AB22516C5460
m_{P113}	D0E0CDE9B595546B96C4F8066B469020
m_{P114}	E99F743A451431C8B427054A4E6F2007
m_{P115}	C0D21A344A2C07DF2A6EBE6250C7B91E
m_{P116}	F031223E282CF7A4D8EF174A908668AE
m_{P117}	E4BD244AC16C55C7137FB068FD44280C
m_{P118}	C44920DE2028F19FC2AAB36A0DCFDAD0
m_{P119}	3FA7054E77135250699E6C8A11600742
m_{P120}	D5740B4D8870C1C5B5A214C4266FC537
m_{P121}	F0B7942D43BB6F38446442EB8126AB80
m_{P122}	83DB9534EAD6238FA8968798CDF04848
m_{P123}	EB9663CDDC2B291690703125BABCB800
m_{P124}	84D547225D4BBD20DEF1A583240C6E0F
m_{P125}	B51F6A771838BE934724AEA6A2669802
m_{P126}	D92AC05E10496794BBDC115233B1C068
m_{P127}	D3ACF0078EDA9856BBB0AF8651132103

B.2   Association between Midambles and Channelisation Codes

The following mapping schemes apply for the association between midambles and channelisation codes if no midamble is allocated by higher layers. Secondary channelisation codes are marked with (*). These associations apply for both UL and DL.
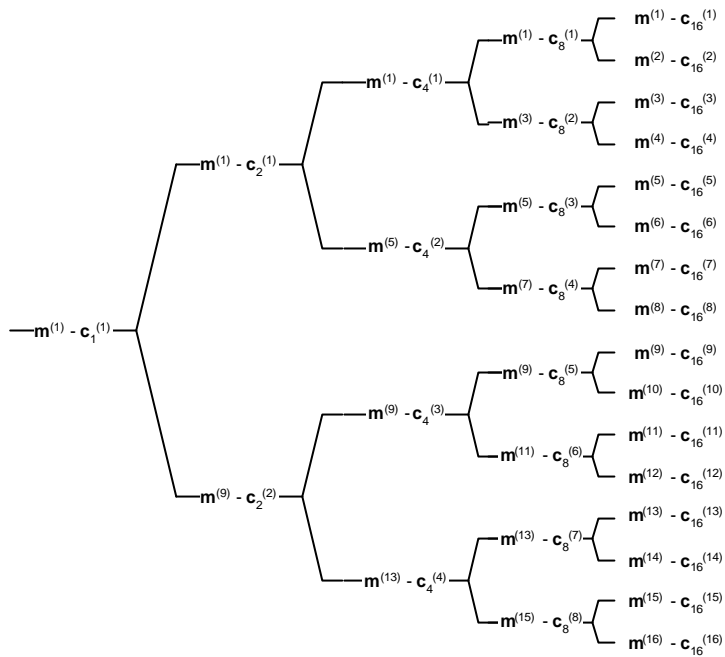
B.2.1 Association for K=16 Midambles

Figure B.2.1: Association of Midambles to Spreading Codes for K=16
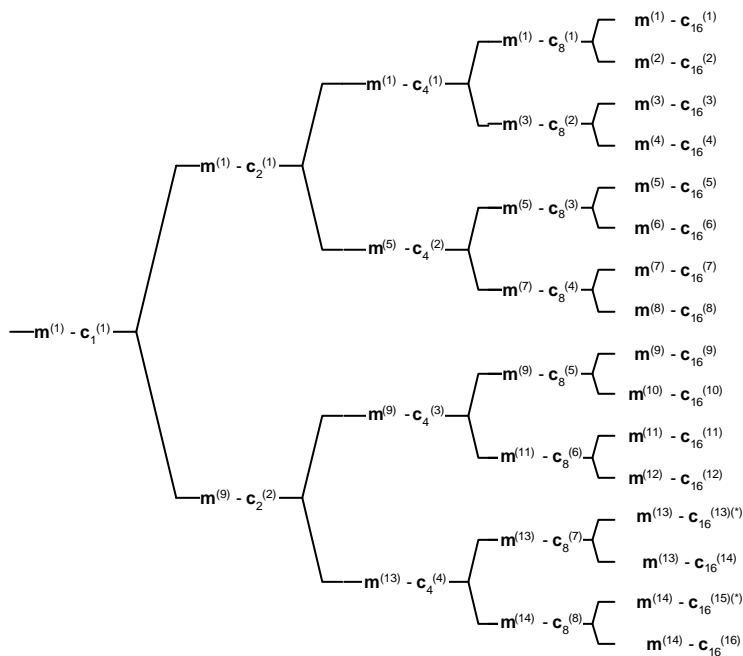
B.2.2 Association for K=14 Midambles

Figure B.2.2: Association of Midambles to Spreading Codes for K=14
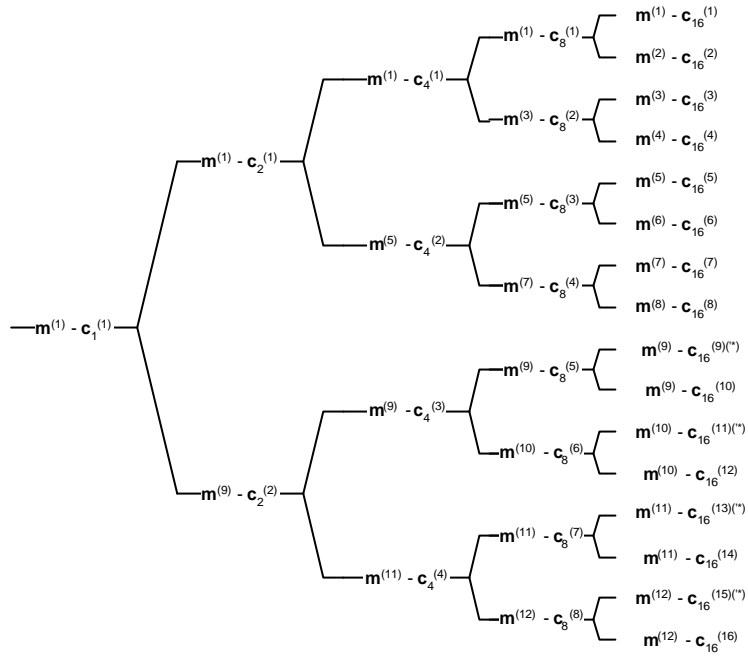
B.2.3 Association for K=12 Midambles

Figure B.2.3: Association of Midambles to Spreading Codes for K=12
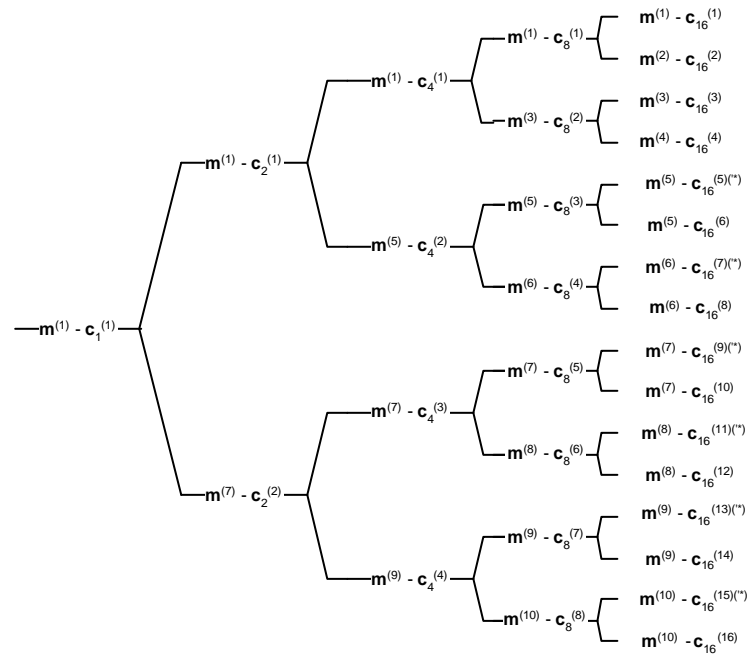
B.2.4 Association for K=10 Midambles

Figure B.2.4: Association of Midambles to Spreading Codes for K=10
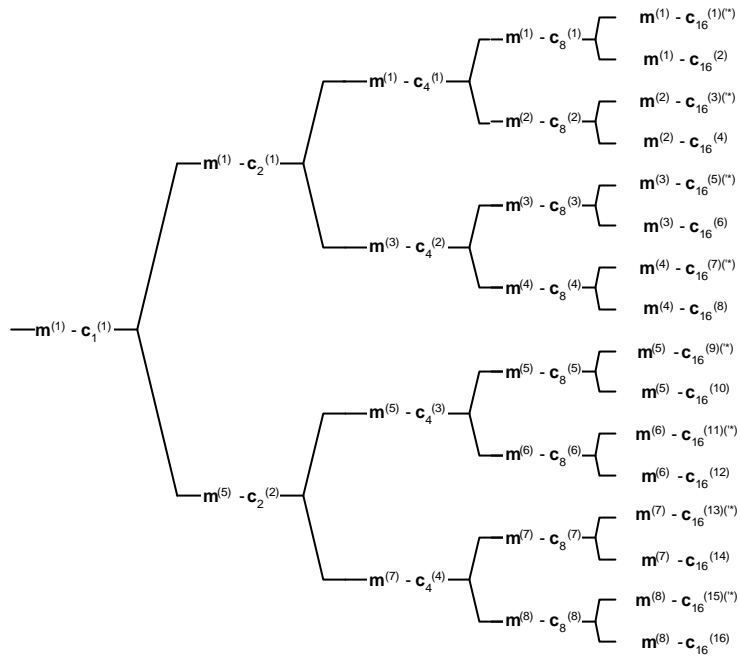
B.2.5   Association for K=8 Midambles

Figure B.2.5: Association of Midambles to Spreading Codes for K=8

B.2.6   Association for K=6 Midambles

Figure B.2.6: Association of Midambles to Spreading Codes for K=6

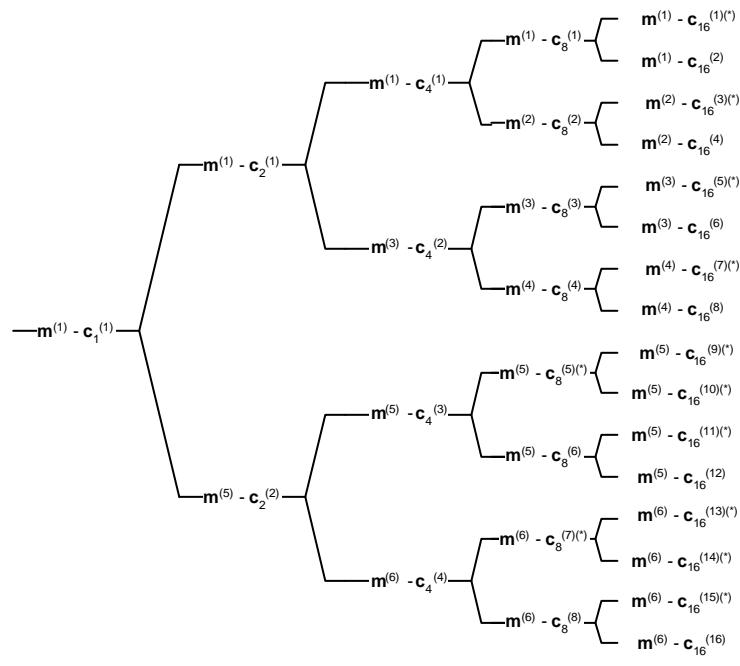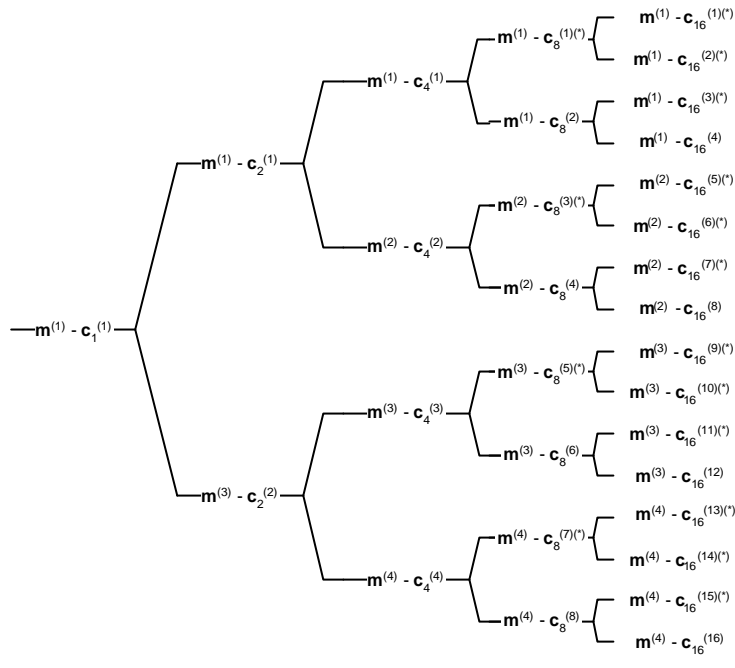## B.2.7 Association for K=4 Midambles

Figure B.2.7: Association of Midambles to Spreading Codes for K=4
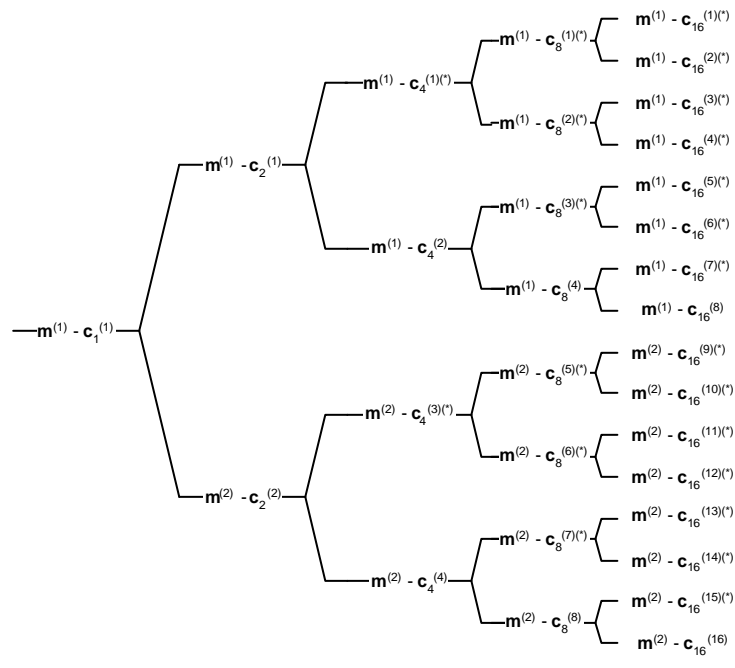
B.2.8 Association for K=2 Midambles

Figure B.2.8: Association of Midambles to Spreading Codes for K=2

Annex ~~B~~ C (normative)
Signalling of the number of channelisation codes for the DL common midamble case for 3.84Mcps TDD

Annex D (normative)
Signalling of the number of channelisation codes for the DL common midamble case for 1.28Mcps TDD

The following mapping schemes shall apply for the association between the number of channelisation codes employed in a timeslot and the use of a particular midamble shift in the DL common midamble case. In the following tables the presence of a particular midamble shift is indicated by '1'. Midamble shifts marked with '0' are left unused.

D.1 Mapping scheme for K=16 Midambles

m1	m2	m3	m4	m5	m6	M7	M8	m9	m10	m11	m12	M13	m14	m15	m16	
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1 code
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2 codes
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3 codes
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	4 codes
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	5 codes
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	6 codes
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	7 codes
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	8 codes
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	9 codes
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	10 codes
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	11 codes
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	12 codes
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	13 codes
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	14 codes
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	15 codes
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	16 codes

D.2 Mapping scheme for K=14 Midambles

m1	m2	m3	m4	m5	m6	M7	M8	m9	m10	m11	m12	M13	m14	
1	0	0	0	0	0	0	0	0	0	0	0	0	0	1 or 15 code(s)
0	1	0	0	0	0	0	0	0	0	0	0	0	0	2 or 16 codes
0	0	1	0	0	0	0	0	0	0	0	0	0	0	3 codes
0	0	0	1	0	0	0	0	0	0	0	0	0	0	4 codes
0	0	0	0	1	0	0	0	0	0	0	0	0	0	5 codes
0	0	0	0	0	1	0	0	0	0	0	0	0	0	6 codes
0	0	0	0	0	0	1	0	0	0	0	0	0	0	7 codes
0	0	0	0	0	0	0	1	0	0	0	0	0	0	8 codes
0	0	0	0	0	0	0	0	1	0	0	0	0	0	9 codes
0	0	0	0	0	0	0	0	0	1	0	0	0	0	10 codes
0	0	0	0	0	0	0	0	0	0	1	0	0	0	11 codes
0	0	0	0	0	0	0	0	0	0	0	1	0	0	12 codes
0	0	0	0	0	0	0	0	0	0	0	0	1	0	13 codes
0	0	0	0	0	0	0	0	0	0	0	0	0	1	14 codes

D.3   Mapping scheme for K=12 Midambles

m1	m2	m3	m4	m5	m6	M7	M8	m9	m10	m11	m12	
1	0	0	0	0	0	0	0	0	0	0	0	1 or 13 code(s)
0	1	0	0	0	0	0	0	0	0	0	0	2 or 14 codes
0	0	1	0	0	0	0	0	0	0	0	0	3 or 15 codes
0	0	0	1	0	0	0	0	0	0	0	0	4 or 16 codes
0	0	0	0	1	0	0	0	0	0	0	0	5 codes
0	0	0	0	0	1	0	0	0	0	0	0	6 codes
0	0	0	0	0	0	1	0	0	0	0	0	7 codes
0	0	0	0	0	0	0	1	0	0	0	0	8 codes
0	0	0	0	0	0	0	0	1	0	0	0	9 codes
0	0	0	0	0	0	0	0	0	1	0	0	10 codes
0	0	0	0	0	0	0	0	0	0	1	0	11 codes
0	0	0	0	0	0	0	0	0	0	0	1	12 codes

D.4   Mapping scheme for K=10 Midambles

m1	m2	m3	m4	m5	m6	M7	M8	m9	m10	
1	0	0	0	0	0	0	0	0	0	1 or 11 code(s)
0	1	0	0	0	0	0	0	0	0	2 or 12 codes
0	0	1	0	0	0	0	0	0	0	3 or 13codes
0	0	0	1	0	0	0	0	0	0	4 or 14 codes
0	0	0	0	1	0	0	0	0	0	5 or 15 codes
0	0	0	0	0	1	0	0	0	0	6 or 16 codes
0	0	0	0	0	0	1	0	0	0	7 codes
0	0	0	0	0	0	0	1	0	0	8 codes
0	0	0	0	0	0	0	0	1	0	9 codes
0	0	0	0	0	0	0	0	0	1	10 codes

D.5   Mapping scheme for K=8 Midambles

m1	m2	m3	m4	m5	m6	m7	m8	
1	0	0	0	0	0	0	0	1 or 9 code(s)
0	1	0	0	0	0	0	0	2 or 10 codes
0	0	1	0	0	0	0	0	3 or 11 codes
0	0	0	1	0	0	0	0	4 or 12 codes
0	0	0	0	1	0	0	0	5 or 13 codes
0	0	0	0	0	1	0	0	6 or 14 codes
0	0	0	0	0	0	1	0	7 or 15 codes
0	0	0	0	0	0	0	1	8 or 16 codes

D.6   Mapping scheme for K=6 Midambles

m1	m2	m3	m4	m5	m6	
1	0	0	0	0	0	1 or 7 or 13 code(s)
0	1	0	0	0	0	2 or 8 or 14 codes
0	0	1	0	0	0	3 or 9 or 15 codes
0	0	0	1	0	0	4 or 10 or 16 codes
0	0	0	0	1	0	5 or 11 codes
0	0	0	0	0	1	6 or 12 codes

D.7   Mapping scheme for K=4 Midambles

m1	m2	m3	m4	
1	0	0	0	1 or 5 or 9 or 13 code(s)
0	1	0	0	2 or 6 or 10 or 14 codes
0	0	1	0	3 or 7 or 11 or 15 codes
0	0	0	1	4 or 8 or 12 or 16 codes

D.8 Mapping scheme for K=2 Midambles

m1	m2	
1	0	1 or 3 or 5 or 7 or 9 or 11 or 13 or 15 code(s)
0	1	2 or 4 or 6 or 8 or 10 or 12 or 14 or 16 codes

Annex ~~C~~ E (Informative):
CCPCH Multiframe Structure for the 3.84 Mcps option

Annex F (Informative):
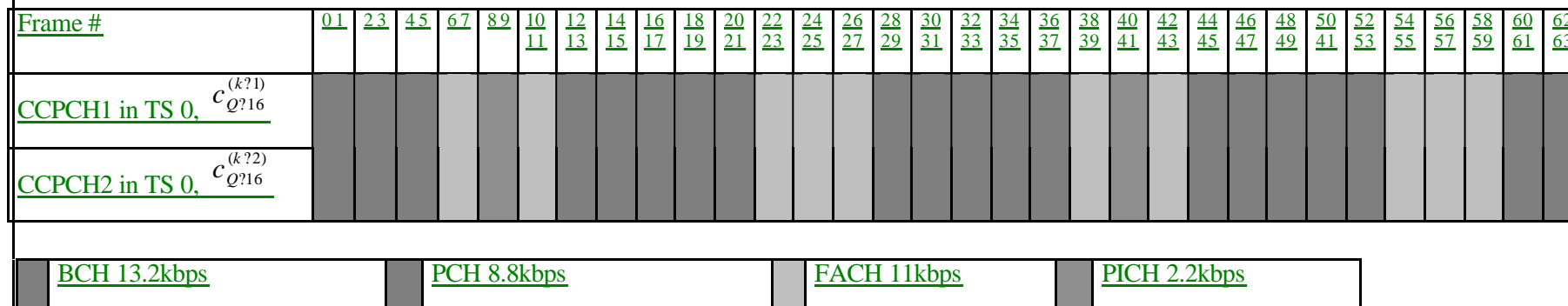## CCPCH Multiframe Structure for the 1.28 Mcps option

| Frame # | 0 1 | 2 3 | 4 5 | 6 7 | 8 9 | 10 11 | 12 13 | 14 15 | 16 17 | 18 19 | 20 21 | 22 23 | 24 25 | 26 27 | 28 29 | 30 31 | 32 33 | 34 35 | 36 37 | 38 39 | 40 41 | 42 43 | 44 45 | 46 47 | 48 49 | 50 41 | 52 53 | 54 55 | 56 57 | 58 59 | 60 61 | 62 63 |

CCPCH1 in TS 0, $c_{Q?16}^{(k?1)}$

CCPCH2 in TS 0, $c_{Q?16}^{(k?2)}$

BCH 13.2kbps   PCH 8.8kbps   FACH 11kbps   PICH 2.2kbps

Figure F.1: Example for a multiframe structure for CCPCHs and PICH that is repeated every 64th frame (128 sub-frame)

| Frame # | 0 1 | 2 3 | 4 5 | 6 7 | 8 9 | 10 11 | 12 13 | 14 15 | 16 17 | 18 19 | 20 21 | 22 23 | 24 25 | 26 27 | 28 29 | 30 31 | 32 33 | 34 35 | 36 37 | 38 39 | 40 41 | 42 43 | 44 45 | 46 47 | 48 49 | 50 41 | 52 53 | 54 55 | 56 57 | 58 59 | 60 61 | 62 63 |

CCPCH1 in TS k, $c_{Q?16}^{(k?i)}$

CCPCH2 in TS k, $c_{Q?16}^{(k?j)}$

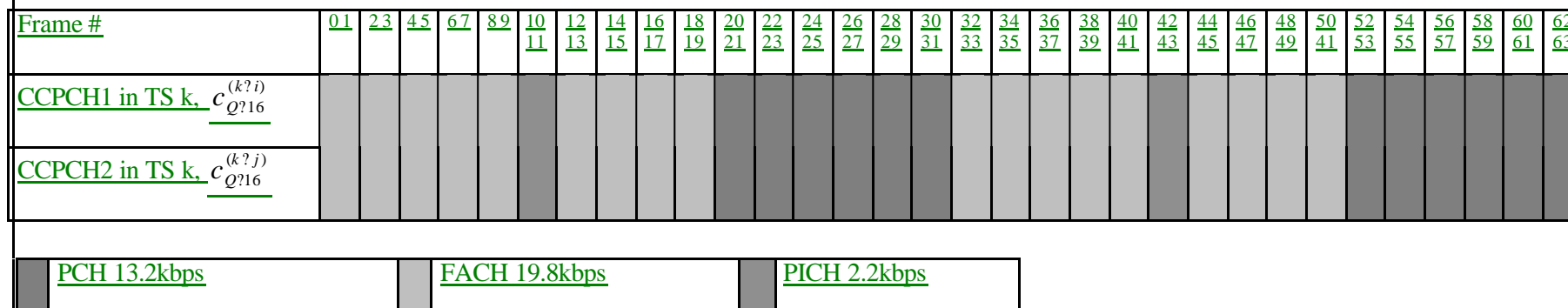PCH 13.2kbps   FACH 19.8kbps   PICH 2.2kbps

Figure F.2: Example for a multiframe structure for S-CCPCHs and PICH that is repeated every 64th frame, i,j=1 ? 16 (i?j),k?0, 1,(128 sub-frame)

Annex G (Informative): Examples of the association of DL TPC commands to UL uplink time slots for 1.28 Mcps TDD

Table G.1 Two examples of the association of DL TPC commands to UL uplink time slots with NULslot=3

In the following two examples of the association of UL TPC commands to UL time slots and CCTrCHs are shown (see 6.2.2.2):

Case 1: $N_{UL\_TPCsymbols}=2$; Case 2: $N_{UL\_TPCsymbols}=4$

Sub-Frame Number	Case 1 (2 UL TPC symbols)		The order of the served UL time slot and CCTrCH pairs (UL time slot and CCTrCH number)	Case 2 (4 UL TPC symbols)	
	The order of UL TPC symbols				The order of UL TPC symbols
SFN'=0	(1st UL$_{pos}$=0)	0	0 (TS3)	0	(1st UL$_{pos}$=0)
		1	1 (TS4)	1	
			2 (TS5)	2	
			0 (TS3)	3	
SFN'=1	(1st UL$_{pos}$=2)	0	0 (TS3)	0	(1st UL$_{pos}$=1)
		1	1 (TS4)	1	
			2 (TS5)	2	
			0 (TS3)	3	
			1 (TS4)		
SFN'=2	(1st UL$_{pos}$=1)	0	0 (TS3)	0	(1st UL$_{pos}$=2)
		1	1 (TS4)	1	
			2 (TS5)	2	
			0 (TS3)	3	
			1 (TS4)		
			2 (TS5)		
. . .	. . .		. . .		. . .

Annex H (Informative): Examples of the association of DL SS commands to UL uplink time slots

In the following two examples of the association of DL SS commands to UL uplink time slots are shown (see 6.2.2.3):

Table H.1 Two examples of the association of DL SS commands to UL uplink time slots with $N_{ULslot}=3$

Case 1: $N_{SSsymbols}=2$; Case 2: $N_{SSsymbols}=4$

Sub-Frame Number	Case 1 (2 DL SS symbols) The order of DL SS symbols		The order of the served UL time slot (UL time slot number)	Case 2 (4 DL SS symbols)	The order of DL SS symbols
SFN'=0	(1st U$L_{pos}=0$)	0	0 (TS3)	0	(1st U$L_{pos}=0$)
		1	1 (TS4)	1	
			2 (TS5)	2	
			0 (TS3)	3	
SFN'=1	(1st U$L_{pos}=2$)	0	0 (TS3)	0	(1st U$L_{pos}=1$)
		1	1 (TS4)	1	
			2 (TS5)	2	
			0 (TS3)	3	
			1 (TS4)		
SFN'=2	(1st U$L_{pos}=1$)	0	0 (TS3)	0	(1st U$L_{pos}=2$)
		1	1 (TS4)	1	
			2 (TS5)	2	
			0 (TS3)	3	
			1 (TS4)		
			2 (TS5)		
. . .	. . .		. . .		. . .

Annex ~~D~~ I (informative): Change history