3GPP TSG-RAN1 Meeting #19
USA, Las Vegas, 27th Feb – 02nd Mar 2001

Tdoc R1-01-0256

CR-Form-v3

CHANGE REQUEST

✍ **TR25.944 CR 06** ✍ rev **-** ✍ Current version: **3.3.0** ✍

*For **HELP** on using this form, see bottom of this page or look at the pop-up text over the ✍ symbols.*

Proposed change affects: ✍ (U)SIM ☐ ME/UE **X** Radio Access Network **X** Core Network ☐

Title: ✍	corrections for TDD sections	
Source: ✍	Siemens AG	
Work item code: ✍		***Date:*** ✍ 22.02.2001
Category: ✍	**F**	***Release:*** ✍ R99

Use one of the following categories:
- ***F*** *(essential correction)*
- ***A*** *(corresponds to a correction in an earlier release)*
- ***B*** *(Addition of feature),*
- ***C*** *(Functional modification of feature)*
- ***D*** *(Editorial modification)*

Detailed explanations of the above categories can be found in 3GPP TR 21.900.

Use one of the following releases:

2	*(GSM Phase 2)*
R96	*(Release 1996)*
R97	*(Release 1997)*
R98	*(Release 1998)*
R99	*(Release 1999)*
REL-4	*(Release 4)*
REL-5	*(Release 5)*

Reason for change: ✍ In meeting WG1#17 cf. R1-00-1003, a fix SF=16 for TFCI and TPC has been specified. Currently there is a misalignment between the current 25.221 and TR25.944.

Summary of change: ✍
- ?? The number of databits for uplink transmissions, using a lower SF than 16 is corrected.
- ?? TFCI "16 bits per user" replaced by "16 bit", since not appropriate here
- ?? Removal of TrBlkSize 360 bit in 4.2.2.1 for RACH
- ?? For S-CCPCH, the TDD-Mac header is 3 Bit larger than that of FDD, therefore TrBlk Sizes changed from 360 and 168 to 363 and 171 repect., cf. T1S-010029 for 34.108

Consequences if not approved: ✍ Misalignment between TR 25.944 and TS 25.221/TS 34.108 resp.

Clauses affected: ✍

Other specs affected: ✍
- ☐ Other core specifications
- ☐ Test specifications
- ☐ O&M Specifications

✍

Other comments: ✍

4.2 TDD mode

4.2.1 Downlink

4.2.1.1 BCH

Table 25: Parameters for BCH

Transport block size	246 bits
CRC	16 bits
Coding	CC, coding rate = 1/2
TTI	20 ms
Midamble	512 chips
Codes and time slots	SF = 16 x 1 x 1 time slot
TFCI	0 bit
TPC	0 bit

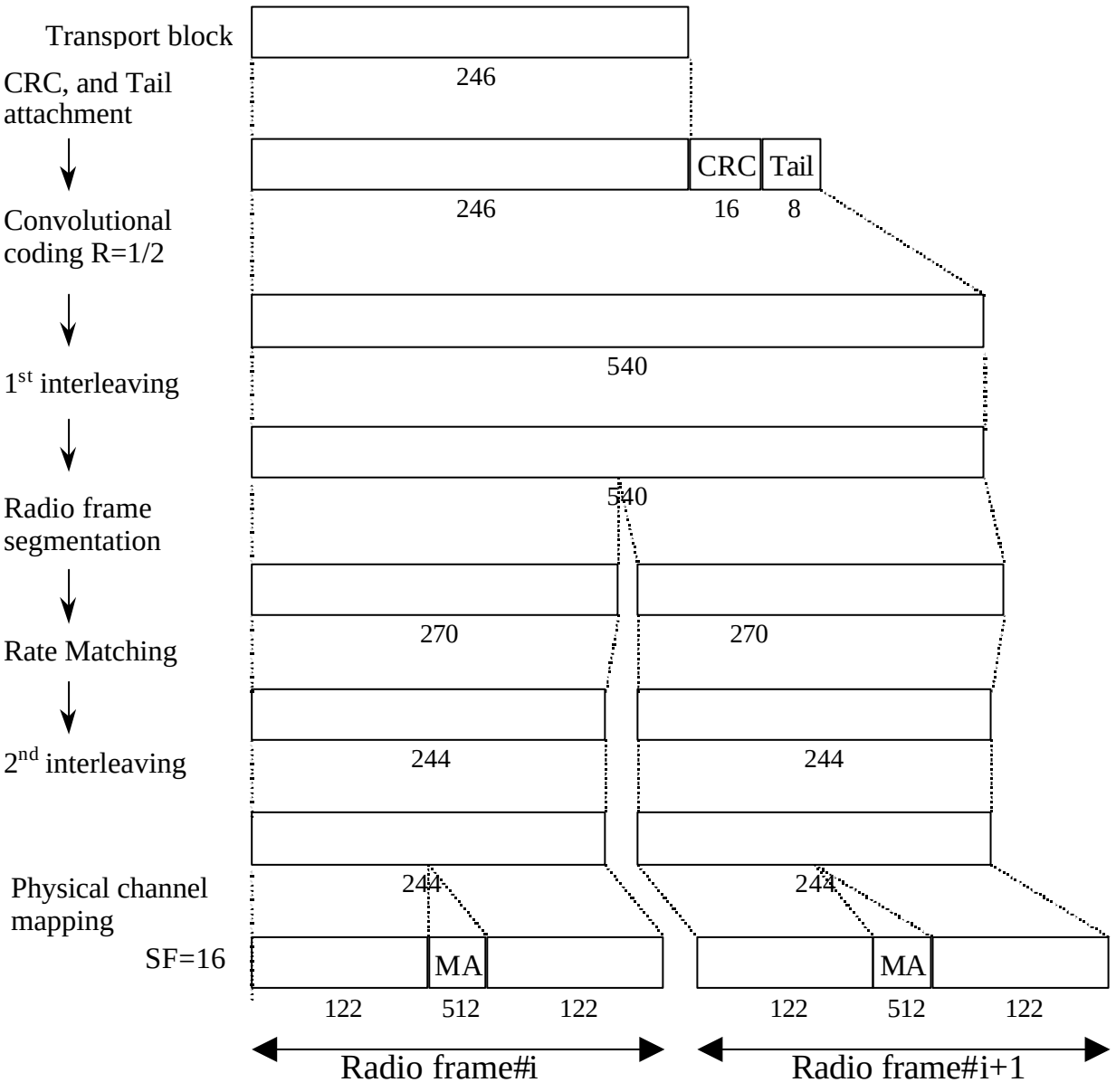

Figure 29: Channel coding for BCH

4.2.1.2 Example for PCH and FACH

Table 26: Parameters for PCH and FACH

Transport block size	PCH	N_{PCH}=80 or 240 bits
	FACH1	~~360~~ 363 bits
	FACH2	~~168~~ 171 bits
Transport block set size	PCH	80*B_{PCH} or 240*B_{PCH} bits (B_{PCH}=0,1)
	FACH1	~~360~~363*B_{FACH1} bits (B_{FACH1}=0,1)
	FACH2	~~168~~171*B_{FACH2} bits (B_{FACH2}=0,1,2)
Coding	PCH, FACH2	CC, coding rate = 1/2
	FACH1	TC
TTI		10 ms
Midamble		512 chips
Codes and time slots		SF = 16 x 2 x 1 time slot
TFCI		16 bit
TPC		0 bit

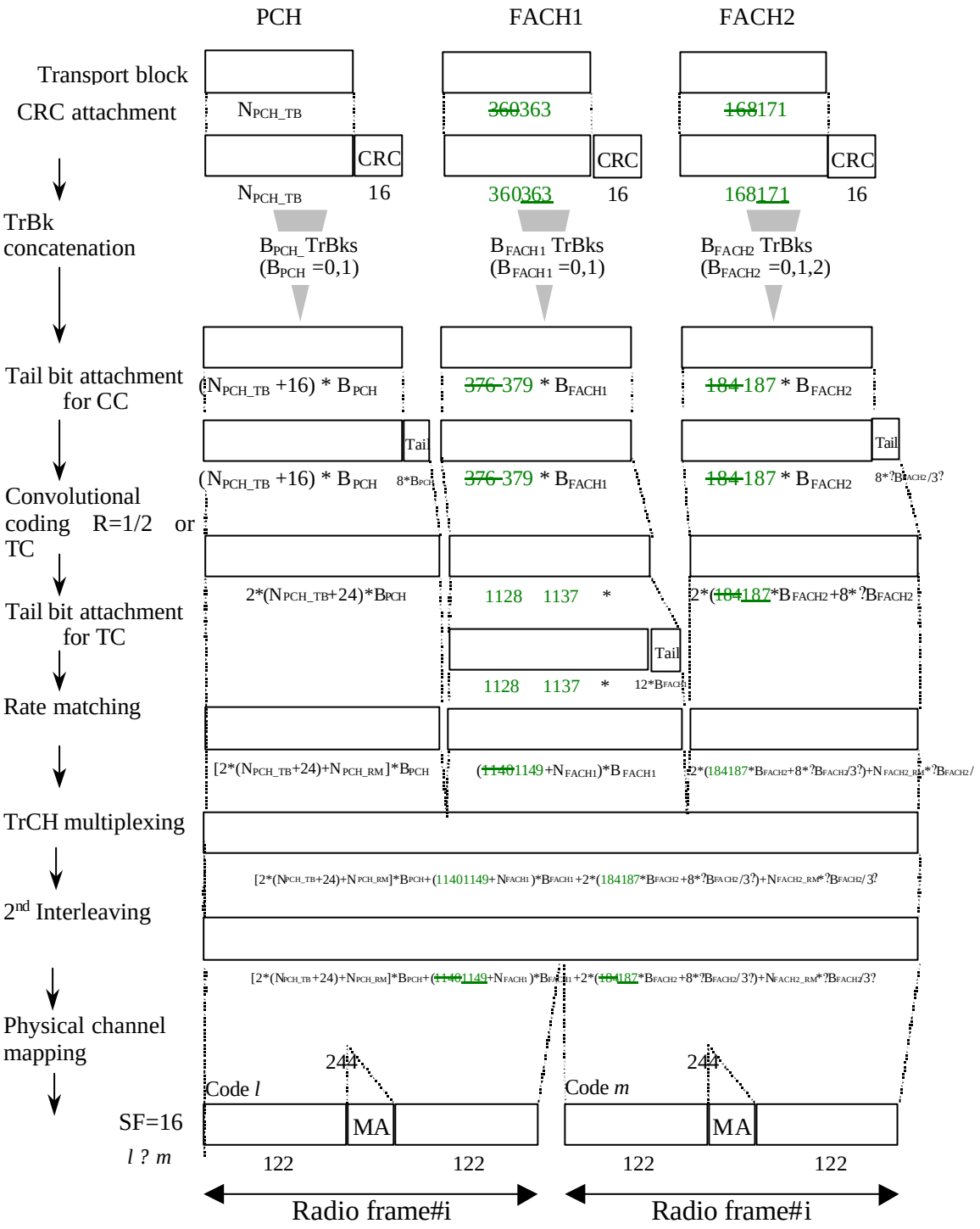

Figure 30: Channel coding and multiplexing example for PCH and FACH

4.2.1.3.2 TrCH multiplexing -> Physical channel mapping

4.2.1.3.2.1 Example for Stand-alone mapping of 3.4 kbps data

NOTE: This example can be applied to Stand-alone mapping of DCCH.

Table 33 shows example of physical channel parameters for Stand-alone mapping of 3.4 kbps data.

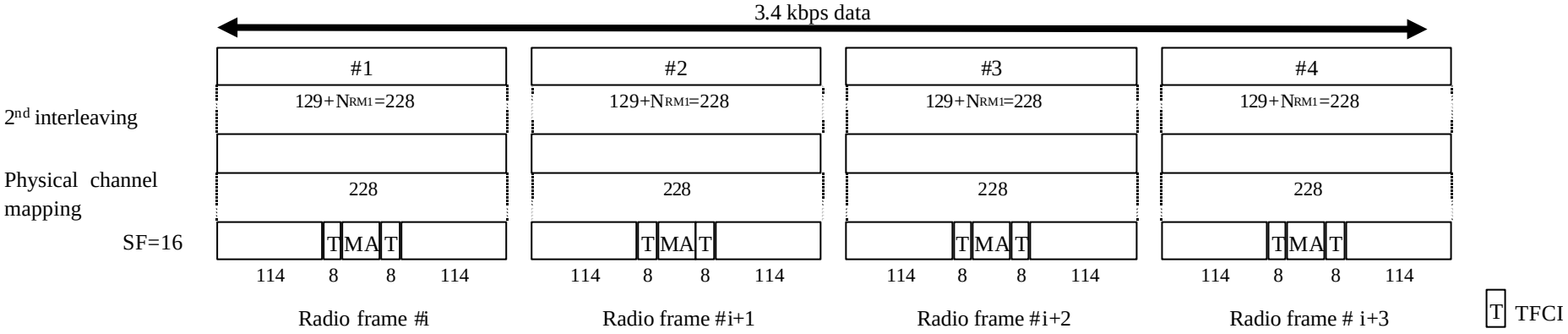

Figure 38: Channel coding and multiplexing example for Stand-alone mapping of 3.4 kbps data

Table 33: Physical channel parameters for Stand-alone mapping of 3.4 kbps data

Midamble	512 chips
Codes and time slots	SF16 x 1 code x 1 time slot
TFCI	16 bit~~s per user~~
TPC	0 bit

4.2.1.3.2.2 Example for multiplexing of 12.2 kbps data and 3.4 kbps data

NOTE: This example can be applied to multiplexing AMR speech and DCCH.

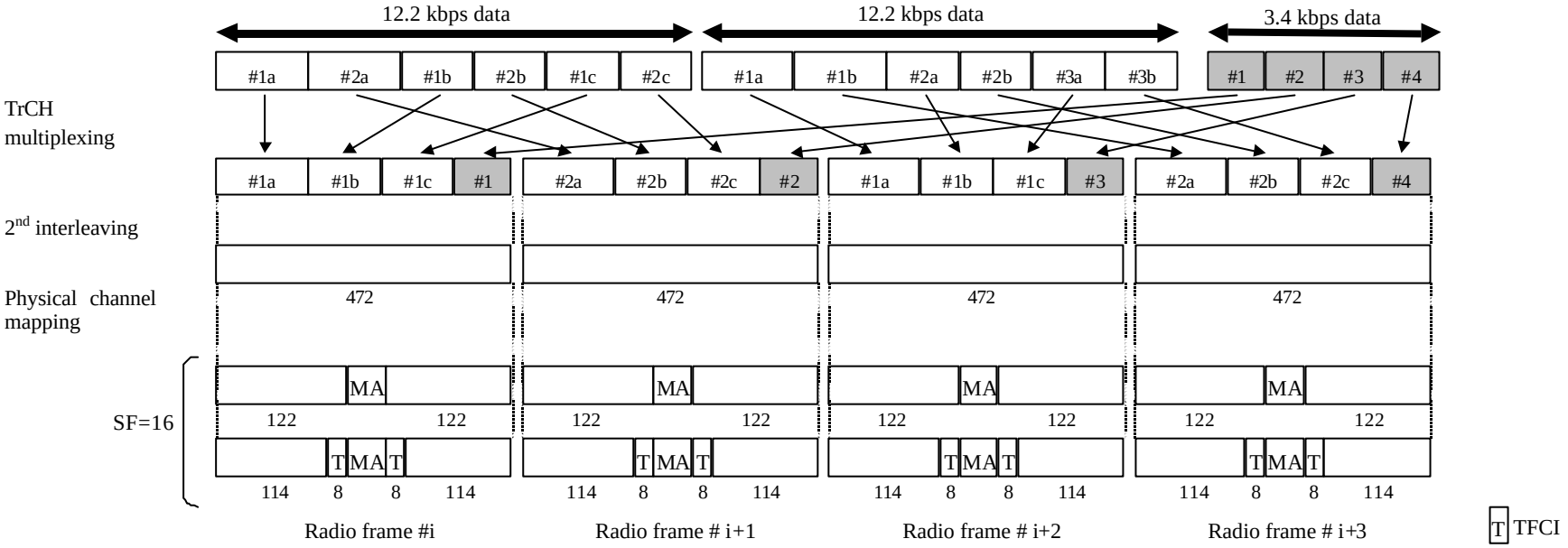

Figure 39: Channel coding and multiplexing example for multiplexing of 12.2 kbps data and 3.4 kbps data

Table 34: Physical channel parameters for multiplexing of 12.2 kbps data and 3.4 kbps data

Midamble	512 chips
Codes and time slots	SF16 x 2 code x 1 time slot
TFCI	16 bit~~s per user~~
TPC	0 bit

4.2.1.3.2.3 Example for multiplexing of 28.8/57.6 kbps data 3.4 kbps data

NOTE: This example can be applied to multiplexing of Modem/FAX and DCCH.

Table 35 shows example of physical channel parameters for multiplexing of 28.8/57.6 kbps data and 3.4 kbps data.

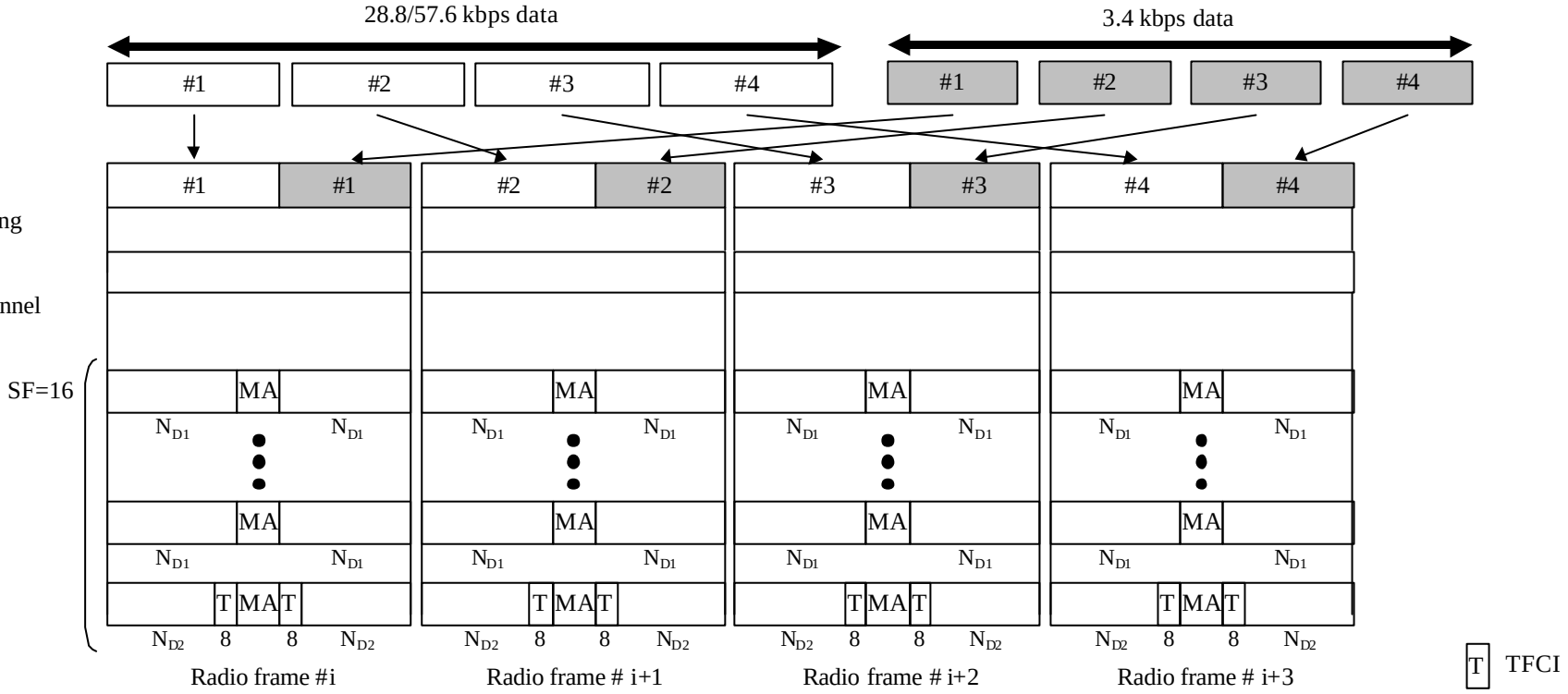

Figure 40: Channel coding and multiplexing example for multiplexing 28.8/57.6 kbps data and 3.4 kbps data

Table 35: Physical channel parameters for multiplexing of 28.8/57.6 kbps packet data and 3.4 kbps data

Midamble	28.8/57.6 kbps	512 chips
N_{D1}, N_{D2}	28.8/57.6 kbps	122 bits, 114 bits
Code & time	28.8 kbps	SF16 x 2 codes x 1 time slot
slots	57.6 kbps	SF16 x 4 codes x 1 time slot
TFCI		16 bits per user
TPC		0 bit

4.2.1.3.2.4 Example for multiplexing of 64/128/144/384 kbps packet data and 3.4 kbps data

NOTE: This example can be applied to multiplexing 64/128/ 144/384 kbps packet data and DCCH.

Table 36 shows example of physical channel parameters for multiplexing of 64/128/ 144/384 kbps packet data and 3.4 kbps data.

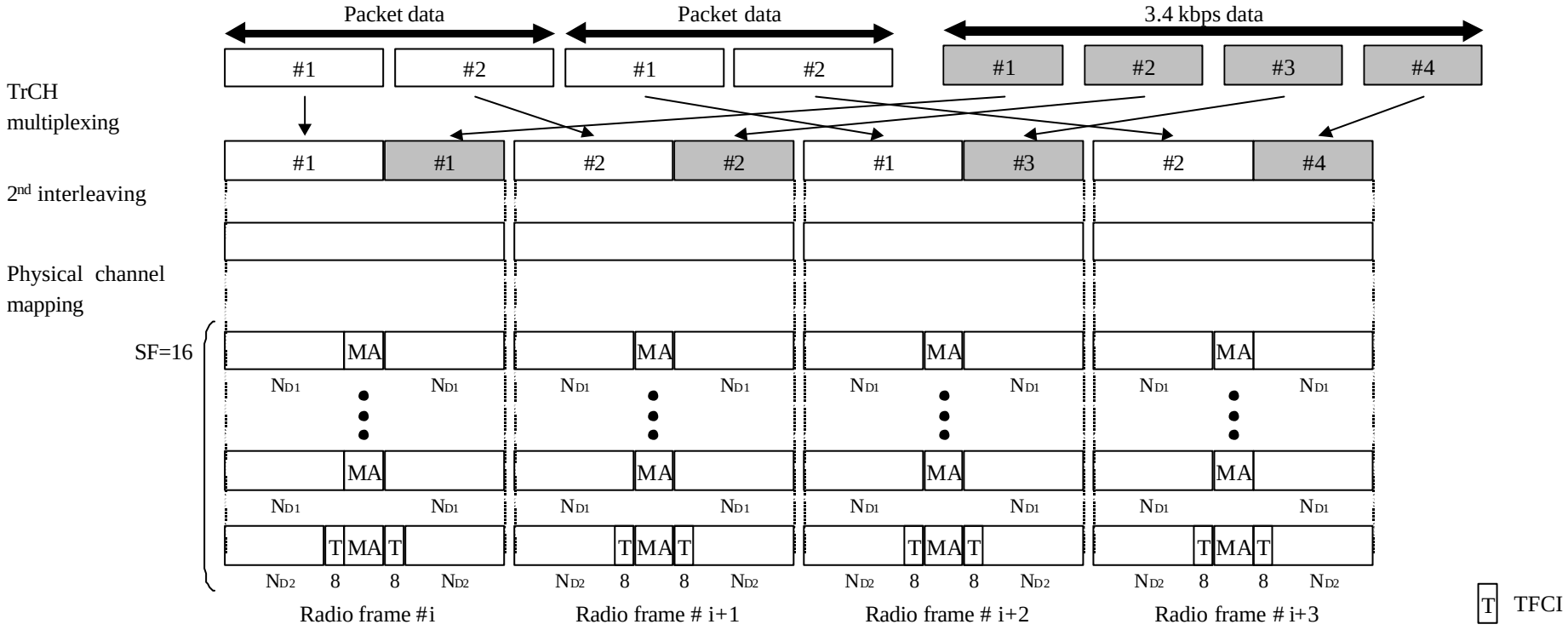

Figure 41: Channel coding and multiplexing example for multiplexing of 64/128/144/384 kbps packet data and 3.4 kbps data

Table 36: Physical channel parameters for multiplexing of 64/128/144/384 kbps packet data and 3.4 kbps data

Midamble	64 kbps	512 chips
	128 & 144 & 384 kbps	256 chips
N_{D1}, N_{D2}	64 kbps	122 bits, 114 bits
	128 & 144 & 384 kbps	138 bits, 130 bits
Code & time	64 kbps	SF16 x 5 codes x 1 time slot
slots	128 kbps	SF16 x 8 codes x 1 time slot
	144 kbps	SF16 x 9 codes x 1 time slot
	384 kbps	SF16 x 8 codes x 3 time slots
TFCI		16 bits per user
TPC		0 bit

4.2.1.3.2.5 Example for multiplexing of 64 kbps data and 3.4 kbps data

NOTE: This example can be applied to multiplexing ISDNs data and DCCH.

Table 37 shows example of physical channel parameters for multiplexing of 64 kbps data and 3.4 kbps data.

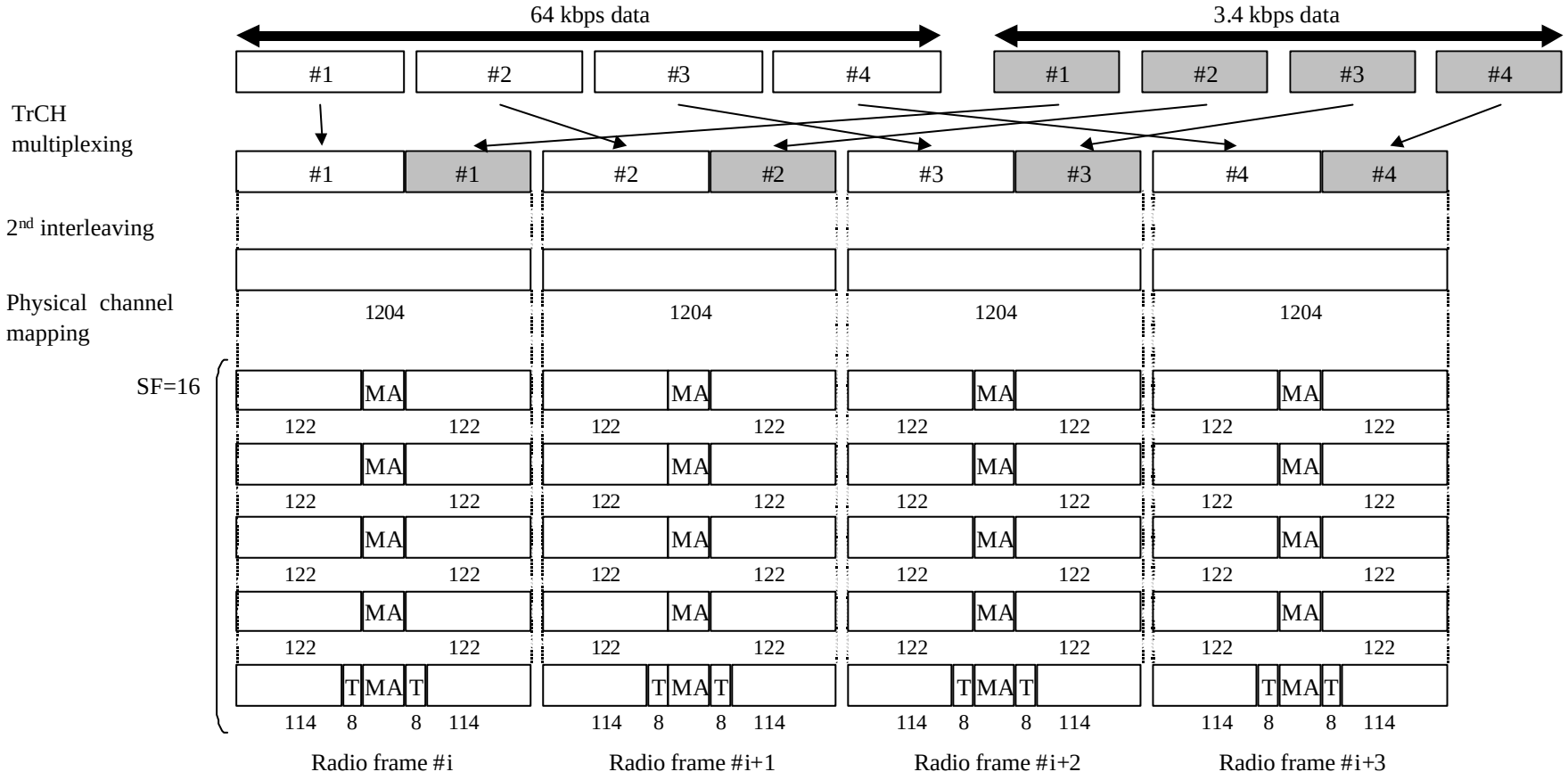

Figure 42: Channel coding and multiplexing example for multiplexing of 64 kbps data and 3.4 kbps data

Table 37: Physical channel parameters for multiplexing of 64 kbps packet data and 3.4 kbps data

Midamble	512 chips
Code & time slots	SF16 x 5 codes x 1 time slot
TFCI	16 bits ~~per user~~
TPC	0 bit

4.2.2 Uplink

4.2.2.1 RACH

Table 39: Parameters for RACH

Transport block size	N_{RACH}=168 ~~or 360~~ bit~~s~~
CRC	16 bit~~s~~
Coding	CC, coding rate = 1/2
TTI	10 ms
Midamble	512 chips
Codes and time slots	SF = 16 x 1 x 1 time slot or SF = 8 x 1 x 1 time slot
TFCI	0 bit
TPC	0 bit

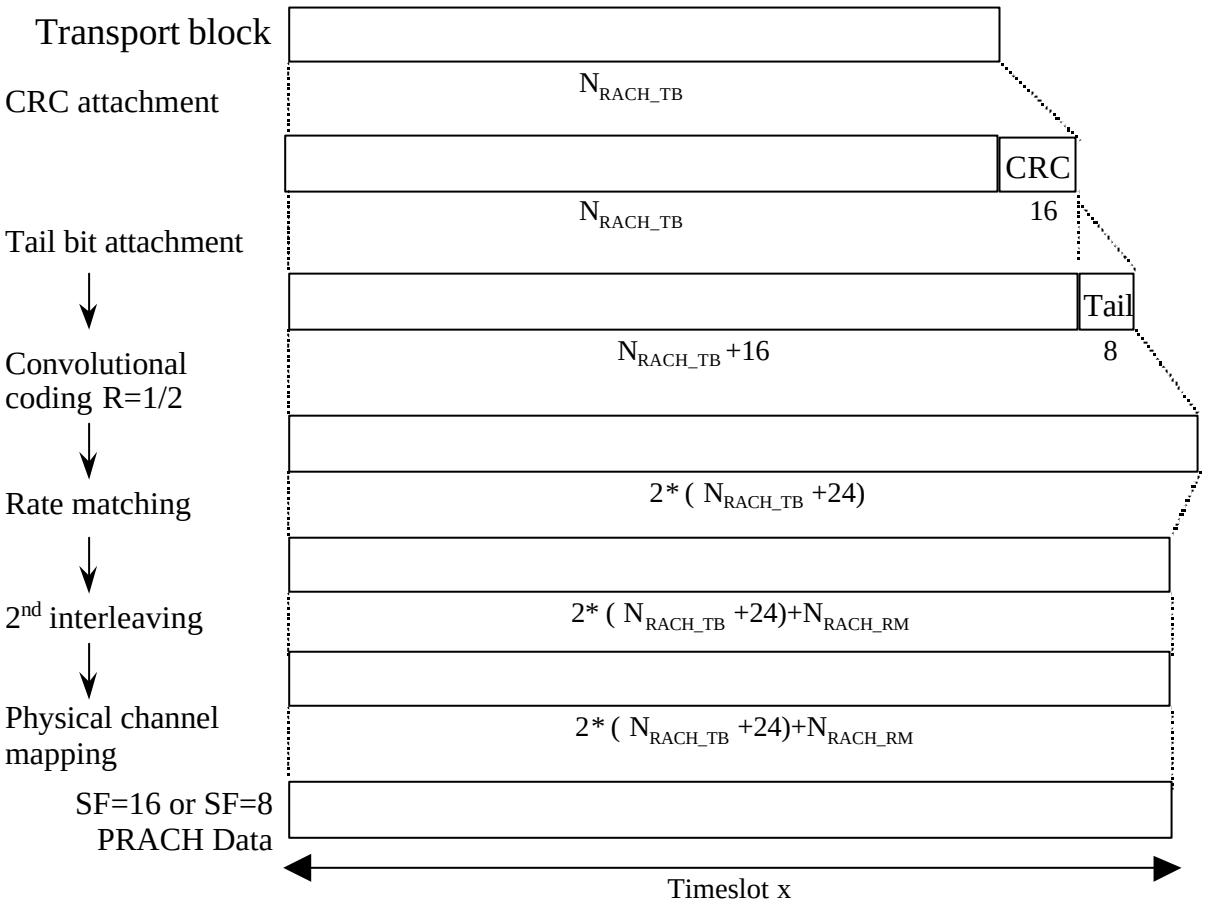

Figure 44: Channel coding and multiplexing example for PRACH

4.2.2.2.2.2 Example for multiplexing of 12.2 kbps data and 3.4 kbps data

NOTE: This example can be applied to multiplexing AMR speech and DCCH.

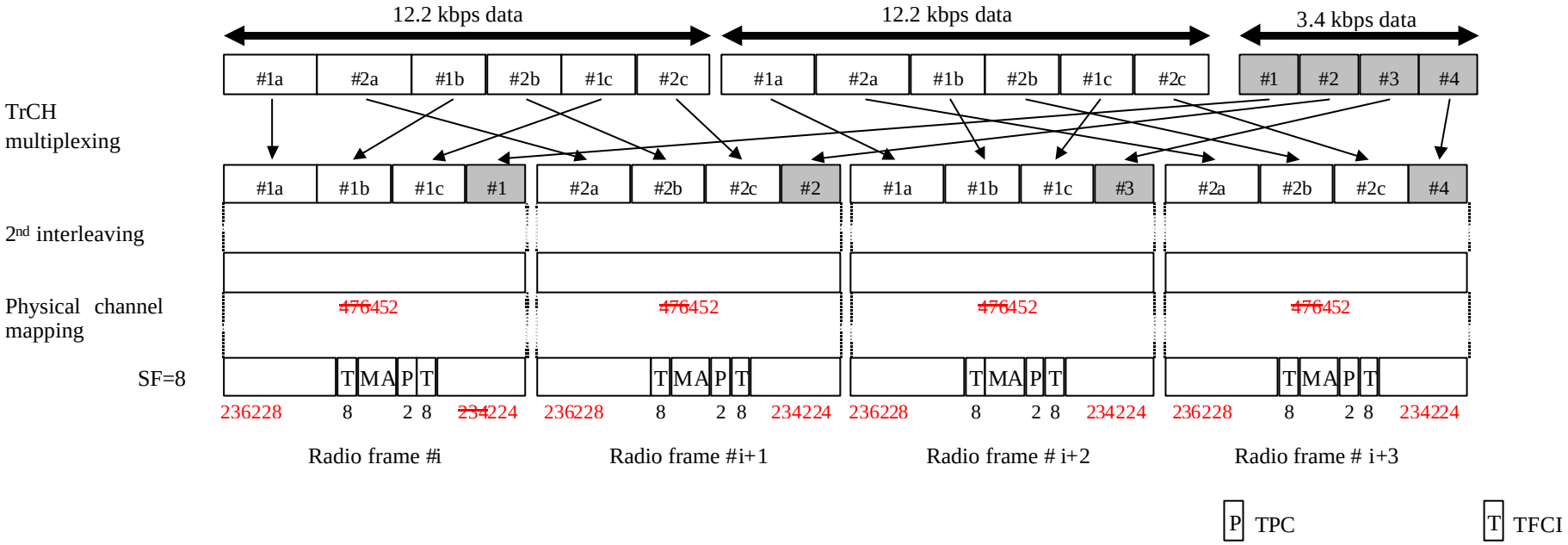

Figure 46: Channel coding and multiplexing example for multiplexing of 12.2 kbps data and 3.4 kbps data

Table 40: Physical channel parameters for multiplexing of 12.2 kbps data and 3.4 kbps data

Midamble	512 chips
Codes and time slots	SF8 x 1 code x 1 time slot
TFCI	16 bit~~s per user~~
TPC	2 bit

4.2.2.2.2.3 Example for multiplexing of 28.8/57.6 kbps data and 3.4 kbps data

NOTE: This example can be applied to multiplexing of Modem/FAX and DCCH.

Table 41 shows example of physical channel parameters for multiplexing of 28.8/57.6 kbps data and 3.4 kbps data.

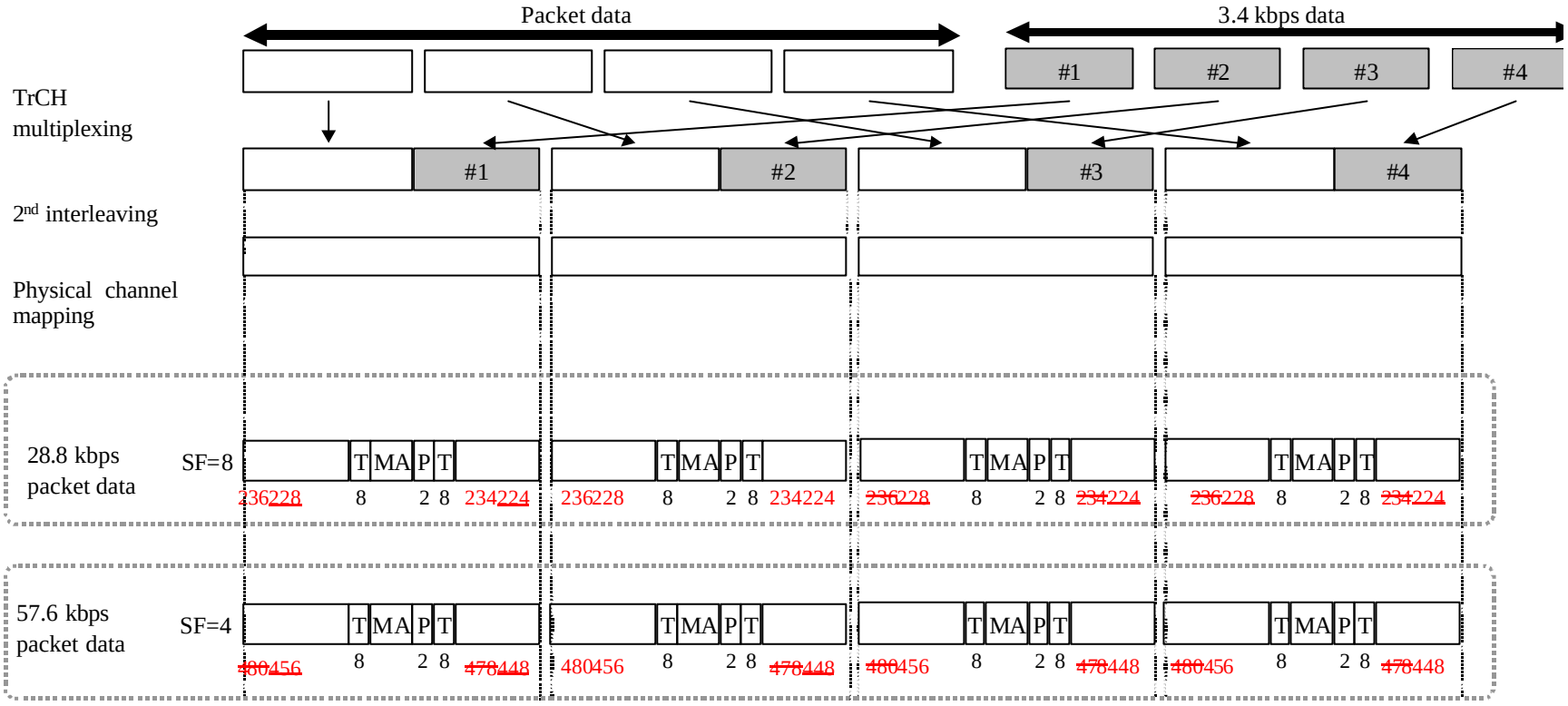

Figure 47: Channel coding and multiplexing example for multiplexing of 28.8/57.6 kbps data and 3.4 kbps data

Table 41: Physical channel parameters for multiplexing of 28.8/57.6 kbps data and 3.4 kbps data

Midamble	28.8/57.6 kbps	512 chips
Codes & time slots	28.8 kbps	(SF8 x 1 code) x 1 time slot
	57.6 kbps	(SF4 x 1 code) x 1 time slot
TFCI		16 bits ~~per user~~
TPC		2 bit

4.2.2.2.2.4 Example for multiplexing of 64/128/144/384 kbps packet data and 3.4 kbps data

NOTE: This example can be applied to multiplexing 64/128/ 144/384 kbps packet data and DCCH.

Table 42 shows example of physical channel parameters for multiplexing of 64/128/ 144/384 kbps packet data and 3.4 kbps data.

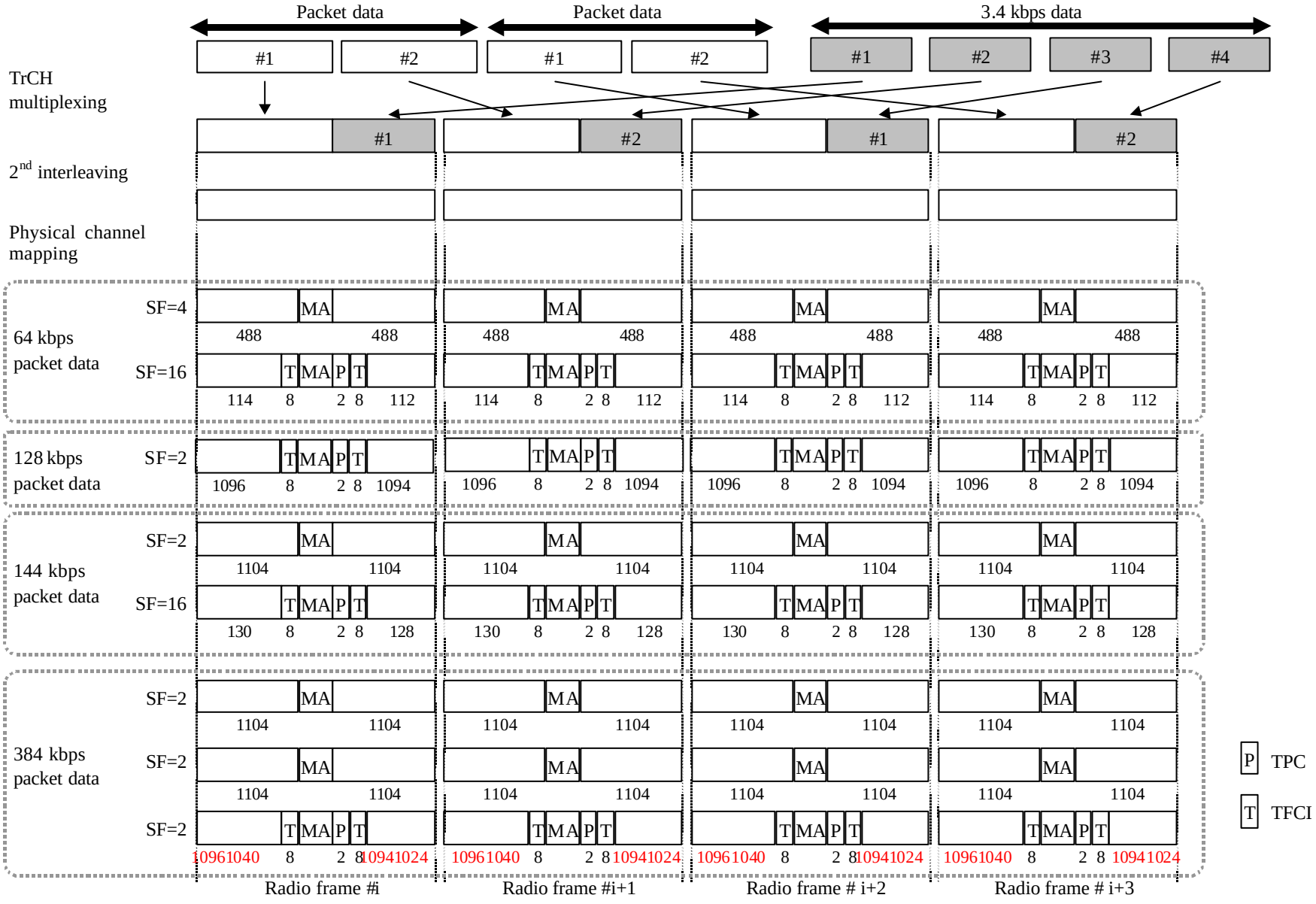
Packet data
Packet data
3.4 kbps data
#1
#2
#1
#2
#1
#2
#3
#4
TrCH multiplexing
2nd interleaving
Physical channel mapping
64 kbps packet data
SF=4
SF=16
128 kbps packet data
SF=2
144 kbps packet data
SF=2
SF=16
384 kbps packet data
SF=2
SF=2
SF=2
MA
T
P
488
114
8
2
112
1096
1094
1104
130
128
10961040
10941024
Radio frame #i
Radio frame #i+1
Radio frame # i+2
Radio frame # i+3
P TPC
T TFCI

Figure 48: Channel coding and multiplexing example for multiplexing of 64/128/144/384 kbps packet data and 3.4 kbps data

Table 42: Physical channel parameters for multiplexing of 64/128/144/384 kbps packet data and 3.4 kbps data

Midamble	64 kbps	512 chips
	128 & 144 & 384 kbps	256 chips
Codes & time	64 kbps	{(SF16 x 1 code) + (SF4 x 1 code)} x 1 time slot
slots	128 kbps	(SF2 x 1 code) x 1 time slot
	144 kbps	{(SF16 x 1 code) + (SF2 x 1 code)} x 1 time slot
	384 kbps	SF2 x 1 code x 3 time slot
TFCI		16 bits ~~per user~~
TPC		2 bit

NOTE: As an additional example, physical channels can also be mapped without using multicode per timeslot, e.g.:

for 64kbps: (SF16 x 1 code x 1 timeslot) + (SF4x 1 code x 1 timeslot)

for 64kbps: (SF2 x 1 code x 1 timeslot)

for 144kbps: (SF16 x 1 code x 1 timeslot) + (SF2x 1 code x 1 timeslot)

for 144kbps: (SF1 x 1 code x 1 timeslot)

4.2.2.2.2.5 Example for multiplexing of 64 kbps data and 3.4 kbps data

NOTE: This example can be applied to multiplexing ISDNs data and DCCH.

Table 43 shows example of physical channel parameters for multiplexing of 64 kbps data and 3.4 kbps data.

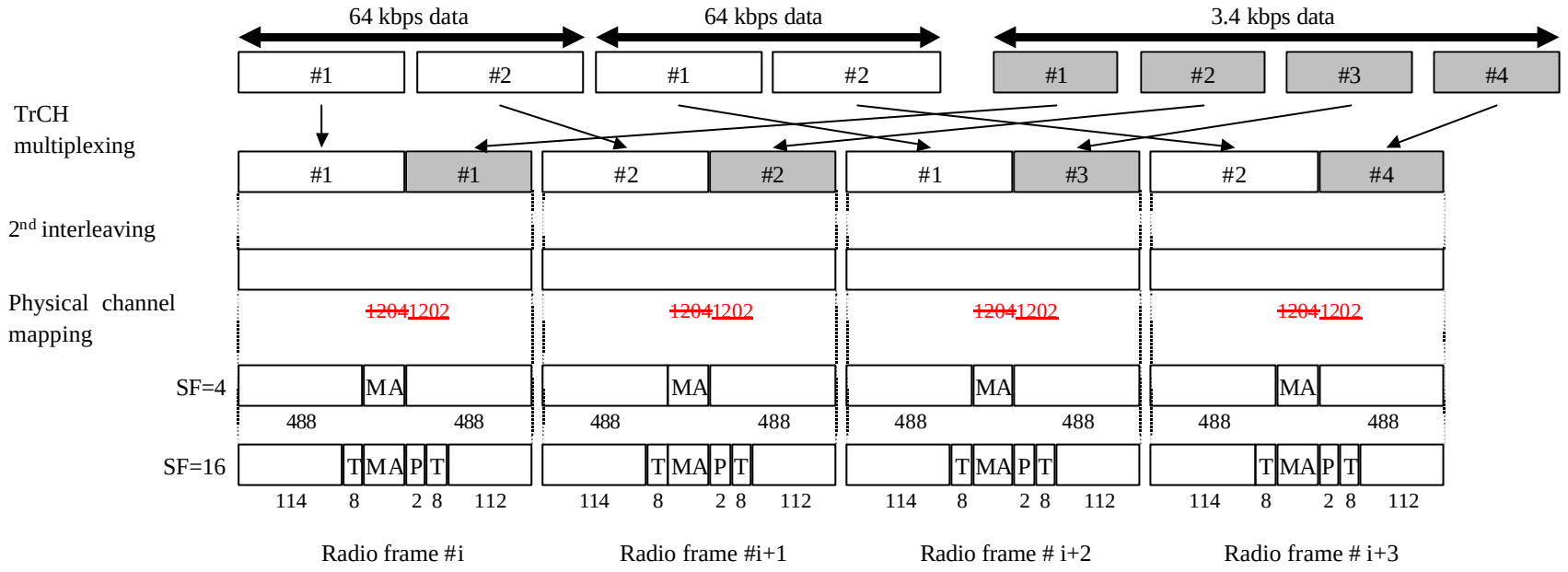

Figure 49: Channel coding and multiplexing example for multiplexing of 64 kbps packet data and 3.4 kbps data

Table 43: Physical channel parameters for multiplexing of 64 kbps packet data and 3.4 kbps data

Midamble	512 chips
Codes & time slots	{(SF16 x 1 code) + (SF4 x 1 code)} x 1 time slot
TFCI	16 bit~~s per user~~
TPC	2 bit

NOTE: As an additional example, physical channels can also be mapped without using multicode per timeslot, e.g.

for 64kbps: (SF16 x 1 code x 1 timeslot) + (SF4 x 1 code x 1 timeslot)

for 64kbps: (SF2 x 1 code x 1 timeslot)