3GPP TSG RAN WG1 Meeting #12
Seoul, Korea, Apr 10 – 13, 2000

Document R1-00-0559
e.g. for 3GPP use the format TP-99xxx
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25.211	CR	047r2	Current Version:	3.2.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

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Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)* (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]

Source: Philips **Date:** 2000-04-12

Subject: Clarifications to power control preamble sections

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	[X]	**Release:**	Phase 2	[ ]
A	Corresponds to a correction in an earlier release	[ ]		Release 96	[ ]
B	Addition of feature	[ ]		Release 97	[ ]
C	Functional modification of feature	[ ]		Release 98	[ ]
D	Editorial modification	[ ]		Release 99	[X]
				Release 00	[ ]

Reason for change: Clarification of slot and pilot formats for power control preambles in both DCH and CPCH.

Clauses affected: 5.2.1, 5.2.2.2.4, 5.2.2.2.5

Other specs affected:

Other 3G core specifications	[ ]	→ List of CRs:
Other GSM core specifications	[ ]	→ List of CRs:
MS test specifications	[ ]	→ List of CRs:
BSS test specifications	[ ]	→ List of CRs:
O&M specifications	[ ]	→ List of CRs:

Other comments:


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5.2 Uplink physical channels

5.2.1 Dedicated uplink physical channels

There are two types of uplink dedicated physical channels, the uplink Dedicated Physical Data Channel (uplink DPDCH) and the uplink Dedicated Physical Control Channel (uplink DPCCH).

The DPDCH and the DPCCH are I/Q code multiplexed within each radio frame (see [4]).

The uplink DPDCH is used to carry the DCH transport channel. There may be zero, one, or several uplink DPDCHs on each radio link.

The uplink DPCCH is used to carry control information generated at Layer 1. The Layer 1 control information consists of known pilot bits to support channel estimation for coherent detection, transmit power-control (TPC) commands, feedback information (FBI), and an optional transport-format combination indicator (TFCI). The transport-format combination indicator informs the receiver about the instantaneous transport format combination of the transport channels mapped to the simultaneously transmitted uplink DPDCH radio frame. There is one and only one uplink DPCCH on each radio link.

Figure 1 shows the frame structure of the uplink dedicated physical channels. Each radio frame of length 10 ms is split into 15 slots, each of length T_{slot} = 2560 chips, corresponding to one power-control period.

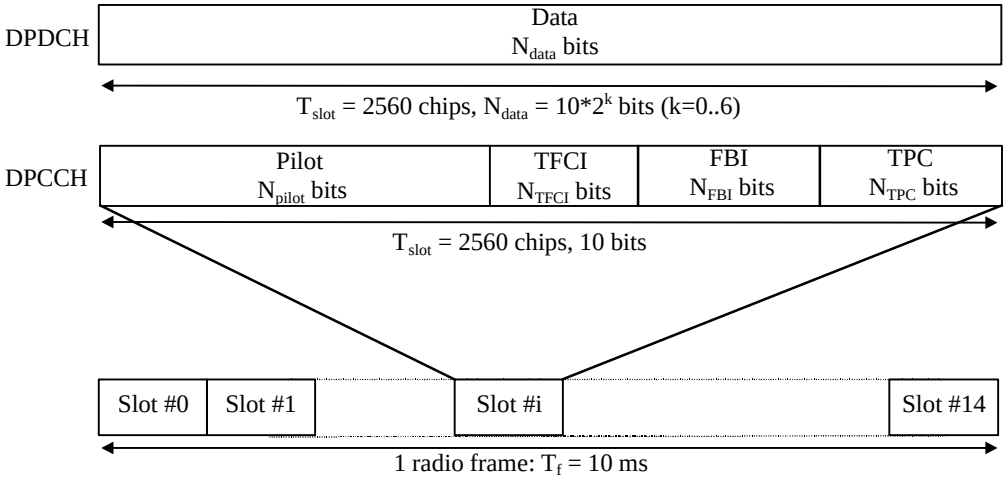

Figure 1: Frame structure for uplink DPDCH/DPCCH

The parameter k in figure 1 determines the number of bits per uplink DPDCH slot. It is related to the spreading factor SF of the DPDCH as SF = $256/2^k$. The DPDCH spreading factor may range from 256 down to 4. The spreading factor of the uplink DPCCH is always equal to 256, i.e. there are 10 bits per uplink DPCCH slot.

The exact number of bits of the uplink DPDCH and the different uplink DPCCH fields (N_{pilot}, N_{TFCI}, N_{FBI}, and N_{TPC}) is given by table 1 and table 2. What slot format to use is configured by higher layers.

The channel bit and symbol rates given in table 1 and table 2 are the rates immediately before spreading. The pilot patterns are given in table 3 and table 4, the TPC bit pattern is given in table 5.

The FBI bits are used to support techniques requiring feedback from the UE to the UTRAN Access Point, including closed loop mode transmit diversity and site selection diversity transmission (SSDT). The structure of the FBI field is shown in figure 2 and described below.

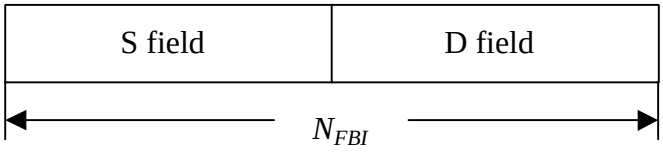

Figure 2: Details of FBI field

The S field is used for SSDT signalling, while the D field is used for closed loop mode transmit diversity signalling. The S field consists of 0, 1 or 2 bits. The D field consists of 0 or 1 bit. The total FBI field size N_{FBI} is given by table 2. Simultaneous use of SSDT power control and closed loop mode transmit diversity requires that the S field consists of 1 bit. The use of the FBI fields is described in detail in [5].

Table 1: DPDCH fields

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}
0	15	15	256	150	10	10
1	30	30	128	300	20	20
2	60	60	64	600	40	40
3	120	120	32	1200	80	80
4	240	240	16	2400	160	160
5	480	480	8	4800	320	320
6	960	960	4	9600	640	640

There are two types of uplink dedicated physical channels; those that include TFCI (e.g. for several simultaneous services) and those that do not include TFCI (e.g. for fixed-rate services). These types are reflected by the duplicated rows of table 2. It is the UTRAN that determines if a TFCI should be transmitted and it is mandatory for all UEs to support the use of TFCI in the uplink. The mapping of TFCI bits onto slots is described in [3].

In compressed mode, DPCCH slot formats with TFCI fields are changed. There are two possible compressed slot formats for each normal slot format. They are labelled A and B and the selection between them is dependent on the number of slots that are transmitted in each frame in compressed mode.

Table 2: DPCCH fields

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{pilot}	N_{TPC}	N_{TFCI}	N_{FBI}	Transmitted slots per radio frame
0	15	15	256	150	10	6	2	2	0	15
0A	15	15	256	150	10	5	2	3	0	10-14
0B	15	15	256	150	10	4	2	4	0	8-9
1	15	15	256	150	10	8	2	0	0	8-15
2	15	15	256	150	10	5	2	2	1	15
2A	15	15	256	150	10	4	2	3	1	10-14
2B	15	15	256	150	10	3	2	4	1	8-9
3	15	15	256	150	10	7	2	0	1	8-15
4	15	15	256	150	10	6	2	0	2	8-15
5	15	15	256	150	10	5	1	2	2	15
5A	15	15	256	150	10	4	1	3	2	10-14
5B	15	15	256	150	10	3	1	4	2	8-9

The pilot bit patterns are described in table 3 and table 4. The shadowed column part of pilot bit pattern is defined as FSW and FSWs can be used to confirm frame synchronization. (The value of the pilot bit pattern other than FSWs shall be "1".)

Table 3: Pilot bit patterns for uplink DPCCH with N_{pilot} = 3, 4, 5 and 6

	N_{pilot} = 3			N_{pilot} = 4				N_{pilot} = 5					N_{pilot} = 6					
Bit #	0	1	2	0	1	2	3	0	1	2	3	4	0	1	2	3	4	5
Slot #0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0
1	0	0	1	1	0	0	1	0	0	1	1	0	1	0	0	1	1	0
2	0	1	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1
3	0	0	1	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0
4	1	0	1	1	1	0	1	1	0	1	0	1	1	1	0	1	0	1
5	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0
6	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	0	0
7	1	0	1	1	1	0	1	1	0	1	0	0	1	1	0	1	0	0
8	0	1	1	1	0	1	1	0	1	1	1	0	1	0	1	1	1	0
9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	0	1	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1
11	1	0	1	1	1	0	1	1	0	1	1	1	1	1	0	1	1	1
12	1	0	1	1	1	0	1	1	0	1	0	0	1	1	0	1	0	0
13	0	0	1	1	0	0	1	0	0	1	1	1	1	0	0	1	1	1
14	0	0	1	1	0	0	1	0	0	1	1	1	1	0	0	1	1	1

Table 4: Pilot bit patterns for uplink DPCCH with N_{pilot} = 7 and 8

	N_{pilot} = 7							N_{pilot} = 8							
Bit #	0	1	2	3	4	5	6	0	1	2	3	4	5	6	7
Slot #0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0
1	1	0	0	1	1	0	1	1	0	1	0	1	1	1	0
2	1	0	1	1	0	1	1	1	0	1	1	1	0	1	1
3	1	0	0	1	0	0	1	1	0	1	0	1	0	1	0
4	1	1	0	1	0	1	1	1	1	1	0	1	0	1	1
5	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0
6	1	1	1	1	0	0	1	1	1	1	1	1	0	1	0
7	1	1	0	1	0	0	1	1	1	1	0	1	0	1	0
8	1	0	1	1	1	0	1	1	0	1	1	1	1	1	0
9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	1	0	1	1	0	1	1	1	0	1	1	1	0	1	1
11	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
12	1	1	0	1	0	0	1	1	1	1	0	1	0	1	0
13	1	0	0	1	1	1	1	1	0	1	0	1	1	1	1
14	1	0	0	1	1	1	1	1	0	1	0	1	1	1	1

The relationship between the TPC bit pattern and transmitter power control command is presented in table 5.

Table 5: TPC Bit Pattern

TPC Bit Pattern		Transmitter power control command
N_{TPC} = 1	N_{TPC} = 2	
1	11	1
0	00	0

Multi-code operation is possible for the uplink dedicated physical channels. When multi-code transmission is used, several parallel DPDCH are transmitted using different channelization codes, see [4]. However, there is only one DPCCH per radio link.

A power control preamble may be used for initialisation of a DCH. Both the UL and DL DPCCHs shall be transmitted during the power control preamble. The length of the power control preamble is a UE-specific higher layer parameter, N_{pcp} (see [5], section 5.1.2.4), signalled by the network, and can take the value 0 slots or 8 slots. The UL DPCCH shall take the same slot format in the power control preamble as afterwards, as given in table 2. When, $N_{pcp} > 0$ the pilot patterns from slot #(15- N_{pcp}) to slot #14 of table 3 and table 4 shall be used. The timing of the power control preamble is shown in Figure 32 in subclause 7.7.

5.2.2 Common uplink physical channels

5.2.2.1 Physical Random Access Channel (PRACH)

The Physical Random Access Channel (PRACH) is used to carry the RACH.

5.2.2.1.1 Overall structure of random-access transmission

The random-access transmission is based on a Slotted ALOHA approach with fast acquisition indication. The UE can start the random-access transmission at the beginning of a number of well-defined time intervals, denoted *access slots.* There are 15 access slots per two frames and they are spaced 5120 chips apart, see figure 3. The timing of the access slots and the acquisition indication is described in subclause 7.3. Information on what access slots are available for random-access transmission is given by higher layers.

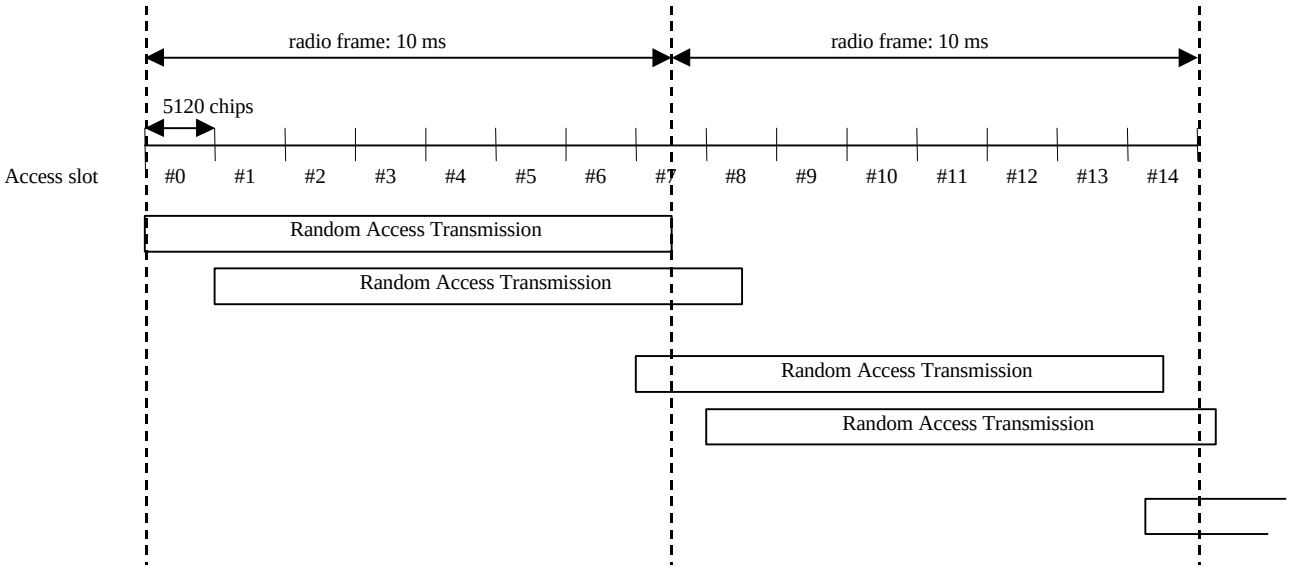

Figure 3: RACH access slot numbers and their spacing

The structure of the random-access transmission is shown in figure 4. The random-access transmission consists of one or several *preambles* of length 4096 chips and a *message* of length 10 ms or 20 ms.

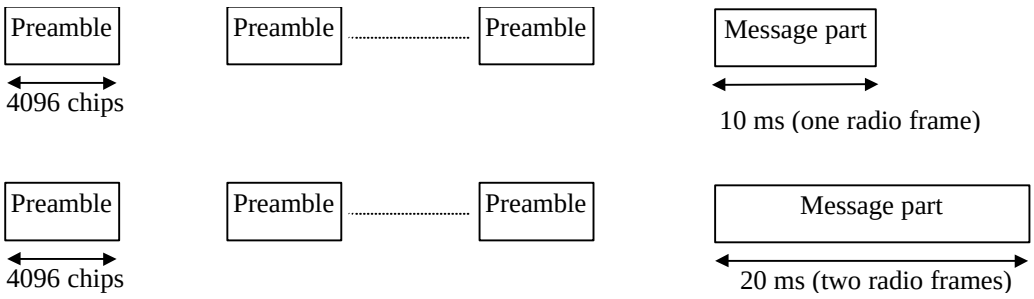

Figure 4: Structure of the random-access transmission

5.2.2.1.2 RACH preamble part

Each preamble is of length 4096 chips and consists of 256 repetitions of a signature of length 16 chips. There are a maximum of 16 available signatures, see [4] for more details.

5.2.2.1.3 RACH message part

Figure 5 shows the structure of the random-access message part radio frame. The 10 ms message part radio frame is split into 15 slots, each of length T_{slot} = 2560 chips. Each slot consists of two parts, a data part to which theRACH transport channel is mapped and a control part that carries Layer 1 control information. The data and control parts are transmitted in parallel. A 10 ms message part consists of one message part radio frame, while a 20 ms message part consists of two consecutive 10 ms message part radio frames. The message part length can be determined from the used signature and/or access slot, as configured by higher layers.

The data part consists of $10*2^k$ bits, where k=0,1,2,3. This corresponds to a spreading factor of 256, 128, 64, and 32 respectively for the message data part.

The control part consists of 8 known pilot bits to support channel estimation for coherent detection and 2 TFCI bits. This corresponds to a spreading factor of 256 for the message control part. The pilot bit pattern is described in table 8. The total number of TFCI bits in the random-access message is 15*2 = 30. The TFCI of a radio frame indicates the transport format of the RACH transport channel mapped to the simultaneously transmitted message part radio frame. In case of a 20 ms PRACH message part, the TFCI is repeated in the second radio frame.

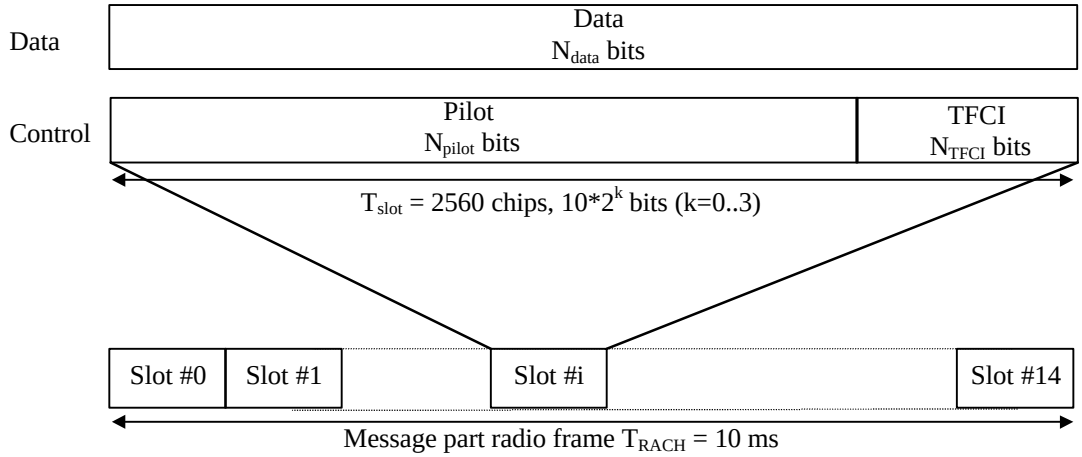

Figure 5: Structure of the random-access message part radio frame

Table 6: Random-access message data fields

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}
0	15	15	256	150	10	10
1	30	30	128	300	20	20
2	60	60	64	600	40	40
3	120	120	32	1200	80	80

Table 7: Random-access message control fields

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{pilot}	N_{TFCI}
0	15	15	256	150	10	8	2

Table 8: Pilot bit patterns for RACH message part with N_{pilot} = 8

	N_{pilot} = 8							
Bit #	0	1	2	3	4	5	6	7
Slot #0	1	1	1	1	1	1	1	0
1	1	0	1	0	1	1	1	0
2	1	0	1	1	1	0	1	1
3	1	0	1	0	1	0	1	0
4	1	1	1	0	1	0	1	1
5	1	1	1	1	1	1	1	0
6	1	1	1	1	1	0	1	0
7	1	1	1	0	1	0	1	0
8	1	0	1	1	1	1	1	0
9	1	1	1	1	1	1	1	1
10	1	0	1	1	1	0	1	1
11	1	1	1	0	1	1	1	1
12	1	1	1	0	1	0	1	0
13	1	0	1	0	1	1	1	1
14	1	0	1	0	1	1	1	1

5.2.2.2 Physical Common Packet Channel (PCPCH)

The Physical Common Packet Channel (PCPCH) is used to carry the CPCH.

5.2.2.2.1 CPCH transmission

The CPCH transmission is based on DSMA-CD approach with fast acquisition indication. The UE can start transmission at the beginning of a number of well-defined time-intervals, relative to the frame boundary of the received BCH of the current cell. The access slot timing and structure is identical to RACH in subclause 5.2.2.1.1. The structure of the CPCH access transmission is shown in figure 6. The PCPCH access transmission consists of one or several Access Preambles [A-P] of length 4096 chips, one Collision Detection Preamble (CD-P) of length 4096 chips, a DPCCH Power Control Preamble (PC-P) which is either 0 slots or 8 slots in length, and a message of variable length Nx10 ms.

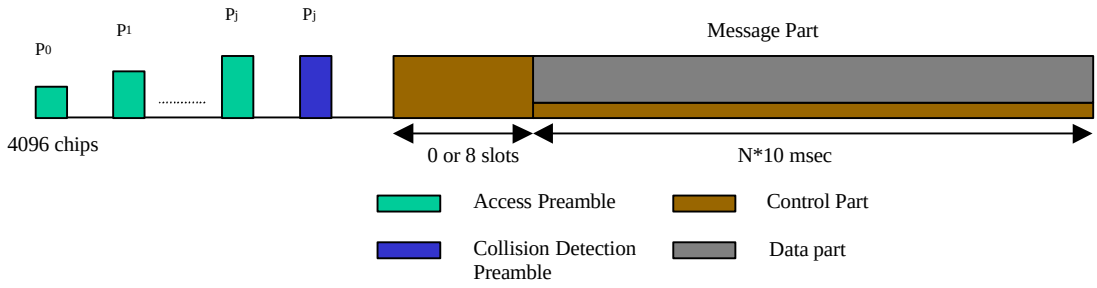

Figure 6: Structure of the CPCH access transmission

5.2.2.2.2 CPCH access preamble part

Similar to 5.2.2.1.2 (RACH preamble part). The RACH preamble signature sequences are used. The number of sequences used could be less than the ones used in the RACH preamble. The scrambling code could either be chosen to be a different code segment of the Gold code used to form the scrambling code of the RACH preambles (see [4] for more details) or could be the same scrambling code in case the signature set is shared.

5.2.2.2.3 CPCH collision detection preamble part

Similar to 5.2.2.1.2 (RACH preamble part). The RACH preamble signature sequences are used. The scrambling code is chosen to be a different code segment of the Gold code used to form the scrambling code for the RACH and CPCH preambles (see [4] for more details).

5.2.2.2.4 CPCH power control preamble part

The power control preamble segment is called the CPCH Power Control Preamble (PC-P) part. T~~able 9 defines t~~he ~~DPCCH fields~~slot format for CPCH PC-P part shall be the same as for the start of the following message part~~and this is identical to slot formats 0, 1, 2, 3, 4, and 5 of table 2 in subclause 5.2.1~~. The Power Control Preamble length is a higher layer parameter, $L_{pc\text{-}preamble}$ (see [5], section 6.2), which shall take the value~~s~~ 0 or 8 slots~~, as set by the higher layers~~. When $L_{pc\text{-}preamble} > 0$, t~~T~~he pilot bit patterns from slot #(15- $L_{pc\text{-}preamble}$) ~~0~~ to slot #14~~7~~ of table 3 and 4 in subclause 5.2.1 shall be used for CPCH PC-P pilot bit patterns ~~when the power control preamble length is set to 8 slots~~.

~~Table 9: DPCCH fields for CPCH power control preamble segment~~

~~Slot Format #i~~	~~Channel Bit Rate (kbps)~~	~~Channel Symbol Rate (ksps)~~	~~SF~~	~~Bits/ Frame~~	~~Bits/ Slot~~	~~N_{pilot}~~	~~N_{TPC}~~	~~N_{TFCI}~~	~~N_{FBI}~~
~~0~~	~~15~~	~~15~~	~~256~~	~~150~~	~~10~~	~~6~~	~~2~~	~~2~~	~~0~~
~~1~~	~~15~~	~~15~~	~~256~~	~~150~~	~~10~~	~~8~~	~~2~~	~~0~~	~~0~~
~~2~~	~~15~~	~~15~~	~~256~~	~~150~~	~~10~~	~~5~~	~~2~~	~~2~~	~~1~~
~~3~~	~~15~~	~~15~~	~~256~~	~~150~~	~~10~~	~~7~~	~~2~~	~~0~~	~~1~~
~~4~~	~~15~~	~~15~~	~~256~~	~~150~~	~~10~~	~~6~~	~~2~~	~~0~~	~~2~~
~~5~~	~~15~~	~~15~~	~~256~~	~~150~~	~~10~~	~~5~~	~~1~~	~~2~~	~~2~~

5.2.2.2.5 CPCH message part

Figure 1 in subclause 5.2.1 shows the structure of the CPCH message part. Each message consists of up to N_Max_frames 10 ms frames. N_Max_frames is a higher layer parameter. Each 10 ms frame is split into 15 slots, each of length T_{slot} = 2560 chips. Each slot consists of two parts, a data part that carries higher layer information and a control part that carries Layer 1 control information. The data and control parts are transmitted in parallel.

The entries of table 1 in subclause 5.2.1 apply to the data part of the CPCH message part. The spreading factor for the control part of the CPCH message part shall be 256. Table 9 defines the slot format of the control part of CPCH message part ~~shall be the same as the control part of CPCH PC-P~~. The pilot bit patterns of table 3 and 4 in subclause 5.2.1 shall be used for pilot bit patterns of the CPCH message part.

Table 9: DPCCH fields for CPCH power control preamble segment

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{pilot}	N_{TPC}	N_{TFCI}	N_{FBI}
0	15	15	256	150	10	6	2	2	0
1	15	15	256	150	10	8	2	0	0
2	15	15	256	150	10	5	2	2	1
3	15	15	256	150	10	7	2	0	1
4	15	15	256	150	10	6	2	0	2
5	15	15	256	150	10	5	1	2	2

Figure 7 shows the frame structure of the uplink common packet physical channel. Each frame of length 10 ms is split into 15 slots, each of length T_{slot} = 2560 chips, corresponding to one power-control period.

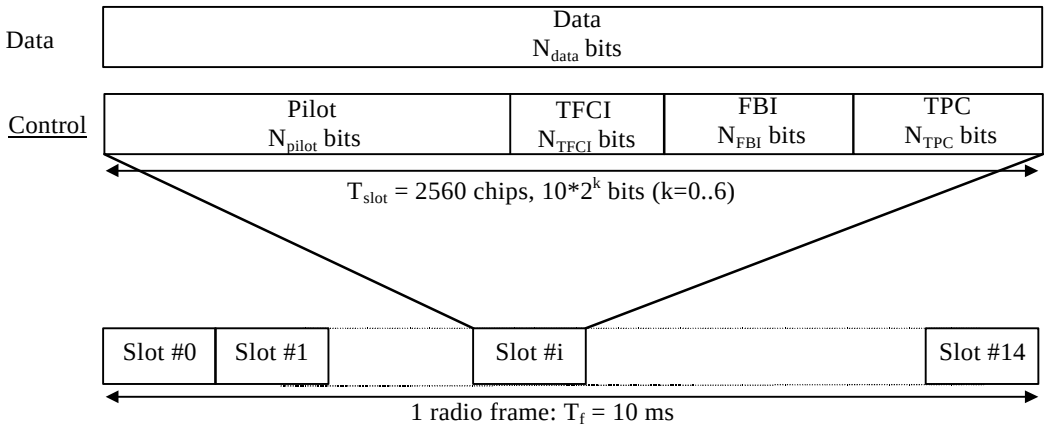

Figure 7: Frame structure for uplink Data and Control Parts Associated with PCPCH

The data part consists of $10*2^k$ bits, where k = 0, 1, 2, 3, 4, 5, 6, corresponding to spreading factors of 256, 128, 64, 32, 16, 8, 4 respectively.

~~The entries of table 1 in subclause 5.2.1 apply to the data part of the CPCH message part. The spreading factor for the control part of the CPCH message part shall be 256. The slot format of the control part of CPCH message part shall be the same as the control part of CPCH PC-P. The pilot bit patterns of table 3 and 4 in subclause 5.2.1 shall be used for pilot bit patterns of the CPCH message part.~~

3GPP TSG RAN WG1 Meeting #12
Seoul, Korea, Apr 10 – 13, 2000

Document R1-00-0559
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25.213	CR	033	Current Version:	3.2.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to:	TSG-RAN #8	for approval	X	strategic		(for SMG use only)
list expected approval meeting # here ↑		for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)*	(U)SIM		ME	X	UTRAN / Radio	X	Core Network	

Source: Philips **Date:** 2000-04-05

Subject: Clarifications to power control preamble sections

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	X	**Release:**	Phase 2	
A	Corresponds to a correction in an earlier release			Release 96	
B	Addition of feature			Release 97	
C	Functional modification of feature			Release 98	
D	Editorial modification			Release 99	X
				Release 00	

Reason for change: Clarification of channelisation and scrambling codes for power control preambles in DCH.

Clauses affected: 4.3.1.2,4.3.2.4

Other specs affected:

Other 3G core specifications		→ List of CRs:
Other GSM core specifications		→ List of CRs:
MS test specifications		→ List of CRs:
BSS test specifications		→ List of CRs:
O&M specifications		→ List of CRs:

Other comments:

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<--------- double-click here for help and instructions on how to create a CR.

4.3 Code generation and allocation

4.3.1 Channelization codes

4.3.1.1 Code definition

The channelization codes of figure 1 are Orthogonal Variable Spreading Factor (OVSF) codes that preserve the orthogonality between a user's different physical channels. The OVSF codes can be defined using the code tree of figure 4.

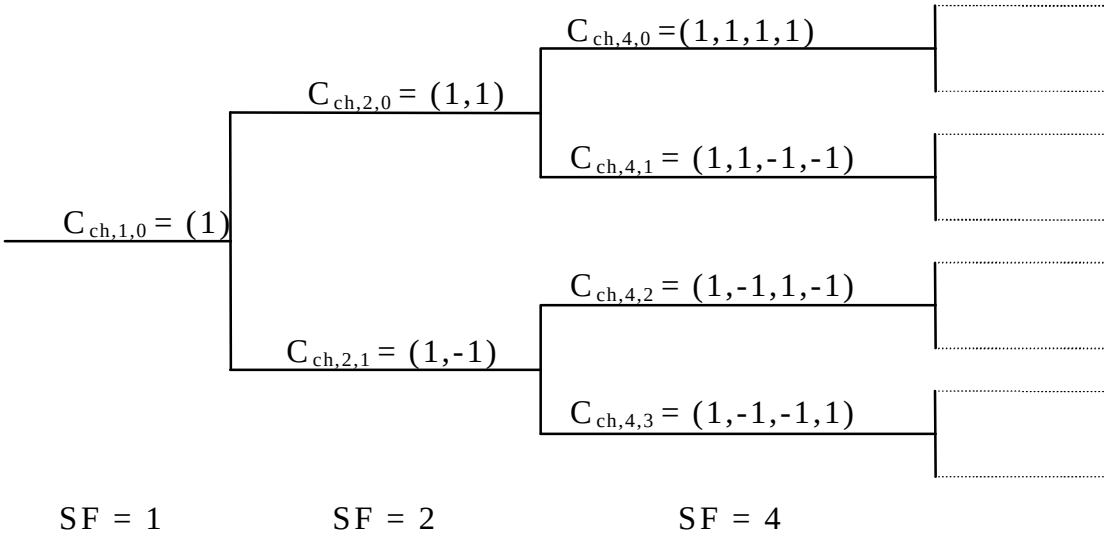

Figure 4: Code-tree for generation of Orthogonal Variable Spreading Factor (OVSF) codes

In figure 4, the channelization codes are uniquely described as $C_{ch,SF,k}$, where SF is the spreading factor of the code and *k* is the code number, $0 \le k \le SF-1$.

Each level in the code tree defines channelization codes of length SF, corresponding to a spreading factor of SF in figure 4.

The generation method for the channelization code is defined as:

$$C_{ch,1,0} = 1,$$

$$\begin{bmatrix} C_{ch,2,0} \\ C_{ch,2,1} \end{bmatrix} = \begin{bmatrix} C_{ch,1,0} & C_{ch,1,0} \\ C_{ch,1,0} & -C_{ch,1,0} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$$

$$\begin{bmatrix} C_{ch,2^{(n+1)},0} \\ C_{ch,2^{(n+1)},1} \\ C_{ch,2^{(n+1)},2} \\ C_{ch,2^{(n+1)},3} \\ \vdots \\ C_{ch,2^{(n+1)},2^{(n+1)}-2} \\ C_{ch,2^{(n+1)},2^{(n+1)}-1} \end{bmatrix} = \begin{bmatrix} C_{ch,2^n,0} & C_{ch,2^n,0} \\ C_{ch,2^n,0} & -C_{ch,2^n,0} \\ C_{ch,2^n,1} & C_{ch,2^n,1} \\ C_{ch,2^n,1} & -C_{ch,2^n,1} \\ \vdots & \vdots \\ C_{ch,2^n,2^n-1} & C_{ch,2^n,2^n-1} \\ C_{ch,2^n,2^n-1} & -C_{ch,2^n,2^n-1} \end{bmatrix}$$

The leftmost value in each channelization code word corresponds to the chip transmitted first in time.

4.3.1.2 Code allocation for DPCCH/DPDCH

For the DPCCH and DPDCHs the following applies:

- The DPCCH is always spread by code $c_c = C_{ch,256,0.}$
- When only one DPDCH is to be transmitted, $DPDCH_1$ is spread by code $c_{d,1} = C_{ch,SF,k}$ where SF is the spreading factor of $DPDCH_1$ and k= SF / 4.
- When more than one DPDCH is to be transmitted, all DPDCHs have spreading factors equal to 4. $DPDCH_n$ is spread by the the code $c_{d,n} = C_{ch,4,k}$, where $k = 1$ if $n \in \{1, 2\}$, $k = 3$ if $n \in \{3, 4\}$, and $k = 2$ if $n \in \{5, 6\}$.

If a power control preamble is used to initialise a DCH, the channelisation code for the DPCCH during the power control preamble shall be the same as that to be used afterwards.

4.3.1.3 Code allocation for PRACH message part

The preamble signature *s*, $0 \le s \le 15$, points to one of the 16 nodes in the code-tree that corresponds to channelization codes of length 16. The sub-tree below the specified node is used for spreading of the message part. The control part is spread with the channelization code c_c (as shown in section 4.2.2.2) of spreading factor 256 in the lowest branch of the sub-tree, i.e. $c_c = C_{ch,256,m}$ where $m = 16 \times s + 15$. The data part uses any of the channelization codes from spreading factor 32 to 256 in the upper-most branch of the sub-tree. To be exact, the data part is spread by channelization code $c_d = C_{ch,SF,m}$ and SF is the spreading factor used for the data part and $m = SF \times s/16$.

4.3.1.4 Code allocation for PCPCH message part

For the control part and data part the following applies:

- The control part is always spread by code $c_c = C_{ch,256,0.}$
- The data part is spread by code $c_d = C_{ch,SF,k}$ where SF is the spreading factor of the data part and k=SF/4.

The data part may use the code from spreading factor 4 to 256. A UE is allowed to increase SF during the message transmission on a frame by frame basis.

4.3.1.5 Channelisation code for PCPCH power control preamble

The channelisation code for the PCPCH power control preamble is the same as that used for the control part of the message part, as described in section 4.3.1.4 above.

4.3.2 Scrambling codes

4.3.2.1 General

All uplink physical channels are subjected to scrambling with a complex-valued scrambling code. The DPCCH/DPDCH may be scrambled by either long or short scrambling codes, defined in section 4.3.2.4. The PRACH message part is scrambled with a long scrambling code, defined in section 4.3.2.5. Also the PCPCH message part is scrambled with a long scrambling code, defined in section 4.3.2.6.

There are 2^{24} long and 2^{24} short uplink scrambling codes. Uplink scrambling codes are assigned by higher layers.

The long scrambling code is built from constituent long sequences defined in section 4.3.2.2, while the constituent short sequences used to build the short scrambling code are defined in section 4.3.2.3.

4.3.2.2 Long scrambling sequence

The long scrambling sequences $c_{long,1,n}$ and $c_{long,2,n}$ are constructed from position wise modulo 2 sum of 38400 chip segments of two binary *m*-sequences generated by means of two generator polynomials of degree 25. Let *x*, and *y* be the two *m*-sequences respectively. The *x* sequence is constructed using the primitive (over GF(2)) polynomial $X^{25}+X^3+1$. The *y* sequence is constructed using the polynomial $X^{25}+X^3+X^2+X+1$. The resulting sequences thus constitute segments of a set of Gold sequences.

The sequence $c_{long,2,n}$ is a 16777232 chip shifted version of the sequence $c_{long,1,n}$.

Let $n_{23} \ldots n_0$ be the 24 bit binary representation of the scrambling sequence number n with n_0 being the least significant bit. The x sequence depends on the chosen scrambling sequence number n and is denoted x_n, in the sequel. Furthermore, let $x_n(i)$ and $y(i)$ denote the i:th symbol of the sequence x_n and y, respectively.

The m-sequences x_n and y are constructed as:

Initial conditions:

- $x_n(0)=n_0$, $x_n(1)= n_1$, … $=x_n(22)= n_{22}$,$x_n(23)= n_{23}$, $x_n(24)=1$.
- $y(0)=y(1)= \ldots =y(23)= y(24)=1$.

Recursive definition of subsequent symbols:

- $x_n(i+25) =x_n(i+3) + x_n(i)$ modulo 2, i=0,…, 2^{25}-27.
- $y(i+25) = y(i+3)+y(i+2) +y(i+1) +y(i)$ modulo 2, i=0,…, 2^{25}-27.

Define the binary Gold sequence z_n by:

- $z_n(i) = x_n(i) + y(i)$ modulo 2, $i = 0, 1, 2, \ldots, 2^{25}-2$.

The real valued Gold sequence Z_n is defined by:

$$Z_n(i) = \begin{cases} +1 & if\ z_n(i) = 0 \\ -1 & if\ z_n(i) = 1 \end{cases} \quad for\ \ i = 0,1,\ldots,2^{25} - 2.$$

Now, the real-valued long scrambling sequences $c_{long,1,n}$ and $c_{long,2,n}$ are defined as follows:

$$c_{long,1,n}(i) = Z_n(i),\ i = 0, 1, 2, \ldots, 2^{25} - 2 \text{ and}$$

$$c_{long,2,n}(i) = Z_n((i + 16777232) \text{ modulo } (2^{25} - 1)),\ i = 0, 1, 2, \ldots, 2^{25} - 2.$$

Finally, the complex-valued long scrambling sequence $C_{long,n}$, is defined as:

$$C_{long,n}(i) = c_{long,1,n}(i)\left(1 + j(-1)^i c_{long,2,n}\left(2\lfloor i/2 \rfloor\right)\right)$$

where $i = 0, 1, \ldots, 2^{25} - 2$ and $\lfloor\ \rfloor$ denotes rounding to nearest lower integer.

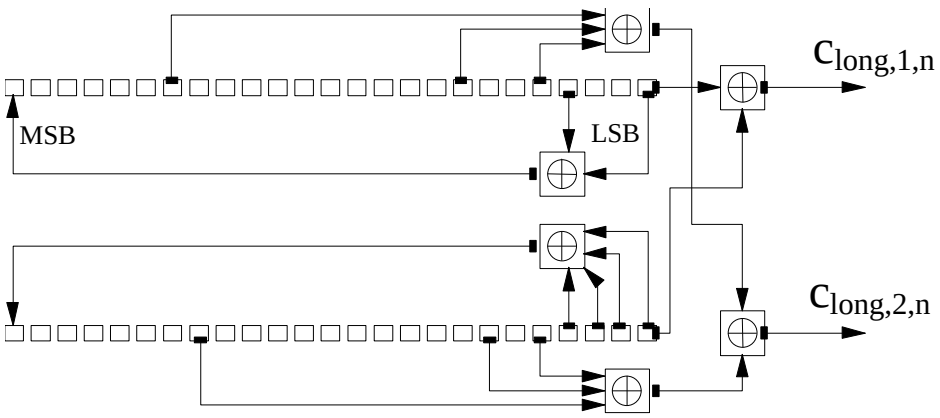

Figure 5: Configuration of uplink scrambling sequence generator

4.3.2.3 Short scrambling sequence

The short scrambling sequences $c_{short,1,n}(i)$ and $c_{short,2,n}(i)$ are defined from a sequence from the family of periodically extended S(2) codes.

Let $n_{23}n_{22}\ldots n_0$ be the 24 bit binary representation of the code number n.

The n:th quaternary S(2) sequence $z_n(i)$, $0 \le n \le 16777215$, is obtained by modulo 4 addition of three sequences, a quaternary sequence $a(i)$ and two binary sequences $b(i)$ and $d(i)$, where the initial loading of the three sequences is determined from the code number n. The sequence $z_n(i)$ of length 255 is generated according to the following relation:

- $z_n(i) = a(i) + 2b(i) + 2d(i)$ modulo 4, $i = 0, 1, \ldots, 254$;

where the quaternary sequence $a(i)$ is generated recursively by the polynomial $g_0(x)= x^8+x^5+3x^3+x^2+2x+1$ as:

- $a(0) = 2n_0 + 1$ modulo 4;
- $a(i) = 2n_i$ modulo 4, $i = 1, 2, \ldots, 7$;
- $a(i) = 3a(i-3) + a(i-5) + 3a(i-6) + 2a(i-7) + 3a(i-8)$ modulo 4, $i = 8, 9, \ldots, 254$;

and the binary sequence $b(i)$ is generated recursively by the polynomial $g_1(x)= x^8+x^7+x^5+x+1$ as

$b(i) = n_{8+i}$ modulo 2, $i = 0, 1, \ldots, 7$,

$b(i) = b(i-1) + b(i-3) + b(i-7) + b(i-8)$ modulo 2, $i = 8, 9, \ldots, 254$,

and the binary sequence $d(i)$ is generated recursively by the polynomial $g_2(x)= x^8+x^7+x^5+x^4+1$ as:

$d(i) = n_{16+i}$ modulo 2, $i = 0, 1, \ldots, 7$;

$d(i) = d(i-1) + d(i-3) + d(i-4) + d(i-8)$ modulo 2, $i = 8, 9, \ldots, 254$.

The sequence $z_n(i)$ is extended to length 256 chips by setting $z_n(255) = z_n(0)$.

The mapping from $z_n(i)$ to the real-valued binary sequences $c_{\text{short},1,n}(i)$ and $c_{\text{short},2,n}(i)$, , $i = 0, 1, \ldots, 255$ is defined in Table 2.

Table 2: Mapping from $z_n(i)$ to $c_{short,1,n}(i)$ and $c_{short,2,n}(i)$, $i = 0, 1, \ldots, 255$

$z_n(i)$	$c_{short,1,n}(i)$	$c_{short,2,n}(i)$
0	+1	+1
1	-1	+1
2	-1	-1
3	+1	-1

Finally, the complex-valued short scrambling sequence $C_{\text{short, n}}$, is defined as:

$$C_{short,n}(i) = c_{short,1,n}(i \bmod 256)\left(1 + j(-1)^i c_{short,2,n}\left(2\left\lfloor (i \bmod 256)/2 \right\rfloor\right)\right)$$

where $i = 0, 1, 2, \ldots$ and $\lfloor\ \rfloor$ denotes rounding to nearest lower integer.

An implementation of the short scrambling sequence generator for the 255 chip sequence to be extended by one chip is shown in Figure 6.

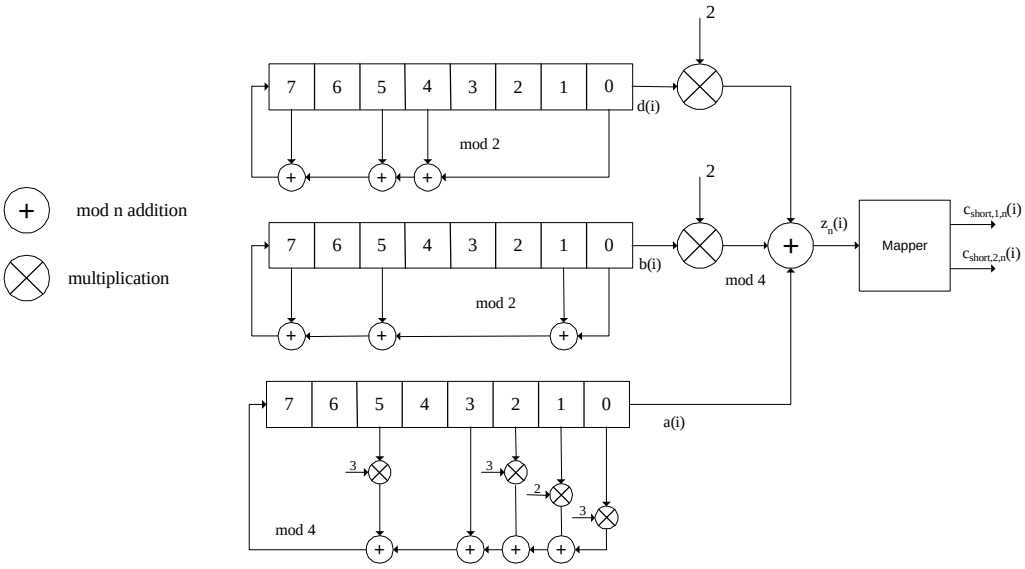

Figure 6: Uplink short scrambling sequence generator for 255 chip sequence

4.3.2.4 DPCCH/DPDCH scrambling code

The code used for scrambling of the uplink DPCCH/DPDCH may be of either long or short type. When the scrambling code is formed, different consituent codes are used for the long and short type as defined below.

The *n*:th uplink scrambling code for DPCCH/DPDCH, denoted $S_{dpch,\ n}$, is defined as:

$$S_{dpch,n}(i) = C_{long,n}(i),\ \ i = 0, 1, \ldots, 38399, \text{ when using long scrambling codes;}$$

where the lowest index corresponds to the chip transmitted first in time and $C_{long,n}$ is defined in section 4.3.2.2.

The *n*:th uplink scrambling code for DPCCH/DPDCH, denoted $S_{dpch,\ n}$, is defined as:

$$S_{dpch,n}(i) = C_{short,n}(i),\ \ i = 0, 1, \ldots, 38399, \text{ when using short scrambling codes;}$$

where the lowest index corresponds to the chip transmitted first in time and $C_{short,n}$ is defined in section 4.3.2.3.

If a power control preamble is used to initialise a DCH, the scrambling code for the DPCCH during the power control preamble shall be the same as that to be used afterwards. The phase of the scrambling code shall be such that the end of the code is aligned with the frame boundary at the end of the power control preamble.