Agenda item:

Source: **Philips**

Title: **Editorial correction to timing relations**

Document for: **Discussion**

Introduction

From comments received, the section on timing for initialisation of DCHs requires some further modification. Therefore the attached CR, CR25.211-050, proposes some corrections to the timing relations described in section 7.7 of TS25.211 for the initialisation of DCHs. These corrections aim to clarify this part of the specification and to ensure that it is aligned with TS25.214 and higher layer specifications (notably TS25.331).

The title of the section is clarified to confirm that it relates to dedicated channels. This includes the DPCCHs which accompany DSCHs.

The main changes relate to the possible use of activation times to specify the starting times of downlink and uplink DCHs.

Downlink

If an activation time is specified to a UE for the start of a downlink DCH, this corresponds to the frame during which the UE should start the process of receiving the DL DPCCH.

Restrictions on the activation time are described in terms of a number of frames "N_{offset_1}". If no activation time is given to the UE, N_{offset_1} should be set to the minimum possible values given by the equations in section 7.7, which means that the UE starts the process of receiving the downlink DPCCH at the earliest opportunity.

Uplink

If an activation time is specified to a UE for the start of an uplink DCH, this corresponds to the frame during which the higher layers in the UE should start the process of transmitting the UL DPCCH. In order for inner loop power control to act on the uplink, any activation time for the UL must allow for N_{offset_2} (the number of frames delay between the UE starting to receive the DL DPCCH and starting to transmit the UL DPCCH) to be greater than or equal to zero. Clearly, for fastest initialisation, the activation time should be chosen to result in N_{offset_2} having the value zero.

If no activation time is specified for the UL, higher layers will determine when to start the UL DPCCH according to the synchronisation procedure in TS25.214 sub-clause 4.3.2.

CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

25.211	CR	**050**	Current Version:	3.2.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑   *↑ CR number as allocated by MCC support team*

For submission to:	TSG-RAN #8	for approval	**X**	strategic		*(for SMG*
list expected approval meeting # here ↑		for information		non-strategic		*use only)*

Form: CR cover sheet, version 2 for 3GPP and SMG   The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc

Proposed change affects: (U)SIM [ ]   ME **X**   UTRAN / Radio **X**   Core Network [ ]
(at least one should be marked with an X)

Source:	Philips	**Date:**	2000-04-07

Subject: Editorial correction to timing relations

Work item:

Category:
(only one category shall be marked with an X)

				Release:	
F	Correction	**X**		Phase 2	
A	Corresponds to a correction in an earlier release			Release 96	
B	Addition of feature			Release 97	
C	Functional modification of feature			Release 98	
D	Editorial modification			Release 99	**X**
				Release 00	

Reason for change: Corrections for clarification and for alignment with TS25.214 and TS25.331.

Clauses affected: 7.7 Timing relations for initialisation of channels

Other specs affected:

Other 3G core specifications		→ List of CRs:	
Other GSM core specifications		→ List of CRs:	
MS test specifications		→ List of CRs:	
BSS test specifications		→ List of CRs:	
O&M specifications		→ List of CRs:	

Other comments:

help.doc

<--------- double-click here for help and instructions on how to create a CR.

7.7 Timing relations for initialisation of <u>dedicated</u> channels

Figure 32 shows the timing relationships between the physical channels involved in the initialisation of a DCH.

The maximum time permitted for the UE to decode the relevant FACH frame before the first frame of the DPCCH is received shall be $T_{B\text{-min}} = 38400$ chips (i.e.15 slots).

The <u>UE shall start the process of receiving the</u> downlink DPCCH ~~shall commence~~ at a time T_B after the end of the relevant FACH frame, where $T_B \geq T_{B\text{-min}}$ according to the following equation:

$$T_B = (T_n - T_k) \times 256 - N_{pcp} \times 2560 + N_{offset\_1} \times 38400 \text{ chips}, \text{ where:}$$

N_{pcp} is a higher layer parameter set by the network, and represents the length (in slots) of the power control preamble (see [5], section 5.1.2.4).

~~N_{offset_1} is a parameter set by higher layers and derived from the activation time if one is specified.~~

In order that $T_B \geq T_{B\text{-min}}$, <u>any activation time specified for the downlink (as descibed in TS25.331) should be such that</u> N_{offset_1} <u>as shown in Figure 32 is</u>~~shall be~~ an integer number of frames such that:

$$N_{offset\_1} \geq \begin{cases} 1 & \text{when } T_n - T_k \geq \dfrac{T_{B-\min}}{256} + 10N_{pcp} - 150 \\[2em] 2 & \text{when } \dfrac{T_{B-\min}}{256} + 10N_{pcp} - 300 \leq T_n - T_k < \dfrac{T_{B-\min}}{256} + 10N_{pcp} - 150 \\[2em] 3 & \text{when } T_n - T_k < \dfrac{T_{B-\min}}{256} + 10N_{pcp} - 300 \end{cases}$$

T_n and T_k are parameters defining the timing of the frame boundaries on the DL DPCCH and S-CCPCH respectively (see section 7.1). These parameters are provided by higher layers.

<u>Any activation time notified to the UE for the downlink DPCCH refers to the frame during which the UE starts receiving the downlink transmission.</u>

<u>If no activation time is given for the downlink, N_{offset_1} shall be set to the minimum values given by the above equations (i.e. 1, 2 or 3 depending on the value of $T_n - T_k$).</u>

The <u>starting time of the</u> uplink DPCCH <u>is shown in Figure 32 as occurring</u> ~~shall commence~~ at a time T_C after the end of the relevant FACH frame. <u>The starting time of the uplink DPCCH is determined by higher layers, according to the activation time of the uplink, if one is specified.</u>

<u>Any activation time specified for the uplink (as described in TS25.331) shall be such that N_{offset_2} is an integer number of frames greater than or equal to zero</u>, where

$$T_C = T_B + T_0 + N_{offset\_2} \times 38400 \text{ chips}, \text{ where } T_0 \text{ is as in section 7.6.3}\text{~~.~~}$$

<u>Any activation time specified for the uplink DPCCH refers to the frame during which the uplink transmission starts.</u>

~~If an activation time for the uplink DPCCH is specified, then N_{offset_2} shall be set to zero.~~ <u>If no activation time is given for the uplink,</u>~~Otherwise~~ the starting time of the uplink DPCCH shall be determined by higher layers according to the procedure in TS 25.214 sub clause 4.3.2, subject to the constraint that N_{offset_2} shall be an integer number of frames greater than or equal to zero.
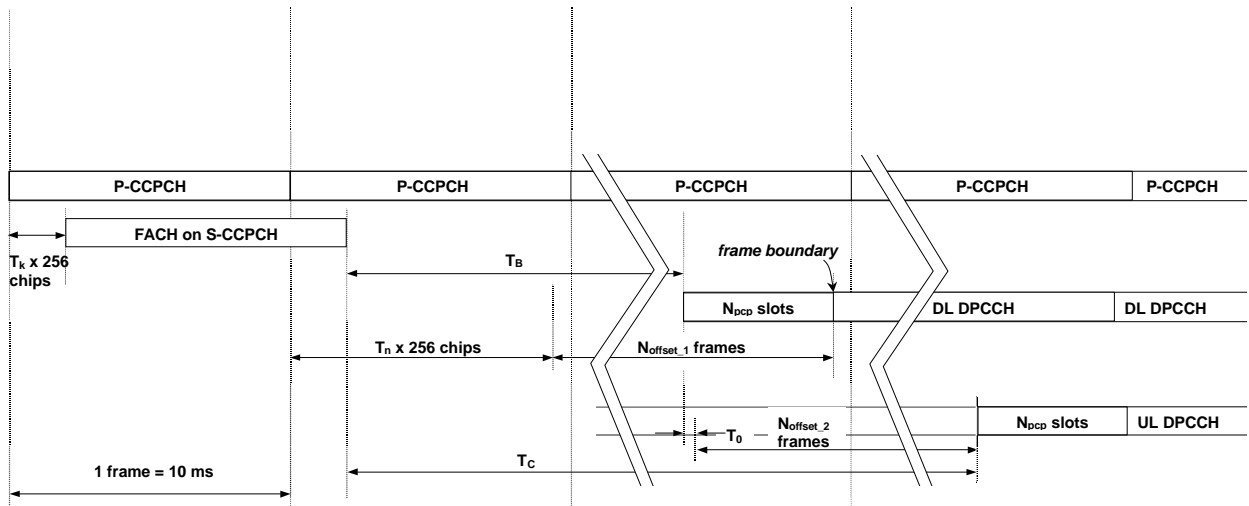
Figure 32: Timing for initialisation of DCH.

The uplink and downlink data channels shall not commence before the end of the respective power control preambles.

The starting time for transmission of data channels shall also satisfy the constraints on adding transport channels to a CCTrCH, as defined in 25.212 sub clause 4.2.14.