TSG-RAN Working Group 1 meeting#12 **TSGR1 (00)0491**

Seoul, Korea, April 10 ~ 13, 2000/3/26

**Agenda Item:**
**Source:** CWTS
**To:** TSG RAN WG1
**Title:** Frame Structure for low chip rate TDD option
**Document for:** Discussion and Approval

---

## Introduction

In 3GPP, there are two options for TDD mode. They are high chip rate option (3.84Mcps) and low chip rate option (1.28Mcps). The current specifications for TDD mode are mainly suitable for the high chip rate option. Due to the difference of the chip rate, a new frame structure for low chip rate TDD option will be proposed in this proposal. To enable the low chip rate with it's specific features and properties, other proposals will also be proposed later on by CWTS.

In WG1 meeting #10, the Tdoc R1-00-0092 for proposal of 'frame structure for low chip rate TDD option' is fully discussed. In this document, some background information, explanations and clarifications are added.

## Conclusion

Based on the discussion and the common understanding, it is proposed to add the following text in section 5.2.1 of TR 25.928

---------- changes to TR25.928 begin ----------

## 7.2 Physical channels

### 7.2.1 Frame structure

[Description:]

For low chip rate option, the frame length is 10ms and the 10ms frame is divided into 2 sub-frames of 5ms. The frame structure for each sub-frame in the 10ms frame length is the same.

The frame structure for each sub-frame is shown in Figure 1

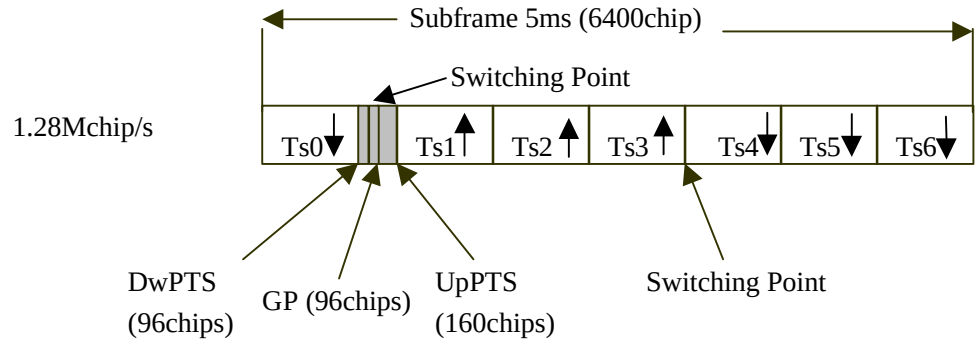


Figure 1 Structure of the sub-frame for low chip rate option

Tsn (n from 0 to 6): the nth normal time slot, 864 chips duration;
DwPTS: downlink pilot time slot, 96 chips duration;
UpPTS: uplink pilot time slot, 160 chips duration;
GP: main guard period for TDD operation, 96 chips duration;

## [Rationale:]

In Figure 1, the total number of normal traffic time slot for uplink and downlink is 7, and the length for each normal time slot is 864 chips duration. Among the 7 normal traffic time slot, Ts0 is always allocated as downlink while Ts1 is always allocated as uplink. The time slots for the uplink and the downlink are separated by a switching point. Between the downlink time slots and uplink time slots, the special period is the switching point to separate the uplink and downlink. In each sub-frame of 5ms for low chip rate option, there are two switching points (uplink to downlink and vise versa). The proposed frame structure has taken some new technologies into consideration, either the smart antenna (beam forming) technology or the uplink synchronization will be well supported.

Using the above frame structure, the low chip rate TDD option can operate on both symmetric and asymmetric mode by properly configuring the number of downlink and uplink time slots; (note that whatever the time slot configuration will be, the GP and DwPTS position within the frame should not change in order not to desynchronise the UEs and in order to allow Node B on air synchronisation procedures which make use of the DwPTS channel!) . It should be noted that in asymmetric operation mode, at least one normal uplink time slot and one downlink time slot will be allocated for traffic (Ts0 for downlink and Ts1 for uplink). The guard period GP of 96 chips can support the cell radius of up to about 11 km for uplink synchronization operation where the uplink transmission is advanced in macro-, micro- and pico- cell of small cells in cities or large cells in rural areas. Here the GP insures that an UE transmitting the UpPTS does not disturb the reception of the DwPTS for other UEs being close by. If this distortion is accepted in the network the cell radius can be bigger. (Note that the UpPTS is not continuously transmitted and the DwPTS is not continuously received.)

The only difference to the last version of the frame structure proposal for low chip rate is the improving of the numbering of the time slots. The physical layer behavior does not change.

## [Explanation of difference:]

For both high chip rate option and low chip rate option, the frame length is 10 ms , But for low chip rate option the 10 ms length is divided into 2 sub-frame of 5 ms to allow the fast update of power control, uplink synchronization, and smart antenna beamforming.

For high chip rate option , each 10 ms frame consists of 15 time slots, each allocated to either the uplink or the downlink . So it has both single and multiple-switching point configuration both for symmetric and asymmetric allocation. While in the low chip rate option, the position of the big Guard Period GP and of the DwPTS and UpPTS physical channels, is always between Ts0 and Ts1 whatever the level of asymmetry be.

### 7.2.2 Burst Types

[Description:]

In correspondence to the frame structure described above, the burst structures for Tsn, DwPTS and UpPTS are proposed. The burst structure for normal time slot (Tsn) is described in Figure 2.

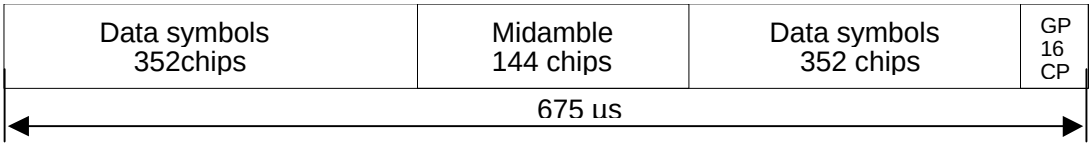


Figure 2 Burst structure for normal traffic time slot

The structure for DwPTS and UpPTS is described in Figure 3 and Figure 4.

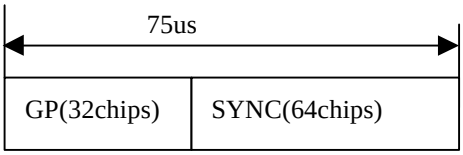


Figure 3 Structure for DwPTS

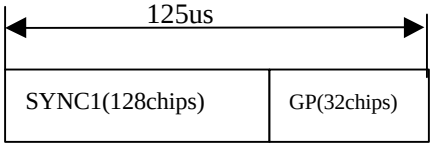


Figure 4 Structure for UpPTS

[Rationale:]

In Figure 2, the data symbols in each side of the midamble are 352 chips. The TPC bits for power control, the TFCI bits and the additional uplink synchronization bits are included in the Data symbols fields of the burst if they are needed. For the power control symbols, the uplink synchronization control symbols and the TFCI the symbols around the midamble are used.

The GP field in Figure 2 for each time slot is used for protection between time slots to avoid the long delay multi-path interference. It should be noted that the GP of the TS0 together with the guard period in DwPTS is 48 chips long which is different with other normal guard period of 16 chips between time slots. This ‘super long’ guard period can be used to avoid the interference between the last normal downlink time slot and the downlink synchronization pilot burst. Otherwise, the interference to the last downlink time slot from the strong powered pilot will be serious to the traffic; and vice versa, the interference to the downlink pilot burst from the last downlink time slot will decrease the performance on downlink synchronization and cell search. Note that if the UEs serving Node B is far away and the UE makes handover measurements it will receive the beginning of the DwPTS of a close by Node B inside these 48 chip. 48 chip corresponds to 11 km difference in distance to the Node B. If the other Node B is more distant to the serving Node B, big guard period can be used for receiving the DwPTS of the handover candidate Node B.

In DwPTS and UpPTS, the content of SYNC and SYNC1 field are used for downlink and uplink pilot. The GP fields are used to separate the downlink (uplink) pilot from the normal downlink (uplink) time slot.

It should be pointed out that the uplink synchronization burst (SYNC1) is not followed by a RACH immediately. First the UL synchronization burst UpPTS is sent by the UE. This UpPTS is used for Node B to determine the received power level and the received timing. Second, the Node B transmits timing and power control information to the UE using the P-FACH (one burst message) within the next 4 frames. Then the P-RACH is

transmitted. Both P-FACH and P-RACH are carrying single burst messages transmitted on a normal traffic time slot (see Fig. 2). This two phase procedure which is different with the GSM of one phase procedure has better performance than the classical approach as used in GSM. In this case, the normal traffic burst and access burst can be active in the same time slot and the interference is reduced for each other if they are time-aligned.

Note that the UpPTS has to be transmitted by the UE in advance (staring in the big GP) to arrive at the Node B at the position indicated in Figure 2. The UpPTS can also be received at a different position if the UE cannot or does not aim at the RX position indicated in Figure 2. Thus, the UpPTS can also start within the guard interval (RX, TX), depending on the situation in the system. This means relaxation to estimate timing in UE, e.g. from pathloss on P-CCPCH.

The proposed frame structure and the related burst structure for low chip rate option can fulfill the requirements for 3rd generation services and can provide the data services up to 2Mbps in a single 1.6MHz carrier. And the proposed frame structure can support all the environments of macro-, micro- and pico- cells. In vehicular environment, the speed can be more than 120km/h. Also in the proposed frame structure, some specific properties for low chip rate option such as smart antenna technology, uplink synchronisation, beamforming, etc can be well supported.

[Explanation difference:]

In high chip rate option, there are 2 burst types of DPCH. They have different midamble lengths. And there is only one burst type of DPCH in the low chip rate option.

---------- changes to TR25.928 end ----------