**3GPP TSG RAN WG1 Meeting #104bis-e R1-210xxxx**

**E-meeting, April 12th – 20th, 2021**

**Source: Moderator (vivo)**

**Title: Discussion summary #1 of [104b-e-NR-52-71GHz-05]**

**Agenda item: 8.2.5**

**Document for:** [Status]

# Introduction

In this contribution, we summarize issues regarding PDSCH/PUSCH enhancements for new SCSs on supporting NR from 52.6 GHz to 71 GHz for the following email discussion in RAN1 #104b-e.

[104b-e-NR-52-71GHz-05] Email discussion/approval on defining maximum bandwidth for new SCSs, timeline related aspects adapted to each of the new numerologies 480kHz and 960kHz and reference signals with checkpoints for agreements on Apr-16, Apr-20 – Huaming (Vivo)

Note that the scope of agenda 8.2.5 including defining maximum bandwidth for new SCSs, time line related aspects adapted to each of the new numerologies 480kHz and 960kHz, reference signals, scheduling particularly w.r.t. multi-PDSCH/PUSCH with a single DCI, HARQ, etc. In this summary, only issues related to bandwidth for new SCSs, time line related aspects adapted to each of the new numerologies 480kHz and 960kHz and reference signals are summarized. Issues related to scheduling particularly w.r.t. multi-PDSCH/PUSCH with a single DCI, HARQ are not in the scope of this summary.

# PDSCH/PUSCH enhancements for new SCSs

In this section, we provide a summary of issues, observations and proposals related to PDSCH/PUSCH enhancements for new SCSs discussed in the submitted contributions.

As in WID, the related objectives for this summary of agenda 8.2.5 are the following.

* Physical layer aspects including [RAN1]:
  + In addition to 120kHz SCS, specify new SCS, 480kHz and 960kHz, and define maximum bandwidth(s), for operation in this frequency range for data and control channels and reference signals, only NCP supported.

Note: Except for timing line related aspects, a common design framework shall be adopted for 480kHz to 960kHz

* + Time line related aspects adapted to 480kHz and 960kHz, e.g., BWP and beam switching timing, HARQ timing, UE processing, preparation and computation timelines for PDSCH, PUSCH/SRS and CSI, respectively.
  + Evaluate, and if needed, specify the PTRS enhancement for 120kHz SCS, 480kHz SCS and/or 960kHz SCS, as well as DMRS enhancement for 480kHz SCS and/or 960kHz SCS.

## 2.1. Channel bandwidth(s) related

### Individual observations/proposals

The following are individual observations/proposals from the contributions.

|  |  |
| --- | --- |
| Sources | Observations/proposals |
| [5, Nokia] | *Observation 1*: *Maximum bandwidth issue is done from RAN1 point of view. The following topics are under the responsibility of RAN4*   * *Maximum bandwidth* * *Channelization* * *Supported CA options.*   *Proposal 1*: *Consider 400 MHz as the minimum channel bandwidth for all SCSs.* |
| [7, CATT] | Proposal 1: RAN1 shall strive to keep current Tc value for supporting SCS=KHz960 KHz and the corresponding maximum system bandwidth (e.g 2GHz/2.16GHz). |
| [18, Sony] | Observation 1: CA (either inter-band or intra-band) can be supported, but we prefer not to rely on CA with maximum bandwidth 400MHz per carrier to achieve 2.16GHz bandwidth.  Proposal 1: Maximum bandwidth supported using a 960 kHz SCS should be 2.16 GHz. |
| [25, NEC] | Proposal 5: For 120 kHz and 480 KHz, Hz. For 960 kHz, Hz. |

### Summary on bandwidth(s) related

In last RAN1 meeting, the following were agreed.

* From RAN1 perspective, for NR operation in 52.6 GHz to 71 GHz,
  + The maximum channel bandwidth for 120 kHz SCS is 400 MHz
  + The maximum channel bandwidth for 480 kHz SCS is 1600 MHz
  + The maximum channel bandwidth for 960 kHz SCS is one of the following options
    - 2000 MHz
    - 2160 MHz
* Send LS to RAN4 to inform about RAN1’s agreement of maximum channel bandwidth and ask RAN4 to decide and feedback the exact value of maximum channel bandwidth for 960 kHz SCS, the corresponding numbers of RBs for the maximum channel bandwidth of SCS(s) supported in 52.6 GHz to 71 GHz.
* From RAN1 perspective, for NR operation in 52.6 GHz to 71 GHz, at least the following options on minimum channel bandwidth are identified.
  + for 120 kHz SCS
    - Option 1-1: 100 MHz
    - Option 1-2: 200 MHz
    - Option 1-3: 400 MHz
  + for 480 kHz SCS
    - Option 2-1: 200 MHz
    - Option 2-2: 400 MHz
  + for 960 kHz SCS
    - Option 3-1: 400 MHz
    - Option 3-2: 800 MHz
    - Option 3-3: same value as the maximum channel bandwidth for 960 kHz SCS
* Further study in RAN1 the above options’ implications on RAN1 design and specification
* Send LS to RAN4 to inform about RAN1’s identified options of minimum channel bandwidth and ask RAN4 to decide and feedback the minimum channel bandwidth

As in above, there’re several agreements reached on the maximum and minimum channel bandwidth for NR operation from 52.6 GHz to 71 GHz. Furthermore, an LS to RAN4 was sent to inform those RAN1 agreements and to request RAN4’s feedback on their decision of maximum/minimum channel bandwidths as well as channelization aspects. Several contributions submitted to this meeting made proposals on the remaining issues related to channel bandwidth(s).

Related to the maximum channel bandwidth, [5, Nokia] thought that maximum bandwidth issue is done from RAN1 point of view and is under the responsibility of RAN4. While [18, Sony] proposed to select 2.16 GHz as the maximum bandwidth for 960 kHz SCS.

Another issue related to the maximum channel bandwidth is the sampling rate/time unit Tc. Currently, Tc is defined as *Tc =*1/(Δ𝑓max ∙ *Nf*), where Δ𝑓max = 480 ∙ 103 Hz and *Nf* = 4096. [7, CATT] proposed to support the maximum channel bandwidth of 2 or 2.16 GHz for 960 kHz SCS without changing Tc value. On the other hand, [25, NEC] proposed to increase sampling rate by defining another time unit only applicable for 960 kHz SCS for better bandwidth utilization for 960 kHz SCS.

[5, Nokia] proposed to take one harmonized value for all the SCSs, i.e. 400 MHz as the minimum channel bandwidth for all SCSs in this frequency range.

Moderator’s comment:

In the last RAN1 meeting, it was agreed that “*ask RAN4 to decide and feedback the exact value of maximum channel bandwidth for 960 kHz SCS”* and “*ask RAN4 to decide and feedback the minimum channel bandwidth”*. It is moderator’s understanding that the decisions of the maximum and minimum channel bandwidth are under the responsibility of RAN4 now and no further discussion/agreement (including the issue of how to specify Tc) is needed in RAN1 before RAN4’s feedback.

Companies are encouraged to provide comments if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Qualcomm | We agree with the moderator to leave this to RAN4 |
| Futurewei | Support the moderator’s recommendation that no further discussion/agreement is needed in RAN1 before RAN4’s feedback. |
| Intel | For 960kHz with maximum of 2000 GHz will result in maximum of 174 PRBs (174 x 12 x 960 kHz = 2000.45 MHz). If we consider practical guard band sizes (95% spectral efficiency), the maximum of useable PRB is going to be likely smaller than 164 PRB. 164 RPB can be represented using 1968 subcarriers, which is less than 2048.  Since Tc is defined as 1/(4098 x 480 kHz), support of signal description for 960kHz with 164 PRB would be sufficient to express using the same Tc value = 1/(2048 x 960 kHz).  So based on our understanding, as long as maximum number of PRB is less than 170 PRB (2040 subcarriers), the existing Tc should be sufficient to express the minimum time unit.  Even if the number of PRB that RAN4 specifies somehow happens to be larger than 170 PRB for 960kHz, it may be possible to describe the specification in unit of Tc by utilizing Tc/2 or Tc/4.  However, in our opinion this is the job for the editors, as representation of a time unit in the specification description is not technical and is purely an editorial work.  It should be noted that Tc has nothing to do with actual sampling rate used by the transceivers. They are logical unit of time used to represent waveforms and timing requirements, but actual sampling rate used by the transceiver could be in fact different. So whether the specification describe the time unit with Tc, or change the Tc, or uses some other form, as long as the behaviors and requirements do not change, this should be up to the editor to fix.  From this point, we don’t think Tc should be an issue that needs consideration for any discussion making process in RAN1 and RAN4. |
| Huawei, HiSilicon | RAN4 actually just agreed today (April 14) on the minimum channel bandwidths of 100 MHz, 400 MHz and 400 MHz for 120/480/960 kHz SCS. Discussion should be left to RAN4 as agreed earlier. |
| NTT DOCOMO | We agree with Moderator’s comment. |
| OPPO | Agree with Moderator |
| Lenovo, Motorola Mobility | Agree with moderator’s comment. |
| vivo | We support Moderator’s proposal |
| LG Electronics | Agree with Moderator’s comment. |
| Nokia/NSB | Agree with Moderator’s comment. |
| Spreadtrum | Agree with Moderator’s comment. |

## 2.2. Timeline

### Individual observations/proposals

The following are individual observations and proposals from the contributions.

|  |  |
| --- | --- |
| Sources | Observations/proposals |
| [1, Huawei] | *Proposal 1: The absolute time of 120 kHz SCS timelines should be adopted by default unless the reduced value for specific timeline(s) can be verified by implementation.*  *Proposal 2: For single slot scheduling with 480 kHz and 960 kHz SCS, N1, N2 and N3 values providing same absolute processing time as that of 120 kHz SCS in FR2 is preferred. The values should be further studied for the case of multi slot scheduling after the detailed schemes are clear.*  *Proposal 3: The unit of k0, k1 and k2 should be defined as multiple slots for multi-PDSCH/PUSCH scheduling for 480 kHz and 960 kHz SCS.*  *Proposal 4: For 480 kHz and 960 kHz SCS, Z1, Z2 and Z3 values providing same absolute processing time as that of 120 kHz SCS in FR2 is preferred.* |
| [4, vivo] | Proposal 5: The following ranges of UE processing timelines can be used as starting point for further discussion.   1. N1/N3   For SCS=480kHz, the range should be 39~41;  For SCS=960kHz, the range should be 53~57.   1. For N2   For SCS=480kHz, the range should be 87~95;  For SCS=960kHz, the range should be 137~153.   1. For Z1   For SCS=480kHz, the range should be 119~123;  For SCS=960kHz, the range should be 202~209.   1. For Z’1   For SCS=480kHz, the range should be 102~114;  For SCS=960kHz, the range should be 172~201.  As de-ICI is necessary to compensate the phase noise for SCS of 120 KHz and high MCS for NR operation beyond 52.6 GHz, and de-ICI approach needs extra implementation complexity in UE for DL and gNB for UL, thus the constants N1, N2, N3 can be a little larger based on the ranges above.  Proposal 6: The default set of PDSCH-to-HARQ\_feedback timing indicator should be adapted to the SCS of PDSCH. |
| [5, Nokia] | Table 2. Proposed processing times for PDSCH and PUSCH    Proposal 3: Consider proposing times shown in Table 2 for PDSCH and PUSCH.  Observation 2: CSI computation delay has relation with PDCCH decoding complexity including BD/CCE limt.  Proposal 4: Consider CSI computation delay parameters for new SCSs only after determination of BD/CCE limit for new SCSs.  Observation 3: Rel-15/16 schemes for CPU can be reused for 480kHz and/or 960kHz SCS.  Proposal 5: Deprioritize the discussion on the additional processing timelines below.   * *UE PDSCH reception preparation time with cross carrier scheduling with different subcarrier spacings for PDCCH and PDSCH* * *SRS, PUCCH, PUSCH, PRACH cancellation with dynamic SFI* * *ZP CSI Resource set activation/deactivation* * *Application delay of the minimum scheduling offset restriction* * *timing aspects related to cross carrier operation* |
| [7, CATT] | Proposal 2: Compare to processing time of 120KHz SCS, considering the maximum system bandwidth and maximum PRB number can be scheduled, N1/N2 is proposed as follows   * for SCS=480KHz , the N1/N2 can be 1.5 times as 120KHz N1/N2 value. * for SCS=960KHz , the N1/N2 can be 1.25 times as 480KHz N1/N2 value.   Proposal 3: The range of k1 value specified for PDSCH HARQ process operation for 480 kHz/960 kHz SCS should take the N1 processing time into account with the starting slot from the value.  Proposal 4: The range of k2 value specified for PUSCH process for 480 kHz/960 kHz SCS should take the N2 processing time into account with the starting slot from the value. |
| [10, Ericsson] | 1. UE PDSCH/PUSCH processing timelines for SCS > 120 kHz need to be tightened compared to those for 120 kHz SCS to enable high performance NR operation in 52.6 to 71 GHz. 2. RAN1 should strive to narrow down the range of UE processing latencies early in the WI phase, particularly those related PDSCH/PUSCH processing (N1, N2, N3), to enable multi-PDSCH/PUSCH design to proceed. A reasonable starting point for discussion is an exponential function fitted to the Rel-15 values that provides extrapolated values of N1, N2, and N3 for 480 and 960 kHz (µ = 5 and 6, respectively).   Observation 2 The current ranges for PDSCH scheduling offset (K0), PDSCH HARQ feedback delay (K1) and PUSCH scheduling offset (K2) need to be increased to support multi-PDSCH/PUSCH scheduling in the frequency bands above 52.6 GHz at least for 480/960 kHz SCS, if the relevant timelines are not significantly tightened with reference to the existing requirement for 120 kHz SCS in FR2.  Proposal 15 The discussion on increasing K0, K1 and K2 for multi-PDSCH/PUSCH scheduling should be based on the outcome from the discussion on the UE processing timeline tightening.  Observation 3 Defining K1 granularity in slot bundle places unnecessary restriction on HARQ ACK scheduling which can result in longer HARQ feedback latency.  Observation 4 For legacy single-slot PDSCH transmission, restricting K1 being multiple times of slot bundle size makes it almost impossible to multiplex HARQ ACKs corresponding to adjacent PDSCHs in a single PUCCH transmission. |
| [11, Xiaomi] | *Proposal 2: For PUSCH scheduled by RAR or by the fallback RAR, Δ value should also be considered for new SCS 480/960kHz.*  *Proposal 3: Specify different default K1 value sets for different SCS, and each K1 set with a maximum number of 8 values to keep the K1 bit field in DCI 1-0 unchanged.*  *Proposal 4:*  *RRC configurable K1 value range can be extended to, for example, 0~128 to cover higher SCS. Separately configure different default K1 value sets for different SCS, and each set with a maximum number of 8 values*  *Proposal 5: Impacts on PDSCH/PUSCH processing time (N1/N2) may need be considered if defining maximum number of BDs/CCEs for multi-slot span PDCCH monitoring and/or with* *CORESET duration larger than 3 symbols.* |
| [12, Lenovo] | *Proposal 8: For supporting NR between 52.6 GHz and 71 GHz with high subcarrier spacing values including 480kHz and 960kHz, following enhancements should be supported to efficiently utilize UE’s limited processing capability to reduce latency and efficiently handle processing/preparation of CSI reports associated with multiple numerologies in parallel:*   * *Same reference symbols duration (possibly the shortest duration corresponding to maximum supported SCS value) could be used for checking CPU availability corresponding to different CSI reports associated with different SCS values* |
| [15, Apple] | *Proposal 1: Timelines are derived on a case-by-case basis and not a model based approach.* |
| [16, Qualcomm] | Proposal 12: The timeline calculations need to take into account the different cases for PDCCH monitoring, i.e., per-slot or multi-slot. This will require either one of the following   * Timeline is calculated based on the worst case * gNB and UE applies different processing timeline depending on PDCCH monitoring periodicity   Proposal 13: Introduce new default TDRA PDSCH and PUSCH tables depending on the used SCS, e.g., 960kHz and 480kHz SCS, to be able to schedule all the resources between any two adjacent PDCCH monitoring occasions. The slot offsets in these tables should cover up to the PDCCH monitoring periodicity. For the slots without PDCCH monitoring, L=14 can be considered.  Proposal 14: RAN1 design for 480kHz and 960kHz SCS, should assume a timeline similar to the absolute timeline of 120kHz. |
| [17, Samsung] | Proposal 1: RAN1 shall determine absolute values for processing timing for 480 and 960 KHz case by case, with the consideration of reasonable UE complexity, potential latency and impact of signal/channel/physical layer procedures.  Proposal 2: Processing time for procedures based on PDCCH reception should take into account the extra complexity/time for a UE when PDCCH Monitoring enhancement methods discussed in 8.2.3 A.I. (e.g. multi-slot span PDCCH monitoring) is configured.  Proposal 3: Support SCS-specific K1/K2 by reusing existing default/configured K1/K2 plus a SCS specific offset. |
| [19, LG] | Proposal #12: Consider additional UE PDSCH processing procedure time (i.e., N1 symbols) when UE is required to perform both of CPE and ICI compensation, e.g., for 120 kHz SCS and 64 QAM.  Proposal #13: Indicated (or configured) value(s) for k0/k1/k2 can be interpreted as multiplied by M where M denotes the number of slots in a slot-group (if configured).  Proposal #14: The configuration and default value of k1 (or PDSCH-to-HARQ\_feedback), should be adjusted to practical value considering the increased N1.  Proposal #15: The configuration and default value of k2 should be adjusted to practical value considering the increased N2.  Proposal #16: The configuration and default value of k0 should be adjusted to practical value considering the UE PDSCH reception preparation time with cross carrier scheduling with different numerologies for PDCCH and PDSCH.  Proposal #17: Consider the dependence of each other when determining the value range of k0 and k1.  Proposal #18: Consider CSI processing timeline enhancements for better availability for CPUs for multiple CSI reports associated with different numerologies. |
| [22, InterDigital] | *Proposal 14: Evaluate required UE processing time for higher frequencies considering the differences on antenna/panel structure, narrower beamwidth, BWP size and new subcarrier spacings.*  *Observation 13: Existing processing time determination methods are based on worst case scenarios and may require more redundant processing time for higher frequencies.*  *Proposal 15: Study application of different processing time requirements based on parameters which contribute UE processing time.* |
| [24, ZTE] | Proposal 6: For above 52.6GHz, a new UE capability for timeline related aspects should be defined based on slot (or symbol)-group granularity.  Proposal 7: Consider the phase noise estimation and compensation time on timeline design when PTRS is configured.  Proposal 8: The following methods can be considered to interpret k0, k1 and k2, and we prefer Method 1.   * Method 1: slot-group level unit can be defined for the value of k0, k1 and k2, that is the value indicated in the DCI is not the slot offset but the slot group offset. One slot group can include M slots. * Method 2: some new candidate values of k0, k1 and k2 should be defined considering the UE processing capability. * Method 3: the value range of k0, k1 and k2 is not changed and the unit is still the slot, but the actually used k0, k1 and k2 is an offset of the indicated value in the DCI, and the offset value is different for different SCS. |
| [26, NTT DOCOMO] | Proposal 1: FFS how to derive the accurate timeline values for 480/960kHz SCS for NR52.6-71GHz. |

### Summary on timeline

#### Dependence to scheduling and/or PDCCH monitoring

Several contributions mentioned the dependence of determining some UE processing timeline with some related discussions.

[4, vivo], [16, Qualcomm], [19, LG] and [24, ZTE] all mentioned to consider the phase noise estimation and compensation time on timeline design.

[11, Xiaomi] proposed that impacts on PDSCH/PUSCH processing time (N1/N2) may need to consider maximum number of BDs/CCEs for multi-slot span PDCCH monitoring. [17, Samsung] proposed that processing time for procedures based on PDCCH reception should take into account the extra complexity/time for a UE when multi-slot span PDCCH monitoring is configured. Similarly, [16, Qualcomm] proposed the timeline calculations need to take into account the different cases for PDCCH monitoring, i.e., per-slot or multi-slot and it proposed two options: timeline is calculated based on the worst case or gNB and UE applies different processing timeline depending on PDCCH monitoring periodicity

Moderator’s comment:

There seems to be a fundamental question toward the determination of timelines considering NR operation in this frequency range need to support single PDSCH/PUSCH and multi-PDSCH/PUSCH scheduling as well as difference in terms of UE PDCCH monitoring capability.

##### Discussion point 2-1:

Whether to define a single or separate sets of timelines for single PDSCH/PUSCH and multi-PDSCH/PUSCH scheduling for NR operation in 52.6 GHz to 71 GHz?

* If a single set of timelines for single PDSCH/PUSCH and multi-PDSCH/PUSCH scheduling, whether to target the worst case?
* If different sets of timelines for single PDSCH/PUSCH and multi-PDSCH/PUSCH scheduling, what is the deciding factor(s) for those different sets?
  + PDCCH monitoring periodicity, e.g., per slot or multi-slot PDCCH monitoring
  + The number of scheduled PDSCH/PUSCH by a single DCI
  + Other?

Companies are encouraged to provide answers/views to the above questions and/or comments/proposals.

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| Company Name | Comments/Views |
| Qualcomm | In case of defining a single set of timelines, it should be based on the worst case, otherwise we can consider different sets of timelines, taking into account at least the PDCCH monitoring periodicity. |
| Futurewei | Recommend prioritizing the single PDSCH/PUSCH timeline, taking into account aspect such as ICI compensation time on timeline design. The timeline for multi-PDSCH/PUSCH can be complicated and can be deferred until agreements from other sub-agenda items are made, e.g., PDCCH monitoring periodicity and beam-switching related aspects. |
| ZTE, Sanechips | We also suggest to first consider to define the single PDCSH/PUSCH timeline, since currently it’s not clear that whether multi-PUSCH/PDSCH can be applied to all SCSs, besides, the maximum scheduling number is not determined.  We share similar view with Futurewei that phase noise compensation time should be considered on timeline design. |
| Intel | From required processing time, we don’t see strong motivation to differentiate single PDSCH/PUSCH and multi-PDSCH/PUSCH. Since the fundamental signal structure and encoding is identical for each slot, common set of requirements should be applicable for both cases. |
| Huawei, HiSilicon | RAN1 should progress on the multi-PDSCH/PUSCH scheduling operation before we can conclude on the question. The answer may also depend on which timeline we are discussing (is the question only about processing timelines N1, N2 and N3?). |
| DOCOMO | We prefer a single set of timelines for single PDSCH/PUSCH and multi-PDSCH/PUSCH scheduling with considering the worst case.  In our understanding, there may be two motivations to introduce separate timeline sets. The first motivation is different maximum BD/CCEs number for different PDCCH monitoring granularities (e.g. per slot PDCCH monitoring or multi-slot PDCCH monitoring) may require different decoding time. However, we don’t think per slot or multi-slot PDCCH monitoring equals to single PDSCH/PUSCH or multi-PDSCH/PUSCH scheduling. It is not excluded for PDCCH monitored per multi-slot to schedule single PDSCH/PUSCH. The second motivation is larger number of PDSCHs/PUSCHs may need longer processing time. However, from this perspective, we may need to define a number of timeline sets based on how many number of PDSCHs/PUSCHs are scheduled. We would also like to point out that multi-PUSCH scheduling is supported in Rel-16 without introducing separate timeline. |
| OPPO | The discussion for processing timeline should be separated for PDSCH and PUSCH. For multi-PUSCH scheduling, in R16, there is no need to define a different processing timeline for single or multi- PUSCH scheduling. Thus, we think single processing timeline should be enough.  For multi-PDSCH scheduling, it can be further investigated if there is a need for defining different processing timeline for single or multi-PDSCH scheduling. At this stage, we still don’t see the need. |
| Lenovo, Motorola Mobility | We prefer to have single timeline requirements for multi PDSCH/PUSCH scheduling and don’t see a strong reason to define separate timeline requirements in terms of scheduling. However, it would be good to clarify exactly which timelines are being discussed here. |
| vivo | Agree with Futurewei and ZTE that the timeline for single PDSCH/PUSCH should be prioritized taking into account de-ICI time. We are open to discuss timeline for multi-PDSCH/PUSCH scheduling further. |
| LG Electronics | We support a single set of timelines with considering the worst case as commented by Qualcomm, Intel and DOCOMO. |
| Nokia/NSB | Based on the WID, new SCSs are optional features for the UE operating at 60 GHz already. We think that it doesn’t make sense to define multiple sets of timelines for the high SCSs. This would just create additional complexity e.g. for the scheduler operation.  For the single set of timelines, we think that the worst case is not a sufficient target.  The timelines should be determined in such that 32 HARQ processes are enough for achieving contiguous DL or UL transmission in the case of multi-slot scheduling.   * 4 slots by a single DCI with 480 kHz SCS   8 slots by a single DCI with 960 kHz SCS. |
| CATT | We suggest to first consider to define the single PDCSH/PUSCH timeline. |
| Spreadtrum | We prefer a single set of timelines with targeting the worst case. |
| Ericsson | We assume the discussion here is about N1, N2, N3. We prefer single set of timeline values.  We agree with the comments from Intel – no need to differentiate single/multiple PDSCH scheduling. Just because multiple PDSCHs are scheduled by a single DCI, it doesn't mean that the per-slot processing requirement becomes larger. We agree with the observation from DOCOMO that multi-PUSCH was introduced in Rel-16 without introducing a new timeline.  It is not clear what "worst case" means in this context. Worst case in terms of what? |

#### Methodology

In the last RAN1 meeting, it was agreed to further study how to derive timeline values, e.g., whether to take case by case study approach or adopt some model-based approach for selected timelines, e.g. exponential models, projection based on log-linear regression, etc.

Regarding how to derive the UE processing timeline for new SCSs, several contributions have discussed different approaches.

Both [4, vivo] and [10, Ericsson] adopted exponential models whose parameters are obtained based on some simple formulae fitted with the existing Rel-15 processing times. The new values for new SCSs are extrapolated using the fitted formulae. Note that those models are for selected delay and timeline values.

[5, Nokia] proposed the minimum processing times for the case when 32 HARQ processes are used for 480 kHz and 960 kHz SCSs. [7, CATT] analyzed and proposed the UE processing timeline for 480 kHz and 960 kHz SCSs considering the maximum channel bandwidth, number of PRBs and LDPC code processing.

[15, Apple] argued that the use of a model based approach to select the value for processing timelines may result in selection of unrealistic values and hence proposed that the timelines are derived on a case-by-case basis and not a model based approach. Similarly, in [17, Samsung], it also proposed to determine absolute values for processing timing for 480 and 960 KHz case by case, with the consideration of reasonable UE complexity, potential latency and impact of signal/channel/physical layer procedures.

In [1, Huawei], it proposed to adopt the absolute time of 120 kHz SCS timeline by default, except for the cases identified to be able to reduce from implementation perspective. Similar proposal was made in [16, Qualcomm]. However, [5, Nokia] argued that keeping the absolute processing time the same for all SCSs would either considerably increase the amount of HARQ processes needed or reduce the data rate due to HARQ process starvation. On the same topic, [10, Ericsson] also examined the latency of new SCSs if keep the same absolute time as 120 kHz SCS processing and observed that UE PDSCH/PUSCH processing timelines for SCS > 120 kHz need to be further tightened compared to those for 120 kHz SCS to enable high performance NR operation in 52.6 to 71 GHz.

Moderator’s comment:

Viewing the companies’ views expressed, it seems clear that there’s not one approach which is agreeable to all companies here.

Given it was already agreed in last RAN1 meeting to use the absolute time duration for 120 kHz SCS as the upper bound for the discussion of UE processing timelines (not related to PDCCH monitoring) for 480 kHz and 960 kHz SCS and RAN1 strives to reduce the absolute time durations from the upper bound if feasible, it is suggested to continue the discussion of timeline case-by-case if any common methodology cannot be agreed to derive the timelines.

##### Discussion point 2-2:

Companies are encouraged to provide comments and/or suggestions on how to proceed on the methodology for timeline.

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| --- | --- |
| Company Name | Comments/Views |
| Qualcomm | We agree with the moderator to continue discussion while using SCS 120kHz absolute time numbers as assumption for other designs |
| Futurewei | Support to reduce the absolute time duration from the upper bound if feasible and support a case-by-case manner of discussion if common methodology cannot be agreed. |
| ZTE, Sanechips | We agree to continue the discussion case by case. |
| Huawei, HiSilicon | It is fine to discuss case by case on Nx, kx and Zx timelines, starting with Nx. Regarding the absolute time discussion, it seems clear from the contributions that the only known feasible timeline based on real implementation is that of 120 kHz SCS. In terms of methodology, we suggest agreeing first that one capability for 480/960 kHz SCS for N1, N2 and N3 is reusing the same absolute timeline defined for 120 kHz in FR2, and other capabilities can be further discussed. |
| DOCOMO | Agree with Moderator’s suggestion. |
| Lenovo, Motorola Mobility | We agree to have case by case discussion as well and agree with moderator’s comment |
| Vivo | Agree with Moderator’s comment |
| LG Electronics | We agree to continue the discussion case by case with 120 kHz absolute time as a baseline if any common methodology cannot be agreed. |
| Nokia/NSB | Agree with case-by-case approach.  We think that processing timelines for PDSCH and PUSCH should be considered first.  One approach is the decide the number of HARQ processes first. |
| CATT | Agree with Moderator’s suggestion. |
| Spreadtrum | We agree with moderator’s suggestion. |
| Ericsson | We agree that the discussion of timeline values and the number of HARQ processes is coupled, and needs to be discussed at the same time. If the number of HARQ processes is not increased, and the timelines are not tightened compared to 120 kHz, clearly HARQ process starvation will occur and it will not be possible to take advantage of the large bandwidth available in 52.6 – 71 GHz to achieve high throughput.  We are okay to discuss values of N1, N2, and N3 for each SCS separately. The purpose of a model is mainly to provide a useful tool to establish a starting point for discussion on further timeline tightening. |

#### N1, N2 and N3

[1, Huawei] proposed that for single slot scheduling with 480 kHz and 960 kHz SCS, N1, N2 and N3 values providing same absolute processing time as that of 120 kHz SCS in FR2 is preferred. The values should be further studied for the case of multi slot scheduling after the detailed schemes are clear.

[16, Qualcomm] proposed that RAN1 design for 480kHz and 960kHz SCS, should assume a timeline similar to the absolute timeline of 120kHz.

[4, vivo] adopted exponential models whose parameters are obtained based on some simple formulae fitted with the existing Rel-15 processing times. It proposed a range of values for N1, N2 and N3 as starting point for discussion. [10, Ericsson] took the same approach and also provided some values for N1, N2 and N3 as starting point for discussion.

[5, Nokia] analysed the relationship between UE processing timeline and the number of HARQ process and provided some example values of N1 and N2. [7, CATT] provided their values of N1 and N2 based on an analysis on the impact of channel bandwidth, the number of PRB and LDPC coding to UE processing timeline.

Table 1 PDSCH processing time arrange for PDSCH processing capability 1

|  |  |  |
| --- | --- | --- |
|  | PDSCH decoding time *N1* [symbols] | |
| *dmrs-AdditionalPosition* = pos0 in  *DMRS-DownlinkConfig* in both of  *dmrs-DownlinkForPDSCH-MappingTypeA*, *dmrs-DownlinkForPDSCH-MappingTypeB* | *dmrs-AdditionalPosition* ≠ pos0 in  *DMRS-DownlinkConfig* in either of  *dmrs-DownlinkForPDSCH-MappingTypeA*, *dmrs-DownlinkForPDSCH-MappingTypeB*  *or if the higher layer parameter is not configured* |
| 3 (120 kHz) | 20 | 24 |
| 5 (480 kHz) | 80 ([1, Huawei], [16, Qualcomm])  39~41 ([4, vivo])  40 ([5, Nokia])  30 ([7, CATT])  37 ([10, Ericsson]) | 36 ([7, CATT]) |
| 6 (960 kHz) | 160 ([1, Huawei], [16, Qualcomm])  53~57 ([4, vivo])  80 ([5, Nokia])  42 ([7, CATT])  50 ([10, Ericsson]) | 50 ([7, CATT]) |

Table 2 PUSCH preparation time for PUSCH timing capability 1

|  |  |
| --- | --- |
|  | PUSCH preparation time *N2* [symbols] |
| 3 (120 kHz) | 36 |
| 5 (480 kHz) | 144 ([1, Huawei], [16, Qualcomm])  87~95 ([4, vivo])  52 ([5, Nokia])  60 ([7, CATT])  91 ([10, Ericsson]) |
| 6 (960 kHz) | 288 ([1, Huawei], [16, Qualcomm])  137~153 ([4, vivo])  108 ([5, Nokia])  72 ([7, CATT])  144 ([10, Ericsson]) |

Table 3 Minimum gap between the second detected DCI and the beginning of the first PUCCH resources

|  |  |
| --- | --- |
|  | HARQ-ACK multiplexing timeline *N3* [symbols] |
| 3 (120 kHz) | 20 |
| 5 (480 kHz) | 80 ([1, Huawei], [16, Qualcomm])  39~41 ([4, vivo])  37 ([10, Ericsson]) |
| 6 (960 kHz) | 160 ([1, Huawei], [16, Qualcomm])  53~57 ([4, vivo])  50 ([10, Ericsson]) |

Moderator’s comment:

No clear majority on any values of N1, N2 and N3.

Given it was already agreed in last RAN1 meeting to use the absolute time duration for 120 kHz SCS as the upper bound for the discussion of UE processing timelines (not related to PDCCH monitoring) for 480 kHz and 960 kHz SCS and RAN1 strives to reduce the absolute time durations from the upper bound if feasible, it is suggested to continue the discussion of individual timeline case-by-case to derive the timeline values.

##### Discussion point 2-3:

Companies are encouraged to provide comments and/or proposals.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Qualcomm | RAN 1 design for 480kHz and 960kHz should be based on the absolute timeline of 120kHz, it is not expected to have a significant reduction for the timelines of these SCSs. |
| Futurewei | Recommend tightening from the upper bound case-by-case if common methodology is not agreed. |
| ZTE, Sanechips | We agree to continue the discussion case by case. |
| Huawei, HiSilicon | We agree with Qualcomm. Regarding the absolute time discussion, it seems clear from the contributions that the only known feasible timeline based on real implementation is that of 120 kHz SCS. So we suggest agreeing first that one capability for 480/960 kHz SCS for N1, N2 and N3 is reusing the same absolute timeline defined for 120 kHz in FR2, and other capabilities can be further discussed. |
| DOCOMO | Agree with Moderator’s suggestion. |
| Lenovo, Motorola Mobility | Agree with moderator’s comment |
| |  |  | | --- | --- | | vivo | Agree with moderator’s comment. | | |  |  | | --- | --- | | vivo | Agree with moderator’s comment. | |
| LG Electronics | We agree to continue the discussion case by case. Specifically, for N1, additional processing time for ICI cancellation should be considered for all SCSs (including 120 kHz). |
| Nokia/NSB | The timelines should be determined in such that 32 HARQ processes are enough for achieving contiguous DL or UL transmission in the case of multi-slot scheduling.   * 4 slots by a single DCI with 480 kHz SCS * 8 slots by a single DCI with 960 kHz SCS. |
| CATT | We agree to continue the discussion case by case. |
| Spreadtrum | We agree with moderator’s suggestion. |
| Ericsson | We agree that the discussion of N1,N2,N3 and the number of HARQ processes is coupled, and needs to be discussed at the same time. If the number of HARQ processes is not increased, and the timelines are not tightened compared to 120 kHz, clearly HARQ process starvation will occur and it will not be possible to take advantage of the large bandwidth available in 52.6 – 71 GHz to achieve high throughput.  We are okay to discuss values of N1, N2, and N3 for each SCS separately. The purpose of a model is mainly to provide a useful tool to establish a starting point for discussion on further timeline tightening. |

#### k0, k1 and k2

[4, vivo] proposed the default set of PDSCH-to-HARQ\_feedback timing (k1) indicator should be adapted to the SCS of PDSCH. Similarly, [19, LG] proposed that the configuration and default value of k1 and k2, should be adjusted to practical value considering the increased N1 and N2 respectively.

[11, Xiaomi] proposed to specify different default K1 value sets for different SCS, and each K1 set with a maximum number of 8 values to keep the K1 bit field in DCI 1-0 unchanged.It further proposed that RRC configurable K1 value range can be extended to, for example, 0~128 to cover higher SCS. [17, Samsung] proposed to support SCS-specific K1/K2 by reusing existing default/configured K1/K2 plus a SCS specific offset.

[7, CATT] proposed the range of k1 (k2) value specified for PDSCH (PUSCH) HARQ process operation for 480 kHz/960 kHz SCS should take the N1 (N2) processing time into account with the starting slot/offset from the value⌊N1/14⌋ (⌊N2/14⌋).

[24, ZTE] proposed to define a new UE capability for timeline related aspects based on slot (or symbol)-group (multiple slot/symbol) granularity. [24, ZTE] also proposed multiple methods to interpret k0, k1 and k2 where their preferred method is to define slot-group level unit for the value of k0, k1 and k2, that is the value indicated in the DCI is not the slot offset but the slot group offset where one slot group can include M slots. [1, Huawei] also proposed that the unit for k0, k1 and k2 should be multi-slots for multi-PDSCH/PUSCH scheduling. [19, LG] proposed that the indicated (or configured) value(s) for k0/k1/k2 can be interpreted as multiplied by M where M denotes the number of slots in a slot-group (if configured). On this topic, [10, Ericsson] argued that defining K1 granularity in slot bundle places unnecessary restriction on HARQ ACK scheduling which can result in longer HARQ feedback latency. Is was also observed in [10, Ericsson] that if k1 unit is defined as slot-group then for legacy single-slot PDSCH transmission, it is almost impossible to multiplex HARQ ACKs corresponding to adjacent PDSCHs in a single PUCCH transmission.

[7, CATT] thought the range of K0 value should not be changed for 480 kHz and 960 kHz SCS. While [19, LG] proposed the configuration and default value of k0 should be adjusted to practical value considering the UE PDSCH reception preparation time with cross carrier scheduling with different numerologies for PDCCH and PDSCH.

Moderator’s comment:

Considering the potential relationship between some of the values of k0/k1/k2 to UE processing time (N1/N2/N3), it is suggested to discuss and decide the values of k0/k1/k2 after N1/N2/N3.

##### Discussion point 2-4:

Companies are encouraged to provide comments and/or proposals.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Qualcomm | We agree that k0/k1/k2 can be discussed later after the agreement on both   * UE processing time (N1/N2/N3) * PDCCH periodicity as the default values of k0/k2 should be extended to be able to cover all the resources between two PDCCH monitoring occasions.   If needed, we can start by discussing k0. |
| Futurewei | Support further discussion of the values k0/k1/k2 next meeting(s), after N1/N2/N3 is determined later this meeting. |
| ZTE, Sanechips | Agree with moderator. |
| Huawei, HiSilicon | We agree with the proposed workplan. |
| DOCOMO | We are fine with Moderator’s suggestion to decide k0/k1/k2 after N1/N2/N3. And we think default k1 sets need to be defined for new SCSs. But we don’t prefer to re-interpretate the granularity of k1. If larger k1 values are needed, it can be achieved by larger values configured in k1 set. |
| Lenovo, Motorola Mobility | This can be discussed in the next RAN1 meeting once we have made progress on N1/N2/N3 |
| vivo | Agree with moderator |
| LG Electronics | We are ok with moderator’s suggestion in principle. However, there can be a lot of timeline aspects to be handled in a few RAN1 meetings. And, we already agreed that k0/k1/k2 as well as N1/N2/N3 should be prioritized. So, we think it would be better to start discussion for k0/k1/k2 in parallel to N1/N2/N3 discussion. |
| Nokia/NSB | Agree with Moderator’s proposal. |
| CATT | Agree with Moderator’s proposal. |
| Spreadtrum | We agree with moderator’s proposal. |
| Ericsson | Agree with Moderator's proposal. There is a clear dependence of k0,k1,k2 on N1,N2,N3, so N1,N2,N3 should be decided first. |

#### Z1, Z2 and Z3

[1, Huawei] proposed that for 480 kHz and 960 kHz SCS, Z1, Z2 and Z3 values providing same absolute processing time as that of 120 kHz SCS in FR2 is preferred. [16, Qualcomm] proposed that RAN1 design for 480kHz and 960kHz SCS, should assume a timeline similar to the absolute timeline of 120kHz.

[4, vivo] adopted exponential models whose parameters are obtained based on some simple formulae fitted with the existing Rel-15 processing times. It proposed a range of values for Z1 as a starting point for discussion.

[5, Nokia] thought CSI computation delay has relation with PDCCH decoding complexity including BD/CCE limit and proposed to consider CSI computation delay parameters for new SCSs only after determination of BD/CCE limit for new SCSs. It also argued that in Rel-15, N\_CPU is independent from numerology, and proposed that the existing specification can be reused for 480kHz and 960kHz SCS

Moderator’s comment:

Without much input on these Z1, Z2 and Z3 values, it is not possible to derive any agreeable values.

##### Discussion point 2-5:

Companies are encouraged to provide comments and/or proposals.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Qualcomm | We can use the absolute values of SCS 120kHz as baseline for the design for 480kHz and 960kHz SCSs |
| Futurewei | Support further discussion of the values Z1/Z2/Z3 next meeting(s), after more inputs are available. |
| ZTE, Sanechips | Agree with moderator. |
| Huawei, HiSilicon | We agree with the proposed workplan. |
| DOCOMO | We agree with Moderator’s observation. Maybe same or similar absolute processing time as 120kHz SCS can be a starting point. |
| Lenovo, Motorola Mobility | Agree. Can be discussed in future meetings |
| Vivo | Agree with moderator |
| LG Electronics | We agree with Moderator’s view. Since, in last meeting, we agreed that the discussion on Z and Z’ can be deprioritized than N1/N2/N3/k0/k1/k2, we can discuss it later with more companies’ inputs. |
| Nokia/NSB | We propose to decide the PDCCH capabilities first. |
| CATT | Agree with moderator. |
| Spreadtrum | We suggest to use the absolute processing timing of 120kHz SCS as the upper bound for that of 480kHz and 960kHz SCS. |
| Ericsson | We note that long latencies are observed for the CSI computation time (Z1, Z2, and Z3) as defined in clause 5.4 of 38.214 when extrapolated to 480/960 kHz SCS; thus tightening w.r.t. 120 kHz should be discussed. However, discussions on tightening of these processing times can occur later in the work item as they do not block design of multi-PDSCH/PUSCH. |

#### Other issue(s)

Please provide comments if any on any missed issue(s) about timeline.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | Discussion on CSI processing unity availability should also be handled here. In our view, it is critical to handle CPU availability check for UEs when it is required to process multiple CSI reports associated with different SCS values ranging from 15kHz to 960kHz.  Sub-symbol level CPU availability check should be discussed for lower SCS value where the symbol duration is quite long, otherwise the opportunities for CPU availability might be very less for such CSI processing in comparison to high SCS with short symbol duration |
|  |  |
|  |  |

## 2.3. PTRS

### Individual observations/proposals

The following are individual observations/proposals from the contributions.

|  |  |
| --- | --- |
| Sources | Observations/proposals |
| [1, Huawei] | *Observation 5:* *Block PTRS with the designed sequence has better BLER and spectrum efficiency than distributed PTRS with narrow scheduled bandwidth when power boosting is enabled.*  *Proposal 14:* *Support block PTRS with ZC sequence as a base sequence and circular sequence attached in both head and tail of the base sequence for 120 kHz, 480 kHz and 960 kHz SCS with CP-OFDM for ICI estimation of high MCS, when power boosting is enabled.*  *Observation 6:* *With more PTRS groups and less PTRS samples per PTRS group denoted as (*, *) = (16, 2), the BLER performance of all the SCSs are improved significantly.*  *Proposal 15:* *A* *new PTRS pattern with more PTRS groups and less PTRS samples per PTRS group denoted as (*, *) = (16, 2) within one DFT-s-OFDM symbol should be supported for large scheduling bandwidth and high scheduled MCS.*  *Observation 7: Due to Rx timing shift, (at least part of) a PTRS group placed at the tail of the transmitter’s DFT-s-OFDM symbol, may wrap-around to the head of the symbol from the receiver’s perspective, thus spoiling the original intention of the design and unnecessarily increasing Rx complexity, as well as deteriorating PN compensation performance, especially for the high MCS.*  *Observation 8: New PTRS location which is in the middle of each interval can solve the influence on BLER performance caused by Rx advance timing shift.*  *Proposal 16: For PTRS with , the mapping of last PTRS group should consider potential Rx timing shift and avoid the last X pre-DFT symbol(s).* |
| [4, vivo] | Observation 1:  - The performance of de-ICI with K\_PTRS = 2 is the worst when PDSCH RB number <= 8, and K\_PTRS = 1 helps to improve the performance of de-ICI in this case;  - When PDSCH RB number <= 8, CPE only with K\_PTRS = 2 has much better performance than de-ICI with K\_PTRS = 1.  - de-ICI with K\_PTRS = 1 is not the preferred PN compensation method (i.e. with the best performance) for different simulation setup (the number of RB allocation, SCS and MCS). Therefore, there is no benefit to introduce K\_PTRS = 1 in terms of performance.  Proposal 1: There is no need to introduce higher PTRS frequency density as K\_PTRS =1.  Observation 2: With current simulation parameters, the performance of de-ICI with Rel-15 PTRS pattern outperforms the performance of block-based PTRS pattern with cyclic ZC sequence.  Proposal 2: Do not support block-based PTRS pattern with cyclic ZC sequence.  Observation 3: For MCS-7, MCS-16 and MCS-22, the performance gap is less than 0.8 dB between (CN, CS) = (8, 4) and combination with the best performance; while for MCS-26, only the option (CN, CS) = (16, 4) can achieve 10% BLER. As DFT-s-OFDM is mainly used for UL coverage, it is unlikely that very high MCS, such as MCS-26, is scheduled to the UE configured with this waveform.  Proposal 3: The necessity to introduce more PTRS chunk number needs further discussion as there is no significant performance benefit. If a new configuration with more PTRS chunk number needs to be added, the SCS and MCS should be within the condition of applying this configuration. |
| [5, Nokia] | *Observation 6. Existing PTRS configurations provide good allocation flexibility to achieve good performance for any bandwidth, SCS, or MCS.*  *Observation 7. Existing PTRS configurations provide the best performance for CPE compensation, and increasing frequency density does not provide any gain.*  *Observation 8. CPE compensation cannot provide reasonable performance for 120kHz SCS with 400MHz bandwidth when 64-QAM is used.*  *Observation 9. CPE compensation cannot provide reasonable performance for 480kHz SCS with 1600MHz bandwidth when 64-QAM is used.*  *Observation 10. CPE compensation provides good performance for 960kHz SCS with 2000MHz bandwidth even when 64-QAM is used.*  *Observation 11. Existing PTRS configurations provide the best performance for ICI compensation, and increasing frequency density does not provide any gain.*  *Observation 12. Phase noise compensation is an implementation specific aspect.*  *Proposal 18. Use existing PTRS configurations for CP-OFDM.*  *Observation 13. Based on the evaluations, it does not make sense to provide new specification burden by introducing PTRS enhancements for OFDM, because existing specification can well adapt to different cases.*  *Observation 14. PUSCH performance of DFT-s-OFDM may be improved by increasing the maximum number of PTRS groups with well affordable PTRS overhead.*  *Observation 15. New PTRS configurations can give performance gains for high order modulations.*  *Observation 16. Performance can be significantly improved by combinations of existing PTRS patterns.*  *Proposal 19. Consider increasing number of PTRS groups for DFT-s-OFDM to make high order modulations robust to phase noise when a large number of PRBs is used.*  *Proposal 20. Support the new PTRS configurations as combinations of existing PTRS configurations to a single configuration.* |
| [9, Futurewei] | *Observation 4: Comb-PT-RS is more scattered over frequency-domain, thus may capture better global information for ICI estimation/cancellation; comb-PT-RS has more ICI on adjacent data subcarriers, thus has low opportunity to enjoy the benefit from power-boosting.*  *Observation 5: Block-PT-RS is the least scattered pattern over frequency-domain, thus captures rather local information over frequency; Block-PT-RS has less neighboring data subcarriers, thus lower ICI on data, and in turn higher opportunity to benefit from power-boosting.*  *Proposal 3: If block-PT-RS is used for beyond 52.6GHz, power-boosting is a recommended technique to improve ICI cancellation.*  *Observation 6: Cluster-PT-RS is a pattern that can achieve a tradeoff between the scattering over frequency-domain and the level of ICI imposed on data subcarriers.*  *Observation 7: Cluster-PT-RS with non-uniform selective boosting window can improve performance while limit excessive power usage.* |
| [10, Ericsson] | Observation 5 For every tested scenario, the Rel-15 distributed PTRS structure with multiple settings for the PTRS density and direct de-ICI receiver parameters can be used to outperform the best settings for cyclic block PTRS with circulant ICI filter approximation while achieving lower phase noise compensation complexity at the same time.  Observation 6 Enhanced Rel-15 PT-RS with 1 PT-RS every RB (K = 1) does not provide additional performance gain over the existing Rel-15 PT-RS structure (K = 2).  Observation 7 For every tested scenario, the Rel-15 distributed PTRS structure with multiple settings for the PTRS density and direct de-ICI receiver parameters without PT-RS power boosting can be used to outperform the best settings for cyclic block PTRS with PT-RS power boosting while achieving comparable or lower phase noise compensation complexity at the same time.  Observation 8 Cyclic block PTRS with circulant ICI filter approximation with or without PT-RS power boosting tends to require longer ICI compensation filters than Rel-15 PTRS structure with direct de-ICI filtering because of the various fundamental design issues identified in Section 2.4.1:  1. ICI filter approximation with block PTRS does not fully utilize all received PTRS symbols.  2. Phase noise compensation with ICI filter approximation approach relies on an auto-deconvolution assumption that is not valid in practice.  3. The construction of a circulant matrix with cyclic block PTRS sequence relies on an assumption that is invalid for frequency selective channels.  4. ICI filter approximation with circulant PTRS matrix involves anti-match-filter combining, which amplifies noise from clusters and subcarriers with weak received SNR.  Proposal 23 For NR operation in 52.6 to 71 GHz with OFDM, support only the existing Rel-15 distributed PT-RS design. Cyclic block PT-RS structure is not supported. |
| [13, Mitsubishi] | Observation 1: *In bands above 52.6GHz, the ICI component of the phase noise becomes predominant on CPE.*  Observation 2: *Distributed PT-RS pattern shows poor performance results with CPE phase noise estimation* *regardless of the PT-RS pattern density.*  Observation 3: *For a distributed PT-RS pattern, at small carrier allocations, the performance is poor even with de-ICI filtering, due to an insufficient number of PT-RS samples*.  Observation 4: *For a distributed PT-RS pattern, de-ICI Wiener filtering outperforms CPE in all cases, but high MCS still not reach FER=0.1*.  Observation 5: *Distributed PT-RS patterns are not robust enough to ensure system performance in bands above 52.6GHz.*  Observation 6: *For a similar overhead, block PT-RS (with any ordinary sequence) is outperformed by distributed PT-RS pattern when a same de-ICI Wiener filter is used at the receiver side*.  Observation 7: *Block PT-RS with cyclic sequence significantly outperforms the distributed PT-RS pattern with ICI compensation*. *The gain increases with the carrier frequency*.  Observation 8: *Block PT-RS with cyclic sequence requires lower complexity phase noise compensation filtering than the de-ICI filter needed for the distributed PT-RS pattern*.  Proposal : *Support block PT-RS with cyclic sequence for OFDM waveform.*  Proposal : *A PT-RS sequence for OFDM waveform composed of KP samples includes a cyclic prefix of floor(KP/2) samples.*  Proposal : *Support density extension of current Rel.15 PT-RS for DFTsOFDM waveform.* |
| [14, Intel] | **Observation 1:** the PTRS frequency densities currently specified in NR don’t allow to support 64QAM for allocations <12 PRB (Rank 1) and ≤32 PRB (Rank 2).  **Observation 2:** K=1 allows the support of FDRA down to 8 PRB with for Rank 1 64QAM Tx.  **Observation 3:** K=0.5 allows the support of FDRA down to 4 PRB with Rank 1 64QAM Tx.  Proposal 9: NR to support new PTRS frequency densities K=0.5, 1.  **Observation 4:** 7 tap de-ICI filter doesn’t allow to support MCS>26 with rank 1 Tx and MCS>24 with rank 2 Tx.  Proposal 10: Study the means of supporting MCS>24 with rank 2 Tx with advanced phase noise compensation techniques while factoring into account receiver processing complexity.  Observation 5: Unequal distribution of PN estimation error among DFT-s-ODFM samples may lead to systematic unbalance between code blocks’ BLERs.  Observation 6: PUSCH PTRS patterns with only 4 and 8 PTRS groups provide acceptable performance with 120kHz SCS.  Observation 7: Code blocks interlacing within a DFT-s-OFDM symbol provides performance gain from 0.5dB to 1.7dB at MCS22.  Proposal 11: RAN1 to consider code blocks interlacing for PUSCH with transform precoding. |
| [15, Apple] | *Proposal 10: Investigate the behavior of block based PTRS in the presence of correlated phase noise.*  *Proposal 11: RAN1 should support frequency domain power boosting for PTRS where regulations allow.* |
| [16, Qualcomm] | Observation 1: Comparing the different PTRS patterns   * The best performance is obtained with block PTRS pattern with zero-power tones. * The legacy pattern performance is very close to block PTRS pattern with zero-power tones.   Observation 2: The block PTRS pattern with ZP tones and the legacy pattern outperforms the cyclic patterns based on ZC sequences.  Observation 3: With 7 clusters each with 9 tones, 8 ZP PTRS tones and a single NZP tone in the centre, the two algorithms with the clustered pattern have almost the same performance, and they slightly outperform the legacy pattern.  Observation 4: For small RB allocation, e.g., 16 or 8 RBs, sending the PTRS over every RB, i.e., K=1, enhances the performance as it helps in having a more accurate ICI filter calculations or CPE estimate.  Proposal 1: For SCS 120kHz, the complexity of phase noise ICI compensation and its effects on the UE processing timeline need to be considered.  Proposal 2: New PTRS patterns other than the Rel-15 design, even though with similar de-ICI performance, should not be precluded from the discussion if they can significantly reduce the complexity of the ICI compensation.  Proposal 3: As PTRS enhancement for assisting ICI compensation, increasing the frequency domain density, of Rel. 15 PTRS, for small RB allocation can be considered.  Observation 5: For MCS 22, there is no significant enhancement for increasing the total number of PTRS samples to 64, while small gains can be observed with MCS 24. In addition, increasing the number of PTRS samples beyond 64 is not helping the performance.  Proposal 4: No need to increase the PTRS sample density for SC-FDM waveform. |
| [17, Samsung] | Observation 1: In the scenario of our evaluation, we don’t observe significant performance gain for block PTRS pattern with cyclic sequence comparing to Rel-15 PTRS with de-ICI algorithm.  Observation 2: Alternative ICI estimation algorithm taking advantage of the cyclic structure of PTRS pattern may provide better performance for block PTRS pattern with cyclic sequence. |
| [19, LG] | Proposal #8: Retain the existing distributed PT-RS structure for all SCS in FR-X. It seems that further improvement either by advanced estimation algorithms or by new PT-RS pattern cannot achieve a noticeable improvements.  Proposal #9: Consider to introduce new K values more than 4 to achieve the additional enhancements from large RB allocation. |
| [20, CEWiT] | Observation 1: The specification impact due to the introduction of new PTRS design should be carefully studied.  Proposal 5: Support for new PT-RS for NR above 52.6GHz at least for 120KHz SCS.  Proposal 6: Support for Block-PTRS as one of the candidates for new PTRS design for NR above 52.6GHz.  Proposal 7: Time density based on MCS, as in FR1 and FR2, is supported. |
| [22, InterDigital] | *Observation 11:* *Compared to Rel-15 PTRS configuration, block PTRS designs with similar PTRS overhead does not provide significant performance gains.*  *Observation 12: A low-complex 3 taps de-ICI filter () based on existing Rel-15 NR PTRS structure can provide protection against performance degradation due to phase noise.*  *Proposal 13:* *PTRS enhancement is not considered for NR 52.6 – 71 GHz.* |
| [24, ZTE] | Observation 3: Block PTRS with cyclic sequence cannot provide performance gain compared with legacy PTRS.  Observation 4: Block PTRS with power boosting cannot achieve better performance than legacy PTRS.  Proposal 9: Reuse the Rel-15 legacy PTRS pattern for 52.6GHz~71GHz.  Observation 5: Enhancement on PTRS density for DFT-s-OFDM waveform can bring benefit to performance of 120kHz SCS and 64QAM modulation. |

### Summary on PTRS

#### For CP-OFDM

In last RAN1 meeting, the following was agreed.

* At least existing PTRS design for CP-OFDM is supported for NR operation in 52.6 to 71 GHz.
* Companies are encouraged to study the need of potential PTRS enhancement for CP-OFDM with respect to phase noise compensation performance considering at least the following aspects:
  + PTRS density/pattern (e.g. distributed, block-based) and sequence (e.g. cyclic sequence)
  + Frequency domain power boosting and its impact to PDSCH performance and PDSCH to DMRS EPRE
  + Receiver complexity, including possible aspects related to supporting both existing PTRS design and potential PTRS enhancement
  + Possible specification impact of supporting potential PTRS enhancement in addition to existing PTRS design
  + Note: PTRS overhead should be accounted for in the evaluations, e.g. by showing spectral efficiency results and/or reporting effective coding rate

The following sources submitted to this meeting evaluated and compared different PN compensation performance using the existing Rel-15 NR distributed PTRS structure against new PTRS density/patterns and/or new sequence.

[1, Huawei] compared BLER performance of Rel-15 PTRS with K=4 and a block PTRS with cyclic sequence in CDL- D 20ns delay spread for MCS 22 (for 64, 128 and 256 RB) and MCS 26 (for 64 RB) when ICI PN compensation is used. Note that a 3dB power boosting was applied in the simulation for both PTRS patterns. It observed a performance gain (0.2~1 dB) for block PTRS with cyclic sequence compared to Rel-15 PTRS with K=4. The performance gain is shown to be ~0.2 dB for 256 RB (120 and 480 kHz, MCS 22), ~0.5 dB for 128 RB (120 and 480 kHz, MCS 22) and ~1dB for 64 RB (120 kHz with MCS 22, 480 and 960 kHz with MCS 26).

[4, vivo] first evaluated and compared the performance of different PTRS density (K=1 and K=2) with de-ICI (3 taps) and CPE only PN compensation methods with different number of PDSCH RB allocation and different MCS for all SCSs. It observed that while increased PTRS density (K\_PTRS = 1) may help improve the performance of de-ICI compared to K\_PTRS =2 when PDSCH RB number <= 8, a better performance is obtained for CPE only with K\_PTRS = 2 in this case. Given de-ICI with K\_PTRS =1 is not the PN compensation method providing the best performance in any of the evaluated cases, it proposed not to increase PTRS density. [4, vivo] then evaluated CP-OFDM performance for CPE with Rel-15 PTRS, de-ICI filter with Rel-15 PTRS, ICI filter approximation with a block PTRS with Rel-15 sequence and ICI filter approximation with a block PTRS with cyclic sequence for all SCSs. It observed that the performance of de-ICI with Rel-15 PTRS pattern outperforms the performance of block-based PTRS pattern with cyclic ZC sequence.

[5, Nokia] evaluated both CPE and ICI performance and observed that existing PTRS configurations provide the best performance for CPE and ICI compensation, and increasing frequency density (e.g. K=1) does not provide any gain. It is also observed that phase noise compensation in general (including ICI filtering) is an implementation issue.

[10, Ericsson] provided evaluation results on three aspects of PTRS enhancements: increased PTRS density (K=1); clustered-PTRS with cyclic sequence; and power boosting. It is observed that Rel-15 PT-RS with 1 PT-RS every RB (K = 1) does not provide additional performance gain over the existing Rel-15 PT-RS structure (K = 2). Comparing the performance of Rel-15 PTRS and a block-PTRS with cyclic sequence, it is observed that the Rel-15 distributed PTRS structure with multiple settings for the PTRS density and direct de-ICI receiver parameters without PT-RS power boosting can be used to outperform the best settings for cyclic block PTRS with PT-RS power boosting while achieving comparable or lower phase noise compensation complexity at the same time.

[13, Mitsubishi] compared phase noise compensation performance for the following four cases: CPE-based for Rel-15 PTRS, de-ICI for Rel-15 PTRS, de-ICI for block PTRS and ICI filtering for block PTRS with cyclic sequence for 120 kHz SCS. It is observed that for a similar overhead, block PTRS is outperformed by Rel-15 distributed PTRS patterns when a same de-ICI Wiener filter is used at the receiver side. It also observed that ICI filtering for block-based PTRS and cyclic sequence outperforms de-ICI Wiener filtering with Rel-15 distributed PTRS.

[14, Intel] evaluated PDSCH BLER performance with de-ICI for different allocated PRB number for 120 kHz SCS. It is observed that increased PTRS density (K=0.5 and K=1) provide better performance when the number of allocated PRB is small (i.e. 4 or 8) for Rank 1 64QAM and proposed to support K=0.5 and K=1. [14, Intel] also evaluated de-ICI performance with high MCS (MCS 25, 26 and 27) with large RB number and observed that 7 tap de-ICI filter doesn’t allow to support MCS>26 with rank 1 Tx and MCS>24 with rank 2 Tx.

[15, Apple] compared the performance of a distributed PTRS as in Rel-15 and a block PTRS for 480 kHz SCS and showed a performance loss of the block based PTRS design at high delay spreads. However, it showed a performance gain of block PTRS with correlated PN across antennas (assuming a UE and gNB architecture with a single local oscillator per device).

[16, Qualcomm] evaluated ICI compensation performance for 120 kHz SCS at MCS 22 and MCS 26 with multiple PTRS patterns: clustered PTRS with different number of ZP tones, block PTRS with cyclic sequence and Rel-15 PTRS with K=4. It is observed that block PTRS pattern with zero-power tones and the legacy pattern outperforms the cyclic patterns based on ZC sequences. It also observed that for small RB allocation, e.g., 16 or 8 RBs, sending the PTRS over every RB, i.e., K=1, enhances the performance as it helps in having a more accurate ICI filter calculations or CPE estimate.

[17, Samsung] compared the performance of three schemes: de-ICI for Rel-15 PTRS pattern, ICI filtering for a block PTRS pattern with non-cyclic random sequence ( and ) and ICI filtering for a block PTRS pattern with cyclic ZC sequence ( and ). For the case evaluated (120 kHz SCS with 256 RB, TDL-A 5 ns, MCS22), it observed no significant performance gain for block PTRS pattern with cyclic sequence comparing to Rel-15 PTRS with de-ICI algorithm.

[19, LG] compared the performance difference between ideal cases (no PN or ideal filter estimation) and simple ICI compensation based on Rel-15 PTRS for all SCSs and showed that the potential performance gain by advanced estimation algorithms or by new PT-RS pattern is well bounded (< 1 dB). [19, LG] also showed small performance gain (<0.5 dB) of reduced PTRS density (K=6) for large RB allocation (MCS 28, 480 kHz SCS with 192 RB).

[22, InterDigital] evaluated PN compensation performance for different PTRS density of Rel-15 PTRS and observed that compared to Rel-15 PTRS configuration, block PTRS designs with similar PTRS overhead does not provide significant performance gains.

[24, ZTE] evaluated PDSCH with CP-OFDM performance with the legacy PTRS, block PTRS with cyclic PN sequence and block PTRS with cyclic ZC sequence for 120 and 480 kHz SCS with MCS 22. It is observed that the performance of ICI compensation based on legacy PTRS is always better than block PTRS with cyclic (PN or ZC) sequence. It also compared the performance of block PTRS with 3dB power boosting with that of legacy PTRS without power boosting and showed that the performance of legacy PTRS without power boosting is still better than block PTRS with 3 dB power boosting.

In addition to PTRS pattern/density and sequence, some other aspects of potential PTRS enhancements are also discussed.

[9, Futurewei] evaluated the impact of power boosting on PDSCH with CP-OFDM BLER performance for 120 KHz SCS for comb-, block- and clustered-PTRS with de-ICI. It is observed that block-PTRS may benefit more from power boosting than comb-PTRS and recommended to use power boosting for ICI if block-PTRS is used. [15, Apple] proposed to support frequency domain power boosting for PTRS where regulations allow to account for the increase in PN variance at the higher frequencies.

[10, Ericsson] studied different ICI approaches and observed that cyclic block PTRS with circulant ICI filter approximation with or without PT-RS power boosting tends to require longer ICI compensation filters than Rel-15 PTRS structure with direct de-ICI filtering due to various identified issues: ICI filter approximation with block PTRS does not fully utilize all received PTRS symbols; phase noise compensation with ICI filter approximation approach relies on an auto-deconvolution assumption that is not valid in practice; the construction of a circulant matrix with cyclic block PTRS sequence relies on an assumption that is invalid for frequency selective channels; ICI filter approximation with circulant PTRS matrix involves anti-match-filter combining, which amplifies noise from clusters and subcarriers with weak received SNR.

Submitted evaluation results showing significant performance gain of new PTRS pattern/density with cyclic sequence for CP-OFDM are summarized below.

Yes: [1, Huawei], [13, Mitsubishi], ([15, Apple] reported gain when correlated PN assumed across antennas)

No: [4, vivo], [10, Ericsson], ([15, Apple] reported performance loss of new PTRS pattern with cyclic sequence when correlated PN not assumed across antennas which is aligned with agreed evaluation assumptions), [16, Qualcomm], [17, Samsung], [24, ZTE]

Moderator’s comment:

Looking at these extensive evaluation results from contributions, majority results from companies showed no significant performance gain of new PTRS patterns with cyclic sequence compared to existing PTRS. Hence, there’s no consensus with respect to the support of block PTRS with cyclic sequence.

##### Discussion point 3-1:

* Conclude that block PTRS with cyclic sequence is not supported as PTRS enhancement for CP-OFDM for NR operation in 52.6 to 71 GHz in Rel-17.

Companies are encouraged to provide comments if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Qualcomm | We agree to preclude the block PTRS with cyclic sequence (without ZP tones) for the discussion of PTRS enhancements as most of the companies observed no performance enhancement with such pattern. Also, we propose further evaluations and discussion of the block PTRS with ZP tones at the edges of each block and a NZP tone at the center as shown in the figure below.    The block PTRS with single NZP tone at the center can be a good candidate for the higher band as it can significantly reduce the complexity of filter calculations by removing matrix inversion steps. The complexity of applying the ICI filter on the received tones will be common for all schemes and several mechanisms can be used to efficiently implement such FIR filter. Therefore, new block PTRS pattern should not be precluded if they can significantly reduce the complexity of ICI filter estimation, even if the performance is similar. |
| Futurewei | Suggest keeping new sequence design for block/multi-block PTRS open, despite that a particular sequence may or may not be notably better than the legacy, considering the importance of ICI cancellation for B52 band. |
| ZTE, Sanechips | We support moderator’s conclusion.  Since most companies do not observe performance loss based on legacy PTRS in Rel-15, we don’t think it’s necessary to introduce further enhancement on PTRS design. |
| Huawei, HiSilicon | Before proposing such conclusion in point 3-1, RAN1 should discuss the submitted results and gain some understanding on the reasons for the varying results.  For example, some receiver assumptions (e.g. in [10, Ericsson]) are not conducive to observing performance gains, whereas a different receiver assumption (with a larger PTRS block size, and/or de-ICI algorithm applied to block PTRS) would likely show gains. The block size and number of blocks used in [10, Ericsson] leads to much fewer valid PTRS for algorithm 2 (ICI filter approximation) when compared with Rel-15 PTRS with algorithm 1 (direct de-ICI filtering). Another problem is that the number of valid PTRS doesn’t match with the needed ICI order (the total number of valid PTRS should be 4 or 5 times larger than 2u+1) for block PTRS, or the ICI order is not the best one for the block PTRS pattern. In summary, fewer blocks with larger block size should have been evaluated instead.  It would therefore be reasonable that the study should continue with better alignment on evaluation assumptions, including kinds of block size and block number, different algorithms of ICI estimation based on block PTRS, and different value of u under a given block PTRS pattern.  We also found that not many evaluations considered the benefit of power boosting (e.g. [17, Samsung]) for block PTRS. In other contributions (e.g. [24, ZTE] and [4, Vivo]) we could not clearly understand the block PTRS pattern that was evaluated. Furthermore, the BLER performance shown in some contributions (e.g. [4, vivo], Figure7 and Figure8) is not conclusive because the minimum BLER is higher than 0.88 or 0.18.  Qualcomm’s use of ZP-PTRS won’t allow efficient power boosting (not evaluated by Qualcomm) because the maximum power boosting value for the NZP PTRS should be restricted for meeting the spectrum mask, or it will limit the block size of the ZP-PTRS pattern. Note that block PTRS with ZP-tones can be seen as a special case for block PTRS with circular sequence, where the sequence is […, 0, 0, s, 0, 0…].  So we cannot accept the conclusion proposed in point 3-1. |
| NTT DOCOMO | We support the proposal. |
| OPPO | Support moderator’s proposal |
| Mitsubishi | Strongly disagree with the current proposal.  Concerning the proposal from Qualcomm, it is a special case of block with cyclic sequence, where part of the samples in the sequence are 0. This proposal can be further investigated under the framework of “block with cyclic sequence”, where the sequence itself can be further refined.  Concerning the different conclusions drawn by some companies, while some companies did not report the pattern which was used e.g. how many blocks, what length (for example vivo [4], or ZTE [24]), and others chose rather different patterns and/or receiver strategies, we are unable to draw any conclusions without further technical discussion. |
| Lenovo, Motorola Mobility | We support the proposal and block PTRS is not needed |
| vivo | We support the proposal.  Regarding the power boosting for block PTRS, can Huawei provide more details about the power setting for PTRS and PDSCH data RE respectively?  In HW’s simulation, is power boosting on PTRS also applied to R15 distributed PTRS pattern? Same total power of OFDM symbol with PTRS between block PTRS pattern and R15 distributed PTRS pattern?  Response to Huawei’s question:  In our simulation, the block PTRS pattern with cyclic ZC sequence is designed as below:   * Only one block of PTRS, and the block size = R15 PTRS overhead; * The length of base PTRS sequence = floor (the block size/2), while the length of head PTRS sequence = the length of tail PTRS sequence = floor (the block size/4);   The simulation result of figure 7 and figure 8 in [4, vivo] is for SCS as 120 KHz and MCS-26. In your contribution, there is no result with SCS as 120 KHz and MCS-26, therefore, you can just take figure 5 and figure 6 (SCS as 120 KHz and MCS-22) for comparison. |
| LG Electronics | We share the same view with Qualcomm. In our contribution, we have shown that block PTRS with ZP tones has similar BLER performance as legacy distributed PTRS pattern with de-ICI filtering. However, this PTRS pattern could be beneficial in terms of filtering complexity as commented by Qualcomm. We think that this type of PTRS pattern should not be precluded without a sufficient analysis with respect to the performance and complexity of ICI compensation. |
| Nokia/NSB | Support the moderator’s conclusion. |
| CATT | We support the proposal. |
| Spreadtrum | We support the proposal. |
| Ericsson | We support the moderator's conclusion. This issue should be closed.  Extensive performance evaluation has been done comparing Rel-15 PTRS to Block PTRS with cyclic sequence in multiple scenarios with both designs compared on an equal footing (i.e., same PTRS overhead). Rel-15 PTRS with the best density setting and the best receiver settings always outperforms Block PTRS with Cyclic Sequence with an equivalent PTRS density and the best receiver settings. Moreover, when comparing the best settings for each, the complexity for de-ICI is always lower.  **@Mitsubishi**. We think that the comparison of performance and complexity is not correct, as it is assumed that the number of filter taps for de-ICI is always L = 11. As we show in our contribution, L = 11 is always inferior to lower values. L should be chosen appropriately depending on the PTRS density and # of RBs. By choosing L appropriately, Rel-15 PTRS + de-ICI outperforms the best setting of block PTRS with cyclic sequence and achieves lower complexity.  **@Huawei**. We have also analyzed power boosting with block PTRS + cyclic sequence and compared to Rel-15 PTRS with K = 1, 2, and 4. We find that when compared on the basis of equal overhead, Rel-15 PTRS always outperforms cyclic block PTRS and achieves lower complexity.  Regarding Huawei's comment about investigating fewer blocks with larger block size, we did exactly that in our evaluations. For example, for the case of 64 RBs and Rel-15 PTRS with K = 4 (16 total PTRS symbols) we compared this to block PTRS considering 3 blocks with 5 PTRS, 2 blocks with 9 PTRS, and 1 block with 17. The choice of these settings is so that one can compare Rel-15 PTRS to block PTRS on the basis of the same overhead.  Regarding Huawei's comment about considering de-ICI applies to block PTRS, we have done that comparison in the last two meetings, and Rel-15 + de-ICI always outperforms block PTRS + de-ICI. My understanding is that Mitsubishi has made similar observations.  **@Qualcomm**. We have serious concerns about the block PTRS structure with ZP tones and one NZP tone. It is claimed that this structure is advantageous since it avoids matrix inversions. We show in our contribution that the complexity due to matrix inversion is only a small portion of the overall complexity when considering also filtering. The filtering is the dominant contributor to complexity, and as pointed out by Qualcomm is common to all schemes. Furthermore, block PTRS generally requires longer filters than de-ICI to achieve the same level of performance.  For the PTRS structure with only one NZP tone, very high power boosting is needed, and it is not likely that this will be allowed by RAN4. Such high levels of boosting are not attractive from a PAPR/CM perspective, and it creates an out of band emission issue due to inter-modulation distortion. |
| Charter | We support the proposal. |

Companies’ results showing significant performance gain and preference to support increased PTRS density (e.g., K=0.5, 1) than Rel-15 are summarized below.

Yes: [14, Intel] (K=0.5, 1 for small RB allocation), [16, Qualcomm] (K=1 for small RB allocation)

No: [4, vivo], [5, Nokia], [10, Ericsson], [22, InterDigital]

Moderator’s comment:

Again, looking at available evaluation results from contributions, more results from companies showed no significant performance gain of increased PTRS density compared to existing PTRS. Hence, there’s no consensus with respect to the support of increased PTRS density.

##### Discussion point 3-2:

* Conclude that increased PTRS frequency density is not supported as PTRS enhancement for CP-OFDM for NR operation in 52.6 to 71 GHz in Rel-17.

Companies are encouraged to provide comments if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Qualcomm | Based on our evaluations, we concluded that the higher density is beneficial for small RB allocations such as 16 and 8 RBs, we observed several dBs performance loss at 1%BLER point. Therefore, we suggest that we agree on several small values for RB allocations for further evaluations and then decide based on the observed performances from different companies. |
| Futurewei | Support the moderator’s conclusion that increasing density of PTRS does not lead to non-trivial performance gain, for most of cases studied. While we are also interested in further studies on other cases, e.g., whether higher density is beneficial if small RB is allocated, as proposed by Qualcomm. |
| ZTE, Sanechips | We support moderator’s conclusion.  Regarding Qualcomm’s observation, according to Vivo’s simulation results, for smaller number of PRB allocation, CPE only with lower PTRS density(K=2) will have better performance than ICI compensation with higher density(K=1). |
| Huawei, HiSilicon | We cannot accept the conclusion proposed in point 3-2. From the results submitted by various companies, it seems there may be some benefit to increase the PTRS frequency density depending on the bandwidth and the MCS. Further evaluations should be conducted. |
| NTT DOCOMO | We support the proposal. |
| OPPO | Support |
| Mitsubishi | Not agree. This conclusion seems valid in some scenarios, but at least debatable for others, depending on the bandwidth choice, possibly on MCS also. |
| Lenovo, Motorola Mobility | Agree |
| vivo | We support moderator’s conclusion. The following table summarizes the best scheme with different MCS, SCS and PDSCH RB number. It is observed that CPE-only (K\_PTRS=2) is better thant de-ICI (K\_PTRS=1) in small RB allocation case as mentioned by Qualcomm. Therefore, there is no benefit to introduce K\_PTRS = 1 in terms of performance. |
| LG Electronics | We support Moderator’s conclusion. However, we are open to further discuss it although we have shown in our contribution (R1-2103346) that current PTRS density (i.e., K=2 or 4) will be optimal even for small RB allocation. In addition, we think that decreasing PTRS frequency density, e.g., K=6, in large RB allocation can be also discussed together for PTRS overhead reduction. |
| Nokia/NSB | Support the moderator’s conclusion. |
| CATT | We support the proposal. |
| Spreadtrum | We support the proposal. |
| Ericsson | We support the moderator's conclusion. In all cases we investigated, the best receiver settings with PTRS density K = 2 always outperform the best receiver settings with PTRS density K = 1. |
| Charter | We support the proposal. |

#### For DFT-s-OFDM

In last RAN1 meeting, the following was agreed.

Companies are encouraged to study at least the following aspects for potential PTRS enhancement for DFT-s-OFDM for NR operation in 52.6 to 71 GHz

* The need of potential PTRS enhancement
* PTRS pattern with more PTRS groups within one DFT-s-OFDM symbol when a large number of PRBs is scheduled

The following contributions submitted to in this meeting evaluated and studied on the need of potential PTRS enhancement for DFT-s-OFDM.

[1, Huawei] evaluated a new PTRS pattern with more PTRS groups within one DFT-s-OFDM symbol. It is observed that BLER performance of high MCS (e.g, MCS 26) with large scheduled bandwidth can be improved by using a new pattern with more PTRS groups within one DFT-s-OFDM symbol. [1, Huawei] brought up another issue of PTRS group placement for PTRS with It observed that due to Rx timing shift, (part of) a PTRS group placed at the tail of the transmitter’s DFT-s-OFDM symbol, may wrap-around to the head of the symbol from the receiver’s perspective, thus deteriorating PN compensation performance.

[4, vivo] compared PUSCH performance of DFT-s-OFDM with different PTRS configurations. It is observed that for MCS-7, MCS-16 and MCS-22, the performance gain of increasing PTRS chunk number is small (<0.8 dB). The gain is more noticeable for MCS-26. However, a question on the motivation of PTRS enhancement for DFT-s-OFDM is raised in [4, vivo] when it is observed that DFT-s-OFDM is mainly used for UL coverage, it is unlikely that very high MCS, such as MCS-26, is typically used with DFT-s-OFDM.

[5, Nokia] compared PUSCH performance of DFT-s-OFDM with different PTRS configurations and showed performance improvement of 64QAM with 120 kHz SCS by increasing the maximum number of PTRS groups and keeping the same number of samples per group (i.e. with increased total PTRS overhead).

[14, Intel] evaluated PUSCH performance of DFT-s-OFDM with different PTRS configurations and showed that PUSCH PTRS patterns with only 4 and 8 PTRS groups provide acceptable performance with 120kHz SCS. It also showed performance gain from 0.5dB to 1.7dB for code block interlacing within a DFT-s-OFDM symbol at MCS22.

[16, Qualcomm] compared PUSCH performance of DFT-s-OFDM with different number of PTRS samples and observed no significant gain (< 0.4 dB for 10% BLER) for increasing the total number of PTRS samples to 64 for MCS 22, while small gains (~0.6 dB for 10% BLER) for MCS 24. In addition, increasing the number of PTRS samples beyond 64 is not helping the performance.

[24, ZTE] evaluated DFT-s-OFDM PUSCH performance of 120 kHz with 64QAM and showed a gain (~0.5 dB for 10% BLER target and ~2 dB for 1% BLER target) at MCS 22 with TDL-A 10 ns.

Companies’ results showing significant performance gain and preference to support new PTRS configuration with more PTRS groups within one DFT-s-OFDM symbol when a large number of PRBs is scheduled are summarized below.

Yes: [1, Huawei], [5, Nokia], [24, ZTE]

No: [4, vivo], [14, Intel], [16, Qualcomm]

Moderator’s comment:

Looking at available evaluation results from contributions, companies’ views are not aligned on the gain and whether to support new PTRS configuration with more PTRS groups within one DFT-s-OFDM symbol when a large number of PRBs is scheduled. Given no majority views based on the results, suggest to continue study/discussion.

##### Discussion point 3-3:

Continue study at least the following aspects for potential PTRS enhancement for DFT-s-OFDM for NR operation in 52.6 to 71 GHz

* The need of potential PTRS enhancement
* PTRS pattern with more PTRS groups within one DFT-s-OFDM symbol when a large number of PRBs is scheduled

Companies are encouraged to provide comments if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Qualcomm | We are okay with more evaluations, and we think that some patterns need to be defined for evaluations, e.g., specify some examples of chunk sizes and number of chunks. Then, we can decide based on the performance at both 10%/1% BLER points. |
| Futurewei | Given limited results available, support FFS on potential PTRS enhancement for DFT-s-OFDM. |
| ZTE, Sanechips | We agree with moderator’s suggestion to continue the study the need of potential enhancement for DFT-s-OFDM. |
| Intel | We agree that for larger subcarrier spacing such as 960kHz, the need for having dense PTRS is less motivating. However, for smaller subcarrier spacing, e.g. 120kHz, common phase noise compensation isn’t sufficient to provide adequate performance to receive specific MCS and RB allocations and advanced phase noise compensation techniques may need to be looked into at the UE side.  In our evaluations, we found that to order to leverage advanced phase noise compensation techniques, reasonable number of PTRS tones is needed. This means higher density for smaller RB allocation is needed.  If companies do not wish to provide performance guarantees for the smaller RB allocations, we would like to ask to either support capability signalling such that UEs could indicate no support for smaller RB allocations for specific modulation order, or describe in the specification that UE are not require to support such cases.  Basically, we do not want cases when UE cannot reasonably support smaller RB allocations with 64 QAM, to the reason for the UE to indicate it cannot support 64QAM altogether.  So we would be ok to accept the proposed conclusion in 3-2, if additional bullets mention specification will support mechanism to either allow UE to indicate optional support for the problematic cases or will state the problematic cases are not required to be supported by the UE. |
| Huawei, HiSilicon | Some contributions are missing in the summary (Mitsubishi’s) or conclusions may not be clearly reflected in the summary.  It is unclear why in this case where views are not aligned on the gains it is proposed to continue studying, whereas for CP-OFDM where views are also not aligned on the gains it is proposed to stop the discussion. We are in principle fine with point 3-3, but would suggest first identifying the reasons why different companies obtained different results.  In Qualcomm’s evaluations, the number of samples per group could have been reduced to 2 since the additional overhead is not helpful at the high SNR used for scheduling high MCS.  In Vivo’s evaluations, the scheduled bandwidth for DFT-s-OFDM is unclear. |
| NTT DOCOMO | We are ok with the proposal. |
| Mitsubishi | Generally OK, but some simulation assumptions would be helpful in order to be able to make some progress the next time. |
| Lenovo, Motorola Mobility | Fine to further discuss |
| vivo | We agree with moderator’s suggestion.  It should be aligned that DFT waveform is mainly used for UL coverage, thus high MCS (like MCS-26) should not be the major factor for evaluating the performance.  Response to Huawei’s question:  In our contribution, the scheduled bandwidth for DFT-s-OFDM was defined in Table 7: PUSCH allocation (RB) = 256. |
| LG Electronics | We are ok with the Moderator’s suggestion. |
| Nokia/NSB | Support the Moderator’s proposal. |
| CATT | We support the proposal. |
| Spreadtrum | We support the proposal. |

#### Other issue(s)

Please provide comments if any on any missed issue(s) about PTRS.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
|  |  |
|  |  |
|  |  |

## 2.4. DMRS

### Individual observations/proposals

The following are individual observations/proposals from the contributions.

|  |  |
| --- | --- |
| Sources | Observations/proposals |
| [1, Huawei] | *Observation 3: For 480 kHz and 960 kHz, increasing frequency density of DMRS type I provides no gain, when compared with the existed DMRS frequency density.*  *Proposal 12: The existing DMRS density in frequency domain of DMRS type I can be reused for 480 kHz and 960 kHz directly, and increasing the frequency density of DMRS type I is unnecessary.*  *Observation 4: For 480 kHz and 960 kHz, bundling DMRS per multi-slot performs better than the reused DMRS pattern mapped per slot.*  *Proposal 13: Support multiple consecutive symbols of DMRS for the multi-slot scheduling, whose absolute time duration is same as that of 120 kHz DMRS with the same configuration.* |
| [2, OPPO] | Proposal 11: Enhancements to DMRS pattern for 480kHz and 960kHz SCSs in the new frequency range should be supported. |
| [4, vivo] | Observation :   * Comparing with legacy pattern (type-1 with FD-OCC), ‘type-1 no FD-OCC’ has obvious performance gain for DS >= 20ns; * ‘DMRS on every RE with FD-OCC’ has better performance than ‘Type-1 with FD-OCC’ and ‘Type-1 no FD-OCC’, and the performance between DMRS on every RE with/without FD-OCC is very close; * ‘Type-1 no FD-OCC’ and ‘DMRS on every RE with FD-OCC’ still support 2-port transmission, which can be used for MU-MIMO or 2-layer transmission for single UE; * ‘Type-1 no FD-OCC’ still supports data multiplexing in DMRS symbols, while ‘DMRS on every RE’ can’t support this.   Proposal 4: Type-1 without FD-OCC or increasing the DMRS density in frequency (DMRS on every RE with FD-OCC) can be considered. |
| [5, Nokia] | *Observation 17: Existing RAN1 specification provides support for flexible configuration of different DMRS antenna ports belonging into same or different CDM groups for rank-1 and rank-2.*  *Observation 18: For rank-1, type-1 and new type (“comb-1”) w/o OCC-2 can achieve better BLER performance of PDSCH compared with the type-2 DMRS w/o OCC-2 with SCSs =480 and 960 kHz.*  *Observation 19: For rank-2, both type-1 and type-2 DMRS w/o OCC-2 outperfom other DMRS types in BLER performance with SCSs=480 and 960 kHz.*  *Observation 20: Type-1 w/o OCC-2 outperforms in BLER performance other DMRS types in the most of the considered cases.*  *Observation 21: It is reasonable to provide a specification support for DMRS of PDSCH/PUSCH to be optimized only up to rank-2 in Rel-17 for at higher carrier frequencies (>52.6 GHz).*  *Observation 22:* *New DMRS type (irrespective of rank 1 or rank 2) does not provide any possibility for multiplexing of it with any other type of signal/RS/channel into same OFDM symbol.*  *Observation 23: Due to additional RS overhead associated with the new DMRS type, the usage of new DMRS type leads to reduced achievable PUSCH/PDSCH throughput in comparison with type-1 DMRS w/o OCC.*  *Observation 24:* *New DMRS type approximately doubles the computational complexity of the channel estimation associated with PUSCH/PDSCH.*  *Observation 25: It is not feasible to introduce new DMRS type for PUSCH/PDSCH in Rel-17 for above 52.6 GHz.*  *Proposal 21:* *No additional DMRS pattern is supported in Rel-17 for above 52.6 GHz.*  *Proposal 22:* *Support one of following alternatives for enhancement of the rank 1 PDSCH DM-RS reception.*   * *Alt 1: UE assumes no MU-pairing is applied when scheduled with 1 DM-RS port* * *Alt 2: Introduce new antenna port mapping of rank 1 scheduling and no MU-pairing.* |
| [7, CATT] | Proposal 9: Use existing DMRS patterns for NR operation in 52.6 to 71 GHz, different DMRS pattern with increased frequency domain density is not supported.  Proposal 10: Additional potential DMRS enhancement for multi-PDSCH/PUSCH scheduling is not supported. |
| [9, Futurewei] | *Observation 1: The inherent interplays between CE and PN-induced ICI for beyond 52.6GHz worth in-depth further studies.*  *Observation 2: For beyond 52.6GHz with the standard-compliant implementation, symbol-wise ICI cancellation is needed for efficient PN cancellation as observed in prior meetings. On symbols without PT-RS, DMRS is utilized for PN cancellation purpose.*  *Proposal 1: For PN cancellation on symbols without PT-RS, the same number of DMRS tones with the number of PT-RS tones on each symbol is recommended. Using the full DMRS or more tones than the PT-RS symbol tones for the cancellation does not provide non-trivial gain.*  *Observation 3: The CE with dual-purpose PT-RS outperforms legacy CE and CE with DMRS staggering under the larger SCSs with larger DSs for both MSE and BLER.*  *Proposal 2: Consider using PT-RS for both the purpose of ICI cancellation and CE when necessary; consider introducing different staggering levels for different PT-RS symbols to cover as many REs as possible.*  *Observation 9: Channel differences between consecutive slots of multi-PDSCH/PUSCH under higher SCS are typically smaller than that of the lower SCSs, such that one may take advantage of a non-uniform DMRS allocation to improve the CE accuracy.*  *Proposal 4: Consider non-uniform DMRS reallocation in the time-domain to improve CE for multi-PDSCH/PUSCH.* |
| [10, Ericsson] | Proposal 24 For DMRS-Type 1 for 480 and 960 kHz SCS, support a method for rank-1 transmission that enables the UE to assume that all the remaining orthogonal antenna ports within a CDM group are not associated with transmission of PDSCH to another UE.  Proposal 25 The existing DMRS patterns in Rel-15/16 are sufficient for NR operation in 52.6 – 71 GHz. Do not support introduction of a new DMRS pattern with larger density.  Proposal 26 If there is a need to restrict the number of ports that can be indicated for NR operation in the 52.6 – 71 GHz band, that can be discussed in the context of UE capabilities. Do not support introduction of restrictions in RAN1 specifications. |
| [12, Lenovo] | *Observation 1: For higher SCS values such as 480kHz and 960kHz, BLER performance difference between the ideal channel estimation and real channel estimation varies for different SCS values, where, as the subcarrier spacing is increasing, the performance degradation with real channel estimation also increases which could be attributed to the performance of DM-RS configuration with different SCS values.*  *Proposal 6: For supporting NR between 52.6 GHz and 71 GHz with high subcarrier spacing values including 480kHz and 960kHz, new DM-RS configurations should be supported with following criterion:*   * *High frequency density of the DM-RS for high SCS for better channel estimation when channel coherence bandwidth is less than the configured SCS* * *Reduced number of DM-RS ports as the performance gain of high rank MIMO channels is expected to be limited in this FR*   *Proposal 7: For supporting NR between 52.6 GHz and 71 GHz with high subcarrier spacing values including 480kHz and 960kHz, it should be agreed to not support FD-OCC for DMRS type 1 and type 2 configuration and maximum number of orthogonal DMRS ports are reduced*   * *DMRS type 1:*   + *1-symbol: No FD-OCC, maximum # of DMRS ports is 2*   + *2-symbol: No FD-OCC, maximum # of DMRS ports is 4* * *DMRS type 2:*   + *1-symbol: No FD-OCC, maximum # of DMRS ports is 3*   + *2-symbol: No FD-OCC, maximum # of DMRS ports is 6* |
| [14, Intel] | Proposal 6: Indicate to UE that CDM groups, signaled in scheduling DCI, do not contain potential co-scheduled DMRS ports at least for DMRS Type-1 and maxLength=1.  Proposal 7: Use the reserved codepoints from Tables 7.3.1.2.2-1/1A to signal DMRS port(s) without co-scheduled DMRS ports within the same CDM group as given in Table 3‑1 and Table 3‑2.  Table 3‑1. Updated Table 7.3.1.2.2-1 [2]. Modifications are highlighted with red color.   |  |  |  | | --- | --- | --- | | One Codeword:  Codeword 0 enabled,  Codeword 1 disabled | | | | Value | Number of DMRS CDM group(s) without data | DMRS port(s) | | 0 | 1 | 0 | | 1 | 1 | 1 | | 2 | 1 | 0,1 | | 3 | 2 | 0 | | 4 | 2 | 1 | | 5 | 2 | 2 | | 6 | 2 | 3 | | 7 | 2 | 0,1 | | 8 | 2 | 2,3 | | 9 | 2 | 0-2 | | 10 | 2 | 0-3 | | 11 | 2 | 0,2 | | 12 | 1 | 0, no co-scheduled DMRS ports | | 13 | 2 | 0, no co-scheduled DMRS ports | | 14 | 2 | 2, no co-scheduled DMRS ports | | 15 | 2 | 0,2, no co-scheduled DMRS ports |   Table 3‑2. Updated Table 7.3.1.2.2-1A [2]. Modifications are highlighted with red color.   |  |  |  | | --- | --- | --- | | One Codeword:  Codeword 0 enabled,  Codeword 1 disabled | | | | Value | Number of DMRS CDM group(s) without data | DMRS port(s) | | 0 | 1 | 0 | | 1 | 1 | 1 | | 2 | 1 | 0,1 | | 3 | 2 | 0 | | 4 | 2 | 1 | | 5 | 2 | 2 | | 6 | 2 | 3 | | 7 | 2 | 0,1 | | 8 | 2 | 2,3 | | 9 | 2 | 0-2 | | 10 | 2 | 0-3 | | 11 | 2 | 0,2 | | 12 | 2 | 0,2,3 | | 13 | 2 | 0, no co-scheduled DMRS ports | | 14 | 2 | 2, no co-scheduled DMRS ports | | 15 | 2 | 0,2, no co-scheduled DMRS ports |   Proposal 8: Do not introduce new DMRS patterns for NR extension from 52.6 GHz up to 71 GHz. |
| [15, Apple] | *Proposal 8: Use existing DMRS patterns for NR operation in 52.6 to 71 GHz.*  *Proposal 9: To account for transmission with large SCSs in low coherence BW channels,*   * *turn on or off the FD-OCC based on the scenario the channel is in* * *configure the UE with a DMRS port pattern based on the new SCSs and the coherence bandwidth of the channel* |
| [16, Qualcomm] | Observation 6: For rank 1, with SCS 960kHz, for channels with larger DS, the main reason of performance degradation with the larger SCS is the loss of orthogonality, and the gain from increasing the frequency density of the DMRS tones is limited, i.e., the performances of Config.1 with no CDMing and the new configuration with no CDMing are very close to each other.  Observation 7: For rank 1, with SCS 480kHz, even for channels with larger DS, the different DMRS patterns have very comparable performances, and the best performance is obtained Config.1 with no CDMing.  Observation 8: For rank 2, with SCS 960kHz, with DS 20ns all DMRS patterns perform the same, while with DS 50ns, there is a significant performance loss when FD-OCC is ON, and the best performance is obtained with config type 1 with ports from different CDM groups.  Observation 9: For rank 2, with SCS 480kHz, all DMRS patterns perform the same.  Proposal 5: Do not introduce a new pattern with DMRS tones sent over every RE, for the higher band.  Proposal 6: For DMRS enhancement for high SCSs, while communicating over channel with large DS, for rank 1, a single port should be used from one CDM group and the remaining ports from the same group should not be assigned to other UEs. This information should be provided to the UE via the scheduling DCI or additional rules to be defined in the specs based on the scheduled MCS. |
| [17, Samsung] | Proposal 4: Support DMRS overhead reduction in time domain and DMRS bundling across multiple PDSCH/PUSCHs. |
| [18. Sony] | Proposal 9: High frequency dense DMRS mapping should be supported for new SCS |
| [19, LG] | Proposal #10: DM-RS configuration without FD-OCC should be supported for high SCS.  Proposal #11: Further study on how to indicate implicitly that FD-OCC is not applied to DM-RS port is required. |
| [20, CEWiT] | Proposal 8: Support for a new DMRS design for NR above 52.6GHz to improve channel estimation accuracy. |
| [22, InterDigital] | *Observation 1: Type-2 DM-RS shows performance loss due to insufficient RS density in low SNR.*  *Observation 2: Type-1 DM-RS shows performance loss due to FD-CDM in nonconsecutive REs.*  *Observation 3: Dynamic switching between the existing pattern and DM-RS with enhanced density provides best performance.*  *Proposal 1: Support proposed DM-RS pattern with dynamic switching for PDSCH and PUSCH with larger SCSs.*  *Observation 4: Dynamic switching can be achieved by utilizing reserved values for antenna port(s) indication table in DCI.*  *Proposal 2: Support the updated antenna port(s) indication table for enhanced density DM-RS.* |
| [24, ZTE] | Observation 6: With the same total RS power, Rel-15 DMRS Type 1 pattern and the new DMRS pattern that fully occupied in frequency domain show comparable performance.  Proposal 10: Reuse the Rel-15 legacy DMRS pattern for 52.6GHz~71GHz.  Proposal 11: Consider to relax the restriction on DMRS ports for PUSCH and PDSCH when PTRS is configured.  Proposal 12: Consider the impact of phase noise on port number of other reference signals and control signals. |
| [26, NTT DOCOMO] | Proposal 2: Support DMRS configuration, in which FD-OCC is not applied for 480 kHz and 960 kHz SCS, for Type1 and/or Type 2 DMRS  Proposal 3: Support new DMRS pattern with increased frequency domain density than the existing DMRS patterns for 480 kHz and 960 kHz SCS. |
| [28, Charter] | Observation 1: High-density DMRS (12 REs per PRB), enhances PDSCH performance of high MCSs in NR beyond 52.6 GHz when the MCS (effective code rate) is the same as Rel-15 DMRS.  Observation 2: High-density DMRS (12 REs per PRB), when keeping TBS the same with respect to Rel-15 DMRS, may yield a performance degradation for both CPE compensation and de-ICI filtering.  Proposal 1: Do not introduce high-density PDSCH DMRS for 960 kHz SCS. |

### Summary on DMRS

#### Frequency domain density and number of DMRS port

The following was agreed in last RAN1 meeting.

* Existing DMRS patterns are supported for NR operation in 52.6 to 71 GHz with 120 kHz SCS.
* At least existing DMRS patterns are supported for NR operation in 52.6 to 71 GHz with 480 kHz and/or 960 kHz SCS
* Further study on whether to introduce different DMRS pattern with increased frequency domain density (in number of subcarriers) than the existing DMRS patterns for NR operation in 52.6 to 71 GHz with 480 kHz and/or 960 kHz SCS
* Further study on whether and how to restrict DMRS port configuration (e.g., the number of DMRS ports) as in FR2 for NR operation in 52.6 to 71 GHz with 480 kHz and/or 960 kHz SCS

On the need of DMRS enhancement for 480 and 960 kHz SCS, the following contributions submitted to this meeting evaluated and compared BLER performance using the existing comb DMRS pattern against some new DMRS patterns.

[1, Huawei] compared two DMRS frequency densities of type 1: DMRS is mapped on all the subcarriers with no power boosting, and DMRS is mapped on every 2nd subcarrier with 3dB power boosting, which means PDSCH is not multiplexed with DMRS at a same symbol. It is observed that increasing DMRS frequency density provides no gain.

[2, OPPO] compared performance among Type-1 DMRS pattern, Type-2 DMRS pattern and a new DMRS pattern for all SCSs under MCS16. It observed similar performance between the new FDM pattern and Type-1 FDM pattern. It also observed performance gain (0.8 dB for 480 kHz and about 1.5 dB for 960 kHz SCS) of the new CDM pattern compared to existing CDM patterns.

[4, vivo] compared performance of Rel-15 Type-1 DMRS and DMRS on every RE for high MCS with different DS. It is observed that ‘DMRS on every RE with FD-OCC’ has better performance than ‘Type-1 with FD-OCC’.

[5, Nokia] compared BLER performance of rank-1 and rank-2 PDSCH for different DMRS configuration options w/ and w/o OCC-2 (i.e. Rel-15 type-1, Rel-15 type-2 and new type (“comb-1”) ) without any phase noise impairments for 480 and 960 kHz SCS. It is observed that new type DMRS (i.e. comb-1 or increased frequency density) does not outperform Type-1 w/o OCC-2.

[10, Ericsson] compared BLER performance of rank-1 PDSCH for type-1 DMRS with that of an ideal channel estimation for 480 and 960 kHz SCS. It is observed that for MCS 22/24/26/28 the gap in performance between genie/practical channel estimators is insignificant (< 0.9 dB) for all DS evaluated. In other words, there is little room for improvement using an enhanced DMRS design.

[12, Lenovo] evaluated BLER performance of DMRS mapped to each RE in frequency domain and showed about 1 dB gain for 960 kHz SCS compared to existing type-1 DMRS. It also proposed to reduce number of DM-RS ports as the performance gain of high rank MIMO channels is expected to be limited in this FR.

[15, Apple] compared the performance of new pattern (increased density) for the 960 kHz SCS with different channel delay spreads at 5 usec, 10 usecs, and 20 usec for MSCS 22. It observed a small improvement (0.5 dB at 10-1 for DS = 20) in BLER performance and proposed that new pattern should not be adopted.

[16, Qualcomm] compared PDSCH performance of a new DMRS pattern featured by high frequency density (i.e., every RE) and 2-FD-OCC across adjacent REs with existing type-1 and type-2 DMRS patterns with 480 and 960kHz SCS. It is observed that the gain from increasing the frequency density of the DMRS tones is limited (e.g., < 0.2 dB when CDM is off for MCS22).

[17, Samsung] argued that considering the channel in 52.6~71GHz is typically not sufficiently uncorrelated to support large layers and the multiplexed MU-MIMO UEs is limited, Type-2 DMRS is not a typical configuration, thus no need to consider the optimization for Type-2 DMRS. For Type-1 DMRS, the performance is acceptable in case of using FDMed port, e.g. port 0 & 2, which is already supported by the existing DMRS configuration, thus no need to enhance as well.

[22, InterDigital] compared BLER and throughput performances of Rank 1 and Rank 2 for 480 and 960 kHz SCS. It observed performance gain of an enhanced DMRS pattern with increased density for low SNR UEs. It proposed to support new DMRS pattern and dynamic switching of existing and new patterns.

It is observed in [24, ZTE] that with the same total RS power, Rel-15 DMRS Type 1 pattern and the new DMRS pattern that fully occupied in frequency domain show comparable performance.

[26, NTT DOCOMO] have evaluated PDSCH BLERs with 480 and 960 kHz SCS for different DMRS patterns with 2-port configuration, i.e., Rel-15 DMRS type 1 with comb and non-comb (i.e., FD-OCC) based 2-port configuration, Rel-15 DMRS type 2 with comb and non-comb (i.e., FD-OCC) based 2-port configuration, and 2-port DMRS with DMRS on every RE in the symbol containing DMRS. It observed performance gain of full-density DMRS.

[28, Charter] compared PDSCH performance of higher-density DMRS (12 REs per PRB) with that of Rel-15 DMRS for 960 kHz SCS. It observed performance gain of high density when the MCS (effective code rate) is the same as Rel-15 DMRS. However, it also observed when keeping the TBS the same with respect to Rel-15 DMRS, high density DMRS may yield a performance degradation for both CPE compensation and de-ICI filtering.

In addition to BLER performance, other aspects of block DMRS including the possibility for multiplexing of it with any other type of signal/RS/channel into same OFDM symbol, extra overhead and computational complexity of channel estimation are discussed in [5, Nokia].

Companies’ results showing significant performance gain and preference to support increased DMRS frequency density or new pattern are summarized below.

Yes: [2, OPPO], [4, vivo], [12, Lenovo], [22, InterDigital], [26, NTT DOCOMO]

No: [1, Huawei], [5, Nokia], [10, Ericsson], [15, Apple], [16, Qualcomm], [17, Samsung], [24, ZTE], [28, Charter]

Moderator’s comment:

Looking at available evaluation results from contributions, more results showing no significant performance gain of new DMRS pattern (e.g., increased frequency density). Given majority views based on the results and potential support of disabled FD-OCC (as in Discussion point 4-2), suggest the following.

##### Discussion point 4-1:

* Conclude that no new DMRS pattern with increased frequency domain density (in number of subcarriers) than the existing DMRS patterns for NR operation in 52.6 to 71 GHz with 480 kHz and/or 960 kHz SCS in Rel-17
* Further study on whether and how to restrict DMRS port configuration (e.g., the number of DMRS ports) as in FR2 for NR operation in 52.6 to 71 GHz with 480 kHz and/or 960 kHz SCS

Companies are encouraged to provide comments if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Qualcomm | We support precluding introducing new DMRS pattern for the new band. Restricting the DMRS port configuration might not be need in several cases based on the MCS and channel conditions |
| Futurewei | Support the moderator’s comment on not to increase the frequency domain density of DM-RS. Agree with [17, Samsung] that “considering the channel in 52.6~71GHz is typically not sufficiently uncorrelated to support large layers and the multiplexed MU-MIMO UEs is limited, Type-2 DMRS is not a typical configuration, thus no need to consider the optimization for Type-2 DMRS.”  Prefer further study on DM-RS sequence design under the existing density for better CE performance. |
| ZTE, Sanechips | We support moderator’s conclusion.  Regarding the restriction on DMRS port, we share similar view with Qualcomm, in some cases such as lower modulation order(QPSK or 16QAM), there is no need to restrict the DMRS port number. |
| Intel | We agree with the conclusion not to introduce new DMRS pattern |
| Huawei, HiSilicon | Agree with the first bullet point. If the second bullet point is related only to FD OCC then it may only need to be discussed under 2.4.2.2. |
| NTT DOCOMO | According to the evaluation results from multiple companies, there would be some situations where new DMRS pattern with increased frequency domain density seems beneficial. So we prefer to have this functionality even as optional. |
| OPPO | We want to emphasize that from our simulation analysis, the DMRS enhancement was not just the density but rather the CDM orthogonality, which appears to be more problematic for type 1 DMRS than type 2 DRMS. Thus, it is not only an optimization for type 2 DMRS as Samsung and Futurewei pointed. From our simulation, DMRS enhancements can bring considerable gain vs. the legacy DMRS, even keeping the same density.  https://ttpic.myoas.com/g8/M00/88/FC/rBAoMGB2pHqAONCEAACpCCpWLsU545.png?w=389&h=295&s=43272  Secondly, there are proposals to switch off the FD-OCC, which may improve the performance, but we’d like to point that out if this applies to single symbol DMRS, it may impact the MU-MIMO functionality. Thus, it does not come for free.  In summary, to our understanding RAN1 has acknowledged the issue for existing DMRS. There are two alternatives to address the issue  Alt-1: keeping legacy DMRS design but turning off the FD-OCC.  Alt-2: new DMRS design  We think that RAN1 should compare this two alternatives by analyzing the pros and cons before precluding Alt 2 at this stage. |
| Lenovo, Motorola Mobility | We are fine with first bullet to not consider new DMRS.  Regarding second bullet, we think that DMRS port restriction should be discussed under FD OCC as it will be natural outcome if FD OCC switching off is agreed |
| vivo | We think that increasing DM-RS frequency domain density could be discussed together with Frequency domain OCC since they target to increase sampling rate of channel estimation in frequency domain. According to our evaluation, either disabling FD-OCC (i.e. Type 1 DM-RS with no FD-OCC) or increase DM-RS frequency domain density (Keep Type 1 DM-RS design but with increasing density) achieve similar performance which are better than existing scheme (i.e. Type 1 DM-RS with FD-OCC).  Agree with OPPO that two Alternatives can be compared but with the following more concrete Alt-2:  Alt-1: keeping legacy DMRS design but turning off the FD-OCC.  Alt-2: keeping legacy DMRS design but increase density (i.e. DM-RS on every RE) |
| LG Electronics | Same view with Huawei, HiSilicon. |
| Nokia/NSB | Support the Moderator’s proposal, and OK with Huawie’s suggestion. |
| CATT | Fine with first bullet. |
| Spreadtrum | We share the same view as Huawei. |
| Ericsson | Agree on the first bullet.  Regarding the 2nd bullet, I have a question regarding restriction of the number of ports. The claim is made to "restrict the number of ports as in FR2". Where is this restriction in specifications? I don't see it. |
| Charter | We agree not to introduce new DMRS pattern. |

#### Frequency domain OCC

The following was agreed in last RAN1 meeting.

Further study on at least the following aspects of potential DMRS enhancement with respect to FD-OCC:

* whether to support a configuration of DMRS in which FD-OCC is not applied for 480 kHz and 960 kHz SCS
  + Applicability to Type-1 and/or Type-2 DMRS
  + Details on whether and how to indicate that FD-OCC is not applied to DMRS port
  + Impact to UE multiplexing capacity and inter-UE interference in MU-MIMO

The following contributions studied and evaluated performance with respect to FD-OCC.

[4, vivo] compared PDSCH BLER performance of type-1 DMRS with and without FD-OCC for 480KHz and 960 KHz SCS with 64QAM, while the phase noise is compensated with CPE only approach. It observed some gain of type-1 DMRS without OCC for high MCS especially at large delay spread (e.g., TDL-A 40 ns).

[5, Nokia] compared BLER performance of rank-1 and rank-2 PDSCH for different DMRS configuration options w/ and w/o OCC-2 (i.e. Rel-15 type-1, Rel-15 type-2 and new type (“comb-1”) ) without any phase noise impairments. It is observed that Type-1 w/o OCC-2 outperforms other DMRS configurations.

[10, Ericsson] compared BLER performance of rank-2 PDSCH for type-1 DMRS with and without FD-CDM against that of an ideal channel estimation for 480 and 960 kHz SCS. It is observed that for MCS 22/24/26/28, there’s performance gain without FD-CDM especially for large DS and very high MCS.

[12, Lenovo] also evaluated BLER performance of DMRS mapped to each RE in frequency domain and showed about 1 dB gain for 960 kHz SCS compared to existing type-1 DMRS. It also proposed to reduce number of DM-RS ports as the performance gain of high rank MIMO channels is expected to be limited in this FR.

[14, Intel] evaluated PDSCH performance with and without frequency domain OCC being enabled for DMRS. For higher order modulation such as 64QAM (MCS 22), it observed the performance drop when OCC is enabled.

[15, Apple] evaluated PDSCH performance of type-1 DMRS with and without FD-OCC for 960 kHz SCS. It observed that at high frequency selectivity (low coherence bandwidth for large delay spread) there is a benefit in turning off the FD-OCC.

[16, Qualcomm] compared PDSCH performance of a new DMRS pattern featured by high frequency density (i.e., every RE) and 2-FD-OCC across adjacent REs with existing type-1 and type-2 DMRS patterns with 480 and 960kHz SCS. It is observed that for channels with larger DS, the main reason of performance degradation with the larger SCS is the loss of orthogonality. It showed performance gain without CDM for MCS22/26.

[26, NTT DOCOMO] have evaluated PDSCH BLERs with 480 and 960 kHz SCS for different DMRS patterns with 2-port configuration, i.e., Rel-15 DMRS type 1 with comb and non-comb (i.e., FD-OCC) based 2-port configuration, Rel-15 DMRS type 2 with comb and non-comb (i.e., FD-OCC) based 2-port configuration, and 2-port DMRS with DMRS on every RE in the symbol containing DMRS. It observed performance gain when FD-OCC is off for both type 1 and type 2 DMRS.

Based on the evaluation results, multiple sources ([4, vivo], [5, Nokia], [10, Ericsson], [12, Lenovo], [14, Intel], [15, Apple], [16, Qualcomm], [19, LG], [26, NTT DOCOMO]) proposed to support a configuration of DMRS where FD-CDM can be turned off. [12, Lenovo] and [26, NTT DOCOMO] proposed FD-OCC is turn off for both type 1 and type 2 DMRS configuration and to reduce the maximum number of orthogonal DMRS ports.

On how to indicate to UE, [14, Intel] and [16, Qualcomm] proposed to indicate this to UE via DCI while [5, Nokia] proposed an alternative where UE assumes no MU-pairing is applied when scheduled with 1 DM-RS port. [19, LG] preferred to indicate implicitly that FD-OCC is not applied to DM-RS port.

On the other side, [17, Samsung] argued that the necessity of frequency domain OCC on/off mechanism is unclear given channel estimation algorithm depends on UE implementation and applying frequency domain OCC does not necessarily mean the UE has to perform despread operation.

Companies’ results showing significant performance gain and preference to support FD-OCC off are summarized below.

Yes: [4, vivo], [5, Nokia], [10, Ericsson], [12, Lenovo], [14, Intel], [15, Apple], [16, Qualcomm], [19, LG], [26, NTT DOCOMO]

No: [17, Samsung]

Moderator’s comment:

With majority views to support a DMRS configuration with FD-OCC is off, suggest the following.

##### Proposal 4-2:

* At least for DMRS type-1, support a configuration of DMRS in which FD-OCC is not applied for 480 kHz and 960 kHz SCS.
  + FFS whether applies to DMRS type-2
  + FFS details on whether and how to indicate that FD-OCC is not applied to DMRS port

Companies are encouraged to provide comments if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Qualcomm | We support the proposal |
| Futurewei | Support this proposal on DMRS with FD-OCC off for 480kHz and 960kHz SCS. |
| ZTE, Sanechips | We support the proposal. |
| Intel | We support dynamic ON/OFF of FD-OCC at least for DMRS type-1. We also think that SCS 120 kHz also benefits from dynamic ON/OFF of FD-OCC. In our view, the proposal could be modified as follows:   * At least for DMRS type-1, support dynamic indication that there is no co-scheduled DMRS ports within a CDM group (i.e. FD-OCC is not applied to DMRS ports).   + FFS whether applies to DMRS type-2   FFS details on how to support the dynamic indication that there is no co-scheduled DMRS ports within a CDM group |
| Huawei, HiSilicon | DMRS assignments can be chosen by gNB to avoid that UE would have to despread OCC under certain conditions such as MCS. It is likely that there are enough DMRS port numbers in such high frequency scenarios where UEs won’t be scheduled with a large number of MIMO layers. So it is unclear that new DMRS configurations need to be introduced, the specifications seem to already contain sufficient flexibility to allow UE to demodulate without having to despread OCC. |
| NTT DOCOMO | We support the proposal. |
| OPPO | We don’t support, we see this as an alternative to new DMRS design, which resolves a same problem. This should be discussed together with the new DMRS to have a full analysis on the pros and cons before agreeing on one over the other. |
| Lenovo, Motorola Mobility | We support this proposal.  Although we think that simply it could be agreed that FD OCC is always off when applying SCS value of 480kHz and 960kHz and no explicit indication might be needed.  However, we are open to further discuss, if dynamic switching off is needed or not as suggested by Intel. |
| vivo | As we discussed in 4-1, this issue could be discussed together with 4-1 and down select one of them. |
| LG Electronics | We support the proposal. We also open to further discuss on both implicit and explicit indications. |
| Nokia/NSB | Support the proposal. |
| CATT | Support the proposal. |
| Spreadtrum | We support the proposal. |
| Ericsson | We support the proposal, however, we think the proposal might need to be specific to rank-1. As we discussed in the last meeting, for rank-2, Rel-15/16 already supports a configuration where FD-OCC is not applied by virtue of the following:  **Table 7.3.1.2.2-1: Antenna port(s) (1000 + DMRS port), *dmrs-Type*=1, *maxLength*=1**   |  |  |  | | --- | --- | --- | | **One Codeword:**  **Codeword 0 enabled,**  **Codeword 1 disabled** | | | | **Value** | **Number of DMRS CDM group(s) without data** | **DMRS port(s)** | | 0 | 1 | 0 | | 1 | 1 | 1 | | 2 | 1 | 0,1 | | 3 | 2 | 0 | | 4 | 2 | 1 | | 5 | 2 | 2 | | 6 | 2 | 3 | | 7 | 2 | 0,1 | | 8 | 2 | 2,3 | | 9 | 2 | 0-2 | | 10 | 2 | 0-3 | | 11 | 2 | 0,2 | | 12-15 | Reserved | Reserved |   For DM-RS configuration type 1,  - if a UE is scheduled with one codeword and assigned with the antenna port mapping with indices of {2, 9, 10, 11 or 30} in Table 7.3.1.2.2-1 and Table 7.3.1.2.2-2 of Clause 7.3.1.2 of [5, TS 38.212], or  - if a UE is scheduled with one codeword and assigned with the antenna port mapping with indices of {2, 9, 10, 11 or 12} in Table 7.3.1.2.2-1A and {2, 9, 10, 11, 30 or 31} in Table 7.3.1.2.2-2A of Clause 7.3.1.2 of [5, TS 38.212], or  - if a UE is scheduled with two codewords,  the UE may assume that all the remaining orthogonal antenna ports are not associated with transmission of PDSCH to another UE. |

#### DMRS for multi-PDSCH/PUSCH scheduling

[1, Huawei] compared two DMRS patterns in time domain: Rel-15 DMRS pattern (with individual channel estimation per slot), and a bundling DMRS pattern (with joint channel estimation based on all the DMRS symbols across slots). It observed about 0.2dB~0.6dB gain of the bundling DMRS pattern.

[7, CATT] argued that given the channel estimation filter at the UE is usually optimized with fixed filter length based on current DMRS pattern, DMRS bundling will increase the UE implementation complexity since the enhancement depends on the receiver algorithm in UE implementation. With that, it proposed not to support potential DMRS enhancement for multi-PDSCH/PUSCH scheduling.

[9, Futurewei] observed that channel differences between consecutive slots of multi-PDSCH/PUSCH under higher SCS are typically smaller than that of the lower SCSs and proposed to consider a non-uniform DMRS allocation in time-domain to improve CE for multi-PDSCH/PUSCH.

[17, Samsung] proposed for multiple PDSCHs/PUSCHs with contiguous time domain resource, DMRS time domain density can be lower than one DMRS per PUSCH/PDSCH to reduce DMRS overhead and DMRS bundling of multiple PUSCHs/PDSCHs can be applied to improve channel estimation performance.

On the same topic, [5, Nokia] argued that the decoding of each slot in a period is up to implementation, and new (bundled DMRS) pattern increase the complexity and proposed to use the existing DMRS time-domain pattern for multi-slot scheduling unless any critical performance degradation is identified.

Moderator’s comment:

With limited input and diverse views on this topic, suggest companies to study further.

##### Discussion point 4-3:

Further study whether or not to support potential DMRS enhancement for multi-PDSCH/PUSCH scheduling for NR operation in 52.6 to 71 GHz with 480 and/or 960 kHz SCS considering at least the following aspects:

* DMRS overhead reduction (e.g. DMRS-less slot)
* Multi-slot DMRS bundling
* The impact on the UE/gNB processing timeline
* Note: As per usual procedure, duplication of work between work items in Rel-17 should be avoided

Companies are encouraged to provide comments and/or suggestions on agreeable proposals if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Qualcomm | * For multi-PUSCH grant, a similar discussion is ongoing in the coverage enhancement WI, and there is no need to duplicate the effort. * We do not support DMRS time bundling/skipping for multi-PDSCH grants as this will complicate the UE processing and the performance gains are not expected to be significant. |
| Futurewei | We support potential DMRS enhancement for multi-PDSCH/PUSCH. While more studies are needed to show the performance and complexity tradeoff. |
| ZTE, Sanechips | We support moderator’s proposal to further discuss the multi slot DMRS bundling.  From our perspective, to achieve better channel estimation accuracy, the joint channel estimation based on DMRS in multiple slots can be performed with the current DMRS pattern. There is no need to introduce new pattern or reduce DMRS overhead for DMRS bundling. |
| Intel | We are ok with moderator’s proposal 4-3. |
| Huawei, HiSilicon | Assuming that a baseline UE capability for 480/960 kHz is the same absolute processing timeline as for 120 kHz SCS (which is currently the only known feasible timeline), then if DMRS are present in every slot it means that UE will finish processing a multi-slot PDSCH later than the equivalent single-slot PDSCH with 120 kHz SCS. This could be avoided by ensuring that the last DMRS symbol in a multi-slot PDSCH allocation with 480/960 kHz SCS is no later than the equivalent last DMRS symbol in a single-slot PDSCH allocation with 120 kHz SCS. So we would like to add “location of the last DMRS symbol” to the bullet list. A consequence of such approach would be that the channel estimation on one slot would have to be used for demodulation in another slot, which then naturally leads to the question of enabling cross-DMRS symbol channel estimation (and thus DMRS bundling, possible across slots). |
| Lenovo, Motorola Mobility | We agree with Qualcomm that similar work is on-going in coverage enhancements including different aspects for DMRS including potentially new configurations across multiple slots, if needed.  So, we don’t see the need to duplicate the work here. |
| Vivo | We don’t see strong motivation to discuss this in B52.6GHz WI since there is no significant problem if no DM-RS skipping or bundling. |
| LG Electronics | Similar discussions with other WI should be avoided, as stated in the Note in the proposal. If still needed further discussion, the essential aspects for 480/960 kHz SCS and those do not overlap with the discussion in CE WI should be clarified first. |
| Nokia/NSB | We are open to study. |
| CATT | This part should be down prioritized. |
| Spreadtrum | We share the same view as Qualcomm that duplicate work of DMRS enhancement for multi-PUSCH transmission should be avoided. Meanwhile, we are not supportive of DMRS enhancement for multi-PDSCH transmission. Because it will introduce processing latency and complexity when demodulating at the UE side. |
| Ericsson | We do not support the proposal  DMRS bundling for PUSCH is being discussed in coverage enhancement WI, and we should not duplicate the effort here.  We have strong concerns about DMRS bundling for multi-PDSCH with respect to maintaining phase coherency across slots, especially since it is likely that the PDSCHs will not always occupy contiguous slots. In the coverage enhancement work item, RAN4 has performed some analysis for the UL, and found that there are many caveats to being able to maintain phase coherency including contiguous transmissions, no power changes, etc. A similar outcome would be likely for the DL, making phase coherency assumptions very suspect. We agree with Qualcomm, that DMRS bundling/skipping for multi-PDSCH should be avoided.  We have strong concerns also about DMRS-less slot (DMRS skipping). Huawei suggests the following:  "ensuring that the last DMRS symbol in a multi-slot PDSCH allocation with 480/960 kHz SCS is no later than the equivalent last DMRS symbol in a single-slot PDSCH allocation with 120 kHz SCS"  We fail to see how this would bring any meaningful gains in terms of reduction in processing time considering typical DMRS configurations. Such optimizations should be avoided given the large workload already. |

#### Dual-purpose RS

[9, Futurewei] observed inherent interplays between CE and PN-induced ICI for beyond 52.6GHz such as ICI can lead to CE accuracy degradation for reduction of SNR; ICI is changing symbol-wise, which may lead to phase incoherence between DMRS pilots and etc.. It observed that on symbols without PT-RS, DMRS is utilized for PN cancellation purpose and proposed that for PN cancellation on symbols without PT-RS, the same number of DMRS tones with the number of PT-RS tones on each symbol is recommended. [9, Futurewei] further studied the performance of dual-purpose PTRS where it observed that the CE with dual-purpose PT-RS outperforms legacy CE and CE with DMRS staggering under the larger SCSs with larger DSs. To support PT-RS for both the purpose of ICI cancellation and CE, it proposed to introduce different staggering levels for different PT-RS symbols to cover as many REs as possible.

Moderator’s comment:

With limited input on this topic, suggest companies to study further and have more concrete proposals to discuss.

Companies are encouraged to provide comments and/or suggestions on agreeable proposals if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Futurewei | We would like to thank the moderator for capturing our dual-purpose RS design into the summary. The motivation of our proposal is mainly based on the observation that for the B52 band, PTRS is almost always configured to the higher time/frequency density for ICI cancellation purposes, and this brings an opportunity for using PTRS for the second purpose of channel estimation. The issues are what are the best patterns for dual-purpose PTRS and what is the best way of combining the PTRS-based CE with the DMRS based CE.  Further, we would also like to bring into attention that DM-RS symbols are also utilized for ICI cancellation purposes because of the necessity of ICI cancellation on each and every symbol. This observation implies that DM-RS should serve a dual-purpose as well. Therefore, it seems that an additional opportunity to jointly design the pattern of PTRS and DM-RS exist, with moderate changes needed in RRC and DCI indication.  For multi-PDSCH/PUSCH, the dual-purpose RS design can also apply, and CEs based on PTRS may be collected across slots and be combined with CEs based on DM-RS across slots. |
| Lenovo, Motorola Mobility | We are open to further discuss dual purpose RS for channel estimation and ICI cancellation. |
|  |  |

#### Other issue(s)

Please provide comments if any on any missed issue(s) about DMRS.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
|  |  |
|  |  |
|  |  |

# Conclusion

TBD

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