3GPP TSG-RAN WG1 Meeting #104bis-e Tdoc R1-21xxxxx

e-Meeting, 12th – 20th April, 2021

Agenda Item: 7.2.2

Source: Moderator (Ericsson)

Title: Feature lead summary for Maintenance of UL Signals and Channels

Document for: Discussion, Decision

# 1 Introduction

This document contains a summary of proposals related to UL Signals and Channels made under the agenda item 7.2.2 "Maintenance of NR-based Access to Unlicensed Spectrum." Only one issue is identified.

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| **#** | **Issue** | **Contribution(s)** |
| UL-01 | Clarification on DCI size matching rules for DCI 0\_0 | [1]: R1-2103336 |

# 2 Issue UL-01: Clarification on DCI size matching rules for DCI 0\_0

In [1] it is proposed to clarify the DCI size matching rules for DCI 0\_0 in a CSS when UL resource allocation Type 2 (Interlacing) is configured and the SCS of the active UL BWP and the initial UL BWP are different. It is claimed that there can be an ambiguity, for example, if the active UL BWP is 15 kHz (requires X = 6 bits for FDRA field) and the SCS of the initial UL BWP is 30 kHz (requires X = 5 bits for FDRA field). The following is proposed:

**Proposal 1: For DCI format 0\_0 transmitted in CSS, X bit size of FDRA field in the DCI format 0\_0 is determined based on the SCS of the initial UL BWP.**

* **In case when the SCS of active UL BWP is different from that of initial BWP, some handling is required by considering the difference between X bit size of FDRA field in DCI format 0\_0 and the required number of bits for PUSCH resource allocation.**

This issue was raised several times in previous meetings for potential discussion, and a large majority of companies identified this as not an issue or low priority.

Furthermore, it is the moderator's understanding that DCI 0\_0 will typically be zero-padded up to the size of DCI 1\_0 for all practical cases since the FDRA field of DCI 0\_0 in a CSS (5 or 6 bits) is smaller than the FDRA field of DCI 1\_0 for a 20 MHz DL BWP. For example, assuming 50 RBs, the FDRA field size for DCI 1\_0 will be 11 bits. Thus there is always a sufficient number of bits to indicate the interlace allocation.

Hence it is the moderator's view that this issue is not essential discuss; however, companies are free to provide alternative viewpoints.

# References

1. R1-2103336, "Remaining issues of UL channels and HARQ procedure for NR-U," LGE, RAN1#104bis-e, April 2021.