**3GPP TSG RAN WG1#104e R1-21XXXX**

**E-meeting, 25 January – 5 February 2021**

Agenda Item: **8.9.3**

Source: **Moderator (Sony)**

Title: **Timing relationship for IoT-NTN**

Document for: **Discussion**

# Introduction

This document is the feature lead (FL) summary for the “ Support a maximum DL TBS of 1736 bits as a Rel-17 optional UE capability” agenda item 8.9.3 in RAN1#104e.

The LTE-MTC objective on support for Support a maximum DL TBS of 1736 bits as a Rel-17 optional UE capability was added to the Work Item (WI) on “Additional enhancements for NB-IoT and LTE-MTC” in RAN# 88-e [1]:

|  |
| --- |
| * *Add a Rel-17 optional UE capability to support* *a maximum DL TBS of 1736 bits for HD-FDD Cat. M1 UEs in CE mode A only. [LTE-MTC] [RAN1, RAN2]*   + *Determine soft buffer size [RAN1]*   + *Capability signaling without introducing a new UE category [RAN2]*   + *There shall be no changes to: DCI formats, TBS tables, CQI tables*   + *This objective begins work from RAN#90, i.e. December 2020* |

This document aims to provide a consolidated list of issues that have been identified for the support of a 1736 DL TBS in eMTC.

In the first round of email discussion, companies are invited to answer the questions in sections 2.x.1. The questions are highlighted in cyan.

Timeline: This topic is likely to be discussed at the GTW2 call on Thursday 28 January. There is an email discussion checkpoint on Wednesday 27 Jan. It would be appreciated if companies could provide their inputs by 1700 UTC on Wednesday 27 Jan.

# Overview of Issues from Tdocs

The following issues were identified in input Tdocs:

* Number of soft channels bits
* Combinations of features that support 1736 bit DL TBS
* Usage scenarios and potential benefits for 1736 bit DL TBS
* Specification changes required to support 1736 bit DL TBS
* Capability

## Number of soft channel bits

Table 1 lists the different identified potential methods for determining the number of soft channel bits and the rationales behind these methods.

Table 1 – Proposed numbers of soft channel bits for support of 1736 bit DL TBS

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| --- | --- | --- |
| **Number of soft channel bits** | **Rationale** | **companies** |
| 30720 | Based on number of soft channel bits in a physical allocation.  160\*NPRB\*Q\*N, where:  NPRB = 6  Q is max bits / symbol = 4 (16QAM)  N = number of HARQ processes  *FL note: does this account for incremental redundancy?*  *FL note2: does “160” assume no legacy control region and 1 antenna port?* | Sierra Wireless (section 3) |
| 43008 | Assume 8 HARQ processes.  Note that for the 10 HARQ process feature in Rel-14, 8 HARQ processes was used to determine soft buffer size. | HW-HiSi (section 2), ZTE (proposal 4),  Qualcomm (section 3) |
| 43998 | Scaling the Rel-13 soft buffer size by a factor of 1736 / 1000.  Note: assumes soft buffer size is based on 8 HARQ processes.  *FL note: this method does not take into account that CRC size and number of tail bits are constant and do not scale* | NOK-NSB (observation 3), Ericsson (obs 6) |
| 44352 | FBRM using  N = number of HARQ processes = 14  X = TBS = 1000  Note: if the “14 HARQ processes” AI agreed on FBRM with 14 HARQ processes, there would be 44352 soft channel bits. 1736 DL TBS could use the same number of soft channel bits with the larger TBS (and presumably with LBRM) | NOK-NSB (observation 4) |
| 53760 | FBRM using  N = number of HARQ processes = 10  X = TBS = 1736 | NOK-NSB (observation 4), Ericsson (obs 7) |
| 75264 | FBRM using  N = number of HARQ processes = 14  X = TBS = 1736 | NOK-NSB (observation 4), Ericsson (obs 7) |

**Tradeoffs**

The following tradeoffs are considered in input documents:

* Larger soft buffer size increases peak data rate
  + FL note: the peak data rate can be obtained without HARQ, so this benefit is not clear cut
* Larger soft buffer size increases UE complexity
* Larger soft buffer sizes (than Rel-13: 25344 bits) may require a hardware update
* Smaller soft buffer size reduces performance (LBRM)

**Specification change to support new soft buffer size**

Qualcomm propose the following specification change for support the new number of soft channel bits.

Since we are not introducing a new UE category in TS 36.306, we can specify the new soft buffer size directly in TS 36.212 as follows:

If the UE signals *ue-CategoryDL-v14xy* indicating UE category M2, *N*soft is the total number of soft channel bits according to the UE category indicated by *ue-CategoryDL-v14xy*. Otherwise, if the UE signals *ce-largerDLTBS-r17 N*soft = 43008. Otherwise, if the UE signals *ue-CategoryDL-v1310* indicating UE category M1, *N*soft is the total number of soft channel bits according to the UE category indicated by *ue-CategoryDL-v1310*.

### FL view on number of soft channel bits

Most companies prefer to base the number of soft channel bits on an FBRM (full buffer rate matching) equation. The equation has the form:

Where:

*N* = number of HARQ processes

*X* = DL TBS

The other alternatives are to base the number of soft channel bits on either (1) the number of physical bits in a 6 PRB allocation, (2) scale by a factor of 1736 / 1000 relative to the soft buffer size for TBS = 1000, or (3) the number of soft channel bits for 14 HARQ processes using TBS = 1000.

Basing the number of soft channel bits on the FBRM equation seems reasonable, in keeping with legacy methods for determining the number of soft channel bits and the values derived are essentially similar to other methods.

Question 2.1.1-1: Should the number of soft channel bits be based on the FBRM equation:

?

|  |  |  |
| --- | --- | --- |
| **Company** | **Agree / disagree** | **Comment**  **(if not, what alternative; values of X, N)** |
| Qualcomm | See comments | While we agree with the question, we think it would be much easier to just agree on the number 43008 (i.e., assuming N = 8, as has been done since Release 8). The value of X is the maximum TBS as specified in the WID. |
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**Proposals and observations in input documents**

Proposal 1: The soft channel bits for UEs supporting maximum DL TBS of 1736 bits is 43008 bits. HW-HiSi

Observation 3: The total number of soft channel bits for supporting an increased maximum TBS of 1736 bits based on scaling the total number of soft channel bits specified for supporting a maximum TBS of 1000 bits is 43988. NOK-NSB

Observation 4: The total number of soft channel bits calculated based on a Turbo encoder with mother coding rate of 1/3 as

* 53760 for a maximum DL TBS of 1736 bits and 10 HARQ processes → a factor of ~2.12 increase compared to a legacy UE;
* 75264 for a maximum DL TBS of 1736 bits and 14 HARQ processes → a factor of ~2.97 increase compared to a legacy UE;
* 44352 for a maximum DL TBS of 1000 bits and 14 HARQ processes → a factor of 1.75 increase compared to a legacy UE; NOK-NSB

Proposal 4: Further study the tradeoffs between cost and benefits for different soft buffer size candidates for the increased maximum DL TBS of 1736 bits. Nokia-NSB

Proposal 4: New soft buffer size may be defined based on the maximum TBS of 1736 bits and 8 HARQ processes. ZTE

Observation 2: The soft buffer size for the support of a 1736 bit DL TBS should minimize impact on implementation. Ideally, it should be possible to support a 1736 bit DL TBS on existing hardware. SONY

Observation 3: The soft buffer size for the support of a 1736 bit DL TBS does not have to be directly related to the number of physical channel bits available in an allocation. SONY

Proposal 1: When calculating the soft buffer size for the 1736 DL TBS feature, 8 HARQs and 16QAM can be assumed. Sierra Wireless

Proposal 2: The soft buffer size for the 1736 DL TBS feature should be set to 30720 bits. Sierra Wireless

Proposal 2: LBRM is not applied for UEs supporting 1732 max TBS. Qualcomm

Proposal 3: The soft buffer size for category M1 UEs supporting 1732 bits TBS is 43008. Qualcomm

Observation 6 If the current soft buffer size designed for 8 processes, upgraded in Rel-14 to support the 10 processes were simply scaled up according to the larger TBS, then 43998 soft channel bits are estimated to be required. Ericsson

Observation 7 Using an equation that accounts for the number of HARQ processes and the coding rate of the turbo encoder, the required soft buffer size was estimated:

* For 10 HARQ processes: In principle, 53760 soft channel bits are estimated to be required.
* For 14 HARQ processes: In principle, 75264 soft channel bits are estimated to be required. Ericsson

Observation 8 The total number of soft channel bits for Rel-13 Cat-M1 is 25344. In Rel-17, the soft buffer size is at most expected to be increased about 2.12 times for 10 HARQ processes and 2.96 times for 14 HARQ processes to provide peak data rates of ~1.02 Mbps and ~1.23 Mbps respectively. Ericsson

Proposal 2 Discuss the soft buffer size estimated to be required for 10 and 14 HARQ processes (53760 and 75264 soft channel bits respectively), and the feasibility and advantages (e.g., cost reduction) of using a smaller soft buffer size than the ones derived theoretically. Ericsson

## Combinations of features that support 1736 bit DL TBS

Some companies discussed which features should be supported in combination with a 1736 bit DL TBS, as listed in Table 2.

Table 2 – Features that may be supported in combination with 1736 bit DL TBS

|  |  |
| --- | --- |
| **Feature supported in combination with 1736 bit DL TBS** | **Comments** |
| 64QAM | 1736 bits and 64QAM are both features that operate in good coverage  64QAM allows both MPCCH and PDSCH in the same subframe, improving data rates  Widespread support among companies |
| Multi-TB scheduling | Required to support a 1Mbps data rate, according to envisaged use cases.  What is the spec impact? |
| HARQ-ACK bundling | Required to support a 1Mbps data rate, according to envisaged use cases.  What is the spec impact? |
| 14 HARQ process capability | Required to support a 1Mbps data rate, according to envisaged use cases.  What is the spec impact (soft buffer size?) |

Some of the features listed in the table above are required to support a 1Mbps data rate, or at least to enhance data rates.

At the end of the work item, there will need to be a “UE features” discussion, where it is discussed with which existing UE features the 1736 bit DL TBS feature should work. It would be useful to determine if there are other spec impacts at this stage of the work.

### FL view on combinations of features that support 1736 bit DL TBS

64QAM should be assumed as baseline for 1736 bit DL TBS.

Multi-TB scheduling, HARQ-ACK bundling and 14 HARQ process capability are all useful for increasing the data rate and so should be considered in combination with a 1736 bit DL TBS. The issue is whether there are any specification impacts from these combinations, other than to UE feature lists and the impact on soft buffer sizes?

Question 2.2.1-1: Should 64QAM be supported with 1736 bit DL TBS?

|  |  |  |
| --- | --- | --- |
| **Company** | **Agree / disagree** | **Comment**  **(if not, why not?)** |
| Qualcomm | Yes | Unless something is broken, we do not think we have to agree one by one to all the features we have to support / not support. By default, and in line with the WID scope, this is just the introduction of a new capability and a soft buffer size determination. |
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Question 2.2.1-2: What are the potential specification impacts of supporting 1736 bit DL TBS in combination with Multi-TB scheduling?

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| --- | --- |
| **Company** | **Potential impact**  **(e.g. UE feature list, soft buffer size)** |
|  |  |
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|  |  |

Question 2.2.1-3: What are the potential specification impacts of supporting 1736 bit DL TBS in combination with HARQ-ACK bundling?

|  |  |
| --- | --- |
| **Company** | **Potential impact**  **(e.g. UE feature list, soft buffer size)** |
|  |  |
|  |  |
|  |  |

Question 2.2.1-4: What are the potential specification impacts of supporting 1736 bit DL TBS in combination with 14 HARQ process capability?

|  |  |
| --- | --- |
| **Company** | **Potential impact**  **(e.g. UE feature list, soft buffer size)** |
|  |  |
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**Proposals and observations in input documents**

Proposal 3: A maximum DL TBS of 1736 bits is supported both with and without configuration of 64-QAM for PDSCH. NOK-NSB

Observation 1: The following features can be used for determining the soft buffer size for a 1736 bit maximum DL TBS:

* Multi-TB scheduling
* Increased number of HARQ processes with HARQ bundling. Either 10 or 14 HARQ processes can be supported
* 64QAM SONY

Proposal 3: The 1736 DL TBS feature shall support the HARQ-ACK bundling Capability Sierra Wireless

Proposal 4: The 1736 DL TBS feature shall support the Multi-TB grant Capability. Sierra Wireless

Proposal 5: The 1736 DL TBS feature shall support the 64 QAM feature *ce-PDSCH-64QAM-Config-r15* Sierra Wireless

Proposal 6: The 1736 DL TBS feature shall support the 14 HARQ Capability Sierra Wireless

Proposal 1 The new larger DL TBS of 1736 bits should be usable along with the following combinations:

• The Rel-13 TBS table (6 PRBs) should be used with Rel-16 Multi-TB scheduling along with Rel-14 HARQ-ACK bundling and up to 8 HARQ processes. Ericsson

• The Rel-15 (64QAM) TBS table (3 or 4 PRBs) should be used with 1) Single-TB scheduling along with Rel-14 HARQ-ACK bundling and up to 10 or 14 HARQ processes, 2) Multi-TB scheduling along with Rel-14 HARQ-ACK bundling and up to 8 HARQ processes. Ericsson

## Usage scenarios and potential benefits for 1736 bit DL TBS

Ericsson and Sierra Wireless considered some of the usage scenarios and potential benefits of supporting a 1736 bit DL TBS. While these usage scenarios may not impact the design of the baseline 1736 bit DL TBS feature, they may impact the combination of features that can be applied together with a 1736 bit DL TBS.

A peak data rate target of 1Mbps was identified as a goal. Some combinations allowing support for a peak data rate of 1Mbps were identified.

The following potential additional benefits of the 1736 bit DL TBS feature were envisaged:

* Higher spectral efficiency
  + Reduction in the number of HARQ processes to complete a transmission
  + More efficiently handle RRC reconfiguration messages of over 1000 bits
* Power consumption reduction

### FL view on usage scenarios for 1736 bit DL TBS

In order to aid the design of the 1736 bit DL TBS feature, it might be useful to have a common goal for the peak data rate. This peak data rate would be achieved in combination with other Rel-16 [and potentially Rel-17 features].

Question 2.3.1-1: Should the 1736 bit DL TBS feature strive to achieve a peak data rate of 1Mbps?

|  |  |  |
| --- | --- | --- |
| **Company** | **Agree / disagree** | **Comment**  **(if not, what should be the peak data rate goal?)** |
|  |  |  |
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|  |  |  |

**Proposals and observations in input documents**

Observation 1 Enabling the use of a TBS = 1736 bits is not strictly tied to achieving a higher UE throughput, since the spectral efficiency increase it provides is useful for other scenarios, e.g., to reduce the number of required HARQ processes to complete a transmission, to handle more efficiently RRC reconfiguration messages over 1000 bits, etc. Ericsson

Observation 2 The use of a larger TBS provides gains in terms of UE power consumption, since a less amount of time having the UE’s transmitter/receiver active translates into battery savings. Ericsson

Observation 3 In RAN# 88e a set of use cases were discussed to justify the support of “a maximum DL TBS of 1736 bits for HD-FDD Cat. M1 UEs in CE mode A”, where 1 Mbps was the peak data rate required for the identified use cases. Ericsson

Observation 4 The Rel-13 TBS table with 6 PRB and Rel-16 multi-TB scheduling with HARQ-ACK bundling can support ~1 Mbps (992 kbps). Ericsson

Observation 5 The Rel-15 (64QAM) TBS table with 3 or 4 PRBs and single-TB scheduling with Rel-14 HARQ-ACK bundling can support ~1.02 Mbps with 10 HARQ processes and ~1.23 Mbps with 14 HARQ processes. Ericsson

## Specification changes to support a 1736 DL TBS using current MCS tables

A 1736 bit DL TBS can be supported using the combinations of *ITBS*, modulation order and *NPRB* below:

* 16QAM, *ITBS* = 14, *NPRB* = 6
* 64QAM, , *NPRB* = 3,4

Note that other values of *ITBS* and *NPRB* provide TBS values between 1000 bits and 1736 bits.

For 16QAM, Table 3 below shows in yellow the {*ITBS*, *NPRB*} combinations that lead to a DL TBS of 1736 bits. The entries in green show the {*ITBS*, *NPRB*} combinations that lead to a DL TBS of greater than 1000 bits.

Table 3 From Table 7.1.7.2.1-1 in TS36.213v16.4.0: Transport block size table showing increased TBS sizes for Rel-17 with 16QAM

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  | | | | | |
| 1 | 2 | 3 | 4 | 5 | 6 |
| 0 | 16 | 32 | 56 | 88 | 120 | 152 |
| 1 | 24 | 56 | 88 | 144 | 176 | 208 |
| 2 | 32 | 72 | 144 | 176 | 208 | 256 |
| 3 | 40 | 104 | 176 | 208 | 256 | 328 |
| 4 | 56 | 120 | 208 | 256 | 328 | 408 |
| 5 | 72 | 144 | 224 | 328 | 424 | 504 |
| 6 | 328 | 176 | 256 | 392 | 504 | 600 |
| 7 | 104 | 224 | 328 | 472 | 584 | 712 |
| 8 | 120 | 256 | 392 | 536 | 680 | 808 |
| 9 | 136 | 296 | 456 | 616 | 776 | 936 |
| 10 | 144 | 328 | 504 | 680 | 872 | 1032 |
| 11 | 176 | 376 | 584 | 776 | 1000 | 1192 |
| 12 | 208 | 440 | 680 | 904 | 1128 | 1352 |
| 13 | 224 | 488 | 744 | 1000 | 1256 | 1544 |
| 14 | 256 | 552 | 840 | 1128 | 1416 | 1736 |
| 15 | 280 | 600 | 904 | 1224 | 1544 | 1800 |
| 16 | 328 | 632 | 968 | 1288 | 1608 | 1928 |
| 17 | 336 | 696 | 1064 | 1416 | 1800 | 2152 |
| 18 | 376 | 776 | 1160 | 1544 | 1992 | 2344 |
| 19 | 408 | 840 | 1288 | 1736 | 2152 | 2600 |
| 20 | 440 | 904 | 1384 | 1864 | 2344 | 2792 |
| 21 | 488 | 1000 | 1480 | 1992 | 2472 | 2984 |
| 22 | 520 | 1064 | 1608 | 2152 | 2664 | 3240 |
| 23 | 552 | 1128 | 1736 | 2280 | 2856 | 3496 |
| 24 | 584 | 1192 | 1800 | 2408 | 2984 | 3624 |
| 25 | 616 | 1256 | 1864 | 2536 | 3112 | 3752 |
| 26 | 712 | 1480 | 2216 | 2984 | 3752 | 4392 |
| 26A | 632 | 1288 | 1928 | 2600 | 3240 | 3880 |

For 64QAM, Table 4 below shows in yellow the {*ITBS*, *NPRB*} combinations that lead to a DL TBS of 1736 bits, after a “min(TBS’, 1736)” function is applied. The orange entries show how a DL TBS of exactly 1736 bits is achieved. The entries in green show the {*ITBS*, *NPRB*} combinations that lead to a DL TBS of greater than 1000 bits.

Table 4 From Table 7.1.7.2.1-1 in TS36.213v16.4.0: Transport block size table showing increased TBS sizes for Rel-17 with 64QAM

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  | | | | | |
| 1 | 2 | 3 | 4 | 5 | 6 |
| 0 | 16 | 32 | 56 | 88 | 120 | 152 |
| 1 | 24 | 56 | 88 | 144 | 176 | 208 |
| 2 | 32 | 72 | 144 | 176 | 208 | 256 |
| 3 | 40 | 104 | 176 | 208 | 256 | 328 |
| 4 | 56 | 120 | 208 | 256 | 328 | 408 |
| 5 | 72 | 144 | 224 | 328 | 424 | 504 |
| 6 | 328 | 176 | 256 | 392 | 504 | 600 |
| 7 | 104 | 224 | 328 | 472 | 584 | 712 |
| 8 | 120 | 256 | 392 | 536 | 680 | 808 |
| 9 | 136 | 296 | 456 | 616 | 776 | 936 |
| 10 | 144 | 328 | 504 | 680 | 872 | 1032 |
| 11 | 176 | 376 | 584 | 776 | 1000 | 1192 |
| 12 | 208 | 440 | 680 | 904 | 1128 | 1352 |
| 13 | 224 | 488 | 744 | 1000 | 1256 | 1544 |
| 14 | 256 | 552 | 840 | 1128 | 1416 | 1736 |
| 15 | 280 | 600 | 904 | 1224 | 1544 | 1800 |
| 16 | 328 | 632 | 968 | 1288 | 1608 | 1928 |
| 17 | 336 | 696 | 1064 | 1416 | 1800 | 2152 |
| 18 | 376 | 776 | 1160 | 1544 | 1992 | 2344 |
| 19 | 408 | 840 | 1288 | 1736 | 2152 | 2600 |
| 20 | 440 | 904 | 1384 | 1864 | 2344 | 2792 |
| 21 | 488 | 1000 | 1480 | 1992 | 2472 | 2984 |
| 22 | 520 | 1064 | 1608 | 2152 | 2664 | 3240 |
| 23 | 552 | 1128 | 1736 | 2280 | 2856 | 3496 |
| 24 | 584 | 1192 | 1800 | 2408 | 2984 | 3624 |
| 25 | 616 | 1256 | 1864 | 2536 | 3112 | 3752 |
| 26 | 712 | 1480 | 2216 | 2984 | 3752 | 4392 |
| 26A | 632 | 1288 | 1928 | 2600 | 3240 | 3880 |

### FL view on how 1736 bit DL TBS can be supported using current MCS tables

In order to avoid additional changes to TBS tables, MCS tables and DCI formats, the maximum *ITBS* for 16QAM should remain as ITBS = 14.

* If a higher *ITBS* were supported, a 5-bit modulation and coding scheme field in a DCI format would be required.
* If a 4-bit modulation and coding scheme were reused with different TBS values for Rel-17, new TBS tables or MCS tables would be required

**FL proposal: For support of a 1736 bit DL TBS with 16QAM:**

* **a 4-bit modulation and coding scheme field is used in DCI**
* **maximum ITBS = 14**
* **no change to TBS table relative to Rel-16**
* **no change to CQI table relative to Rel-16**
* **no change to MCS table relative to Rel-16**

In order to avoid additional changes to TBS tables, MCS tables and DCI formats, the maximum TBS for 64QAM should be 1736 bits. There are various value of *ITBS* and *NPRB* that enable a 1736 bit TBS to be supported. The TBS can be determined based on the minimum of (1) 1736 bits and (2) the TBS derived from the TBS tables in TS36.213.

**FL proposal: For support of a 1736 bit DL TBS with 64QAM:**

* **a 5-bit modulation and coding scheme field is used in DCI**
* **TBS is calculated as**
* **no change to TBS table relative to Rel-16**
* **no change to CQI table relative to Rel-16**
* **no change to MCS table relative to Rel-16**

Question 2.4.1-1: Should 1736 bit DL TBS be supported with 16QAM as follows:

* a 4-bit modulation and coding scheme field is used in DCI
* maximum ITBS = 14
* no change to TBS table relative to Rel-16
* no change to CQI table relative to Rel-16
* no change to MCS table relative to Rel-16

|  |  |  |
| --- | --- | --- |
| **Company** | **Agree / disagree** | **Comment**  **(if not, what alternative?)** |
| Qualcomm | See comment | There is no need to agree to this, since it is in the WID:  *There shall be no changes to: DCI formats, TBS tables, CQI tables* |
|  |  |  |
|  |  |  |

Question 2.4.1-2: Should 1736 bit DL TBS be supported with 64QAM as follows:

* a 5-bit modulation and coding scheme field is used in DCI
* TBS is calculated as
* no change to TBS table relative to Rel-16
* no change to CQI table relative to Rel-16
* no change to MCS table relative to Rel-16

|  |  |  |
| --- | --- | --- |
| **Company** | **Agree / disagree** | **Comment**  **(if not, what alternative?)** |
| Qualcomm | See comments | The only thing we need to agree is to change the . The rest of the bullets are in the WID. |
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|  |  |  |

**Proposals and observations in input documents**

Observation 1: The existing TBS table enables the use of the increased maximum DL TBS of 1736 bits with 16-QAM only with and . NOK-NSB

Observation 2: The increased maximum DL TBS of 1736 bits can be used with 64-QAM with all TBS indices in the range . NOK-NSB

Proposal 1: For DL TBS increase for 16QAM, TBS less than or equal to TBS14 can be used for each NPRB. ZTE

Proposal 2: For DL TBS increase for 64QAM, TBS less than or equal to 1736 bits can be used for each NPRB. ZTE

Proposal 1: In TS 36.213, Subclause 7.1.7.2, the line does not apply for UEs that support a TBS of 1732. Qualcomm

## Capability

The proposals on UE capability boil down to:

* A capability is introduced for Rel-17 Cat-M1 UEs (BL/CE UEs with DL PDSCH bandwidth of 1.4 MHz) supporting a maximum DL TBS of 1736 bits in CEModeA.
* The use of a maximum DL TBS of 1736 bits for a Rel-17 Cat-M1 UE with the corresponding capability is enabled through higher layer configuration.

### FL view on capability issues

Capability support for the 1736 bit DL TBS feature can be considered at the end of the work item, in the usual way.

Question 2.5.1-1: Can UE capability for the 1736 bit DL TBS feature be considered at the end of work item:

|  |  |  |
| --- | --- | --- |
| **Company** | **Agree / disagree** | **Comment**  **(if disagree, what are the pressing issues?)** |
| Qualcomm | See comment | No need to discuss, this is in the WID: *Add a* ***Rel-17 optional UE capability*** *to support a maximum DL TBS of 1736 bits for HD-FDD Cat. M1 UEs in CE mode A only* |
|  |  |  |
|  |  |  |

**Related proposals**

Proposal 1: A capability is introduced for Rel-17 Cat-M1 UEs (BL/CE UEs with DL PDSCH bandwidth of 1.4 MHz) supporting a maximum DL TBS of 1736 bits in CEModeA. NOK-NSB

Proposal 2: The use of a maximum DL TBS of 1736 bits for a Rel-17 Cat-M1 UE with the corresponding capability is enabled through higher layer configuration. NOK-NSB

## AOB: other comments

Question 2.6.1-1: Are there any other issues that should be addressed in RAN1#104e, other than those listed above?

|  |  |
| --- | --- |
| **Company** | **Other issue** |
|  |  |
|  |  |
|  |  |

# References

1. [RP-201306](http://www.3gpp.org/ftp/TSG_RAN/TSG_RAN/TSGR_88e/Docs/RP-201306.zip), “WID revision: Additional enhancements for NB-IoT and LTE-MTC”, RAN #88e, Electronic Meeting, June 29th – July 3rd, 2020.

The following documents were submitted to RAN1#104e before the Tdoc deadline:

|  |  |  |
| --- | --- | --- |
| [R1-2100255](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2100255.zip) | Support of a max DL TBS of 1736 bits in LTE-MTC | Huawei, HiSilicon |
| [R1-2100509](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2100509.zip) | Support of a maximum DL TBS of 1736 bits for eMTC | Nokia, Nokia Shanghai Bell |
| [R1-2100569](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2100569.zip) | DL TBS increase for eMTC | ZTE |
| [R1-2100869](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2100869.zip) | Support of 1736 bit maximum DL TBS for eMTC | Sony |
| [R1-2101326](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2101326.zip) | Design considerations to support DL TBS of 1736 bits for LTE-M | Sierra Wireless, S.A. |
| [R1-2101511](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2101511.zip) | Support of larger TBS for eMTC | Qualcomm Incorporated |
| [R1-2101700](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2101700.zip) | Support of a maximum DL TBS of 1736 bits in LTE-MTC | Ericsson |