3GPP TSG RAN WG1 #104-e R1-200xxxx

e-Meeting, January 25th – February 05th, 2021

**Agenda item: 8.1.2.1**

**Source:** **Moderator (Nokia, Nokia Shanghai Bell)**

**Title: Summary of Multi-TRP for PUCCH and PUSCH**

**Document for: Discussion and Decision**

# Introduction

The Rel-17 work item for enhancements on MIMO for NR includes an objective to extend specification support for enhancements on multi-TRP/panel transmission. In RAN #86, the objectives were agreed to read as follows:

*Enhancement on the support for multi-TRP deployment, targeting both FR1 and FR2:*

* 1. *Identify and specify features to improve reliability and robustness for channels other than PDSCH (that is, PDCCH, PUSCH, and PUCCH) using multi-TRP and/or multi-panel, with Rel.16 reliability features as the baseline*

In this document, proposals on the reliability and robustness improvements for PUCCH and PUSCH are summarized and several FL proposals are listed in section 2-4 (section 4 to be added later). For additional information, Section 5 contains all the proposals submitted by company contributions. The agreements reached in previous RAN1 meetings are provided in Section 7.

Latest versions of the proposals are highlighted.

# Multi-TRP PUCCH transmission

The first sub-section below summarizes company proposals, the second sub-section provide FL proposals, and the third sub-section allows companies to add further comments on any missing proposals which companies think high-priority.

## 2.1 Summary of contributions

In the last meeting, several agreements were made related to M-TRP PUCCH transmissions. The remaining issues which are highlighted by company contributions are summarized below.

**Table 1: Summary: Supported M-TRP PUCCH schemes**

|  |  |  |
| --- | --- | --- |
| **Issue** | **Summary from Tdocs** | **Moderator comments** |
| 1. M-TRP inter slot repetition (Scheme 1): Number of repetitions | Number of repetitions   * **Support 2/4/8** (same as Rel-15): FW, Oppo * **Other values**: CATT/Xiaomi, E/// (16)   Support dynamic indication   * **Yes**: InterDigital, Lenovo, QC, ZTE, Nokia, MTek, Spreadtrum, TCL, Xiaomi, E/// * **No**: FW, Apple (not in feMIMO)   Method of dynamic indication   * **Associated to the PUCCH resource**: QC, Spreadtrum, Xiaomi | On the number of repetitions, starting with Rel-15 values seems reasonable.  There is good support for the dynamic indication of the number of PUCCH repetition. Based on FL reading,   * The method of dynamic indication may not increase DCI size. * Other WIs will not decide on the dynamic indication for M-TRP (based on RAN guidance). * Coverage enhancement WI has an objective on specifying dynamic indication, feMIMO could refer to the same method of dynamic indication for M-TRP PUCCH repetition.   Please check FL proposal 2.1 |
| 1. Scheme 1: PUCCH format 0/2 | Support PUCCH format 0/2 for Scheme 1   * **Yes**: Oppo, Lenovo, QC, Nokia, Intel, CMCC, Xiaomi, SS, Apple, DCM, Spreadtrum, E/// * **No**: FW, HW | Majority of companies support PUCCH format 0/2 for scheme 1.  Please check FL proposal 2.2 |
| 1. Support of M-TRP intra slot beam hopping (Scheme 2) and M-TRP intra-slot repetition (Scheme 3) | * **Support only Scheme 3**: Oppo, Lenovo, CATT, Nokia, Intel, Spreadtrum, CMCC, SS, E///, TCL * **Support both Scheme 2 & 3**: HW, FW, Vivo, Fujitsu, Xiaomi, DCM, QC/MTek/LG (Support Scheme 3 if supported by Rel-17 eIIoT) | There is majority support for Scheme 3. Only three companies prefer intra-slot repetition scenario to be agreed first in eIIoT.  From FL perspective, there is good support for Scheme 3. Based on RAN guidance, there is no restriction to support Scheme3 only considering M-TRP operation.  Check FL proposal 2.3 |
| 1. PUCCH formats for Scheme 2/3 (if supported): | PUCCH formats for Scheme 3,   * **PUCCH format 0/2**: Lenovo, QC, CATT, Nokia, Intel, Spreadtrum, CMCC, Xiaomi, DCM, E///, Oppo * **All formats**: Spreadtrum, CMCC, Xiaomi, DCM, E/// * **PUCCH format 1/3/4:** FW   PUCCH formats for Scheme 2  **All Formats**: MTek, QC, DCM | Around 11 companies support at least PUCCH format 0 and 2 for the scheme 3.  Check FL proposal 2.3 |
| 1. Power Control: TPC command | * **Option 1:** (4) Oppo, Lenovo, QC, Intel, SS * **Option 2**: (4) HW, APT, SS, ZTE * **Option 3**: (13) Lenovo, CATT, Nokia, MTek, LG, Intel, NEC, CMCC, Xiaomi, Covinda, DCM, E///, FW * **Option 4**: (10) Oppo, Lenovo, QC, CATT, Vivo, LG, Spreadtrum, Apple, E///, ZTE   Use the same solution in PUSCH/PUCCH – Intel, NEC, SS | Both option 3 and 4 seems to be having good support. Down selection during the RAN1 #104e can be done for option 3 and 4.  Several companies also highlighted that the same solution should be used for PUSCH, that makes sense.  Check FL proposal 2.4 |
| 1. Power control: FR1 remaining details | **Support two sets of power control parameters for FR1:** FW, Oppo, Lenovo, ZTE, CATT, Nokia, SS, Apple, DCM  Details of configuration/indication and association to a PUCCH resource:   * RRC configured two sets: CATT, FW, Lenovo * Activated using the same RRC/MAC-CE of spatial relation info: QC, SS (alt.2) * A new MAC-CE to update power control parameters for PUCCH resource (or list): Apple * Enhance the default PUCCH power control without providing spatial relation info: SS (alt.1), Oppo * Associate the PUCCH resource with the 1st and 2nd lowest ID PC parameters – LG | There is good support for extending the power control parameters for FR1 M-TRP operation.  Also, there are some design details, which we could also discuss further during the meeting.  Check FL proposal 2.5 |
| 1. Frequency hopping for Scheme 1 | **FH applied per beam (scheme 1):** Lenovo, QC | There is a working assumption on how repetitions are mapped to beams. By configuring a suitable mapping pattern, there seems to be a possibility of controlling that the beam hopping applies per beam or not.  Check FL proposal 2.6 |
| 1. Beam/power control parameter set mapping | Confirm working assumption: Intel, CMCC, Xiaomi  Study impact due to flexible DL symbols: LG  Configure beam mapping pattern like indication for indicating the power control parameter set: DCM, Lenovo | There are few inputs on beam mapping as RAN1 already has a working assumption on how beams shall be mapped considering FR2 and Scheme 1.  RAN1 shall make agreements on beam mapping for Scheme 3 (if supported) and power control parameter set mapping for FR1.  Check FL proposal 2.7 |
| 1. Switching S-TRP and M-TRP PUCCH repetition scheme(s) | **Support dynamic switch**: Nokia, Intel, Spreadtrum, DCM  Details of switching  **Associating a PUCCH resource with one or two spatial-relation-info**: Intel | Several companies provided details. From FL perspective, similar to Rel-16 URLLC schemes, RAN1 can discuss supporting dynamic switching of S-TRP and M-TRP modes.  Check FL proposal 2.8 |
| 1. Activating multiple spatial relation info per PUCCH resource | **PUCCH grouping for S-TRP and M-TRP**: Intel, ZTE | MAC-CE design details are up to RAN2.  PUCCH grouping was discussed in the past, and FL sees that as a secondary issue. No FL proposal. |
| 1. Multiple PUCCH resources | Multiple PUCCH resources:   * **Yes**: FW, InterDigital, Lenovo, LG, SS, TCL * **No**: Oppo, Vivo, DCM | This was discussed heavily in the last RAN1 meeting from FL perspective, and the majority was not supporting multiple PUSCH resources. RAN1 shall finalize the single PUCCH resource scenario as it is already agreed. No FL proposal is made. |

## 2.2 FL proposals

### Proposal 2.1/2.2

**[Draft for offline] Proposal 2.1:** For M-TRP PUCCH scheme 1,

* Support PUCCH formats 0 and 2 (in addition to agreed PUCCH formats 1,3,4)

**[Draft for offline] Proposal 2.2:** For M-TRP PUCCH scheme 1,

* Values for the total number of repetitions at least contain values 2, 4, and 8.
* When using Rel-15 PUCCH repetition framework, the RRC configured number of slots (repetitions) are applied across both TRPs (e.g if the number of repetitions given by *nrofSlots* in *PUCCH-config* is 8, per TRP limit is 4).
* Support the dynamic indication of the number of repetitions
  + FFS#1: Defining the exact method of dynamic indication
    - Alt.1: Discuss the solution in Rel-17 feMIMO
    - Alt.2: Refer the design details to Rel-17 coverage enhancement.

Please comment preferred changes on the proposal below. Also, provide your preference for FFS.

|  |  |
| --- | --- |
| **Company** | **Comments** |
| NTT Docomo | We support the proposal.  For the FFS part, we prefer alt.2 so that we have a unified design for S-TRP and M-TRP. |
| MediaTek | We do not support Proposal 2.1. Since short PUCCH formats can be easily repeated within a slot, we do not see the need to support PUCCH formats 0 and 2 for inter-slot repetition. Instead, we prefer to have intra-slot beam hopping to shorten the latency. We provide more details of intra-slot beam hopping in additional high priority proposals.  We Support Proposal 2.2. For dynamic indication, we prefer Alt. 2 as there seems no particular issue to be considered from MIMO’s perspective. |
| InterDigital | We support FL’s proposal 2.1 and 2.2. We support Alt. 2 to ensure solutions are consistent. |
| Futurewei | Suggest to consider Proposal 2.1 as lower priority and focus on formats 1, 3, 4 first.  For Proposal 2.2, the clause “When using Rel-15 PUCCH repetition framework” seems not needed, and we suggest to revisit the dynamic indication after the relevant design in Rel-17 coverage enhancement is done. |
| QC | Support both proposals. Regarding FFS#1 of Proposal 2.2, we prefer Alt2 to avoid parallel discussions or multiple solutions. |
| Ericsson | We support both Proposals 2.1 and 2.2. With regards to FFS#1, we prefer Alt 2. |
| Xiaomi | Support the proposals, with adding the following:  **[Draft for offline] Proposal 2.2:** For M-TRP PUCCH scheme 1,   * Values for the total number of repetitions at least contain values 2, 4, and 8.   + FFS: maximum repetition number can be extended to 16. |
| Huawei, HiSilicon | We do not support Proposal 2.1. We don’t see the use case of inter-slot repetition of formats 0/2, since format 0/2 is configured mainly for lower latency and in such scenarios, intra-slot beam hopping can achieve low latency. If latency is not the focus of the performance, formats 1/3/4 can be used together with inter-slot repetition.  For Proposal 2.2, we prefer to align with other WIs on repetition number and dynamic repetition number indication, so we support Alt 2. |
| Intel | Support 2.1 and 2.2. For proposal 2.2 is there a need to decide on the repetition numbers if we leave the details to coverage enhancement ? |
| LG | We do not support Proposal 2.1 since we cannot achieve low latency advantage for short PUCCH format.  Regarding FFS#1 of Proposal 2.2, we support Alt. 2. In the last RAN meeting, it was agreed to discuss dynamic indication of repetition number in CE. |
| Lenovo&MotM | Support the proposal in principle and we support Alt.1 for FFS#1 of Proposal 2.2. |
| Samsung | Support the Proposal 2.1.  Regarding Proposal 2.2, support first two bullets and Alt. 2 in the last bullet. We can use the details of dynamic indication (if supported) from Rel-17 coverage as the method of dynamic indication can be considered with/without multi-TRP operation. |
| ZTE | Regarding FL’s proposal 2.1, we suggest to depriortize the discussion of short formats 0 and 2 compared with long formats 1, 3, and 4.  Regarding FL’s proposal 2.2, we support that up to 16 can be used for PUCCH repetitions. Besides, w.r.t the method of dynamic indication in FFS#1, we share the same view with companies that any increasing of DCI overhead should be avoided. |
| vivo | Support FL’s both proposals. We also think Alt.2 in FFS part is preferred. |
| Apple | We do not know why the following bullets are needed for proposal 2.2. For dynamic indication, it is already agreed in WID of coverage enhancement. Regarding number of repetitions, we think for format 0/2, up to 2 repetitions should be enough.   * When using Rel-15 PUCCH repetition framework, the RRC configured number of slots (repetitions) are applied across both TRPs (e.g if the number of repetitions given by *nrofSlots* in *PUCCH-config* is 8, per TRP limit is 4). * Support the dynamic indication of the number of repetitions   + FFS#1: Defining the exact method of dynamic indication     - Alt.1: Discuss the solution in Rel-17 feMIMO     - Alt.2: Refer the design details to Rel-17 coverage enhancement. |
| Fujitsu | Support FL’s proposal. For proposal 2.2, Alt-2 is preferred. |
| NEC | Support the proposals. And regarding FFS in proposal 2, we prefer Alt 2. |
| Spreadtrum | Support FL’s proposal 2.1 and proposal 2.2.  To avoid any overlapping/parallel discussion of coverage enhancement, we prefer Alt.2 for Proposal 2.2. |
| TCL | Support Proposal 2.1 and 2.2. For FFS#1, we prefer Alt 2. |
| FL update#1 | **Proposal 2**: MTek, HW, LG companies have concerns  @MTek, HW, LG >> Some evaluation results show performance gains for PUCCH format 0 and 2 repetitions in multi-TRP Scheme 1. This proposal is also on scheme 1, and support of other schemes should not be mixed here. If there are latency advantages of PUCCH format 0/2 for other schemes, we could discuss the support of PUCCH format 0/2 when the scheme is agreed to be supported.  **[Draft for offline] Proposal 2.1:** For M-TRP PUCCH scheme 1,   * Support PUCCH formats 0 and 2 (in addition to agreed PUCCH formats 1,3,4)   **Proposal 2.2**:  FFS1: Majority support Alt2.  Several companies raised the need of agreeing details (FW, Apple, SS, Intel). Based on RAN guidance, coverage enhancement may not take the decision on supporting the dynamic indication for M-TRP or not.  Xiaomi, CATT >> maximum repetition number = 16 can be added as FFS, but latency wise, that may not be suitable.  **[Draft for offline] Proposal 2.2:** For M-TRP PUCCH scheme 1,   * Values for the total number of repetitions at least contain values 2, 4, and 8.   + FFS: maximum repetition number can be extended to 16. * When using Rel-15 PUCCH repetition framework, the RRC configured number of slots (repetitions) are applied across both TRPs (e.g if the number of repetitions given by *nrofSlots* in *PUCCH-config* is 8, per TRP limit is 4). * Support the dynamic indication of the number of repetitions   + Refer the design details to Rel-17 coverage enhancement. |
| InterDigital | We support FL Proposals 2.1 and 2.2. |
| Futurewei | Ok with the proposals, but we are still not sure why “When using Rel-15 PUCCH repetition framework” is needed. |
| ZTE | We are supportive of the updated Proposal 2.1.  Regarding the updated Proposal 2.2, for the sake of progress, we support the assessment of Chairman and FL that we can agree with the updated Proposal 2.2. |
| QC | Support. |
| LG | We don’t support Proposal 2.1 since low latency benefit is gone with scheme 1.  We are supportive of the updated Proposal 2.2. |
| FL update#2 | On proposal 2.1, LG object. But Fl suggest keeping the proposal as that is the majority view.  **[Draft for offline] Proposal 2.1:** For M-TRP PUCCH scheme 1,   * Support PUCCH formats 0 and 2 (in addition to agreed PUCCH formats 1,3,4)   On proposal 2.1,  In the last GTW session, few edits were done by the Chairman, the version from the chairman notes is captured below. Removed the text “When using Rel-15 PUCCH repetition framework” as suggested by FW.  **[Draft for offline] Proposal 2.2:**  For M-TRP PUCCH scheme 1,   * Values for the total number of repetitions at least contain values 2, 4, and 8.   + FFS: maximum repetition number can be extended to 16. * ~~When using Rel-15 PUCCH repetition framework, the~~ RRC configured number of slots (repetitions) are applied across both TRPs (e.g if the number of repetitions given by *nrofSlots* in *PUCCH-config* is 8, per TRP limit is 4).   **Conclusion**   * The dynamic indication of the number of repetitions supported for Rel-17 coverage enhancement can be used for multi-TRP operation |
| OPPO | We are open to Proposal 2.1  We support Proposal 2.2.  In order to address some companies’ concern, maybe we can add an FFS part for the dynamic indication as below(Highlighted by YELLOW)   * + FFS: some additional enhancement on top of the solution designed by Rel-17 coverage enhancement session |
| CMCC | Support the updated proposal 2.1 and 2.2. |
| NTT Docomo | Support |
| Sharp | Support |
| Apple | Support proposal 2.1.  For Proposal 2.2, we think 2 repetitions should be enough for format 0/2. The second bullet seems unnecessary. We do not support the conclusion and we can revisit it after we see some designs for dynamic indication of number of repetitions. |
| Nokia/NSB | Support Proposal 2.1  Support Proposal 2.2. We are also fine with the suggested FFS point from OPPO. |
| Futurewei | Support. For the conclusion, maybe we can say “Revisit the dynamic indication of the number of repetitions based on Rel-17 coverage enhancement outcome”. |
| MediaTek | We are fine with Proposal 2.1 to follow the majority view. We have no doubt there would be performance gain for PUCCH format 0 and 2 repetitions in multi-TRP Scheme 1. However, once a scheme with repetitions within a slot is agreed, it is questionable whether supporting PUCCH format 0 and 2 repetitions in multi-TRP Scheme 1 can provide additional benefit. We are still not convinced why S-TRP PUCCH repetition does not support PUCCH formats 0 and 2, but M-TRP PUCCH inter-slot repetition would be better to support them.  We support FL Proposal 2.2. |
| NEC | Support the proposals. |
| Lenovo&MotM | Support. |
| Fujitsu | Support the updated proposal. |
| Xiaomi | Support the proposals and also fine with OPPO’s revision |
| Samsung | Support both updated proposals. |
| vivo | Support FL update#2 |
| Huawei, HiSilicon | We share the same view as LG and MTK. We can be open to this proposal, although we fail to see the use case.  For proposal 2.2, “per TRP limit” may not be needed as by beam mapping patterns, naturally #repetitions will be divided equally between TRPs.  We are fine with the conclusion. |
| FL update#3 | Oppo >> let’s try to separate dynamic repetition from proposal 2.2.  Apple>> For format 0/2, yes, we could make the agreement for number of repetitions equals to two first.  HW, Apple>> Second bullet is not wrong as it carries clarification. Anyways, removed in the update.  MTek, HW >> If I got your reply right, you will not object the majority view. Thanks.  All >> Please see the latest versions. Removed some corrections did before and highlighted the changes on PUCCH format 0/2 applies only for 2 repetitions now.  **Offline Agreement 2.1:** For M-TRP PUCCH scheme 1,   * Support PUCCH formats 0 and 2 (in addition to agreed PUCCH formats 1,3,4)   **Proposal 2.2:**  For M-TRP PUCCH scheme 1,   * For PUCCH formats 1/3/4, values for the total number of repetitions at least contain values 2, 4, and 8.   + FFS: maximum repetition number can be extended to 16. * For PUCCH formats 0/2, the total number of repetitions at least contain 2.   + FFS: other values. * ~~RRC configured number of slots (repetitions) are applied across both TRPs (e.g if the number of repetitions given by~~ *~~nrofSlots~~* ~~in~~ *~~PUCCH-config~~* ~~is 8, per TRP limit is 4).~~   **Offline Conclusion**   * The dynamic indication of the number of repetitions supported for Rel-17 coverage enhancement can be used for multi-TRP operation |

### Proposal 2.3

**[Draft for offline] Proposal 2.3:** For PUCCH reliability enhancement, support multi-TRP intra-slot repetition (Scheme 3) at least for PUCCH formats 0/2.

* The same PUCCH resource carrying UCI is repeated for X consecutive sub-slots within a slot.
  + For 7 symbol sub-slot configuration, X = 2
  + FFS1: values of X for 2 symbol sub-slot configuration
* FFS2: Scheme 3 is also supported across multiple slots
  + Alt.1: extended for multiple slots
  + Alt.2: defined only within a slot
* FFS3: PUCCH formats 1/3/4 are also supported for Scheme 3.
  + Alt.1: support format 1/3/4
  + Alt.2: do not support format 1/3/4

Note: The decision of supporting scheme 3 is only applicable for multi-TRP operation.

Please comment preferred changes below. Also, highlight your preferences for FFS points.

|  |  |
| --- | --- |
| **Company** | **Comments** |
| NTT Docomo | We support the proposal.  For FFS1, we think the number of intra-slot repetition can be configurable similar as inter-slot repetition.  For FFS2, we support alt.1.  For FFS3, we are fine with alt.1, but we would like to note that PUCCH format 1/3/4 can only be supported when the number of symbols is <=7. |
| MediaTek | Support Proposal 2.3.  FFS1: X = 2, 4, 8  FFS2: Alt. 1, but we prefer it listed as UE capability.  FFS3: Alt. 1 |
| InterDigital | We support FL’s proposal.  FFS1: configurable number  FFS2: Alt. 1  FFS3: Alt. 1 |
| Futurewei | We are ok with the proposal. |
| QC | Do not support the proposal. Based on inputs from our IIoT delegates, it seems very likely that the scheme is going to be supported in this meeting in Rel. 17 IIoT for single-TRP. Parallel discussions / multiple solutions should be avoided. We propose the following:  **Proposal 2.3:** For PUCCH reliability enhancement, support multi-TRP intra-slot repetition (Scheme 3) if the scheme is agreed in Rel-17 IIoT for single-TRP.  Alternatively, if we really want to design this scheme only for multi-TRP, then only 2 repetitions are enough. Hence, we can be fine with the following even though the first suggestion above is preferred.  **Proposal 2.3:** For PUCCH reliability enhancement, support multi-TRP intra-slot repetition (Scheme 3) at least for PUCCH formats 0/2.   * The same PUCCH resource carrying UCI is repeated for X=2 consecutive sub-slots within a slot.   + ~~For 7 symbol sub-slot configuration, X = 2~~   + ~~FFS1: values of X for 2 symbol sub-slot configuration~~ * ~~FFS2: Scheme 3 is also supported across multiple slots~~   + ~~Alt.1: extended for multiple slots~~   + ~~Alt.2: defined only within a slot~~ * FFS3: PUCCH formats 1/3/4 are also supported for Scheme 3.   + Alt.1: support format 1/3/4   + Alt.2: do not support format 1/3/4   In addition, given that at least 9 companies support Scheme 2, we think it should be discussed at least. We would like to note that in existing RAN4 spec, transient time is defined for Rel. 15 frequency hopping. Same requirement can be used for beam hopping. This of course may depend on RAN4’s input. Hence, we are open to have a “conditional agreement” (conditioned on RAN4 response to Question 4 of the LS) if that resolves the concerns. |
| Ericsson | For PUCCH format 0 with 1 symbol, repetition is already supported in Rel-15 without sub-slot configuration, thus it makes sense to have it supported also for m-TRP repetition without sub-slot configuration.  For PUCCH format 0 with 2 symbols and PUCCH format 2 with 1 or 2 symbols, supporting repetition for m-TRP without sub-slot configuration is also straightforward. Subslot-slot based configuration is used in Rel-16 to support multiple PUCCH resources in a slot for carrying multiple HARQ Acks for different traffic types, where sub-slot based K2 is needed for indicating different PUCCH resources in a slot. For intra-slot PUCCH repetition for m-TRP, there is no such a need and we do not see a need to limit intra-slot PUCCH repetition to sub-slot configuration, at least not for PUCCH formats 0 and 2.  Hence, we suggest to revise the proposal as follows:  **Proposal 2.3:** For PUCCH reliability enhancement, support multi-TRP intra-slot repetition.   * For PUCCH formats 0 and 2 with 1 or 2 symbols, the same PUCCH resource carrying UCI is repeated in X consecutive symbols within a slot without sub-slot configuration.   + FFS1: value range of X * FFS2: Scheme 3 is also supported across multiple slots   + Alt.1: extended for multiple slots   + Alt.2: defined only within a slot * FFS3: PUCCH formats 1/3/4 are also supported for intra-slot multi-TRP PUCCH repetition with or without sub-slot configuration.   + Alt.1: support format 1/3/4   + Alt.2: do not support format 1/3/4   For FFS2, we support Alt. 2. For FFS3, we support Alt. 1. |
| Xiaomi | Support the FL’s proposal   1. FFS1: agree with QC that X=2 within a slot; 2. FFS3: Alt.1   We think Scheme 2 as an appealing approach should also be discussed in this meeting. |
| Huawei, HiSilicon | We agree with the modification of QC to limit the repetition number to 2. As scheme 3 is being discussed in other topics (URLLC), it would be better to revisit it after decision in URLLC to have a unified design.  We also think scheme 2 should be discussed considering the supporting companies. Scheme 2 is beneficial in terms of latency, especially for PUCCH formats 0 and 2, as we don’t need wait for another subslot for the repetition. |
| LG | In the last RAN plenary meeting, it was agreed to discuss whether to specify or not STRP PUCCH repetition in IIoT/URLLC WI. Therefore, it is recommended to wait for the decision in IIoT/URLLC WI, before discussing MTRP intra-slot PUCCH repetition.  On the other hand, scheme 2 can be discussed separately from IIoT WI. |
| Lenovo&MotM | Support it in principle, but considering there maybe need time to switch beams for different repetitions, whether the sub-slots are consecutive should be further studied. And we support the FFS2 considering the repetition number may be larger than 2 for 7 symbols sub-slot. |
| Samsung | For more reliability, Scheme 3 can be extended for multiple slots. And we don’t need to preclude long PUCCH for Scheme 3 because Scheme 3 can be also useful for long PUCCH with 4~7 symbols.  FFS2: Alt.1  FFS3: Alt 1 |
| ZTE | To avoid any overlapping/parallel discussion of IIOT/URLLC in AI 8.3, we suggest that the further discussion on intra-slot PUCCH repetitions may happen after AI 8.3 discussions or based on additional RAN guidance. |
| vivo | Support FL’s proposals.  We think when sub-slot is configured for the UE, repetitions can be across slot according to the number of PUCCH repetitions. So, for FFD2, we prefer Alt.1.  For FFS3, support Alt.1. |
| Apple | We can defer the decision for intra-slot repetition after we see more outcome from URLLC to avoid potential misalignment. |
| Fujitsu | Support FL’s proposal.  For FFS1, X is preferred to be configurable.  For FFS2, Alt-1 is preferred.  For FFS3, Alt-1 is preferred. |
| NEC | Support the proposal.  FFS1: X is configurable  FFS2: Alt 2.  FFS3: Alt 1. |
| Spreadtrum | Support FL’s proposals.  For FFS1, we also prefer X=2 as QC;  For FFS3, support Alt1. |
| TCL | Support FL’s proposal.  For FFS1, we think the number of intra-slot repetition can be configurable.  For FFS2, intra-slot repetition can be across slot, so Alt.1 is preferred.  For FFS3, Alt.1 is preferred. |
| FL update#1 | @QC, HW, LG, ZTE, Apple >> The issue of dependency between WIs is already discussed in last two RAN meetings, and a clear guidance was given in the last RAN meeting. Yes, there is good chance that sub-slot repetition will be agreed for s-TRP scenario in eIIoT, but they will not make the agreement for M-TRP. Checked also with the FL of the topic in eIIoT. Here, the agreement is scheme 3 to be supported considering multi-TRP operation. After this agreement, feMIMO may refer the design to eIIoT.  @E///>> please see the definition of scheme 3, “*One PUCCH resource carries UCI, another PUCCH resource or the same PUCCH resource in another one or more sub-slots within a slot carries a repetition of the UCI*.” It is true that repetition of PUCCH format 0 is already applied when it has two symbols. But, the intension of the proposal is to use sub-slot configuration, where PF 0 with two symbols (in your example) may be within a sub-slot and another repetition with two symbols happens in another sub-slot.  **If companies wish to support scheme 2, please raise their voice to have a separate proposal.** FL observed lot of companies do not support scheme 2, and that is the reason why there is no proposal on that.  Summary on FFS items:   |  |  |  | | --- | --- | --- | | FFS1 | FFS2 | FFS3 | | **X = 2, 4, 8**: MTek, DCM  **Configurable X**: IDC, CATT, NEC  **X = 2**: QC, Xiaomi, Spreadtrum | **Alt.1**: DCM, MTek, IDC, Lenovo, SS, Fujitsu, Spreadtrum  **Alt.2**: E///, CATT, QC, NEC | **Alt.1:** CATT, Xiaomi, E///, IDC, MTek, DCM, SS, Vivo, Fujitsu, NEC, Spreadtrum |   **[Draft for offline] Proposal 2.3:** For PUCCH reliability enhancement, support multi-TRP intra-slot repetition (Scheme 3) at least for PUCCH formats 0/2.   * The same PUCCH resource carrying UCI is repeated for X = 2 consecutive sub-slots within a slot.   + Revisit if Rel-17 eIIoT defines other values for X and sub-slot repetition across slots * ~~FFS3:~~ PUCCH formats 1/3/4 are also supported for Scheme 3.   + ~~Alt.1: support format 1/3/4~~   + ~~Alt.2: do not support format 1/3/4~~   Note2: The decision of supporting scheme 3 is only applicable for multi-TRP operation. |
| InterDigital | We support FL’s proposal. |
| Lenovo&MotM | We have concern about the ‘consecutive sub-slots within a slot’ in the first sub-bullet. Since the symbol length of sub-slot can be 2 or 7, it may don’t have enough time to switch time for two adjacent repetitions with different beams when the configuration of sub-slot is 2 symbols length. Whether the sub-slots carrying different repetitions with different beams can be consecutive should be further discussed. Therefore, we propose to delete the word ‘consecutive’ in the first sub-bullet. |
| ZTE | Support FL’s updated proposal. |
| QC | Ok with the proposal in principle. Suggest to use similar wording as proposal 2.2  **[Draft for offline] Proposal 2.3:** For PUCCH reliability enhancement, support multi-TRP intra-slot repetition (Scheme 3) at least for PUCCH formats 0/2.   * The same PUCCH resource carrying UCI is repeated for X = 2 consecutive sub-slots within a slot.   + ~~Revisit if Rel-17 eIIoT defines other values for X and sub-slot repetition across slots, and refer the design details to Rel-17 eIIoT~~ * ~~FFS3:~~ PUCCH formats 1/3/4 are also supported for Scheme 3.   + ~~Alt.1: support format 1/3/4~~   + ~~Alt.2: do not support format 1/3/4~~   If Rel-17 eIIoT agreed to support sub-slot based repetition for single-TRP, refer the design details related to sub-slot configurations (e.g. value of X) to Rel-17 eIIoT  Note2: The decision of supporting scheme 3 is only applicable for multi-TRP operation. |
| LG | We don’t support FL’s updated proposal since we don’t even know whether STRP scheme 3 is supported or not yet. What if STRP intra slot repetition is not supported in IIoT? Then, MTRP intra slot repetition is supported but STRP intra slot repetition is not? We should wait for IIoT decision. |
| FL update#2 | Lenovo>> beam switching times related muting could be discussed later after RAN4 LS reply. The idea to use sub-slot repetition from IIoT, and they will not consider such design.  LG >> RAN guidance is the following. The support of scheme should be done in MIMO. There no scheme 3 in IIoT discussion.  *For handling of the PUCCH repetitions it is proposed to proceed as follows:*   * *RAN1 to continue discussion on PUCCH repetition, whether to specify or not, in the IIoT/URLLC WI* ***for single TRP.*** * ***PUCCH repetition issues with multi-TRP******to be handled in Fe-MIMO WI.***   QC>> suggested wording is used.  **Updated Proposal 2.3:** For PUCCH reliability enhancement, support multi-TRP intra-slot repetition (Scheme 3) at least for PUCCH formats 0/2.   * The same PUCCH resource carrying UCI is repeated for X = 2 consecutive sub-slots within a slot.   + ~~Revisit if Rel-17 eIIoT defines other values for X and sub-slot repetition across slots~~ * ~~FFS3:~~ PUCCH formats 1/3/4 are also supported for Scheme 3.   + ~~Alt.1: support format 1/3/4~~   + ~~Alt.2: do not support format 1/3/4~~ * If Rel-17 eIIoT agreed to support sub-slot based repetition for single-TRP, refer the design details related to sub-slot configurations (e.g. value of X) to Rel-17 eIIoT   Note1: The decision of supporting scheme 3 is only applicable for multi-TRP operation. |
| OPPO | Ok with FL’s updated proposal |
| CMCC | Support in principle. |
| NTT Docomo | Support |
| Sharp | Support FL’s updated proposal |
| Apple | Do not support the proposal. We need to wait for RAN4 response to see whether intra-slot repeitition is possible, and we need to see more outcome in URLLC session. |
| Nokia/NSB | Support |
| Futurewei | Support |
| MediaTek | Support |
| NEC | Support |
| Lenovo&MotM | We still have the concern about the ‘consecutive’ for this proposal. |
| Fujitsu | Support |
| Xiaomi | Support FL’s updated proposal, agree that ‘consecutive’ is a bit confusing |
| Samsung | Support the updated proposal |
| ZTE | Support FL’s proposal. |
| vivo | Support FL update#2 in principle.  Since updated proposal 2.3 has support scheme 3 for PUCCH formats 0/2 and 1/3/4, we propose to simplify the proposal as:  **Updated Proposal 2.3:** For PUCCH reliability enhancement, support multi-TRP intra-slot repetition (Scheme 3) ~~at least~~ for all PUCCH formats ~~0/2~~.   * For PUCCH formats 0/2, ~~T~~the same PUCCH resource carrying UCI is repeated for X = 2 consecutive sub-slots within a slot.   + ~~Revisit if Rel-17 eIIoT defines other values for X and sub-slot repetition across slots~~ * ~~FFS3:~~ ~~PUCCH formats 1/3/4 are also supported for Scheme 3.~~   + ~~Alt.1: support format 1/3/4~~   + ~~Alt.2: do not support format 1/3/4~~ * If Rel-17 eIIoT agreed to support sub-slot based repetition for single-TRP, refer the design details related to sub-slot configurations (e.g. value of X) to Rel-17 eIIoT   Note1: The decision of supporting scheme 3 is only applicable for multi-TRP operation. |
| Huawei, HiSilicon | We are fine with FL’s update proposal. |
| FL update#3 | Apple >> we did not ask RAN4 about Scheme 3. So, they will not decide it is feasible or not. Also, sub-slot configuration can configure start symbol of the PUCCH within the sub-slot where the beam switching gaps can be accommodated.  Lenovo, Xiaomi>> your suggestion is to repeat in different sub-slots, we could consider such a need later. I put that wording in brackets for now.  Vivo>> as no one else is objecting format 1/3/4, your update is ok.  All >> Updated based on Vivo’s suggestion.  **Proposal 2.3:** For PUCCH reliability enhancement, support multi-TRP intra-slot repetition (Scheme 3) ~~at least~~ for all PUCCH formats ~~0/2~~.   * The same PUCCH resource carrying UCI is repeated for X = 2 [consecutive] sub-slots within a slot. * If Rel-17 eIIoT agreed to support sub-slot based repetition for single-TRP, refer the design details related to sub-slot configurations (e.g. value of X) to Rel-17 eIIoT * Note1: The decision of supporting scheme 3 is only applicable for multi-TRP operation. |

### Proposal 2.4

**[Draft for offline] Proposal 2.4:** Select one from the following options to support per TRP closed-loop power control for PUCCH/PUSCH,

* Option 3: A second TPC field is added in DCI formats 1\_1 / 1\_2/0\_1/0\_2.
* Option 4: A single TPC field is used in DCI formats 1\_1 / 1\_2/0\_1/0\_2, and indicates two TPC values applied to two PUCCH/PUSCH beams, respectively.

Please comment preferred changes below. Also, highlight your preferences for option 3 and 4.

|  |  |
| --- | --- |
| **Company** | **Comments** |
| NTT Docomo | We support the proposal and prefer option3.  For option4, we suggest more clarification on whether the DCI overhead is expected to be increased with option4, which is beneficial for the comparison between option3 and option4. |
| MediaTek | Our first preference is Option 3, but Option 4 is also fine. |
| InterDigital | We support FL’s proposal, slight preference on Option 3. |
| Futurewei | Support, and we support Option 3.  The two TPC values are uncorrelated, so put them into one TPC field does not reduce overhead or simplify the design, and hence we do not see any benefit of using Option 4. |
| QC | Prefer Option 4 to avoid constant overhead in DCI. Of course, this comes at the cost of reducing the flexibility (only 4 codepoints can be indicated for the pair). But we do not think it is a big issue since the two closed loops can be controlled by other DCIs (when DCI indicates PUCCH resource with one beam of when group-common DCI is used). |
| Ericsson | We support the proposal. We have a slight preference for Option 3.  We agree with NTT DoCoMo’s comment that in Option 4, it should be clarified if the number of bits in the TPC field is expected to be increased over what is supported up to Rel-16. |
| Xiaomi | We prefer Option 3. Option 4 has restrictions for the supported adjustment values for each TRP and also is not backward compatible for single TRP case |
| FL | Moderator made a small update on the DCI formats mentioned in the agreement. |
| Huawei, HiSilicon | We don’t support the proposal, as we have concern on the DCI payload size. By doubling the fields such as TPC, SRI, TPMI, the payload size will be increased by 9 bits (2 bits TPC, 2 bits SRI, and 5 bits TPMI). 9 bits increase in DCI size will significantly impact the reliability of PDCCH, which is contradicting the objection of WID. Therefore, it’s too early to agree on the proposal before estimation of the impact on the PDCCH reliability and possible reduction of DCI payload increase. |
| Intel | We think NW should not be required to use a larger DCI. 2 methods can be supported option 1 (smaller payload) + option 3 (larger payload). If not agreeable, we can start with option 1. |
| LG | Support FL proposal. |
| Lenovo&MotM | Support it while Option 3 is preferred. |
| Samsung | We still prefer Option 1 or Option 2. Without elaborate power control, we can support multi-TRP operation with the other separate power control parameters (p0, PL RS). For sake of progress, Option 3 is ok. |
| ZTE | We support FL’s proposal, and our preference is option 2 or option 4. |
| vivo | For the field design, extending TPC field for PUCCH and TPC field for PUSCH in a common manner is preferred. We can firstly agree on the SRI, TPMI and TPC field extension for PUSCH. |
| Apple | We think option 3 should be the worst solution. If we want to down-select one option, we should list all the them. |
| Fujitsu | Support FL’s proposal. Either option 3 or option 4 is fine. |
| Ericsson2 | For the new FL update, we prefer to discuss separately for PUCCH and PUSCH as DL DCIs are used for PUCCH and UL DCIs are used for PUSCH. |
| NEC | Support option 3. |
| Spreadtrum | Support the FL’s proposal, and we prefer Option4 slightly, which will not change the size of TPC field in DCI. |
| TCL | Support, and we prefer Option 3. |
| FL update#1 | Option 3 is the majority. As there are concerns raised on overhead of DCI, let’s first do the agreement for PUCCH only, where overhead should not be a big issue. Updated proposal,  **[Draft for offline] Proposal 2.4:** To support per TRP closed-loop power control for PUCCH/, a second TPC field is added in DCI formats 1\_1 / 1\_2. |
| InterDigital | We support FL’s proposal. |
| Futurewei | Support the updated proposal. |
| Lenovo&MotM | Support the updated proposal. |
| ZTE | We are NOT supportive of the updated Proposal 2.4.  In RAN1 #103-e, we agreed with three schemes are based on TDMed scheme. Besides, we also agreed that different power control parameters corresponding to different PUCCH spatial relation info. Based on the above two considerations, our further analysis raised as follows.   * For Option 1, it can NOT support beam/SRI-specific power control. * For Option 2, it is the best solution which not only can be used to indicate TDMed TPC command via different spatial relations with the lowest spec impact, but also without any DCI overhead increasing. * For Option 3, it is the worst solution because the second TPC field is not needed due to TDMed PUCCH scheme, which will also leads to extra DCI overhead. * For Option 4, it can support beam/SRI-specific power control, but which may will cause additional DCI overhead in TPC command field.   From the prospective of technology, our recommended order of the four options is Option 2 -> Option 4 -> Option 1 -> Option 3. Although FL have listed option 3 and 4 based on the amount of proponents , we suggest to support Option 2 with technical views. |
| QC | Even though we prefer Option 4, we can accept this proposal for DL DCI if majority of companies support it. |
| LG | Support the updated proposal. Further clarification on what ZTE have in mind for Option 2 will be help us to understand. Could you clarify how does it work? How do you apply TPC command to which closed loop index? We also fine with Option 4. |
| FL Update #2 | After initial set of comments  Intel – option 1, SS/ZTE/HW – option 2, **All others – Ok with option 3**  Please note that the proposal is for PUCCH, where DCI format 1\_1 and 2\_1 are used. And we do not have any other DCI overhead impact there. I would assume Intel, HW, ZTE. SS should be ok with supporting option 3 only for PUCCH.  No changes to the PUCCH proposal (cleaned up only)  **Updated Proposal 2.4-A:** To support per TRP closed-loop power control for PUCCH, a second TPC field (similar to the existing TPC field) is added in DCI formats 1\_1 / 1\_2.  As we do not have separate proposal for PUSCH, the following is proposed further.  **Draft for offline] Proposal 2.4-B:** To support per TRP closed-loop power control for PUSCH,   * Alt.1 : A second TPC field (similar to the existing TPC field) is added in DCI formats 0\_1 / 0\_2. * Alt2 : No changes to the TPC field, and the TPC value applied for one of two PUSCH beams.   + FFS: how the applied PUSCH beam is derived.   For proposal 2.4-A/B, please provide your views. |
| OPPO | Proposal 2.4-A is preferred |
| CMCC | Support the updated proposal 2.4-A and 2.4-B.  For proposal 2.4-B, we prefer Alt 1. |
| NTT Docomo | Support proposal 2.4-A  Support proposal 2.4-B, and prefer Alt 1. |
| Sharp | Support proposal 2.4-A and proposal 2.4-B  For proposal 2.4-B, we prefer Alt. 1. |
| Apple | Do not support the proposal 2.4A/B. Option 3 is the worst solution as we commented. |
| Nokia/NSB | Support Proposal 2.4-A  Support Proposal 2.4-B. We prefer to also adopt Alt.1 |
| Futurewei | Support. And we support Alt 1.  By the way, we think we should consider the same design for GC DCI format 2\_2, otherwise 2\_2 cannot be used for M-TRP PUSCH/PUCCH. Maybe we can add a FFS point for 2\_2? |
| Intel | Not support 2.4-A, why is the gNB required to perform RRC re-config and incur extra DCI overhead ? at least a low overhead option should be available. Similarly for 2.4-B, a low-overhead option should be available to the gNB. We don’t think TPC is an essential enhancement anyways. |
| MediaTek | Support 2.4-A and 2.4-B  For 2.4-B, support Alt 1. |
| NEC | Support the proposals.  And regarding Proposal 2.4-B, we support Alt 1. |
| Lenovo&MotM | Support Proposal 2.4-A, and for Proposal 2.4-B, we support Alt.1. |
| Fujitsu | Support proposal 2.4-A and 2.4-B (prefer Alt-1). |
| Xiaomi | Support the updated proposal 2.4-A and 2.4-B.  For proposal 2.4-B, we prefer Alt 1. |
| Samsung | Support Proposal 2.4-A  Support Proposal 2.4-B and prefer Alt. 1. |
| ZTE | Do NOT support proposal 2.4-A&B. |
| vivo | Our preference is option 4, but we can go with 2.4A and 2.4B Alt. 1. |
| Huawei, HiSilicon | We think that the second TPC field is anyway configurable, so we suggest the following changes:  **Updated Proposal 2.4-A:** To support per TRP closed-loop power control for PUCCH, a second TPC field (similar to the existing TPC field) ~~is added~~ can be configured in DCI formats 1\_1 / 1\_2.   * FFS: for the case that the second TPC field is not configured, while the two spatial filters are indicated.   **Draft for offline] Proposal 2.4-B:** To support per TRP closed-loop power control for PUSCH,   * Alt.1 : A second TPC field (similar to the existing TPC field) ~~is added~~ can be configured in DCI formats 0\_1 / 0\_2.   + FFS: for the case that the second TPC field is not configured, while the two spatial filters are indicated. * Alt2 : No changes to the TPC field, and the TPC value applied for one of two PUSCH beams.   + FFS: how the applied PUSCH beam is derived. |
| FL Update #3 | FW >> DCI format 2\_2 was discussed last time and did not go through. Let’s focus on the formats mentioned in the proposal for now.  Apple, Intel, ZTE >> may be no point of discussing why this is good or bad. I tried to separate PUCCH and PUSCH to accommodate your views on overhead, but majority is in other direction. I will suggest the proposal to discuss in online session.  HW>> Your added text saying the same thing. I would not suggest wording changes as many others might not be Ok with that. Also, it is not essential to discuss RRC configuration mis-matches now. Let’s focus now on basic design.  Alt.1 has majority view.  **Proposal 2.4-A:** To support per TRP closed-loop power control for PUCCH, a second TPC field (similar to the existing TPC field) is added in DCI formats 1\_1 / 1\_2.  **Proposal 2.4-B:** To support per TRP closed-loop power control for PUSCH,   * Alt.1 : A second TPC field (similar to the existing TPC field) is added in DCI formats 0\_1 / 0\_2. * Alt2 : No changes to the TPC field, and the TPC value applied for one of two PUSCH beams.   + FFS: how the applied PUSCH beam is derived. |

### Proposal 2.5

**[Draft for offline] Proposal 2.5:** To support per TRP power control for multi-TRP PUCCH schemes in FR1,

* Two sets of power control parameters are configured via RRC, and each set has a dedicated value of p0, pathloss RS ID and a closed-loop index.
* FFS: details on how a PUCCH resource can be linked to one or both of the two sets of power control parameters.

Please comment preferred changes on the proposal below. Also, provide your preference for FFS.

|  |  |
| --- | --- |
| **Company** | **Comments** |
| NTT Docomo | We support the proposal. |
| MediaTek | Support |
| InterDigital | We support FL’s proposal. |
| Futurewei | Support in principle.  For the first bullet, we think each set may be configured with more than one closed-loop indices (i.e., legacy S-TRP configuration). |
| QC | We prefer to use the same framework as FR2. All that is needed is that the beam information (“referenceSignal”) can be ignored by the UE or can be set to a null value. The benefit is that we can have a unified solution and reuse same RRC and MAC-CE. Even in FR1, the TRPs in the cluster can change due to blockage (e.g. in industrial settings), and an exclusive RRC solution is not preferred by us. |
| Ericsson | Do not support.  We think per TRP power control can be supported with a single pucch-PowerControl parameter with PUCCH-PowerControl information element which contains multiple sets of power control parameters (i.e., P\_0, pathloss RS) and closed-loop indices as it is done in Rel-15/16. We can simply increase the maximum number of sets and closed-loop indices for m-TRP inside the PUCCH-PowerControl information element. A triplet of (P0, pathloss RS, and closed-loop indices) from the sets can be configured for each PUCCH resource for m-TRP. |
| Xiaomi | We prefer QC’s scheme which is simple and has less spec impact. |
| Huawei, HiSilicon | We share similar view with QC so that a unified framework can be used for FR1 and FR2 Note that *PUCCH-SpatialRelationInfo* can be configured for FR1 also, there’s no need to introduce new IEs or new structures for power control. |
| Intel | Do not support – similar view as Ericsson that it can be supported by spec already |
| LG | We support the proposal and also fine with Ericsson’s suggestion. |
| Lenovo&MotM | Support. |
| Samsung | Support the proposal. But more clarification for the set of power control parameters is required. For example, two dedicated values of power control parameters are configured via RRC and they can be applied by default PUCCH power control (lowest p0, PL RS and closed-loop index for TRP 1, next lowest ones for TRP 2) or new RRC parameter for sets of dedicated power control parameters is introduced. |
| ZTE | We support FL’s proposal that two configured PC parameter sets are intuitive from the prospective of specs. Besides, in Rel-16, due to groups of PUCCH resources that can be updated simultaneous for spatial relations, naturally it should be allowed to configure the mapping between PUCCH resource groups and power control parameters per TRP. Thereby, we suggest to revise the part of FFS as below.  FFS: details on how a PUCCH resource or PUCCH resource group can be linked to one or both of the two sets of power control parameters. |
| vivo | We have similar view as QC. To have a common framework of supporting separate power control, two spatial relations can be activated for both FR1 and FR2 if PUCCH repetitions are transmitted to different TRPs. |
| Apple | Support the proposal |
| Fujitsu | Support FL’s proposal. |
| NEC | Support the proposal. |
| Spreadtrum | We support the proposal |
| TCL | Support the proposal. We share similar view with QC. |
| FL update#1 | Majority supports the direction of the proposal.  QC, Xiaomi, HW >> your solution is covered in the FFS, and the proposal do not define the exact method of linking. ‘FFS: details on how a PUCCH resource can be linked to one or both of the two sets of power control parameters.”  Intel, E/// >> The details of RRC may be discussed later. But, I see your point that the proposal may be not correctly interpreted. Please see the update below.  **[Draft for offline] Proposal 2.5:** To support per TRP power control for multi-TRP PUCCH schemes in FR1,   * Two sets of power control parameters are ~~configured~~ used ~~via RRC~~, and each set has a dedicated value of p0, pathloss RS ID and a closed-loop index. * FFS: details on how a PUCCH resource can be linked to one or both of the two sets of power control parameters. |
| InterDigital | We support FL’s proposal. |
| Futurewei | For the updated proposal, can each set (i.e., each TRP) have more than one closed-loop? |
| Lenovo&MotM | Support the updated proposal. |
| ZTE | Support in principle.  For FFS, as we mentioned above, PUCCH resource groups also should be considered to link power control parameter sets for further enhancement in Rel-17. Thus, we suggest:  FFS: details on how a PUCCH resource or PUCCH resource group can be linked to one or both of the two sets of power control parameters. |
| QC | We do not think the proposal in its current form is needed. We already agreed that for FR1 “Support separate power control for different TRP.”, which means two sets of power control parameters are used. |
| LG | Support the updated proposal. |
| FL update#2 | FW >> each set can have one closed-loop index.  ZTE>. Your change is addressed in different FFS point as they can be separated.  QC >> yes, it was agreed that “Support separate power control for different TRP.”, however, that was not giving any details on power control parameters (I would agree that is implicit, but there were proposal on these parameters make things clear). The idea is to go into next level of alternatives for FFS bullet.  **[Draft for offline] Proposal 2.5:** To support per TRP power control for multi-TRP PUCCH schemes in FR1,   * Two sets of power control parameters are ~~configured~~ used ~~via RRC~~, and each set has a dedicated value of p0, pathloss RS ID and a closed-loop index. * FFS: details on how a PUCCH resource can be linked to one or both of the two sets of power control parameters. * FFS: whether PUCCH resource group can be linked to power control parameter sets. |
| OPPO | Support the updated proposal |
| CMCC | Support the updated proposal. |
| NTT Docomo | We support the proposal. |
| Sharp | We are fine with the proposal |
| Apple | Support in principle, but we do not know why we change “configured” into “used”, where should the two sets come from? |
| Nokia/NSB | Support the proposal |
| Futurewei | Support in principle. Related to our question on only 1 closed-loop per TRP, this is different from the legacy design. If a UE is operating with 1 TRP and 2 closed-loops, with another TRP added, the UE has to stop using one of the loops it has been using. This seems a bit too restrictive. If this is the majority view we can accept, but we do not recall seeing the discussions. |
| Intel | This is okay. But we prefer not to add a specific solution as FFS – the first 2 sub-bullets are sufficient. |
| MediaTek | Support |
| NEC | Support the updated proposal. |
| Lenovo&MotM | Support |
| Fujitsu | Support the updated proposal. |
| Xiaomi | Agree with Intel. |
| Samsung | Support the updated proposal |
| ZTE | Support FL’s update#2 proposal. |
| vivo | We want to clarify that the FL update#2 means we haven’t decided yet whether the two sets of power control parameters are configured separately or linked to the spatial relation? |
| Huawei, HiSilicon | We are fine with the updated proposal. |
| FL Update #3 | Apple >> having RRC term there had objections from few companies. As details are FFS, may be people have different things in mind.  Intel>>ZTE has concern with agreeing without the third sub-bullet. As chairman always says, lets not waste time over a FFS bullet.  Vivo>> to answer your question. No, we have not.  All >> this can be endorsed.  **Offline Agreement 2.5:** To support per TRP power control for multi-TRP PUCCH schemes in FR1,   * Two sets of power control parameters are used, and each set has a dedicated value of p0, pathloss RS ID and a closed-loop index. * FFS: details on how a PUCCH resource can be linked to one or both of the two sets of power control parameters. * FFS: whether PUCCH resource group can be linked to power control parameter sets. |

### Proposal 2.6

**[Draft for offline] Proposal 2.6:** For inter-slot frequency hopping in Scheme 1, further discuss the following alternatives,

* Alt.1: frequency hopping is performed among the repetitions with the same beam
* Alt.2: frequency hopping is performed on slot level (as in Rel-15).

Note: Outcome of Alt.1 can also be achieved by Alt.2 when using the sequential beam mapping.

Please comment preferred changes on the proposal below. Mention the support for Alt. 1 or 2.

|  |  |
| --- | --- |
| **Company** | **Comments** |
| NTT Docomo | We think this issue can be discussed after we have agreed on the beam mapping pattern. |
| MediaTek | Support Alt. 1. Alt. 2 cannot exploit all diversity gains when using cyclic beam mapping unless the hopping pattern is modified. |
| InterDigital | Agree with NTT. |
| Futurewei | Agree with NTT Docomo. |
| QC | Support Alt1. For cyclic mapping, Alt2 results in all repetitions of the same beam to be transmitted in the same frequency hop, which is not acceptable. The proposal can be conditioned on cyclic mapping. Also, the benefit of Alt1+cyclic mapping versus Alt1/2+ sequential mapping is that beam diversity is realized earlier (as it is more important especially in FR2) and the same time both beam diversity and frequency diversity are eventually realized. |
| Ericsson | For inter-slot repetition, the Rel-15 intra-/inter-slot FH should be enough and it may be left to the gNB on how to configure it, i.e., with either intra-slot FH on/inter-slot FH off, or the other way around, although intra-slot FH is preferred. |
| Xiaomi | Agree with NTT Docomo. |
| Huawei, HiSilicon | Agree with Docomo to discuss this after decision on beam mapping patterns. |
| Intel | Agree with others that we can re-visit after beam mapping pattern discussion. |
| LG | Support Alt1. In addition, beam mapping pattern when TO is dropped due to invalid UL symbol should be discussed in order to avoid uneven beam dropping. |
| Lenovo&MotMB | Support Alt 1. |
| Samsung | Support Alt. 1. To obtain diversity gain in frequency domain, frequency hopping can be conducted per beam. |
| ZTE | Share the same view with DOCOMO. |
| vivo | We think at least we should agree on the principle of “frequency hopping among the repetitions with the same beam” first. Then how to configure to achieve this can be FFS. Ericsson’s solution seems a good starting point. |
| Apple | Support Alt1, or we should revert the working assumption by removing cycling mapping if Alt2 is selected. |
| Fujitsu | Agree with NTT Docomo. |
| NEC | Agree with NTT Docomo. |
| TCL | Share the same view with DOCOMO. |
| FL update#1 | Majority supports the direction Alt.1. But several others suggest waiting for confirming the working assumption. In FL view, this is not a critical thing anyways as something can be handled as E/// highlighted. |
| Nokia/NSB | We are OK with NTT DOCOMO’s suggestion |

### Proposal 2.7

**[Draft for offline] Proposal 2.7:** For beam mapping /power control parameter set mapping for PUCCH repetitions,

* For M-TRP PUCCH Scheme 1 in FR1, it is possible to configure either cyclic mapping or sequential mapping of power control parameter sets over PUCCH repetitions (similar to spatial relation info’s over PUCCH repetitions).
* For M-TRP PUCCH Scheme 3, reuse the same methods as Scheme 1 (by replacing slots with sub-slots) for beam mapping or power control resource set mapping to sub-slots.

Please comment preferred changes on the proposal below.

|  |  |
| --- | --- |
| **Company** | **Comments** |
| NTT Docomo | We support this proposal in general.  But we think the discussion for FR1 may depend on the progress of proposal 2.5 and can be discussed later. Or we add in the first bullet “if two sets of power control parameters configured via RRC is supported”. |
| MediaTek | Support |
| InterDigital | We support FL’s proposal. |
| Futurewei | Support |
| QC | Support the first bullet. The second bullet depends on the outcome of Proposal 2.3. |
| Ericsson | Similar comment as NTT DoCoMo. The first sub-bullet on FR1 depends on Proposal 2.5. We can discuss the first sub-bullet after discussing Proposal 2.5. |
| Xiaomi | Support FL’s proposal, |
| Huawei, HiSilicon | We are fine with the first bullet, however we need to first decide on proposal 2.3 before discuss the second bullet. Therefore, we propose to modify as below:  **[Draft for offline] Proposal 2.7:** For beam mapping /power control parameter set mapping for PUCCH repetitions,   * For M-TRP PUCCH Scheme 1 in FR1, it is possible to configure either cyclic mapping or sequential mapping of power control parameter sets over PUCCH repetitions (similar to spatial relation info’s over PUCCH repetitions). * FFS: For M-TRP PUCCH Scheme 2 and 3~~, reuse the same methods as Scheme 1 (by replacing slots with sub-slots) for beam mapping or power control resource set mapping to sub-slots.~~ |
| Intel | agree, depends on how 2.5 is resolved |
| LG | Support Huawei’s revision. |
| Lenovo&MotM | Support. |
| Samsung | Support the proposal. But we should consider the beam switching gap between repetitions for Scheme 3 according to RAN4’s reply. |
| ZTE | Share the same view with DOCOMO and other companies that this issue should be addressed after the discussion of Proposal 2.5. |
| vivo | Support FL’s proposal. |
| Apple | We should wait for RAN4 response. |
| Fujitsu | Support FL’s proposal. |
| NEC | Support the proposal. |
| TCL | Support the proposal. |
| FL update#1 | Majority supports the direction of the proposal. The second bullet will be agreed only after agreeing to Scheme 3. For now, do not worry about that aspect, and focus on the wording used.  **[Draft for offline] Proposal 2.7:** For beam mapping /power control parameter set mapping for PUCCH repetitions,   * For M-TRP PUCCH Scheme 1 in FR1, it is possible to configure either cyclic mapping or sequential mapping of power control parameter sets over PUCCH repetitions (similar to spatial relation info’s over PUCCH repetitions). * For M-TRP PUCCH Scheme 3, reuse the same methods as Scheme 1 (by replacing slots with sub-slots) for beam mapping or power control resource set mapping to sub-slots. |
| InterDigital | We support FL’s proposal. |
| Futurewei | Support the updated proposal. |
| Lenovo&MotM | Support the updated proposal. |
| ZTE | The agreement of beam pattern for different schemes is need at first. |
| QC | Support. |
| LG | We support the proposal without last bullet point on Scheme 3. |
| FL update#2 | ZTE>> the working assumption is details are reused in the proposal. We could still make working assumption also for proposal 2.7 as nothing new added on top of the beam mapping working assumption.  LG>> yes, scheme 3 proposal will be treated first.  No change to the proposal.  **[Draft for offline] Proposal 2.7:** For beam mapping /power control parameter set mapping for PUCCH repetitions,   * For M-TRP PUCCH Scheme 1 in FR1, it is possible to configure either cyclic mapping or sequential mapping of power control parameter sets over PUCCH repetitions (similar to spatial relation info’s over PUCCH repetitions).   For M-TRP PUCCH Scheme 3, reuse the same methods as Scheme 1 (by replacing slots with sub-slots) for beam mapping or power control resource set mapping to sub-slots. |
| OPPO | Support |
| CMCC | Support |
| NTT Docomo | We support the proposal. |
| Sharp | Support |
| Apple | This should be discussed after we see the outcome of proposal 2.5 and wait for RAN4’s response |
| Nokia/NSB | Support the proposal |
| Futurewei | Support |
| MediaTek | Support |
| NEC | Support the proposal. |
| Lenovo&MotM | Support |
| Fujitsu | Support the proposal. |
| Xiaomi | Support the proposal |
| Samsung | Support in principle. More details should be discussed after RAN4’s reply. |
| ZTE | Discuss in the next meeting. |
| vivo | Support |
| Huawei, HiSilicon | We are fine with the proposal. |
| FL update#3 | **@Apple, ZTE** >> I see that comments are mainly conditioned on RAN4 LS. As commented before, the below proposal could still be working assumption (similar principal is applied as beam mapping). Please see the brackets “similar to spatial relation info’s over PUCCH repetitions”. You could suggest any wording to reflect what you want to capture as majority is ok with progressing on this.  **Proposal for working assumption 2.7:** For beam mapping /power control parameter set mapping for PUCCH repetitions,   * For M-TRP PUCCH Scheme 1 in FR1, it is possible to configure either cyclic mapping or sequential mapping of power control parameter sets over PUCCH repetitions (similar to spatial relation info’s over PUCCH repetitions). * For M-TRP PUCCH Scheme 3, reuse the same methods as Scheme 1 (by replacing slots with sub-slots) for beam mapping or power control resource set mapping to sub-slots. |

### Proposal 2.8

**[Draft for offline] Proposal 2.8:** For Multi-TRP Scheme 1, support dynamic switching between multi-TRP PUCCH scheme and single-TRP PUCCH transmission by associating,

* a PUCCH resource with one or two spatial-relation-info and PRI bit-field indicating a PUCCH resource (for FR2).
* a PUCCH resource with one or two power control parameter sets and PRI bit-field indicating a PUCCH resource (for FR1)

FFS: support of dynamic switching for Scheme 2/3 (if the schemes supported)

Please comment preferred changes on the proposal below.

|  |  |
| --- | --- |
| **Company** | **Comments** |
| NTT Docomo | We support the proposal in general.  Similar as we comment in proposal 2.7, we think the discussion for FR1 may depend on the progress of proposal 2.5 and can be discussed later. Or we add in the second bullet “if two sets of power control parameters configured via RRC is supported”. |
| MediaTek | Support |
| InterDigital | We support FL’s proposal. |
| Futurewei | We have a clarification question: the S-TRP PUCCH transmission is only for one of the TRPs or for either of the TRPs? That is, the UE is configured with one S-TRP PUCCH resource or two S-TRP PUCCH resources for the two TRPs? |
| QC | We do not see the necessity of this proposal. This should be naturally supported by existing agreements / framework. If there is any specification impact to support dynamic switching, that procedure can be discussed directly. |
| Ericsson | The second sub-bullet related to FR1 depends on Proposal 2.5. Better to discuss this second sub-bullet after discussing Proposal 2.5. |
| Xiaomi | Agree with QC. |
| Huawei, HiSilicon | We support the motivation of the proposal. But the second bullet for fR1 depends on the discussion of proposal 2.5. In fact, this is the reason we propose to *SpatialReltionInfo* for FR1, then we don’t need to specify different methods for FR1&FR2. |
| Intel | Agree with most of it but the second sub-bullet depends on resolution of 2.5 as others have mentioned as well |
| LG | We support FL’s proposal. |
| Lenovo&MotM | Support. |
| Samsung | For FR1, the detail method to support separate power control is discussing. This proposal for FR1 should be discussed after enhancement on separate power control for FR1. |
| ZTE | Share the same view with DOCOMO and other companies that this issue should be addressed after the discussion of Proposal 2.5. |
| vivo | Agree with Huawei. |
| Apple | What’s the spec impact? |
| Fujitsu | Agree with QC. |
| NEC | Support the proposal. |
| Spreadtrum | Share the same view with ZTE and other companies. We prefer to postpone the discussion after the discussion of Proposal 2.5. |
| TCL | Share the same view with DOCOMO. |
| FL update#1 | Different views, but seems companies do not object the direction.  FW >>For your questions, FL have the following understanding,   * TRP depends on the indicated PUCCH which related to the beam or power control parameter set. * 2. single PUCCH resource is assumed in this discussion.   QC, Apple >> there is no agreement to allow dynamic switching, so without this, companies can also mention later that UE does not expect to receive switching when it is in one mode. There may not be spec impact. Anyways, changed the wording to reflect this.  HW>> There are cases that spatial-relation-info is not used, so the second bullet is covering that scenario. Please note that there is one other FFS on linking of PUCCH resource to power control parameters (in proposal 2.5), where the solution you have above can still be discussed. .  **[Draft for offline] Proposal 2.8:** For Multi-TRP Scheme 1, supporting dynamic switching between multi-TRP PUCCH scheme and single-TRP PUCCH transmission is not restricted, and can be done by associating,   * a PUCCH resource with one or two spatial-relation-info and PRI bit-field indicating a PUCCH resource (for FR2). * a PUCCH resource with one or two power control parameter sets and PRI bit-field indicating a PUCCH resource (for FR1)   FFS: support of dynamic switching for Scheme 2/3 (if the schemes supported) |
| InterDigital | We support FL’s proposal. |
| Futurewei | Ok with the proposal. |
| Lenovo&MotM | Support. |
| ZTE | Support FL’s updated proposal. |
| QC | Ok with the updated proposal. |
| FL update#2 | No update to the proposal.  **[Draft for offline] Proposal 2.8:** For Multi-TRP Scheme 1, supporting dynamic switching between multi-TRP PUCCH scheme and single-TRP PUCCH transmission is not restricted, and can be done by associating,   * a PUCCH resource with one or two spatial-relation-info and PRI bit-field indicating a PUCCH resource (for FR2). * a PUCCH resource with one or two power control parameter sets and PRI bit-field indicating a PUCCH resource (for FR1)   FFS: support of dynamic switching for Scheme 2/3 (if the schemes supported)  HW, Apple >> please comment if the above is not agreeable for you. |
| OPPO | For FR2, we think it can be naturally supported with the spatial relation info activated by MAC-CE.  For FR1, it is related to the progress of Proposal 2.5.  One question for clarification: Does the proposal mean as below?  If A PUCCH is configured / activated with ONE spatial-relation-info and it is indicated by PRI, then it is single-TRP transmission  If A PUCCH is configured / activated with TWO spatial-relation-info and it is indicated by PRI, then it is multi-TRP transmission  If the above understanding is correct, we suggest to reword the proposal as below to make it clear  **[Draft for offline] Proposal 2.8:** For Multi-TRP Scheme 1, supporting dynamic switching between multi-TRP PUCCH scheme and single-TRP PUCCH transmission is not restricted, and can be done by ~~associating~~,   * PRI bit-field indicating a PUCCH resource with one or two spatial-relation-info ~~and PRI bit-field indicating a PUCCH resource~~ (for FR2). * PRI bit-field indicating a PUCCH resource with one or two power control parameter sets ~~and PRI bit-field indicating a PUCCH resource~~ (for FR1)   FFS: support of dynamic switching for Scheme 2/3 (if the schemes supported) |
| CMCC | Ok with the updated proposal. |
| NTT Docomo | We support the proposal. |
| Apple | We do not think this proposal is necessary. |
| Nokia/NSB | Support the proposal. |
| Futurewei | Support in principle. Related to OPPO’s question, RRC/MAC are not very dynamic, but the proposal mentions “dynamic” a couple of time. Can this be clarified? |
| MediaTek | Support |
| NEC | Support the updated proposal. |
| Lenovo&MotM | Support |
| Fujitsu | Support the updated proposal. |
| Xiaomi | We do not think the proposal is necessary. |
| Samsung | Support the updated proposal. |
| vivo | We are fine with OPPO’s version, note that it depends on the outcome of Proposal 2.5 for FR1.  @Futurewei: we think “dynamic” here means DCI-based PRI indication between a PUCCH with two spatial relation info and a PUCCH with one spatial relation info. |
| Huawei, HiSilicon | We can be fine with the update proposal. |
| FL update#3 | Oppo >> Yes, your understanding is correct.  **Apple, Xiaomi** >> It seems you do not think this is needed. Without this, companies might say that dynamic switching between S-TRP and M-TRP is not allowed. That was the case in some Rel-16 M-TRP URLLC scheme switching, for example, even when certain parameter setting allowed switching possibilities, RAN2 debated later to support or not. In that sense, even though this is automatically supported with the PUCCH associating multiple beams/parameters sets, this type of agreement is needed. Also, that is the majority view.  **Proposal 2.8:** For Multi-TRP Scheme 1, supporting dynamic switching between multi-TRP PUCCH scheme and single-TRP PUCCH transmission is not restricted, and can be done by associating,   * a PUCCH resource with one or two spatial-relation-info and PRI bit-field indicating a PUCCH resource (for FR2). * a PUCCH resource with one or two power control parameter sets and PRI bit-field indicating a PUCCH resource (for FR1)   FFS: support of dynamic switching for Scheme 2/3 (if the schemes supported) |

## 2.3 Additional high priority proposals

In this FL summary, we have not included any FL proposals based on certain other directions suggested by one or two companies. Such proposals are not considered if that is not critical for the basic design framework or can be discussed in a later stage once the basic framework is agreed. Please see the full list of company contribution proposals in Section 5. If companies wish to bring any additional aspects related to PUCCH during RAN1 #104-e, please comment below.

|  |  |
| --- | --- |
| Company | Comments |
| LG | Beam mapping in case of PUCCH dropping due to invalid UL symbols should be discussed.  If beams are mapped to PUCCH TO without considering dropping, PUCCH TO for one TRP can be dropped much more than PUCCH TO for another TRP. As a result, diversity gain from MTRP transmission can decrease or disappear. |
| Lenovo&MotM | Beam determination of PUSCH scheduled by DCI format 0\_0 while the PUCCH resources with the lowest index is configured with two beams. |
| ZTE | For multi-TRP PUCCH transmissions in Rel-17, due to different beams of one PUCCH resource can targeting to two TRP, it is naturally to allow one same PUCCH resource is included in two PUCCH resource groups, such that the resource can be configured with two beams. Besides, as we mentioned in Proposal 2.5, PUCCH resource group is associated with spatial relation update per TRP, it is also related to the power control parameters per TRP. Thus, we believe this issue should be discussed in this meeting.  In order to enhance this feature, one reserved bit in the existing “Enhanced PUCCH Spatial Relation Activation/Deactivation MAC CE” can be used to indicate which one of PUCCH Groups with the same PUCCH resource should be updated. |
| MediaTek | Intra-slot beam hopping should be supported. Rather than adapting from the frequency hopping design, we prefer a design similar to intra-slot TDM developed for mutli-TRP PDSCH. In particular, the same code block of UCI are repeated towards two TRPs, rather than only part of the code block is sent to a TRP.  Our reason to support intra-slot beam hopping is as follows. First, not all UEs support URLLC, so UEs do not need to support sub-slot operation. If blockage probability can be 10%, then the reliability of PUCCH should be enhanced for eMBB as well. However, solely relying on inter-slot repetition may not be suitable for all services due to longer delay and no UCI multiplexing is allowed. Thus, there is a need to have intra-slot beam hopping. |
| Apple | We suggest to discuss the default beam for PUSCH scheduled by DCI format 0\_0 when two special relations are configured for a PUCCH resource. |
| FL | Depending on how much we progress with current proposals. We can address these in phase #2 |
| Nokia/NSB | We suggest discussing, if the UE is not provided pathlossReferenceRSs, how to enable the UE to determine two RS resources needed to calculate two pathloss values for PUCCH power control. |
|  |  |
|  |  |

# Multi-TRP PUSCH transmission

The first sub-section below summarizes company proposals, the second sub-section provide FL proposals, and third allows companies to add further comments on any missing proposals which companies think high priority.

## 3.1 Summary of contributions

In the last meeting, several agreements were made related to M-TRP PUSCH transmissions. The remaining issues which are highlighted by company contributions are summarized below.

**Table 2: Summary: Supported M-TRP PUSCH schemes**

|  |  |  |
| --- | --- | --- |
| **Issue** | **Summary from Tdocs** | **Moderator comments** |
| 1. Codebook-based and non-codebook : Support the indication of two SRIs | * **Alt1 (Bit-field of SRI shall be enhanced):** * **Separate SRI fields**: FW, OPPO, Lenovo, ZTE, CATT, SS, APT, NEC, Xiaomi, QC, Sharp, DCM, E///, Nokia, CMCC (?), HW(?), Fraunhofer (?), Apple * **Re-interpret enhanced SRI field**: Vivo, Intel, Spreadtrum, LG, Convida (?) * **Alt2 (No changes on SRI field):** | Almost all companies support enhanced SRI field.  There seem to be two main variants for enhanced SRI field, where majority support that SRIs are indicated separately for corresponding two SRS resource sets.  See FL proposal 3.1. |
| 1. Max Rank for M-TRP PUSCH | * **Limit the max rank for MTRP PUSCH repetition to 2**: LG, OPPO, Xiaomi, APT * **No**: Apple | When supporting M-TRP repetition schemes, DCI overhead is a valid concern.  See FL proposal 3.2 |
| 1. Codebook-based: Indication of two TPMIs | * **Alt. 1 (Support two fields):** (14)   FW, OPPO, Lenovo, ZTE, LG, APT, NEC, Xiaomi, QC, Sharp, Convida, DCM, E///, Nokia, Apple   * **Reduced second TPMI field:** NEC, ZTE, Oppo, Covinda, QC * **Use TPMI index restriction**: Lenovo * **Alt. 2 (single/extended field, use the TPMI field as a codepoint):** (6)   HW, Vivo, CATT, Fraunhofer, Intel, Spreadtrum   * **Single TPMI table to jointly indicate two TPMIs**: Intel, HW | Majority support two TPMI fields.  Several companies highlighted that the size of the DCI might increase with Alt.1, but based on the analysis provided by few contributions, using an extended TPMI field (with codepoints indicating combinations of TPMIs) may not reduce the overhead, and that may also create extra RAN1 work.  To address the increase of DCI payload, proposal 3.2 (max rank for PUSCH repetition limited to two) may help.    See FL proposal 3.3 |
| 1. PTRS-DMRS association | For maxRank = 2:   * **No changes needed on the field** (Reinterpret the bit field): Oppo, QC, Vivo, ZTE, Nokia * **MSB and LSB can be used for two TRPs**: ZTE, LG, QC   For maxRank >2:   * A second field is needed: QC, Nokia * Existing field used for TRP1, and entries/bits of DM-RS port indication used for TRP2: ZTE   Other   * Support PT-RS to DMRS port association cycling: Apple * New MAC CE can be considered for the enhancement on PTRS-DMRS association: Spreadtrum * Enhancement on PTRS-DMRS association for single-DCI based is not necessary: SS | The design details is clear to maxRank = 2.  Also considering proposal 3.2, higher ranks are not considered.  See FL proposal 3.4 |
| 1. Number of layers for non-CB-based PUSCH repetition | **The same number of layers:** Huawei, ZTE, LG, Nokia | A TB's repetitions can not be done with different layers unless different MCS and other parameters are changed. So, this may not require an additional agreement. |
| 1. Power Control: TPC command | * **Option 1:** (5) OPPO, Lenovo, Intel, SS, QC * **Option 2:** (4) Huawei, APT, SS, ZTE * **Option 3:** (12) FW, Lenovo, CATT, MTek, NEC, CMCC, Xiaomi, Convida, Sharp, DCM, E///, Nokia * **Option 4:** (11) OPPO, Lenovo, CATT, vivo, Intel, Fujitsu, Spreadtrum, Apple, QC, E///, ZTE | This also related to the proposal in PUCCH, therefore, handled together.  See FL **proposal 2.4 (previous section)** |
| 1. Power control: parameter sets | Support up to two power control parameter sets (SRI-PUSCH-PowerControl) depending on SRI field: Vivo, QC, FW, ZTE  Linking SRIs to SRI-PUSCH-PowerControl   * Select two *SRI-PUSCH-PowerControl* from two *sri-PUSCH-MappingToAddModList*: Vivo * Configuring each SRI-PUSCH-PowerControl with SRS resource set ID ( “sri-resource-setId”) - QC   Other   * Two *srs-PowerControlAdjustmentStates* included in both SRS-ResourceSets have same value ‘sameAsFci2’ – SS * Study open-loop power control parameter set indication– Vivo, QC * Study on PHR reporting: QC, Apple | Two SRIs should indicate two sets of power control parameters, and companies provided further details on how signalling should work.  See FL proposal 3.5 |
| 1. Dynamic switching between single-TRP and multi-TRP | **Support dynamic switching:** Huawei, ZTE, NEC, QC, Nokia, DCM, Intel, Xiaomi, CATT   * **Exploit the SRI field(s)**: Huawei, NEC, QC, Vivo, ZTE(for non-codebook scheme) * **Exploit TPMI field(s)**: ZTE(for codebook scheme) * **Group DCI:** Xiaomi | There is good support for dynamic switching between single and multi-TRP operations. Majority of companies think that SRI fields can indicate the mode of operation.  See FL proposal 3.6 |
| 1. M-DCI PUSCH repetition | **Support**: FW, Vivo, LG, CMCC, Samsung, TCL, Nokia  **No**: Apple, Intel | This was discussed a lot in the last meeting, and FL suggested that companies bring simulation results.  Vivo provided a set of simulations that shows gains on m-DCI PUSCH schemes.  See FL proposal 3.7 |
| 1. RV mapping method for PUSCH repetition type B | **Support the same method as Type A**: OPPO (RV cycling across actual repetition), Vivo, LG, Fujitsu, Ericsson  Other methods: Xiaomi, Fujitsu | The majority thinks to support the same method as Type A repetition.  See FL proposal 3.8 |
| 1. CG PUSCH | * **Single CG configuration (Alt.1):** InterDigital, OPPO, HW, CATT, MTek, Lenovo, Fujitsu, Apple, Fraunhofer, QC, DCM, E/// * **More than one CG configuration (At.2):** Vivo, APT, Lenovo, Nokia   Other   * Enhanced timing relationship between SRS and CG PUSCH to allow automatic beam update: SS * Same mapping pattern as the dynamic grant: DCM | Majority support a single CG configuration.  See FL proposal 3.9 |
| 1. Beam mapping | * Support dropping symbols of two adjacent PUSCH repetitions due to beam switching: Lenovo, Xiaomi, Nokia, APT * Single PUSCH transmission with beam hopping: Vivo, LG * Confirm working assumption: CMCC, HW * Association between frequency hopping pattern and beam pattern – Vivo, QC | No FL proposals as these partly depend on RAN4 LS.  Association between FH and beam pattern will be addressed in phase 2 as a similar discussion happens in PUCCH. |
| 1. CSI related enhancements | * Support CSI multiplexing on at least two PUSCH occasion – E///, HW, QC | No FL proposal until the basic framework is finalized. |

## 3.2 FL proposals

### Proposal 3.1

**[Draft for offline] Proposal 3.1:** For single DCI based M-TRP PUSCH repetition schemes, in both codebook and non-codebook based PUSCH, two SRI fields corresponding to two SRS resource sets are included in DCI formats 0\_1/0\_2.

* Each SRI field uses the Rel-15/16 SRI field design of DCI format 0\_1/0\_2

Please comment preferred changes on the proposal below.

|  |  |
| --- | --- |
| **Company** | **Comments** |
| QC | Support the main proposal. For the bullet, we think to enable dynamic switching between sTRP and mTRP, a minor change to each SRI field is needed: One codepoints indicates no SRS resource is selected from that SRS resource set. Note that there is already a reserved codepoint in most of the SRI tables that can be reused (no need to increase number of bits in most cases). |
| Huawei, HiSilicon | We don’t support the proposal. As we commented to proposal 2.4, we have concern on the DCI payload size. By doubling the fields such as TPC, SRI, TPMI, the payload size will be increased by 9 bits (2 bits TPC, 2 bits SRI, and 5 bits TPMI). 9 bits increase in DCI size will significantly impact the reliability of PDCCH, which is contradicting the objection of WID. Therefore, it’s too early to agree on the proposal before estimation of the impact on the PDCCH reliability and possible reduction of DCI payload increase.  In addition, the design of SRI fields should be discussed separately for codebook based and non-codebook based PUSCH. For non-codebook based PUSCH, the SRI field size can be reduced assuming the same rank for two TRPs, similar to what we have agreed for codebook based PUSCH. |
| Intel | We think dynamic switching (sTRP/mTRP) should be discussed first, similar concerns as HW on DCI size as well. A first step could be to list all the options on the table based on DCI size impact. Further it will be good to align dynamic switching solutions for CB and NCB together. |
| LG | We don’t support the proposal. Minimizing DCI payload size is important to achieve PDCCH reliability. Single joint SRI field always requires equal or smaller payload that two SRI field. Therefore, we support a single field with adding bits. In case of two SRI field, we need to add a codepoint to indicate STRP PDCCH transmission so that SRI field size increases. Proponents may argue that reserved codepoint can be used for free, but there are several cases without reserved codepoint such as Lmax=1, Nsrs=2 or 4 for nonCB and Nsrs=2 or 4 for CB. Also, even if reserved codepoint is used, single joint SRI requires equal or smaller bits. For example, when Lmax=2 and Nsrs=4 for nonCB, two RSI fields need 4+4=8bits but single field needs 7 bits assuming the same rank restriction. |
| Lenovo&MotM | Support. |
| Samsung | Support the proposal. |
| vivo | We think two separate SRI field solution has some disadvantages. One SRI field with joint encoding is preferred.  Firstly, there is good support for dynamic switching between single and multi-TRP operations by SRI field indications. However, the two SRI field solution is unable to indicate the SRI of one TRP is not being selected.  Secondly, dynamically switching the order of SRIs of two TRPs, which we think is necessary, cannot be supported by the two SRI field solution either. |
| MediaTek | We support two SRI fields for codebook based PUSCH but share a similar view that the SRI field may need to be modified to support dynamic switching between sTRP and mTRP. The SRI field(s) for non-codebook based PUSCH can be discussed after determining whether to enforce a same number of layers. |
| NTT Docomo | Support the main proposal. Similar view as Qualcomm that dynamic switching between S-TRP and M-TRP should be considered. |
| Apple | Support |
| Fujitsu | Support FL’s proposal. |
| Ericsson | Support the proposal. We also agree with QC that one reserved codepoint in each SRI field can be used to indicate enabling/disabling of the corresponding SRI field. With this approach, it should be possible to easily support dynamic switching between S-TRP and M-TRP.  To maintain the same scheduling flexibility, solutions based on single joint SRI field will also incur an increase in DCI payload. Enhancing single joint SRI field while supporting dynamic switching between single-TRP PUSCH and multi-TRP PUSCH would require additional bits in DCI, and also would require more standardization effort (e.g., design of new SRI table, etc). We think two SRI fields is a cleaner solution with less specification effort. |
| NEC | We share similar view with QC and Ericsson. One reserved codepoint in each SRI field should be used for dynamic switching between single-TRP and multi-TRP. |
| ZTE | Support in principle. As companies mentioned above, in order to enable dynamic switching between STRP and MTRP as well as minimize DCI overhead, we think the methods of two SRIs indication for codebook based and non-codebook based schemes should be separately discuss.  For non-codebook based scheme, we believe it is better to address the following issues one by one for progress.   * Firstly, we should clear that whether the number of SRS ports between two SRS resource sets should be same. As per our view, RAN1 agreed that the number of SRS ports between two TRPs are same for code-book based scheme. Likewise, it is natural to keep alignment with non-codebook based scheme that the number of SRS ports between two SRS resource sets should be same. * Secondly, regarding the method of two SRIs indication, we support to used two separate SRI fields. Where the 1st SRI field is the same as Rel-16 (consider enabling full power Modes) and can indicate the SRS ports number/ transmission rank, the 2nd SRI field is part of 1st SRI field depends on the case of one specific rank with the most entries. Based on that, 1 or more bits can be saved compared with the copy-paste of 1st first field. * Thirdly, based on the second part, two reserved entries in 2nd SRI field can be used to indicate dynamic switching between STPR and MTRP as well as minimize DCI overhead for single-DCI scheme, which is a method of achieving two things with one stroke. Besides, two separate SRI field can be benefit to easily and intuitively configure the mapping between SRI and power control parameters of PUSCH with low spec impact and effort.   For codebook based scheme, we support to use two separate SRI fields, where both the 1st SRI field and 2nd SRI field are same as Rel-16 (also consider enabling full power Modes). W.r.t support dynamic switching between STRP and MTRP, we can use two reserved entries in 2nd TPMI field to indicate it, which also can guarantee the minimized DCI overhead. Likewise, an unified design is applied for both code-book based and non-codebook based schemes. Meanwhile, the configured mapping between SRI and power control parameters can be intuitive for code-book based scheme, too.  In the light of above above elaboration, we suggest to revise the proposal as below:  **[Draft for offline] Proposal 3.1:** For single DCI based M-TRP PUSCH repetition schemes, in both codebook and non-codebook based PUSCH, two SRI fields corresponding to two SRS resource sets are included in DCI formats 0\_1/0\_2.   * FFS: How to design each SRI field for codebook based and non-codebook based schemes, respectively. ~~Each SRI field uses the Rel-15/16 SRI field design of DCI format 0\_1/0\_2~~ |
| Xiaomi | Support the proposal |
| Spreadtrum | We do not support the proposals. We share the similar view as Huawei and LGE that DCI payload size should be carefully considered for the reliability of PDCCH. |
| Fraunhofer IIS/HHI | Agree with the concerns raised by companies on DCI payload size and dynamic STRP-MTRP switching. Enhancing the SRI bit-field to jointly indicate the two SRIs would be a better option. |
| TCL | Support in principle. We share similar view with QC. One reserved codepoint in each SRI field should be used for dynamic switching between single-TRP and multi-TRP. |
| FL update#1 | Majority support the direction of the proposal but few companies think that having two fields increase the DCI size. To FL understanding, unless we introduce significant change in the specification, there is no way out from this extra overhead in DCI.  Also, based on the comments, several companies suggest discussing dynamic switching together with SRI fields. Considering both proposal 3.1 and 3.6, the following updates are proposed,  **Draft for offline] Proposal 3.1:** For single DCI based M-TRP PUSCH repetition schemes, in both codebook and non-codebook based PUSCH,   * Support two SRI fields (each field based on Rel-15/16 framework) corresponding to two SRS resource sets are included in DCI formats 0\_1/0\_2. * Support dynamic switching between multi-TRP and single-TRP operation by using two SRI fields * FFS: Details of SRI field interpretations |
| InterDigital | We support FL’s proposal. |
| Futurewei | Support the updated proposal. |
| Lenovo/MotM | Support the updated proposal. |
| ZTE | We have strong concern of this updated proposal.  From our perspective, the usage of SRI for codebook based and non-codebook based schemes are different. One the other hand, for single DCI based PUSCH scheme, the most sensitive issue is about DCI overhead for enabling several intentions, e.g., indicating two SRIs/TPMIs as well as dynamic switching between STRP and MTRP for codebook based scheme, indicating two SRIs as well as dynamic switching between STRP and MTRP for non-codebook based scheme.  For the sake of progress, we suggest to split the discussions of Proposal 3.1 and Proposal 3.6 to avoid a deadlock situation. Correspondingly, we can firstly discuss how to design the two SRI fields for these two schemes (codebook and non-codebook) in this proposal, respectively.   * **Draft for offline] Proposal 3.1:** For single DCI based M-TRP PUSCH repetition schemes, in both codebook and non-codebook based PUSCH, support two SRI fields corresponding to two SRS resource sets are included in DCI formats 0\_1/0\_2. * FFS: Details of the two SRI fields interpretations for codebook based and non-codebook based schemes, respectively. |
| QC | Support the FL proposal.  We do not think dynamic switching aspects should be separate from this proposal. |
| LG | It seems better to compare SRI field design in terms of payload size and dynamic STRP/MTRP switching flexibility. So, we would like to share Table below. Please feel free to correct it, if I made a mistake. Please feel free to add new SRI field design and payload if you have in mind. We can use this table to make a decision. Note that even though we see the need of max rank restriction, we consider all rank for analysis. Also, we assume the same Nsrs for two TRP for initial analysis.   * A single joint field supports STRP/MTRP dynamic switching and assumes same rank restriction between MTRP PUSCHs. * Two SRI field design 1 supports STRP/MTRP dynamic switching by using reserved codepoint (or new codepoint if there is no reserved codepoint, which is marked with ‘\*’). * Two SRI field design 2 does not supports STRP/MTRP dynamic switching but rank information is excluded in 2nd SRI field considering same rank restriction between MTRP PUSCHs.  |  |  |  |  | | --- | --- | --- | --- | | SRI field design  (Non-CB) | A single joint field | Two SRI field design 1 | Two SRI field design 2 | | Lmax=1, Nsrs=1 | 2bit:  2 codepoints for STRP  1 codepoints for MTRP | 1+1=2bit\*  for STRP/MTRP | 0bit  Only for MTRP | | Lmax=1, Nsrs=2 | 3bit:  4 codepoints for STRP  4 codepoints for MTRP | 2+2=4bit\* | 1+1=2bit | | Lmax=1, Nsrs=3 | 4bit:  6 codepoints for STRP  9 codepoints for MTRP | 2+2=4bit | 2+2=4bit | | Lmax=1, Nsrs=4 | 5bit:  8 codepoints for STRP  16 codepoints for MTRP | 3+3=6bit\* | 2+2=4bit | | Lmax=2, Nsrs=1 | 2bit:  2 codepoints for STRP  1 codepoints for MTRP | 1+1=2bit\*  for STRP/MTRP | 0bit  Only for MTRP | | Lmax=2, Nsrs=2 | 4bit:  6 codepoints for STRP  4 codepoints for rank 1+1 MTRP  1 codepoints for rank 2+2 MTRP | 2+2=4bit | 2+1=3bit | | Lmax=2, Nsrs=3 | 5bit:  12 codepoints for STRP  9 codepoints for rank 1+1 MTRP  9 codepoints for rank 2+2 MTRP | 3+3=6bit | 3+2=5bit | | Lmax=2, Nsrs=4 | 7bit:  20 codepoints for STRP  16 codepoints for rank 1+1 MTRP  36 codepoints for rank 2+2 MTRP | 4+4=8bit | 4+3=7bit | | Lmax=3, Nsrs=1 | 2bit:  2 codepoints for STRP  1 codepoints for MTRP | 1+1=2bit\*  for STRP/MTRP | 0bit  Only for MTRP | | Lmax=3, Nsrs=2 | 4bit:  6 codepoints for STRP  4 codepoints for rank 1+1 MTRP  1 codepoints for rank 2+2 MTRP | 2+2=4bit | 2+1=3bit | | Lmax=3, Nsrs=3 | 6bit:  14 codepoints for STRP  9 codepoints for rank 1+1 MTRP  9 codepoints for rank 2+2 MTRP  1 codepoints for rank 3+3 MTRP | 3+3=6bit | 3+2=5bit | | Lmax=3, Nsrs=4 | 7bit:  28 codepoints for STRP  16 codepoints for rank 1+1 MTRP  36 codepoints for rank 2+2 MTRP  16 codepoints for rank 3+3 MTRP | 4+4=8bit | 4+3=7bit | | Lmax=4, Nsrs=1 | 2bit:  2 codepoints for STRP  1 codepoints for MTRP | 1+1=2bit\*  for STRP/MTRP | 0bit  Only for MTRP | | Lmax=4, Nsrs=2 | 4bit:  6 codepoints for STRP  4 codepoints for rank 1+1 MTRP  1 codepoints for rank 2+2 MTRP | 2+2=4bit | 2+1=3bit | | Lmax=4, Nsrs=3 | 6bit:  14 codepoints for STRP  9 codepoints for rank 1+1 MTRP  9 codepoints for rank 2+2 MTRP  1 codepoints for rank 3+3 MTRP | 3+3=6bit | 3+2=5bit | | Lmax=4, Nsrs=4 | 7bit:  30 codepoints for STRP  16 codepoints for rank 1+1 MTRP  36 codepoints for rank 2+2 MTRP  16 codepoints for rank 3+3 MTRP  1 codepoints for rank 4+4 MTRP | 4+4=8bit | 4+3=7bit |  |  |  |  |  | | --- | --- | --- | --- | | SRI field design  (CB) | A single joint field | Two SRI field design 1 | Other design | | Nsrs=1 | 2bit:  2 codepoints for STRP  1 codepoints for MTRP | 1+1=2bit\*:  for STRP/MTRP |  | | Nsrs=2 | 3bit:  4 codepoints for STRP  4 codepoints for MTRP | 2+2=4bit\* |  | | Nsrs=3 | 4bit:  6 codepoints for STRP  9 codepoints for MTRP | 2+2=4bit |  | | Nsrs=4 | 5bit:  8 codepoints for STRP  16 codepoints for MTRP | 3+3=6bit\* |  | |
| CATT | Support the updated proposal. |
| FL update #2 | ZTE/LG >> understand your concern and I do not say that is not the case. But the spec changes will be huge, and majority prefer otherwise. I tried to capture your concern as below.  As companies use reserved entry for dynamic switching indication, the interpretation can already describe for some extent. Reusing SRI fields may not always be the case when the field size is 1 bit. Tried to capture that scenario as well.  **Draft for offline] Proposal 3.1:** For single DCI based M-TRP PUSCH repetition schemes, in both codebook and non-codebook based PUSCH,   * Support two SRIs ~~fields~~ ~~(each field based on Rel-15/16 framework)~~ corresponding to two SRS resource sets are included in DCI formats 0\_1/0\_2.   + Working assumption: each SRI field indicating SRI per TRP, where the SRI field based on Rel-15/16 framework   + FFS : whether or not to support one enhanced SRI field indicating two SRIs instead of the working assumption * Support dynamic switching between multi-TRP and single-TRP operation by using ~~two~~ SRI fields (or field)   + For two SRI fields, dynamic switching is supported at least when there is a reserved entry for one SRI field.     - FFS: whether to support dynamic switching if the SRI fields does not have a reserved entry   FFS: further details of SRI field interpretations |
| OPPO | Support FL updated proposal |
| CMCC | We don’t support the updated proposal.  We have the same view with ZTE and LG. The SRI should be discussed separately for codebook based and non-codebook based PUSCH.  For codebook based PUSCH, two SRI fields could be supported with Rel-15/16 framework simply. However, for non-codebook based PUSCH, the SRI field size can be reduced assuming the same rank for two TRPs. Besides, we don’t support the working assumption in the first sub-bullet either. |
| NTT Docomo | We support the proposal. |
| ZTE | We suggest to **separately discuss CB and non-CB**.  **The first reason** is the functionality of SRI between CB and non-CB is different. For non-CB, SRI indicates the number layers and precoder, it seems like TPMI for CB.  **The second reason**, if we support each SRI field based on Rel-15/16 framework, there is no reserved entry in SRI at all for CB (each Rel-15, 0 bit for one resource in set and 1 bit for two resources in set). However, there maybe some reserved entries in SRI for non-CB.  **The third reason**, in Proposal 3.3, for codebook based PUSCH, the 2nd TPMI field is limited with same rank between MTRP PUSCHs due to the rank can be indicated by 1st TPMI field. Likewise, for non-codebook based PUSCH, the 2nd SRI field should be limited with same rank between MTRP PUSCHs due to the rank can be indicated by 1st SRI field. Therefore, for non-codebook based scheme, it makes no sense to assume that two SRI fields are based on Rel-15/16 framework (the second SRI is different from Rel-15/16 because of no rank).  For codebook based scheme, two SRI fields can be based on Rel-15/16 framework, because STRP/MTRP dynamic switching can be indicated by 2nd TPMI field for minimizing DCI overhead. For example, when only one SRS resource in two SRS resource sets simultaneous, due to two entries in 2nd TPMI field can be used to indicated these two SRSs towards two TRPs, there is no overhead is needed for two SRI field, which also means the DCI overhead is 0bit. Therefore, for codebook based scheme, the two SRI fields are based on Rel-15/16 framework as well as minimizing DCI overhead when indicating STRP/MTRP dynamic switching.   * Non-CB   For non-codebook based scheme, it makes no sense to assume that two SRI fields are based on Rel-15/16 framework as we elaborate above,and the 2nd SRI field should be limited with same rank between MTRP PUSCHs due to the rank can be indicated by 1st SRI field. In such case, two entries in the 2nd SRI field can be used to indicate STRP/MTRP dynamic switching without additional DCI overhead at all.  In the light of the above elaboration, we suggest:  **Draft for offline] Proposal 3.1:** For single DCI based M-TRP PUSCH repetition schemes, in non-codebook based PUSCH,   * Support two SRIs fields ~~(each field based on Rel-15/16 framework)~~ corresponding to two SRS resource sets are included in DCI formats 0\_1/0\_2.   + FFS : whether or not to support one enhanced SRI field indicating two SRIs instead of the working assumption * Support dynamic switching between multi-TRP and single-TRP operation by using ~~two~~ SRI fields (or field)   + For two SRI fields, dynamic switching is supported at least when there is a reserved entry for one SRI field.     - FFS: whether to support dynamic switching if the SRI fields does not have a reserved entry   FFS: further details of SRI field interpretations. Further analysis is needed from DCI overhead perspective.   * CB   For CB, the first TPMI is the same as Rel-15/16, the reserved entries in second TMI can be used for dynamic switching between STRP and MTRP as we explained in proposal 3.3.  For example, one SRS resource in each set, then 0 bits are needed for two SRI fields. The second TPMI entry 30, or 31 is used to select SRS resource set. Therefore, there is no need to increase SRI bits at all.    Thus, our proposed wording is  **Draft for offline] Proposal 3.1:** For single DCI based M-TRP PUSCH repetition schemes, in codebook based PUSCH,   * Support two SRIs fields (each field based on Rel-15/16 framework) corresponding to two SRS resource sets are included in DCI formats 0\_1/0\_2.   + FFS : whether or not to support one enhanced SRI field indicating two SRIs instead of the working assumption * Support dynamic switching between multi-TRP and single-TRP operation by using ~~two~~ SRI fields (or field) or TPMI field(s).   FFS: further details of SRI field interpretations. Further analysis is needed from DCI overhead perspective. |
| Apple | We are ok to discuss CB/NCN separately as ZTE suggested. It is true that SRI indication for CB/NCB has different functionalities. |
| Nokia/NSB | Support the proposal. |
| Futurewei | Support |
| Intel | We have similar view as LG/ZTE that there is no hurry to down-select in this meeting. It makes sense to list joint coding of 2 SRI fields as a valid option to minimize the DCI field width. |
| LG | We believe one filed and two field design finally achieve the same thing and we don’t think one has more spec impact that the other. The key is payload size. Based on our analysis, payload of one field is equal or smaller than two field design and provides full flexibility for STRP/MTRP switching. Even though our preference is one field, we are fine with listing both options can discuss further but not OK with making two field as working assumption. In addition, for the sub-bullets of the 2nd bullet, it is 2nd level detail, which can be discussed further if Alt 1 is agreed, and it is already captured in the last FFS. So, our proposed wording is  **Draft for offline] Proposal 3.1:** For single DCI based M-TRP PUSCH repetition schemes, in ~~both codebook and~~ non-codebook based PUSCH,   * Support two SRIs ~~fields~~ ~~(each field based on Rel-15/16 framework)~~ corresponding to two SRS resource sets are included in DCI formats 0\_1/0\_2.   + ~~Working assumption~~ Alt 1: each SRI field indicating SRI per TRP, where the SRI field based on Rel-15/16 framework   + ~~FFS : whether or not to support~~ Alt 2 : one enhanced SRI field indicating two SRIs ~~instead of the working assumption~~ * Support dynamic switching between multi-TRP and single-TRP operation by using ~~two~~ SRI fields ~~(~~or field~~)~~   + ~~For two SRI fields, dynamic switching is supported at least when there is a reserved entry for one SRI field.~~      - ~~FFS: whether to support dynamic switching if the SRI fields does not have a reserved entry~~   FFS: further details of SRI field interpretations  Question to ZTE: for non-CB, could you elaborate bit size of SRI field you have in mind by using Table we shared above. You mention that, with same rank restriction, two entries in the 2nd SRI field can be used to indicate STRP/MTRP dynamic switching, but there are several cases there is no reserved codepoint. Anyway, it will be helpful to check payload size of your design. Thank you. |
| MediaTek | Support |
| NEC | We share similar view with ZTE and Apple that CB and NCB can be separately discussed.  We are fine with the two proposals updated by ZTE. |
| Lenovo&MotM | Support |
| CMCC | We have a same option with ZTE and Apple. We could discuss CB and NCB separately since their different functionalities.  We are ok with the two updated proposals by ZTE. |
| OPPO | By going through all the discussion, we tend to agree ZTE’s view that codebook based and non-codebook based can be discussed separately since the DCI fields indicating the layer information are different for these two schemes.  Therefore, we can treat Proposal 3.3 and 3.3x and make some agreement(s). Then, Proposal 3.1 can be updated accordingly based on the output of Proposal 3.3 and 3.3x |
| Fujitsu | Support FL’s updated proposal. |
| NTT Docomo2 | Based on current discussion, we are also fine with ZTE’s suggestion to separate the discussion of CB and NCB. |
| Xiaomi | Support the proposal and prefer a clearer solution of two separate SRI fields. |
| Samsung | Support FL’s updated proposal. |
| ZTE | Support separate discussion for CB and NCB, and copy-paste our updated Proposal 3.1 as below for legibility.  **Draft for offline] Proposal 3.1:**   * For single DCI based M-TRP PUSCH repetition schemes, in non-codebook based PUSCH, * Support two SRIs fields ~~(each field based on Rel-15/16 framework)~~ corresponding to two SRS resource sets are included in DCI formats 0\_1/0\_2.   + FFS : whether or not to support one enhanced SRI field indicating two SRIs instead of the working assumption * Support dynamic switching between multi-TRP and single-TRP operation by using ~~two~~ SRI fields (or field)   + For two SRI fields, dynamic switching is supported at least when there is a reserved entry for one SRI field.     - FFS: whether to support dynamic switching if the SRI fields does not have a reserved entry   FFS: further details of SRI field interpretations. Further analysis is needed from DCI overhead perspective.   * For single DCI based M-TRP PUSCH repetition schemes, in codebook based PUSCH, * Support two SRIs fields (each field based on Rel-15/16 framework) corresponding to two SRS resource sets are included in DCI formats 0\_1/0\_2.   + FFS : whether or not to support one enhanced SRI field indicating two SRIs instead of the working assumption * Support dynamic switching between multi-TRP and single-TRP operation by using ~~two~~ SRI fields (or field) or TPMI field(s).   FFS: further details of SRI field interpretations. Further analysis is needed from DCI overhead perspective. |
| vivo | Before moving forward, we think we should firstly decide on the functionality and comparison metric for the field design including SRI and TPMI, etc.  At least we see following requirements for the DCI indication for both CB-based and non-CB-based MTRP PUSCH repetitions:   1. Dynamic switching between STRP and MTRP operation 2. Dynamic switching the order of TRPs (SRIs)   We have consensus on supporting the first requirement. For the second requirement, we can recall that it has been supported in Rel-16 MTRP PDSCH by configuring two TCI codepoint with swapping TCI state pairs. For UL, TRP ordering switching is also beneficial for scheduling flexibility. An example is given below:  The beam of the first TRP may not always be available for the first PUSCH repetition transmission. In this case, the first repetition can be scheduled to transmit towards the second TRP instead of waiting for the first beam to be valid to reduce the transmission latency. As shown in the following figure, TRP\_x is configured for UE1 as the first TRP while it is also configured for UE2 as the second TRP. If cyclic beam mapping pattern is configured for both UE1 and UE2, and same RX beam1 is required for TRP\_x to receive certain PUSCH repetitions from UE1 and UE2. In a), RX beam1 of TRP\_x will be occupied until the end of last PUSCH repetition, i.e., from slot n to n+3, because the TRP\_x has to receive the PUSCH repetitions from two UEs alternatively in different slots. Under this circumstance, TRP\_x cannot schedule a third UE with other Rx beams in any slots from n to n+3. If the scheduling DCI of UE2 dynamically indicates that TRP\_x is the first TRP that the first PUSCH repetition targeting to, TRP\_x is available to schedule other UEs at slot n+1 and n+3, which is shown in b).    a)    b)    Regarding SRI indication, we share similar view with LG. Therefore, we propose to modify LG’s proposal as:  **Draft for offline] Proposal 3.1:** For single DCI based M-TRP PUSCH repetition schemes, in both codebook and non-codebook based PUSCH,   * Support two SRIs ~~fields~~ ~~(each field based on Rel-15/16 framework)~~ corresponding to two SRS resource sets are included in DCI formats 0\_1/0\_2.   + ~~Working assumption~~ Alt 1: each SRI field indicating SRI per TRP, where the SRI field based on Rel-15/16 framework   + ~~FFS : whether or not to support~~ Alt 2 : one enhanced SRI field indicating two SRIs ~~instead of the working assumption~~ * Support dynamic switching between multi-TRP and single-TRP operation by using ~~two~~ SRI fields ~~(~~or field~~)~~ * Support dynamic switching the order of two TRPs.   + ~~For two SRI fields, dynamic switching is supported at least when there is a reserved entry for one SRI field.~~      - ~~FFS: whether to support dynamic switching if the SRI fields does not have a reserved entry~~   FFS: further details of SRI field interpretations |
| Huawei, HiSilicon | We share similar view with other that CB and NCB should be discussed separately, due to the difference of the functionality of SRI field for CB and NCB.  For CB, using one SRI field seems the most efficient way, with limited spec impact (the combination seems far less than NCB case). Therefore, we prefer the following modification based on ZTE’s modification:  **Draft for offline] Proposal 3.1:** For single DCI based M-TRP PUSCH repetition schemes, in codebook based PUSCH,   * Support two SRSs~~SRIs fields (each field based on Rel-15/16 framework)~~ corresponding to two SRS resource sets are included in DCI formats 0\_1/0\_2.   + FFS : whether or not to support one enhanced SRI field indicating two SRSs~~SRIs instead of the working assumption~~ * Support dynamic switching between multi-TRP and single-TRP operation by using ~~two~~ SRI fields ~~(~~or a single SRI field~~)~~ or TPMI field(s).   FFS: further details of SRI field interpretations. Further analysis is needed from DCI overhead perspective.  For NCB, to be simpler, same principle between the design of TPMI field and SRI field, such as the same rank, can be considered to reduce the DCI overhead. We can be fine with the ZTE’s or LG’s modification.  As we commented, the DCI overhead is very critical for PDCCH reliability. To me, it seems to make no sense to add too many bits under the name of reliability enhancement. And we should thoroughly evaluate the DCI overhead and spec impact of solutions before down-selections. |
| FL update #3 | Seems nothing going well here. Let me try to come-up with a plan for this. |

### Proposal 3.2

**[Draft for offline] Proposal 3.2:** For single DCI based M-TRP PUSCH repetition schemes, in both codebook and non-codebook based PUSCH, *maxRank* is not configured to be larger than 2.

Please comment preferred changes on the proposal below.

|  |  |
| --- | --- |
| **Company** | **Comments** |
| QC | If maxRank is restricted, then even when sTRP is scheduled (e.g. no repetition), we are always limited to rank 2. In our understanding, for repetition Type A, UE does not expect to be scheduled with more than rank 1 anyway. For repetition Type B, we do not see a strong need to limit the rank given that it was not limited in Rel. 16. |
| Huawei, HiSilicon | We don’t see the necessity of this proposal, as there are cases that large number of ranks can be used in multi-TRP cases. |
| Intel | The motivation is not clear, also agree with QC that current Type B repetition has no rank restriction |
| LG | Support FL proposal. High rank is need for eMBB not for URLLC and it may cause inter-layer interference and transmission power reduction per layer, which decreases reliability. Furthermore, max rank has an impact on DCI payload size such as PTRS field and SRI field. In order to minimize DCI overhead rank limitation is needed. Also, same rank restriction for each PUSCH TO is needed to simplify DCI field design for MTRP PUSCH.  **Proposal 3.2:** For single DCI based M-TRP PUSCH repetition schemes, in both codebook and non-codebook based PUSCH, *maxRank* is not configured to be larger than 2.  Rank for each PUSCH transmission occasion is the same. |
| Lenovo&MotM | Support. |
| Samsung | Support the proposal. Similarly to multi-TRP PDSCH repetition, rank restriction can be considered. |
| vivo | Support the FL’s proposal.  From the aspect of DCI payload size, this can reduce the TMPI field size. When a UE is scheduled a PUSCH repetition to a single TRP, rank can be relaxed to legacy way. |
| MediaTek | Support the proposal. |
| NTT Docomo | Similar view as QC. We don’t see the necessity of the restriction. |
| Apple | We failed to see the benefit. |
| Fujitsu | This proposal may not be necessary. |
| Ericsson | We agree with QC’s comments. We do not see the need to restrict the rank for repetition Type B. |
| NEC | Not support this proposal. |
| ZTE | Do NOT support this proposal.  Regarding PUSCH transmission rank, in Rel-16, RAN1 supported that the *maxRank* = 4 for PUSCH repetitions (both TypeA w/o DG and TypeB). For Rel-17 FeMIMO, it can not to be seen the logic to penalize enhanced PUSCH by disallowing it to enable higher transmission rank. Besides, higher rank can be used to obtain better spectrum efficiency, etc. On the other hand, some companies mentioned that limit transmission ran can be used for reducing DCI overhead of two SRIs/TPMIs field. In fact, it is in vain due to the overhead of non-codebook based SRIs indication and/or codebook based SRIs/TPMIs indication actually depends on the case of rank 1/2 instead of rank 3/4. Therefore, it makes no sense to limit maxrank = 2 for both codebook and non-codebook based scheme.  Besides, another issue about whether the number of transmission rank per TRP for non-codebook based scheme should be same need to be discussed and addressed. Echo our elaboration in Proposal 3.1, we suggest to change this proposal as below:  **[Draft for offline] Proposal 3.2:** For single DCI based M-TRP PUSCH repetition schemes, in both codebook and non-codebook based PUSCH, the transmission rank between two SRS resource sets should be same.*~~maxRank~~* ~~is not configured to be larger than 2.~~ |
| Xiaomi | Same view with Vivo, The restriction is for multi-TRP transmission only. |
| Spreadtrum | We do not support the proposal. The motivation of such restriction is unclear. |
| TCL | We agree with QC’s comments. |
| FL update#1 | As majority did not like to restrict the scenario for M-TRP, the proposal is not considered anymore. |

### Proposal 3.3

**[Draft for offline] Proposal 3.3:** For single DCI based M-TRP PUSCH repetition schemes, two TPMI fields are included in DCI formats 0\_1/0\_2.

* The first TPMI field uses the Rel-15/16 TPMI field design of DCI format 0\_1/0\_2
* The second TPMI field only indicates the second TPMI index.
  + FFS1: Details of second TPMI interpretation

Please comment preferred changes on the proposal below. Also, provide views for FFS.

|  |  |
| --- | --- |
| **Company** | **Comments** |
| QC | Support the proposal. Suggest to clarify that the number of layers for each repetition is determined from the first field. |
| Huawei, HiSilicon | As we commented on previous proposals, we have concern on the DCI payload size. By doubling the fields such as TPC, SRI, TPMI, the payload size will be increased by 9 bits (2 bits TPC, 2 bits SRI, and 5 bits TPMI). 9 bits increase in DCI size will significantly impact the reliability of PDCCH, which is contradicting the objection of WID. Therefore, it’s too early to agree on the proposal before estimation of the impact on the PDCCH reliability and possible reduction of DCI payload increase.  As for TPMI field, as pointed out by QC that the second TPMI field just indicate the TPMI with the same layer as the first TPMI field. However, this can save only small number of bits (e.g., 1 bit for Table 7.3.1.1.2-2), therefore, more discussion may be needed. |
| Intel | Do not support, we have concerns on DCI size as well, our proposal is to re-visit the precoder and layer information tables (PINL). Even some TPMIs provide minimum benefit for example, when the number of coherent ports is equal to the number of layers – these can be reduced. |
| LG | Support the proposal and comment from QC. |
| Lenovo&MotM | Support. |
| Samsung | Support the proposal. |
| vivo | One TPMI field with joint encoding is preferred. |
| MediaTek | Support the proposal |
| NTT Docomo | Support the proposal. |
| Apple | Support the proposal |
| Fujitsu | Support the proposal. |
| Ericsson | Support the proposal, but with the following comment:  In order to support dynamic switching between single-TRP and multi-TRP PUSCH, we think it is better to have the same design for the first and the second SRI fields. For instance, when PUSCH is scheduled towards only the 2nd TRP, it would be good to also indicate the number of layers for the PUSCH transmission to the 2nd TRP in addition to the TPMI. So we suggest the following modification:  **[Draft for offline] Proposal 3.3:** For single DCI based M-TRP PUSCH repetition schemes, two TPMI fields are included in DCI formats 0\_1/0\_2.   * The first and second TPMI fields use the Rel-15/16 TPMI field design of DCI format 0\_1/0\_2 |
| NEC | Support the proposal. |
| ZTE | Support this proposal.  Besides, we share the same view with QC that one clarification like “**the 1st TPMI field can be used to indicate the transmission rank for each repetition**” should be add into the first bullet.  **[Draft for offline] Proposal 3.3:** For single DCI based M-TRP PUSCH repetition schemes, two TPMI fields are included in DCI formats 0\_1/0\_2.   * The first TPMI field uses the Rel-15/16 TPMI field design and can be used to indicate the transmission rank for each repetition of DCI format 0\_1/0\_2 * The second TPMI field only indicates the second TPMI index.   + FFS1: Details of second TPMI interpretation |
| Xiaomi | Support the proposal |
| Fraunhofer IIS/HHI | Support the use of a single codepoint of the TPMI field to indicate two TPMIs |
| vivo2 | One TPMI field with joint encoding is preferred, which can at least save TPMI payload in some cases. It has been agreed in RAN1#103-e that same number of layers for both TRPs is supported hence it is straightforward to extend the TPMI table e.g. for 2Tx non-coherent subset as below, which saves 1 bit.   |  |  | | --- | --- | | Bit field mapped to index | *codebookSubset* = *nonCoherent* | | 0 | 1 layer per TRP: TRP1 TPMI=0，TRP2 TPMI=0 | | 1 | 1 layer per TRP: TRP1 TPMI=0，TRP2 TPMI=1 | | 2 | 1 layer per TRP: TRP1 TPMI=1，TRP2 TPMI=0 | | 3 | 1 layer per TRP: TRP1 TPMI=1，TRP2 TPMI=1 | | 4 | 2 layers per TRP: TRP1 TPMI=0，TRP2 TPMI=0 | | 5-7 | Reserved |   In addition, utilizing some limitations e.g. coherent character, size of codebook subset etc., MAC CE can down select some combinations to further reduce the bit width of the only TPMI field. |
| TCL | Support the proposal. |
| ZTE2 | Further elaboration of our solution about two separate TPMI fields to enable dynamic switching between STRP and MTRP.  Following table illustrate the 2nd TPMI field when PUSCH transmitted by 4 full-coherent ports, where the 1st TPMI field with 6 bits is the same as Rel-16.     * It is obvious that the DCI overhead of 2nd TPMI field is 5 bits, which means the total overhead of two separate TPMI fields is 6 + 5 = 11 bits. Furthermore, this 2nd TPMI field can be used to indicate dynamic switching between STR and MTRP without any DCI overhead increasing. when the index of 2nd TPMI field is 30 or 31, it means that PUSCH transmissions based on single-TRP operation, and the index of TPMI field 2 is 30 or 31 indicates that 1st TPMI field will be used for TRP1 or TRP 2 respectively to determine precoder matrix and transmission rank. When the index of 2nd TPMI field is any one of 0 to 27, it means that PUSCH transmission is based on multi-TRP operation, and TPMI field 1 and TPMI field 2 are used for TRP1 and TRP2, respectively. Besides, the method can be used to indicate SRI(s) for STRP or MTRP operations as well as further minimize DCI overhead. For example, when there is only one SRS resource in each SRS resource set in STR operation, the DCI overhead of two SRI fields is 0 bit, because the reserved entries 30 and 31 can be used to indicate the single SRI towards which one out of two TRPs. * As a contrast, when use one extended TPMI field for two TPMIs indication, the total number of all candidates in the extended TPMI field is 62 (legacy) + 28×28 (rank 1) + 22×22 (rank 2) + 7×7 (rank 3) + 5×5 (rank 4) = 1404, which means the DCI overhead of Alt 1 is 11 bits. Based on that, w.r.t the indication of dynamic switching, at least 2 additional bits are inevitably needed (1 bit for STRP or MTRP indication, 1 bit for one out two TRPs indication in STRP). Besides, such as the above case, list all the combinations in the spec will not only cause a terrible huge effort, but also lead to poor readability of the specifications. * As another contrast, some companies raised that to use one extended SRI field for two SRI indication as well as indicating dynamic switching. Echo the same example that one SRS resource in each SRS resource set in STR operation, the DCI overhead of the one extended SRI field is always 2 bits. It means up to 2 bits are mandatorily needed. Besides, as we mentioned before, due to the configured power control parameters are SRI-specific in current specs, how to indicate the mapping between PC parameters and SRIs in MTRP operation is unclear, which also will lead to more spec impacts.   For non-codebook based scheme, the same method can be used to two SRIs indication. Where the 1st SRI field is the same as Rel-16 and can indicate transmission rank, the 2nd SRI field is the part of 1st SRI field which have the same transmission rank. Likewise, two reserved entries can be used to indicate dynamic switching between STR and MTRP.  Generally speaking, the intentions of our solution to two separate TPMI/SRI fields for codebook based and non-codebook based schemes are that (1) enable dynamic switching between STR and MTRP and minimize the DCI overhead as much as possible, (2) adopt the unified design for both codebook and non-codebook based PUSCH, and (3) easily and intuitively configure the mapping between SRI and power control parameters of PUSCH with low spec impact, (4) guarantee the specs to be legibility and make the editorial effort as ease as possible in future.  Therefore, we believe that RAN1 should support to used two separate TPMI/SRI fields for such above benefits. |
| FL update#1 | Majority support the direction. And there is a suggestion to include rank of the transmission in the first TMPI field.  **[Draft for offline] Proposal 3.3:** For single DCI based M-TRP PUSCH repetition schemes, two TPMI fields are included in DCI formats 0\_1/0\_2.   * The first TPMI field uses the Rel-15/16 TPMI field design (which includes TPMI index and the number of layers) of DCI format 0\_1/0\_2 * The second TPMI field only indicates the second TPMI index. The same number of layers are applied as indicated in the first TPMI field.   + FFS1: Details of second TPMI interpretation |
| InterDigital | We support FL’s proposal. |
| Futurewei | Support the updated proposal. |
| Lenovo&MotM | Support the updated proposal. |
| ZTE | Support FL’s updated proposal. |
| QC | Support the FL’s updated proposal. |
| LG | Support FL’s updated proposal. We wonder if ZTE’s proposal on 2nd TPMI can apply all codebook since, in case of nonCoherent 2 Tx codebook, there is no reserved codepoint to be used for dynamic switching. |
| CATT | Support the updated proposal. |
| FL update #2 | No objections at least for now.  HW, Intel, E///, Vivo>> please check and confirm.  **[Draft for offline] Proposal 3.3:** For single DCI based M-TRP PUSCH repetition schemes, two TPMI fields are included in DCI formats 0\_1/0\_2.   * The first TPMI field uses the Rel-15/16 TPMI field design (which includes TPMI index and the number of layers) of DCI format 0\_1/0\_2 * The second TPMI field only indicates the second TPMI index. The same number of layers are applied as indicated in the first TPMI field.   + FFS1: Details of second TPMI interpretation |
| OPPO | Support FL’s updated proposal |
| CMCC | Support FL’s updated proposal. |
| NTT Docomo | We support the proposal. |
| ZTE | We support FL’s proposal.  Besides, for non-codebook based scheme, due to the precoder and rank are indicated by SRI field only, it is natural to use the same framework for two SRI fields in non-codebook based MTRP PUSCH scheme. More specifically, the The first SRI field uses the Rel-15/16 SRI field design (which includes TPMI index and the number of layers) of DCI format 0\_1/0\_2, the second SRI field only indicates the second SRS selection. The same number of layers are applied as indicated in the first TPMI field.  **Proposal 3.3x:** For single DCI based M-TRP PUSCH repetition schemes, two SRI fields are included in DCI formats 0\_1/0\_2 for non-CB based PUSCH.   * The first SRI field uses the Rel-15/16 SRI field design (which includes the number of layers R and SRS resource selection) of DCI format 0\_1/0\_2 * The second SRI field only selects R resources from the second SRS set. The same number of layers are applied as indicated in the first SRI field.   + FFS1: Details of second TPMI interpretation |
| Apple | I have realized there may be some editorial issues – we do not have TPMI field in R15. TRI and TPMI are jointly coded. Therefore we suggest the following changes:  **[Draft for offline] Proposal 3.3:** For single DCI based M-TRP PUSCH repetition schemes, one TPMI field is introduced in DCI formats 0\_1/0\_2.   * The introduced TPMI field only indicates the second TPMI index. The same number of layers are applied as indicated in the precoder and number of layers field.   + FFS1: Details of second TPMI interpretation |
| Nokia/NSB | Support the proposal. |
| Futurewei | Support |
| Intel | Same view as vivo, HW, joint indication of layer and 2 TPMIs should be considered, and further reduction of certain TPMIs that are not very beneficial can be eliminated (e.g. same number of layers and co-herent ports). |
| LG | Question to ZTE: We wonder if your proposal on 2nd TPMI can apply all codebook since, in case of nonCoherent 2 Tx codebook, there is no reserved codepoint to be used for dynamic switching. |
| MediaTek | Support |
| NEC | Support the updated FL proposal.  Besides, regarding non-codebook based PUSCH transmission, we share similar view with ZTE, and we are fine with Proposal 3.3x from ZTE (with FFS1: Details of second ~~TPMI~~ SRI interpretation) |
| Lenovo&MotM | Support. |
| CMCC | Support the updated FL proposal.  Also, we have a same option with ZTE for NCB, and the proposal 3.3x from ZTE is ok for us. |
| OPPO | For codebook-based PUSCH, support FL’s proposal  ZTE provided a new (i.e., Propossal 3.X) for the optimization of non-codebook based PUSCH. It is beneficial from the technical perspective. Thus, we also support Proposal 3.3s proposed by ZTE. We also agree with NEC’s correction. |
| Fujitsu | Support FL’s updated proposal in principle and also fine with the update by Apple. |
| NTT Docomo2 | Support FL’s proposal.  Regarding ZTE’s proposal of proposal3.x for NCB, we are OK to further discuss. Regarding the interpretation of 2nd SRI field for NCB, we think whether same number of SRS resources is applied for 2 SRI fields in NCB can be discussed and agreed first, similar as what we have for CB. |
| Xiaomi | Support the updated FL’s proposal |
| Samsung | Support the updated proposal. |
| LG | For Proposal 3.3x, we don’t support it since it requires more payload based on analysis.  For CB, we provides SRI bit size including ZTE’s proposal as well in the below table. Since dynamic switching can be done with 2nd PMI field based on ZTE’s proposal, SRI itself requires equal or smaller payload than other design. If 2nd TPMI field has more than 1 reserved codepoint, total payload size for 2nd PMI + 2nd SRI field based on ZTE’s proposal is equal or smaller than other design. Otherwise, it is equal, smaller, or larger than other design depending on Nsrs. We wonder if ZTE have the same understanding and double check the table.   * A single joint field supports STRP/MTRP dynamic switching and assumes same rank restriction between MTRP PUSCHs. * Two SRI field design 1 supports STRP/MTRP dynamic switching by using reserved codepoint (or new codepoint if there is no reserved codepoint, which is marked with ‘\*’). * Two SRI field design 2 from ZTE  |  |  |  |  | | --- | --- | --- | --- | | SRI field design  (CB) | A single joint field | Two SRI field design 1 | Two SRI field design 2 (by ZTE) | | Nsrs=1 | 2bit:  2 codepoints for STRP  1 codepoints for MTRP | 1+1=2bit\*:  for STRP/MTRP | 0 | | Nsrs=2 | 3bit:  4 codepoints for STRP  4 codepoints for MTRP | 2+2=4bit\* | 1+1=2 | | Nsrs=3 | 4bit:  6 codepoints for STRP  9 codepoints for MTRP | 2+2=4bit | 2+2=4 | | Nsrs=4 | 5bit:  8 codepoints for STRP  16 codepoints for MTRP | 3+3=6bit\* | 2+2=4 | | comments |  |  | 2nd TPMI field (without rank) can be increased by up to 1bit if the # of reserved PMI codepoint is less than 2, depending on FullpowerMode/codebookSubset/#of antenna port)  e.g. 2nd TPMI field has no or only one reserved codepoint when  4Tx and FullpowerMode1 and ( codebookSubset = partialAndNonCoherent or nonCoherent) or  2Tx and codebookSubset = nonCoherent | |
| ZTE | @LG, for clarification, Proposal 3.3x only targets to two SRI fields for **NCB PUSCH**. Please note there is not TPMI field for CB PUSCH and that’s why we propose to separate discuss CB and NCB in Proposal 3.1. Following reasons for supporting two SRI fields of NCB PUSCH.  **The first reason**, it is intuitive that DCI overhead can be always smaller than or equal to single joint SRI field. Here, we echo LG’s table as below for elaboration.   |  |  |  | | --- | --- | --- | | SRI field design**(NCB)** | A single joint field | Two separate SRI field design | | Lmax=1, Nsrs=2 | **4bit:**  4 codepoints for STRP  8 codepoints for MTRP | 1+2=**3bit:**  1st SRI filed: 2 SRIs  2nd SRI field: 2 SRIs and 2 entries for STRP/MTRP | | Lmax=1, Nsrs=3 | **5bit:**  6 codepoints for STRP  18 codepoints for MTRP | 2+3=**5bit:**  1st SRI filed: 3 SRIs  2nd SRI field: 3 SRIs and 2 entries for STRP/MTRP | | Lmax=1, Nsrs=4 | **6bit:**  8 codepoints for STRP  32 codepoints for MTRP | 2+3=**5bit:**  1st SRI filed: 4 SRIs  2nd SRI field: 4 SRIs and 2 entries for STRP/MTRP | | Lmax=2, Nsrs=2 | **5bit:**  6 codepoints for STRP  18 codepoints for MTRP | 2+3=5bit:  1st SRI filed: 3 SRIs  2nd SRI field: 3 SRIs and 2 entries for STRP/MTRP | | Lmax=2, Nsrs=3 | **7bit:**  12 codepoints for STRP  72 codepoints for MTRP | 3+3=6bit:  1st SRI filed: 6 SRIs  2nd SRI field: 6 SRIs and 2 entries for STRP/MTRP | | Lmax=2, Nsrs=4 | **8bit:**  20 codepoints for STRP  200 codepoints for MTRP | 4+4=8bit:  1st SRI filed: 10 SRIs  2nd SRI field: 10 SRIs and 2 entries for STRP/MTRP | | Lmax=3, Nsrs=2 | **5bit:**  6 codepoints for STRP  18 codepoints for MTRP | 2+3=5bit:  1st SRI filed: 3 SRIs  2nd SRI field: 3 SRIs and 2 entries for STRP/MTRP | | Lmax=3, Nsrs=3 | **7bit:**  14 codepoints for two STRP  98 codepoints for MTRP | 3+4=7bit:  1st SRI filed: 7 SRIs  2nd SRI field: 7 SRIs and 2 entries for STRP/MTRP | | Lmax=3, Nsrs=4 | **9bit:**  28 codepoints for STRP  392 codepoints for MTRP | 4+4=8bit:  1st SRI filed: 14 SRIs  2nd SRI field: 14 SRIs and 2 entries for STRP/MTRP | | Lmax=4, Nsrs=2 | **5bit:**  6 codepoints for STRP  18 codepoints for MTRP | 2+3=**5bit:**  1st SRI filed: 3 SRIs  2nd SRI field: 3 SRIs and 2 entries for STRP/MTRP | | Lmax=4, Nsrs=3 | **7bit:**  14 codepoints for STRP  98 codepoints for MTRP | 3+3=**6bit:**  1st SRI filed: 7 SRIs  2nd SRI field: 7 SRIs and 2 entries for STRP/MTRP | | Lmax=4, Nsrs=4 | **9bit:**  30 codepoints for STRP  450 codepoints for MTRP | 4+5=**9bit:**  1st SRI filed: 14 SRIs  2nd SRI field: 15 SRIs and 2 entries for STRP/MTRP | | Comments | [ZTE]: @LG, note that the mapping between SRIs and TRPs should be indicated for MTRP. |  |   **The second reason**, from the perspective of rank indication, in Rel-15/16, TPMI field is used for CB PUSCH and SRI field is used for NCB PUSCH. Therefore, the unified design for two TPMI fields for CB and two SRI fields for NCB is fulfilled.  **The third reason**, in Rel-15/16, the configured mapping between SRI and power control parameters are clear due to only one single SRI field used for one TRP. In Rel-17, when two SRI fields are used, the configured mapping is still clear, RAN1 just need to design the association between PC parameter sets and TRPs/SRS resource sets. However, if single joint SRI field is used, how to configure the mapping between SRI and PC parameters is unclear, which also will cause spec impact. @LG, could you please show the solution to indicate/configure the SRI\_PC parameters mapping here?  From the prospective of technology, two SRI fields is benefit for NCB PUSCH with the following reasons: (1) adopt the unified design for rank indication for both codebook and non-codebook based PUSCH, (2) enable dynamic switching between STR and MTRP and minimize the DCI overhead as much as possible, (3) easily and intuitively configure the mapping between SRI and power control parameters of PUSCH with low spec impact, and (4) guarantee the specs to be legibility and make the spec effort as ease as possible.  Therefore, we suggest to agree Proposal 3.3x as below (with one correction mentioned by companies).  **Proposal 3.3x:** For single DCI based M-TRP PUSCH repetition schemes, two SRI fields are included in DCI formats 0\_1/0\_2 for non-CB based PUSCH.   * The first SRI field uses the Rel-15/16 SRI field design (which includes the number of layers R and SRS resource selection) of DCI format 0\_1/0\_2 * The second SRI field only selects R resources from the second SRS set. The same number of layers are applied as indicated in the first SRI field.   + FFS1: Details of second SRI ~~TPMI~~ interpretation |
| vivo | We still have concerns on the overhead of two TPMI fields. To further reduce the overhead of DCI format 0\_1/0\_2, the only enhanced TPMI field which can save 1 bit in some cases. Besides, the two requirements mentioned in our vivo2’s comment should be satisfied in SRI field and TPMI field design. |
| Huawei, HiSilicon | We can accept the updated proposal if it is majority view. However, we prefer to consider further overhead reduction mechanism as mentioned by Intel and vivo. So we suggest to add FFS to the proposal:  FFS: overhead reduction methods for TPMI indication. |
| FL update #3 | Same as proposal 3.1, there seems to be concerns. Will provide my update soon. |
| vivo | @ZTE: it seems in your table, the SRI bit size doesn’t remove the entries of SRIs for the 2nd TRP whose ranks are different from that of the 1st TRP neither for a single joint field nor separate SRI fields.  As it has been agreed that the same number of layers are applied for both TPMIs if two TPMIs are indicated, we recalculate the bit size for both designs.  Referring the two requirements in our previous comment in Proposal 3.1, if the SRI field(s) only support dynamic switching between STRP and MTRP operation, but dynamic switching the order of TRPs (SRIs) is not supported, the bit size are updated in the following table.   |  |  |  | | --- | --- | --- | | SRI field design**(NCB)** | A single joint field | Two separate SRI field design | | Lmax=1, Nsrs=2 | **3bit:**  4 codepoints for STRP  4 codepoints for MTRP | 1+2=**3bit:**  1st SRI filed: 2 SRIs  2nd SRI field: 2 SRIs and 2 entries for STRP/MTRP | | Lmax=1, Nsrs=3 | **5bit:**  6 codepoints for STRP  9 codepoints for MTRP | 2+3=**5bit:**  1st SRI filed: 3 SRIs  2nd SRI field: 3 SRIs and 2 entries for STRP/MTRP | | Lmax=1, Nsrs=4 | **5bit:**  8 codepoints for STRP  16 codepoints for MTRP | 2+3=**5bit:**  1st SRI filed: 4 SRIs  2nd SRI field: 4 SRIs and 2 entries for STRP/MTRP | | Lmax=2, Nsrs=2 | **4bit:**  6 codepoints for STRP  5 codepoints for MTRP | 2+2=4bit:  1st SRI filed: 3 SRIs  2nd SRI field: 2 SRIs and 2 entries for STRP/MTRP | | Lmax=2, Nsrs=3 | **6bit:**  12 codepoints for STRP  18 codepoints for MTRP | 3+3=6bit:  1st SRI filed: 6 SRIs  2nd SRI field: 3 SRIs and 2 entries for STRP/MTRP | | Lmax=2, Nsrs=4 | **7bit:**  20 codepoints for STRP  52 codepoints for MTRP | 4+3=7bit:  1st SRI filed: 10 SRIs  2nd SRI field: 6 SRIs and 2 entries for STRP/MTRP | | Lmax=3, Nsrs=2 | **4bit:**  6 codepoints for STRP  5 codepoints for MTRP | 2+2=4bit:  1st SRI filed: 3 SRIs  2nd SRI field: 2 SRIs and 2 entries for STRP/MTRP | | Lmax=3, Nsrs=3 | **6bit:**  14 codepoints for two STRP  19 codepoints for MTRP | 3+3=6bit:  1st SRI filed: 7 SRIs  2nd SRI field: 3 SRIs and 2 entries for STRP/MTRP | | Lmax=3, Nsrs=4 | **7bit:**  28 codepoints for STRP  68 codepoints for MTRP | 4+3=7bit:  1st SRI filed: 14 SRIs  2nd SRI field: 6 SRIs and 2 entries for STRP/MTRP | | Lmax=4, Nsrs=2 | **4bit:**  6 codepoints for STRP  5 codepoints for MTRP | 2+2=**4bit:**  1st SRI filed: 3 SRIs  2nd SRI field: 2 SRIs and 2 entries for STRP/MTRP | | Lmax=4, Nsrs=3 | **6bit:**  14 codepoints for STRP  20 codepoints for MTRP | 3+3=**6bit:**  1st SRI filed: 7 SRIs  2nd SRI field: 3 SRIs and 2 entries for STRP/MTRP | | Lmax=4, Nsrs=4 | **7bit:**  30 codepoints for STRP  69 codepoints for MTRP | 4+3=**7bit:**  1st SRI filed: 14 SRIs  2nd SRI field: 6 SRIs and 2 entries for STRP/MTRP | | Comments | [ZTE]: @LG, note that the mapping between SRIs and TRPs should be indicated for MTRP. |  |     Furthermore, if the SRI field support both requirements, i.e., SRI field(s) is able to indicate dynamic switching between STRP and MTRP operation, and dynamic switching the order of TRPs (SRIs), the bit size are given in the following table which is quoted from our Tdoc. |
| ZTE | @vivo:  please note our comment inline the table that the mappings between SRI and TRP are included in MTRP cases. For example, {Lmax=1, Nsrs=3} highlighted by you, for MTRP it should be 3x3x2=18 with 5bits overhead, due to opposite orders for two SRS(s) which come from two SRS resource sets, respectively. For another example, {Lmax=2, Nsrs=3} highlighted by you, it should be 3x3x2+3x3x3=36 with 6bits overhead, same as the opposite orders for two SRS(s) which come from two SRS resource sets, respectively. Otherwise, please shown your solution for single joint SRI field in MTRP as well as indicate the mapping between SRS selection and TRPs.  Besides, the same question to you that how to configure/indicate the mapping between SRI and PC parameter sets in your mind? |
| LG | @ZTE:  Thanks for the sharing Table for NCB. We have some comments and questions.   * We need SRI field for Lmax=1,2,3,4 and Nsrs=1, which is excluded in the Table you shared, since STRP/MTRP switching needs to be supported by SRI field. * Same rank restriction should be applied in a single joint field but it seems not applied in the Table you shared * We don’t see a strong need of switching the order of the two TRPs for MTRP transmission but it seems to be counted in a single joint field in the Table you shared. If my understanding is correct, two SRI field design does not support switching the order of the two TRPs as well since SRI field 1 and 2 are used for TRP 1 and 2 in case of MTRP tranmission, respectively. * Considering above 2nd and 3rd bullet, payload for single field is revised in red.  |  |  |  | | --- | --- | --- | | SRI field design**(NCB)** | A single joint field | Two separate SRI field design | | Lmax=1, Nsrs=1 | 2bit:  2 codepoints for STRP  1 codepoints for MTRP |  | | Lmax=1, Nsrs=2 | 3bit:  4 codepoints for STRP  4 codepoints for MTRP | 1+2=**3bit:**  1st SRI filed: 2 SRIs  2nd SRI field: 2 SRIs and 2 entries for STRP/MTRP | | Lmax=1, Nsrs=3 | 4bit:  6 codepoints for STRP  9 codepoints for MTRP | 2+3=**5bit:**  1st SRI filed: 3 SRIs  2nd SRI field: 3 SRIs and 2 entries for STRP/MTRP | | Lmax=1, Nsrs=4 | 5bit:  8 codepoints for STRP  16 codepoints for MTRP | 2+3=**5bit:**  1st SRI filed: 4 SRIs  2nd SRI field: 4 SRIs and 2 entries for STRP/MTRP | | Lmax=2, Nsrs=1 | 2bit:  2 codepoints for STRP  1 codepoints for MTRP |  | | Lmax=2, Nsrs=2 | 4bit:  6 codepoints for STRP  4 codepoints for rank 1+1 MTRP  1 codepoints for rank 2+2 MTRP | 2+3=5bit:  1st SRI filed: 3 SRIs  2nd SRI field: 3 SRIs and 2 entries for STRP/MTRP | | Lmax=2, Nsrs=3 | 5bit:  12 codepoints for STRP  9 codepoints for rank 1+1 MTRP  9 codepoints for rank 2+2 MTRP | 3+3=6bit:  1st SRI filed: 6 SRIs  2nd SRI field: 6 SRIs and 2 entries for STRP/MTRP | | Lmax=2, Nsrs=4 | 7bit:  20 codepoints for STRP  16 codepoints for rank 1+1 MTRP  36 codepoints for rank 2+2 MTRP | 4+4=8bit:  1st SRI filed: 10 SRIs  2nd SRI field: 10 SRIs and 2 entries for STRP/MTRP | | Lmax=3, Nsrs=1 | 2bit:  2 codepoints for STRP  1 codepoints for MTRP |  | | Lmax=3, Nsrs=2 | 4bit:  6 codepoints for STRP  4 codepoints for rank 1+1 MTRP  1 codepoints for rank 2+2 MTRP | 2+3=5bit:  1st SRI filed: 3 SRIs  2nd SRI field: 3 SRIs and 2 entries for STRP/MTRP | | Lmax=3, Nsrs=3 | 6bit:  14 codepoints for STRP  9 codepoints for rank 1+1 MTRP  9 codepoints for rank 2+2 MTRP  1 codepoints for rank 3+3 MTRP | 3+4=7bit:  1st SRI filed: 7 SRIs  2nd SRI field: 7 SRIs and 2 entries for STRP/MTRP | | Lmax=3, Nsrs=4 | 7bit:  28 codepoints for STRP  16 codepoints for rank 1+1 MTRP  36 codepoints for rank 2+2 MTRP  16 codepoints for rank 3+3 MTRP | 4+4=8bit:  1st SRI filed: 14 SRIs  2nd SRI field: 14 SRIs and 2 entries for STRP/MTRP | | Lmax=4, Nsrs=1 | 2bit:  2 codepoints for STRP  1 codepoints for MTRP |  | | Lmax=4, Nsrs=2 | 4bit:  6 codepoints for STRP  4 codepoints for rank 1+1 MTRP  1 codepoints for rank 2+2 MTRP | 2+3=**5bit:**  1st SRI filed: 3 SRIs  2nd SRI field: 3 SRIs and 2 entries for STRP/MTRP | | Lmax=4, Nsrs=3 | 6bit:  14 codepoints for STRP  9 codepoints for rank 1+1 MTRP  9 codepoints for rank 2+2 MTRP  1 codepoints for rank 3+3 MTRP | 3+3=**6bit:**  1st SRI filed: 7 SRIs  2nd SRI field: 7 SRIs and 2 entries for STRP/MTRP | | Lmax=4, Nsrs=4 | 7bit:  30 codepoints for STRP  16 codepoints for rank 1+1 MTRP  36 codepoints for rank 2+2 MTRP  16 codepoints for rank 3+3 MTRP  1 codepoints for rank 4+4 MTRP | 4+5=**9bit:**  1st SRI filed: 14 SRIs  2nd SRI field: 15 SRIs and 2 entries for STRP/MTRP |   Regarding ZTE’s question on PC mapping for single SRI field, there can be several approach. If we add second sri-PUSCH-PathlossReferenceRS-Id/sri-P0-PUSCH-AlphaSetId/sri-PUSCH-ClosedLoopIndex in SRI-PUSCH-PowerControl as mentioned by NTT, SRI codepoint indicating MTRP is mapped to first PC set and second PC set of corresponding SRI-PUSCH-PowerControl.  @ VIVO:  Thanks for sharing Table. Isn’t it 4 bit for 15 codepoints for Lmax=1, Nsrs=3? we have similar question for other entries as well. |

### Proposal 3.4

**[Draft for offline] Proposal 3.4:** For single DCI based M-TRP PUSCH repetition schemes, the number of bits for the indication of PTRS-DMRS association is the same as Rel-15/16.

* For maxRank = 2, MSB and LSB separately indicating the association between PTRS port and DMRS port for two TRPs.
* FFS: Interpretation for other scenarios (if maxRank >2 is agreed).

Please comment preferred changes on the proposal below. Also, provide views for FFS.

|  |  |
| --- | --- |
| **Company** | **Comments** |
| QC | Support the proposal. Furthermore, we would like to point out that the proposal is only needed for repetition Type B since max number of layers is 1 for repetition Type A. |
| Huawei, HiSilicon | This proposal may depends on the discussion of proposal 3.2, prefer to discuss proposal 3.2 firstly. |
| Intel | We are supportive of the intent here but may be better to discuss this after 3.2 resolution (at least the sub-bullets are not preferable) |
| LG | Support the proposal. |
| Samsung | PTRS-DMRS association field can be interpreted differently whether maxRank = 2 or larger than 2. So, support the main proposal but suggest to discuss this issue later. |
| Vivo | Support the main proposal. The second sub-bullet is not preferable. |
| MediaTek | The main proposal is agreeable but the sub-bullets can be discussed after Proposal 3.2. |
| NTT Docomo | Support the proposal. |
| Apple | We think PT-RS port cycling is better since for reliability enhancement gNB may not have clear understanding which layer is the best. |
| Fujitsu | Support the proposal. |
| Ericsson | Support the proposal. We also agree with QC that the proposal is only needed for PUSCH repetition Type B, as PUSCH repetition Type A is limited to a single layer in current specifications. |
| ZTE | Support this proposal.  Likely, as we elaborate in Proposal 3.2, we do NOT agree any limitation of *maxRank* in this item. More specially, in Rel-16, only DG based PUSCH repetition A has the limitation that *maxRank* = 1.  Regarding the case of *maxRank* > 2 in FFS, our intention is that to enable PTRS-DMRS indication for MTRP operation as well as without any DCI overhead increasing, which is suitable to any case based on the current TS 38.212. |
| Xiaomi | Support the proposal, this relates to 3.2. |
| Spreadtrum | We prefer to postpone the discussion after the discussion of Proposal 3.2. |
| TCL | Support the proposal. |
| FL update#1 | Majority agrees with the proposal. As QC, E/// suggested, this only applies to Type B repetition.  **[Draft for offline] Proposal 3.4:** For single DCI based M-TRP PUSCH Type B repetition schemes, the number of bits for the indication of PTRS-DMRS association is the same as Rel-15/16.   * For maxRank = 2, MSB and LSB separately indicating the association between PTRS port and DMRS port for two TRPs. * FFS: Interpretation for other scenarios (if maxRank >2 is agreed). |
| InterDigital | We support FL’s proposal. |
| Futurewei | Support the updated proposal. |
| ZTE | We prefer the previous version of this proposal.  As we mentioned above, in Rel-16, only PUSCH repetition A based on dynamic scheduling has the limitation that *maxRank* = 1. Out of the serious consideration, we think the added wording “Type B” is NOT needed. |
| QC | Support the proposal. |
| LG | We would like to remove the last bullet point. Rank >2 for URLLC is useless and degrades reliability due to interlayer interference and per layer power reduction and it also increase PTRS field size. |
| CATT | Support the updated proposal. |
| FL update#2 | Based on ZTE suggestion, Type B is removed. That is seems redundant if Type A anyways cannot use maxRank = 2.  LG>> We did not make the agreement for rank to be limited. So, we could keep the FFS.  **[Draft for offline] Proposal 3.4:** For single DCI based M-TRP PUSCH ~~Type B~~ repetition schemes, the number of bits for the indication of PTRS-DMRS association is the same as Rel-15/16.   * For maxRank = 2, MSB and LSB separately indicating the association between PTRS port and DMRS port for two TRPs. * FFS: Interpretation for other scenarios (if maxRank >2 is agreed). |
| OPPO | Support FL updated#1, but can also live with FL updated#2 |
| NTT Docomo | We support the proposal. |
| Apple | We do we treat maxRank=2 specially? |
| Nokia/NSB | Support the proposal |
| Futurewei | Support |
| Intel | We prefer to not have the sub-bullets. |
| MediaTek | Support |
| NEC | Support the proposal. |
| Fujitsu | Support the updated proposal. |
| Xiaomi | Support the proposal if3.2 is confirmed |
| Samsung | We think that the maximum number of PTRS ports is also considered for the enhancement. So, we suggest the following updated proposal:  **[Draft for offline] Proposal 3.4:** For single DCI based M-TRP PUSCH ~~Type B~~ repetition schemes, the number of bits for the indication of PTRS-DMRS association is the same as Rel-15/16.   * For maxRank = 2, MSB and LSB separately indicating the association between PTRS port and DMRS port for two TRPs.   FFS: Interpretation for other scenarios (if maxRank >2 is agreed).  FFS: how to interpret PTRS-DMRS association according to the number of PTRS ports (if maxNrofPorts =1 or 2) |
| ZTE | Support FL’s proposal in principle.  In Rel-16, when maxRank = 1, the indication of PTRS-DMRS association is NOT needed. We suggest change the wording “maxRank” to “rank” in Proposal. Besides, “(if maxRank >2 is agreed)” in FFS is NOT needed due to the first bullet is agreed when Proposal 3.4 is endorsed. We suggest:  **[Draft for offline] Proposal 3.4:** For single DCI based M-TRP PUSCH ~~Type B~~ repetition schemes, the number of bits for the indication of PTRS-DMRS association is the same as Rel-15/16.   * For ~~maxR~~rank = 2, MSB and LSB separately indicating the association between PTRS port and DMRS port for two TRPs.   FFS: The method of rank > 2.~~Interpretation for other scenarios (if maxRank >2 is agreed).~~ |
| vivo | Now that the discussion on limitation of max rank is removed, the second bullet shall be updated. And from our side, 2 bits are not enough to indicate PTRS-DMRS association for both TRPs when maxRank>2. Considering the case that maxRank is configured to 4 and number of PTRS ports is configured to 2, at least 4 bits are required with the following interpretation:   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **value** | **TRP1** | | **TRP2** | | | **The 1st bit** | **The 2nd bit** | **The third bit** | **The fourth bit** | | **PTRS port0** | **PTRS port1** | **PTRS port0** | **PTRS port1** | | 0 | 1st DMRS port | 1st DMRS port | 1st DMRS port | 1st DMRS port | | 1 | 2nd DMRS port | 2nd DMRS port | 2nd DMRS port | 2nd DMRS port |   Hence, we suggest to modify the proposal as follows:  **[Draft for offline] Proposal 3.4:** For single DCI based M-TRP PUSCH ~~Type B~~ repetition schemes, ~~the number of bits for the indication of PTRS-DMRS association is the same as Rel-15/16.~~   * For maxRank = 2, the number of bits for the indication of PTRS-DMRS association is the same as Rel-15/16, MSB and LSB separately indicating the association between PTRS port and DMRS port for two TRPs. * ~~FFS: Interpretation for other scenarios (if maxRank >2 is agreed).~~   FFS: the indication of PTRS-DMRS association for maxRank >2. |
| FL update #3 | Three different suggestions from Vivo, ZTE, SS, but it seems others are ok.  SS>> the FFS added by you already solved for maxrank = 2 by MSB and LSB separately indicating the association between PTRS port and DMRS port for two TRPs”. For other scenarios, FFS can discuss that and not require any more clairifcation.  ZTE>> Tables in 38.212 are defined for *maxRank*, so using that is ok. However, it is ok to delete “(if maxrank > 2 is agreed)”  Vivo >> changes on wording does not change the thing we try to agree here.  Apple >> yes, this is maxRank= 2, as other cases are not aligned between companies.  **Proposal 3.4:** For single DCI based M-TRP PUSCH repetition schemes, the number of bits for the indication of PTRS-DMRS association is the same as Rel-15/16.   * For maxRank = 2, MSB and LSB separately indicating the association between PTRS port and DMRS port for two TRPs. * FFS: Interpretation for other scenarios ~~(if maxRank >2 is agreed).~~ |
| ZTE | @FL, please note that our intention to change “maxRank” to “rank” just for avoiding ambiguity. For the sake of clarification and progress, the wording “maxRank > 2” is needed in FFS for explain what is the “other scenarios”.  **Proposal 3.4:** For single DCI based M-TRP PUSCH repetition schemes, the number of bits for the indication of PTRS-DMRS association is the same as Rel-15/16.   * For maxRank = 2, MSB and LSB separately indicating the association between PTRS port and DMRS port for two TRPs.   FFS: Interpretation for other scenarios when maxRank > 2. ~~(if maxRank >2 is agreed).~~ |

### Proposal 3.5

**[Draft for offline] Proposal 3.5:** For single-DCI based M-TRP PUSCH repetition schemes, up to two power control parameter sets (using *SRI-PUSCH-PowerControl*) can be applied when two SRI fields are included in DCI format 0\_1/0\_2.

* FFS1: Details on linking SRI fields to two power control parameters,
  + Alt. 1: Add second *sri-PUSCH-MappingToAddModList,* andselect two *SRI-PUSCH-PowerControl* from two *sri-PUSCH-MappingToAddModList*
  + Alt. 2: Add SRS resource set ID in *SRI-PUSCH-PowerControl,* and select *SRI-PUSCH-PowerControl* from *sri-PUSCH-MappingToAddModList* considering the SRS resource set ID
  + Alt. 3: Let RAN2 handle this
  + Alt. 4: …
* FFS2: Enhancements on open-loop power control parameter set indication
* FFS3: Consideration on *srs-PowerControlAdjustmentStates*
* FFS4: Impact of multi-TRP PUSCH repetition on PHR reporting

Please comment preferred changes on the proposal below. Also, provide views for FFS.

|  |  |
| --- | --- |
| **Company** | **Comments** |
| QC | Support the proposal. For FFS1, we prefer Alt2, which has smaller RRC overhead and less surgery on the existing structure. We think this may not be only a RAN2 issue. |
| Huawei, HiSilicon | We have not agreed on the SRI fields, therefore, we propose the following modification:  **[Draft for offline] Proposal 3.5:** For single-DCI based M-TRP PUSCH repetition schemes, up to two power control parameter sets (using *SRI-PUSCH-PowerControl*) can be applied when SRS resources from two SRS resource sets ~~two SRI fields~~ are ~~included~~indicated in DCI format 0\_1/0\_2.   * FFS1: Details on linking SRI fields to two power control parameters,   + Alt. 1: Add second *sri-PUSCH-MappingToAddModList,* andselect two *SRI-PUSCH-PowerControl* from two *sri-PUSCH-MappingToAddModList*   + Alt. 2: Add SRS resource set ID in *SRI-PUSCH-PowerControl,* and select *SRI-PUSCH-PowerControl* from *sri-PUSCH-MappingToAddModList* considering the SRS resource set ID   + Alt. 3: Let RAN2 handle this   + Alt. 4: … * FFS2: Enhancements on open-loop power control parameter set indication * FFS3: Consideration on *srs-PowerControlAdjustmentStates* * FFS4: Impact of multi-TRP PUSCH repetition on PHR reporting |
| Intel | Slightly prefer modification from Huawei |
| LG | Support Huawei’s revision. |
| Lenovo&MotM | Support Alt 1. |
| Samsung | This proposal is depending on the proposal 3.1. As the method to indicate two SRI for multi-TRP, details on FFS1 can be discussed. So, FFS1 should be discussed after the proposal 3.1 and details depending on indication method of two SRI values can be studied further. |
| vivo | Agree with Huawei’s comments. |
| MediaTek | We support Huawei’s revision. |
| NTT Docomo | Support the proposal. For FFS1, we think another alternative can be   * Alt.4. Add second sri-PUSCH-PathlossReferenceRS-Id/sri-P0-PUSCH-AlphaSetId/sri-PUSCH-ClosedLoopIndex in SRI-PUSCH-PowerControl. |
| Apple | Support in principle |
| Fujitsu | Support the revision from HW. |
| Ericsson | We support the proposal. On FFS1, we prefer Alt. 3 as the details on how to link the two SRI fields to the two power control parameters can be left to RAN2 to handle. |
| NEC | Support the proposal. |
| ZTE | Support this proposal in principle.  Regarding FFS1, our preference is Alt 2.  Besides, when the SRI(s) of any one out of two SRS resource set is absent, one issue is that the set(s) of power control parameters towards the specific TRP should be clarified. Thus, we add one FFS in this proposal as below:  **[Draft for offline] Proposal 3.5:** For single-DCI based M-TRP PUSCH repetition schemes, up to two power control parameter sets (using *SRI-PUSCH-PowerControl*) can be applied when two SRI fields are included in DCI format 0\_1/0\_2.   * FFS1: Details on linking SRI fields to two power control parameters,   + Alt. 1: Add second *sri-PUSCH-MappingToAddModList,* andselect two *SRI-PUSCH-PowerControl* from two *sri-PUSCH-MappingToAddModList*   + Alt. 2: Add SRS resource set ID in *SRI-PUSCH-PowerControl,* and select *SRI-PUSCH-PowerControl* from *sri-PUSCH-MappingToAddModList* considering the SRS resource set ID   + Alt. 3: Let RAN2 handle this   + Alt. 4: … * FFS2: Enhancements on open-loop power control parameter set indication * FFS3: Consideration on *srs-PowerControlAdjustmentStates* * FFS4: Impact of multi-TRP PUSCH repetition on PHR reporting * FFS5: Enhancement on power control parameters per TRP when SRI(s) indication of two SRS resource sets is absent. |
| Xiaomi | Support in principle |
| TCL | Support the revision from HW. |
| FL update#1 | Majority supports this.  FL suggest to use the version updated by HW which make things general (as we do not have an agreement on two SRIs yet). Added also the ZTE suggested FFS.  **[Draft for offline] Proposal 3.5:** For single-DCI based M-TRP PUSCH repetition schemes, up to two power control parameter sets (using *SRI-PUSCH-PowerControl*) can be applied when SRS resources from two SRS resource sets ~~two SRI fields~~ are ~~included~~indicated in DCI format 0\_1/0\_2.   * FFS1: Details on linking SRI fields to two power control parameters,   + Alt. 1: Add second *sri-PUSCH-MappingToAddModList,* andselect two *SRI-PUSCH-PowerControl* from two *sri-PUSCH-MappingToAddModList*   + Alt. 2: Add SRS resource set ID in *SRI-PUSCH-PowerControl,* and select *SRI-PUSCH-PowerControl* from *sri-PUSCH-MappingToAddModList* considering the SRS resource set ID   + Alt. 3: Let RAN2 handle this   + Alt. 4: … * FFS2: Enhancements on open-loop power control parameter set indication * FFS3: Consideration on *srs-PowerControlAdjustmentStates* * FFS4: Impact of multi-TRP PUSCH repetition on PHR reporting * FFS5: Enhancement on power control parameters per TRP when SRI(s) indication of two SRS resource sets is absent. |
| InterDigital | We support FL’s proposal. |
| Futurewei | Support the updated proposal. |
| Lenovo&MotM | Support the updated proposal. |
| ZTE | OK with FL’s updated proposal. |
| QC | Support the proposal. |
| LG | OK with FL’s updated proposal. |
| CATT | Support the updated proposal. For FFS1, Alt.3 is preferred. |
| FL update#2 | I will make this offline agreement.  **Offline Agreement 3.5:** For single-DCI based M-TRP PUSCH repetition schemes, up to two power control parameter sets (using *SRI-PUSCH-PowerControl*) can be applied when SRS resources from two SRS resource sets ~~two SRI fields~~ are ~~included~~indicated in DCI format 0\_1/0\_2.   * FFS1: Details on linking SRI fields to two power control parameters,   + Alt. 1: Add second *sri-PUSCH-MappingToAddModList,* andselect two *SRI-PUSCH-PowerControl* from two *sri-PUSCH-MappingToAddModList*   + Alt. 2: Add SRS resource set ID in *SRI-PUSCH-PowerControl,* and select *SRI-PUSCH-PowerControl* from *sri-PUSCH-MappingToAddModList* considering the SRS resource set ID   + Alt. 3: Let RAN2 handle this * FFS2: Enhancements on open-loop power control parameter set indication * FFS3: Consideration on *srs-PowerControlAdjustmentStates* * FFS4: Impact of multi-TRP PUSCH repetition on PHR reporting * FFS5: Enhancement on power control parameters per TRP when SRI(s) indication of two SRS resource sets is absent. |
| OPPO | Support he updated proposal and prefer Alt.1 for FFS1 |
| NTT Docomo | Support  For FFS1, we think other alternatives can be considered, for example,   * Add second sri-PUSCH-PathlossReferenceRS-Id/sri-P0-PUSCH-AlphaSetId/sri-PUSCH-ClosedLoopIndex in SRI-PUSCH-PowerControl. |
| Apple | Support in principle. |
| Nokia/NSB | Support the proposal. |
| Futurewei | Support, and support Docomo’s example. |
| MediaTek | Support |
| NEC | Support the proposal. |
| Lenovo&MotM | Support |
| Fujitsu | Support the updated proposal. For FFS1, prefer Alt-3. |
| Xiaomi | Support, slightly prefer alt.2 for FFS1 which is simpler |
| Samsung | Support the updated proposal |
| ZTE | Support FL’s proposal. |
| vivo | Support |
| Huawei, HiSilicon | Support the updated proposal. |
| FL update#3 | Added DCM option.  **Offline Agreement 3.5:** For single-DCI based M-TRP PUSCH repetition schemes, up to two power control parameter sets (using *SRI-PUSCH-PowerControl*) can be applied when SRS resources from two SRS resource sets indicated in DCI format 0\_1/0\_2.   * FFS1: Details on linking SRI fields to two power control parameters,   + Alt. 1: Add second *sri-PUSCH-MappingToAddModList,* andselect two *SRI-PUSCH-PowerControl* from two *sri-PUSCH-MappingToAddModList*   + Alt. 2: Add SRS resource set ID in *SRI-PUSCH-PowerControl,* and select *SRI-PUSCH-PowerControl* from *sri-PUSCH-MappingToAddModList* considering the SRS resource set ID   + Alt. 3: Let RAN2 handle this   + Alt.4: Add second *sri-PUSCH-PathlossReferenceRS-Id/sri-P0-PUSCH-AlphaSetId/sri-PUSCH-ClosedLoopIndex* in *SRI-PUSCH-PowerControl*. * FFS2: Enhancements on open-loop power control parameter set indication * FFS3: Consideration on *srs-PowerControlAdjustmentStates* * FFS4: Impact of multi-TRP PUSCH repetition on PHR reporting * FFS5: Enhancement on power control parameters per TRP when SRI(s) indication of two SRS resource sets is absent. |

### Proposal 3.6

**[Draft for offline] Proposal 3.6:** For single-DCI based M-TRP PUSCH repetition schemes, support dynamic switching between multi-TRP and single-TRP operation by using two SRI fields indicated in DCI format 0\_1/0\_2.

* FFS: details of SRI field indications.

Please comment preferred changes on the proposal below. Also, provide views for FFS.

|  |  |
| --- | --- |
| **Company** | **Comments** |
| QC | This proposal can be discussed together with Proposal 3.1 as there are dependencies. |
| Huawei, HiSilicon | We support the motivation of the proposal, however, the SRI fields depends on the discussion of proposal 3.1. Before decision on proposal 3.1, we proposal the following modification:  **[Draft for offline] Proposal 3.6:** For single-DCI based M-TRP PUSCH repetition schemes, support dynamic switching between multi-TRP and single-TRP operation by using ~~two~~ SRI field(s) indicated in DCI format 0\_1/0\_2.   * FFS: details of SRI field indications. |
| Intel | prefer to agree to the intent: “For single-DCI based M-TRP PUSCH repetition schemes, support dynamic switching between multi-TRP and single-TRP operation by using ~~two SRI fields indicated in~~ DCI format 0\_1/0\_2” |
| LG | Support Huawei’s revision. |
| Samsung | Support the proposal but this proposal is also discussed after the proposal 3.1. |
| vivo | Agree with Huawei’s comments. |
| MediaTek | We prefer Intel’s revision. Huawei’s revision is also agreeable. |
| NTT Docomo | Considering the dependency with proposal 3.1, prefer Intel’s revision. |
| Apple | This can be jointly disscussed with proposal 3.1. |
| Fujitsu | This issue is associated with 3.1. |
| Ericsson | Support the proposal and agree with QC’s comment. |
| NEC | Support the proposal, and agree with QC and Ericsson’s comment. |
| ZTE | Support in principle.  From our perspective, the intention of dynamic switching between STRP and MTRP as well as minimize DCI overhead. Based on that, as we have elaborated in Proposal 3.1 and 3.3, the indication method should be discussed separately for codebook based and non-codebook based schemes. Thereby, we suggest to revise this proposal as below:  **[Draft for offline] Proposal 3.6:** For single-DCI based M-TRP PUSCH repetition schemes, support dynamic switching between multi-TRP and single-TRP operation for both code-book based and non-codebook based schemes ~~by using two SRI fields indicated~~ in DCI format 0\_1/0\_2.   * FFS: details of the method to indicate the dynamic switching. ~~SRI field indications.~~ |
| Xiaomi | We are open for the discussion. |
| Spreadtrum | Agree with Huawei’s comments. |
| Fraunhofer IIS/HHI | Support Huawei’s revision |
| vivo2 | Besides the switching between multi-TRP and single-TRP operation, we also prefer to support dynamic switching the ordering of SRIs when two TRPs are required for PUSCH transmission to allow scheduling flexibility.  Hence, we proposal the following modification based on Huawei’s comment:  **[Draft for offline] Proposal 3.6:** For single-DCI based M-TRP PUSCH repetition schemes, support dynamic switching between multi-TRP and single-TRP operation and dynamic switching the ordering of two TRPs by using ~~two~~ SRI field(s) indicated in DCI format 0\_1/0\_2.  FFS: details of SRI field indications. |
| TCL | Support the proposal, and Ericsson’s comment. |
| FL update#1 | Refer proposal 3.1. merged with that. |
| ZTE | We think it makes no sense to merge this proposal with Proposal 3.1 directly.  From the perspective of technology, the most critical issue of single-DCI based PUSCH scheme is about DCI overhead. As our previous elaborations in Proposal 3.1 and Proposal 3.3, utilize two SRI fields to indicate dynamic operation switching for codebook based scheme will inevitably lead to DCI overhead increasing. From our perspective, the most technical solution is to support dynamic operation switching as well as minimize DCI overhead for single-DCI based PUSCH transmission. Therefore, we hold the technical view that this part should be split with Proposal 3.1, then we can discuss about how to design the solution for dynamic operation switching for codebook based and non-codebook based schemes, respectively. We suggest:  **[Draft for offline] Proposal 3.6:** For single-DCI based M-TRP PUSCH repetition schemes, support dynamic switching between multi-TRP and single-TRP operation for both code-book based and non-codebook based schemes ~~by using two SRI fields indicated~~ in DCI format 0\_1/0\_2.  FFS: details of the method to indicate this dynamic switching. ~~SRI field indications.~~ |
| FL update#2 | Refer proposal 3.1. merged with that. |

### Proposal 3.7

**[Draft for offline] Proposal 3.7:** For M-TRP PUSCH reliability enhancement, down-select one from the following,

* Alt.1: Support multi-DCI based PUSCH repetition scheme.
  + The same TB is repeated towards multiple TRPs with different beams, where one or more PUSCH repetitions are scheduled by one DCI and another one or more PUSCH repetitions are scheduled by another DCI.
  + Changes on Rel-15/16 MCS, TBS determination, and UL resource allocation are not expected from this scheme.
* Alt.2: No further discussion on multi-DCI based PUSCH repetition in Rel-17 feMIMO.

Please comment preferred changes on the proposal below. Also, provide your preference for alternatives.

|  |  |
| --- | --- |
| **Company** | **Comments** |
| QC | Support Alt2. Multi-DCI based approach is already possible in Rel. 16 when the second TRP schedules a retransmission. Optimizations to send the retransmission grant before the first transmission occurs not only are hard from implementation perspective, but also violate the exiting restrictions in the sepc. |
| Huawei, HiSilicon | The multi-DCI is still under discussion in Rel-16 UE feature. We prefer to postpone the discussion on multi-DCI here. |
| Intel | Support Alt 2, agree with QC that multi-DCI is already possible – optimizations are significantly disruptive to UE implementation whereas no benefits have been shown. |
| LG | Support Alt 1. |
| Lenovo&MotM | Support Alt 1. |
| Samsung | Support Alt. 1. Multi-DCI based PUSCH repetition should be introduced to increase the reliability because flexible resource allocation per TRP can be supported. Furthermore, many multi-TRP related parameters (e.g. separate power control, SRI and TPMI) can be indicated naturally. Therefore, multi-DCI based PUSCH repetition should be also supported. |
| Vivo | Support Alt. 1.  As agreed in the last meeting,  For M-TRP PUSCH reliability enhancement, further discuss multi-DCI based PUSCH transmission/repetition scheme(s) considering the following aspects.  • …  • The scheme is considered to be supported only if there are gains over single DCI based PUSCH repetition schemes and a similar scheme is not supported by m-TRP PDCCH (e.g. Option 3).  Obvious performance gain is shown in our paper, so the scheme is considered to be supported. Apart from the gain over single-DCI based PUSCH repetition schemes, multi-DCI based PUSCH repetition has little specification impact to support PUSCH repetition. Moreover, multi-DCI based scheme is more future-proof in the sense that it can enable repetitions towards more than 2 TRPs straightforwardly with minimum change. |
| MediaTek | Support Alt. 2. We share the same view as QC and Intel. |
| NTT Docomo | Support alt.2. Agree with Qualcomm and Intel that multi-DCI based scheme is already possible. |
| Apple | Support Alt2. We propvided simulation results that show mDCI performance is worst than sDCI. |
| Fujitsu | Agree with QC. |
| Ericsson | Support Alt1. |
| ZTE | Support Alt 2. We can also be general to depriorize the discussion of multi-DCI based PUSCH repetitions. |
| Xiaomi | Support Alt.2. |
| Spreadtrum | Support Alt.2. Agree with QC’s comments that M-DCI based scheme is already possible. |
| vivo2 | The benefits of M-DCI scheme are not only caused by PDCCH reliability, but also from the freedom of scheduling parameters, as companies commented. In addition, a UE with PUCCH enhancement is not necessarily capable of MTRP PDCCH enhancement. Benefit from adaptive scheduling of each repetition transmission, M-DCI based scheme outperforms the S-DCI one with more than 5dB at the target BLER of 10-3. Obvious performance gain is observed, so the scheme is considered to be supported according to last meeting’s agreement.    What we are discussing in this AI is the reliability enhancement of PUSCH, it is a kind of optimization in essence. However, current retransmission realized in Rel-16 certainly causes longer latency which is not friendly to URLLC services. In our mind, supporting M-DCI scheme is a simpler way to achieve PUSCH reliability because it doesn’t have any issues on redesigning of DCI. Apart from the gain over single-DCI based PUSCH repetition schemes, multi-DCI based PUSCH repetition has little specification impact to support PUSCH repetition. Moreover, multi-DCI based scheme is more future-proof in the sense that it can enable repetitions towards more than 2 TRPs straightforwardly with minimum change. |
| TCL | Support Alt 1. |
| FL update#1 | The following proposal seems to be the way forward. This will be only discussed if companies wish to have an official agreement.  **[Draft for offline] Proposal 3.7:** For M-TRP PUSCH reliability enhancement, no further discussion on multi-DCI based PUSCH repetition in Rel-17 feMIMO. |
| InterDigital | We support FL’s proposal. |
| Futurewei | Support Alt 1 in the original proposal. |
| ZTE | We are okay to discuss this issue in this release if majority prefers, and we are okay either way. |
| QC | Support the proposal. |
| FL update#2 | Not enough support on Alt.1  **[Draft for offline] Proposal 3.7:** For M-TRP PUSCH reliability enhancement, no further discussion on multi-DCI based PUSCH repetition in Rel-17 feMIMO. |
| OPPO | Support the updated proposal |
| CMCC | Support Alt 1 in the original proposal. To support flexible indication of TPMI, RI, SRI, DMRS port, and TPC command, multi-DCI based PUSCH scheduling is more suitable for multi-TRP transmission, and there are fewer spec impacts in multi-DCI based PUSCH transmission than in single-DCI scheme |
| NTT Docomo | Support |
| Apple | Support |
| Nokia/NSB | Although we prefer to also support M-DCI, we can be fine with the proposal |
| Futurewei | Ok with this as a conclusion. |
| MediaTek | Support |
| NEC | Support |
| Fujitsu | Support |
| Xiaomi | Support |
| Samsung | Don’t support the updated proposal. We have same view with vivo. And also, for single DCI based scheme, enhancement details for indication of two SRI and TPMI values are complicated and companies’ views diverge, whereas multi-DCI based scheme can support mTRP PUSCH repetition with less spec impact. Therefore, multi-DCI based mTRP PUSCH repetition should not be precluded because we can support multi-TRP PUSCH repetition with simpler method.  We support Alt 1 in the original proposal. |
| ZTE | Support FL’s assessment. |
| vivo | According to last meeting’s agreement, M-DCI based PUSCH repetition scheme is considered to be supported if there are gains compared to S-DCI. Benefit from adaptive scheduling of each repetition transmission, M-DCI based scheme outperforms the S-DCI one with more than **5dB at the target BLER of 10-3**. Obvious performance gain is observed, so the scheme is to be supported.  We cannot assume the PDCCH enhancement is used for performance comparison, as it may be separate UE capabilities to support PDCCH enhancement and PUSCH enhancement. Regarding UEs not supporting the enhanced PDCCH, M-DCI based schemes is more robust to confront the blockage. As pointed out by some companies, M-DCI scheme is possible in Rel-16 as the following figure, in which the second DCI schedules a retransmission towards the second TRP. Obviously, this type of scheduling will lead to larger delay, which is aginst to the motivation of PUSCH enhancement mainly targeting URLLC services. So, the scheduling pattern to further reduce the latency shall be further discussed. When multiple DCIs can schedule the same or different TB also need to further study.    To reduce the latency in M-DCI scheduling scheme, OOO is required. It is known that OOO is already supported in the framework of Rel-16 M-DCI based MTRP enhancement. At least M-DCI based PUSCH repetition scheme can be enhanced based on the framework M-DCI based MTRP to ensure minimum change on current spec.  Based on the above description, we propose to modify the proposal as:  **[Draft for offline] Proposal 3.7:** Support multi-DCI based PUSCH repetition scheme.   * + Further discuss scheduling timeline restriction of multiple DCIs.   + The same TB is repeated towards multiple TRPs with different beams, where one or more PUSCH repetitions are scheduled by one DCI and another one or more PUSCH repetitions are scheduled by another DCI.   + Changes on Rel-15/16 MCS, TBS determination, and UL resource allocation are not expected from this scheme. |
| Huawei, HiSilicon | Support. Note that in eMIMO UE features, it’s still under discussion to add a UE capability for R16 mutli-TRP to allow the second DCI to schedule re-transmission of the PUSCH that is scheduled by the first DCI. We need to understand what extra spec impact is needed for the discussion here, on top of that R16 capability. |
| FL update#3 | Majority supports this. But, I do not think this is needed as an agreement.  **Proposal 3.7:** For M-TRP PUSCH reliability enhancement, no further discussion on multi-DCI based PUSCH repetition in Rel-17 feMIMO. |

### Proposal 3.8

**[Draft for offline] Proposal 3.8:** For single DCI based M-TRP PUSCH repetition Type B, support the following RV mapping,

* DCI indicates the first RV for the first PUSCH actual repetition, and the RV pattern (0 2 3 1) is applied separately to PUSCH actual repetitions of different TRPs with a possibility of configuring RV offset for the starting RV for the first actual repetition towards second TRP (The same method as PDSCH scheme 4).

Please comment preferred changes on the proposal below.

|  |  |
| --- | --- |
| **Company** | **Comments** |
| QC | Support the proposal. |
| Huawei, HiSilicon | Support FL’s proposal. |
| Intel | Support |
| LG | Support FL’s proposal. |
| Lenovo&MotM | Support. |
| Samsung | Support the proposal. |
| Vivo | Support FL’s proposal. |
| MediaTek | Support |
| NTT Docomo | Support the proposal. |
| Apple | Support |
| Fujitsu | Support |
| Ericsson | Support |
| NEC | Support the proposal. |
| ZTE | Support FL’s proposal. |
| Xiaomi | Fine with the majority view. |
| Spreadtrum | Support the proposal. |
| Fraunhofer IIS/HHI | Support the proposal. |
| TCL | Support the proposal. |
| FL update#1 | Everyone support. |
| FL update#2 | **Agreement**  For single DCI based M-TRP PUSCH repetition Type B, support the following RV mapping,  DCI indicates the first RV for the first PUSCH actual repetition, and the RV pattern (0 2 3 1) is applied separately to PUSCH actual repetitions of different TRPs with a possibility of configuring RV offset for the starting RV for the first actual repetition towards second TRP (The same method as PDSCH scheme 4). |

### Proposal 3.9

**[Draft for offline] Proposal 3.9:** Support CG PUSCH transmission towards M-TRPs using a single CG configuration.

* Use same beam mapping principals as dynamic grant PUSCH repetition scheme.
* FFS: Required changes on CG parameters (ConfiguredGrantConfig)

Please comment preferred changes on the proposal below. Indicate your views on FFS.

|  |  |
| --- | --- |
| **Company** | **Comments** |
| QC | Support the proposal. |
| Huawei, HiSilicon | Support FL’s proposal. |
| Intel | Support |
| Lenovo&MotM | Support it for a single CG configuration while we think multiple CG configuration should be studied too. |
| Samsung | Support the proposal. |
| vivo | We don’t support the proposal.  Considering type 2 CG PUSCH transmission towards MTRPs using single CG configuration, bit width extension in SRI, TPMI and TPC field of single-DCI costs a high overhead. And, for UEs that do not support complicated single-DCI PUSCH enhancement, they may also not be able to support the type 2 CG. So, CG PUSCH transmission towards M-TRPs using multiple CG configuration is preferred. |
| MediaTek | Support |
| NTT Docomo | Support the proposal. |
| Apple | Support the proposal |
| Fujitsu | Support the proposal |
| Ericsson | Support FL’s proposal |
| NEC | Support the proposal. |
| ZTE | Support FL’s proposal. |
| Xiaomi | Support the proposal |
| Spreadtrum | Support the proposal. |
| Fraunhofer IIS/HHI | Support the proposal. |
| vivo2 | There are some companies support CG PUSCH transmission towards different TRPs using multiple CG configuration. We think Multi-CG is also a promising solution for CG PUSCH enhancement. So we propose to update the proposal as follows:  **[Draft for offline] Proposal 3.9:** Support CG PUSCH transmission towards M-TRPs using a single CG configuration.   * Use same beam mapping principals as dynamic grant PUSCH repetition scheme. * FFS: Required changes on CG parameters (ConfiguredGrantConfig)   FFS: Support CG PUSCH transmission towards M-TRPs using multiple CG configurations. |
| TCL | Support FL’s proposal. |
| FL update#1 | Majority view is to support the proposal. Let’s keep that as it is. |
| FL update#2 | **Agreement**  Support CG PUSCH transmission towards M-TRPs using a single CG configuration.   * Use same beam mapping principals as dynamic grant PUSCH repetition scheme. * FFS: Required changes on CG parameters (ConfiguredGrantConfig)   The feature is UE optional |

## 3.3 Additional high priority proposals

In this FL summary, we have not included any FL proposals based on certain other directions suggested by one or two companies. Such proposals are not considered if that is not critical for the basic design framework or can be discussed in a later stage once the basic framework is agreed. Please see the full list of company contribution proposals in Section 5. If companies wish to bring any additional aspects related to PUSCH during RAN1 #104-e, please comment below.

|  |  |
| --- | --- |
| Company | Comments |
| QC | We suggest to start the discussions on reporting AP-CSI on two PUSCH repetitions for mTRP given that this was proposed by at least three companies. |
| Huawei, HiSilicon | We also think the reporting AP-CSI on two PUSCH repetitions is very important for multi-TRP. |
| LG | Beam mapping in case of PUSCH dropping due to invalid UL symbols should be discussed.  If beams are mapped to PUSCH TO without considering dropping, PUSCH TO for one TRP can be dropped much more than PUSCH TO for another TRP. As a result, diversity gain from MTRP transmission can decrease or disappear. |
| Lenovo&MotM | Dropping some symbols of repetitions to switch beams while whether the dropped symbols are considered as invalid symbols. |
| Samsung | We suggest to discuss the association between two SRIs and SRS resources in first and second SRS resource sets, respectively. In current specification, the indicated SRI in slot n is associated with the most recent transmission of SRS resource identified by the SRI. Therefore, clarification is required if two SRIs are indicated for multi-TRP PUSCH repetition. |
| vivo | We propose SRI codepoint mapping activation and TPMI selection by MAC CE to reduce DCI overhead.  In addition, single TPMI indication for MTRP PUSCH repetitions should be supported.  In current spec, power control parameters of CG retransmission are acquired from CG configuration. Considering the case in which CG PUSCH transmits towards one TRP while retransmission transmits towards another TRP, power control parameters applied for CG PUSCH transmission will not be applied to retransmission. Hence, the Power control of CG retransmission in MTRP scenario shall be further discussed.  For PUSCH transmission without repetition, beam switching of PUSCH is applied for the two hops. |
| Ericsson | Similar to Qualcomm and Huawei comments, we suggest to discuss A-CSI multiplexing on two PUSCH repetitions towards two TRPs. |
| FL update#1 | Let’s try to finalize first set of proposals and I will add some more proposals if there is progress. |
| Futurewei | We still think the two UL TA offsets are needed in general. We have provided analysis to show that even if the DL timings are within one CP, the UL timings may not. We are willing to hear other companies’ solution to this issue, but no other technical discussions were provided. |

# Second Phase

## 4.1 Agreements

**Agreement**

For single DCI based M-TRP PUSCH repetition Type B, support the following RV mapping,

* DCI indicates the first RV for the first PUSCH actual repetition, and the RV pattern (0 2 3 1) is applied separately to PUSCH actual repetitions of different TRPs with a possibility of configuring RV offset for the starting RV for the first actual repetition towards second TRP (The same method as PDSCH scheme 4).

**Agreement**

Support CG PUSCH transmission towards M-TRPs using a single CG configuration.

* Use same beam mapping principals as dynamic grant PUSCH repetition scheme.
* FFS: Required changes on CG parameters (ConfiguredGrantConfig)

The feature is UE optional

## 4.2 Proposals for Online discussion

**Dynamic indication of the number of repetitions**

The following was discussed many times during the last few meetings and this meeting. No point of wasting time further.

**Conclusion**

**Alt.1 :** The dynamic indication of the number of repetitions supported for Rel-17 coverage enhancement can be used for multi-TRP operation

**Alt.2:** The dynamic indication of the number of repetitions is not supported for multi-TRP operation.

**Support of Scheme 3**

Scheme 3 is supported by almost all companies. Discussed two times already in RAN on which WI should take the decision. RAN guidance is the following.

*For handling of the PUCCH repetitions it is proposed to proceed as follows:*

* *RAN1 to continue discussion on PUCCH repetition, whether to specify or not, in the IIoT/URLLC WI* ***for single TRP.***
* ***PUCCH repetition issues with multi-TRP******to be handled in Fe-MIMO WI.***

Rel-17 IIoT will not make the agreement for m-TRP operation.

**Proposal 2.3:**

**Alt.1**: For PUCCH reliability enhancement, support multi-TRP intra-slot repetition (Scheme 3) ~~at least~~ for all PUCCH formats ~~0/2~~.

* The same PUCCH resource carrying UCI is repeated for X = 2 [consecutive] sub-slots within a slot.
* If Rel-17 eIIoT agreed to support sub-slot based repetition for single-TRP, refer the design details related to sub-slot configurations (e.g. value of X) to Rel-17 eIIoT

Note1: The decision of supporting scheme 3 is only applicable for multi-TRP operation.

**Alt.2:** Support of Scheme 3 is not further considered in Rel-17 feMIMO.

**TPC Commands**

There may be valid technical concerns on supporting other schemes. In both proposals 2..4-A and 2.4.-B, **Alt.1 is the majority view.** RAN1 needs to move-on here.

**Proposal 2.4-A:**

**Alt1:** To support per TRP closed-loop power control for PUCCH, a second TPC field (similar to the existing TPC field) is added in DCI formats 1\_1 / 1\_2.

**Alt.2**: To support per TRP closed-loop power control for PUCCH, select one from the below options,

* Option.1: A single TPC field (the existing TPC field) is used in DCI formats 1\_1 / 1\_2, and the TPC value applied for both PUCCH beams
* Option.2: A single TPC field (the existing TPC field) is used in DCI formats 1\_1 / 1\_2, and the TPC value applied for one of two PUCCH beams at a slot. The TPC value may be applied for the other PUCCH beam at an another slot.
* Option 3: A second TPC field (similar to the existing TPC field) is added in DCI formats 1\_1 / 1\_2.
* Option 4: A single TPC field is used in DCI formats 1\_1 / 1\_2, and indicates two TPC values applied to two PUCCH beams, respectively.

**Proposal 2.4-B:**

**Alt.1 :** To support per TRP closed-loop power control for PUSCH, a second TPC field (similar to the existing TPC field) is added in DCI formats 0\_1 / 0\_2.

**Alt2 :** To support per TRP closed-loop power control for PUSCH, select one from the below options,

* Option.1: A single TPC field (the existing TPC field) is used in DCI formats 0\_1 / 0\_2, and the TPC value applied for both PUSCH beams
* Option.2: A single TPC field (the existing TPC field) is used in DCI formats 0\_1 / 0\_2, and the TPC value applied for one of two PUSCH beams at a slot.
* Option 3: A second TPC field (similar to the existing TPC field) is added in DCI formats 0\_1 / 0\_2.
* Option 4: A single TPC field is used in DCI formats 0\_1 / 0\_2, and indicates two TPC values applied to two PUSCH beams, respectively.

**Beam mapping/power control parameter set mapping**

RAN1 sent an RAN4 LS in the last meeting for checking the transient time, beam switching gaps, supporting of cyclical mapping, and about scheme 2. Few companies suggest waiting for RAN4 reply. The following proposal is using the same mapping principals applied for scheme 1 in FR2 operation and can be taken as working assumption from the view of majority.

**Proposal for working assumption 2.7:**

**Alt.1 :**

For beam mapping /power control parameter set mapping for PUCCH repetitions,

* For M-TRP PUCCH Scheme 1 in FR1, it is possible to configure either cyclic mapping or sequential mapping of power control parameter sets over PUCCH repetitions (similar to spatial relation info’s over PUCCH repetitions).
* For M-TRP PUCCH Scheme 3, reuse the same methods as Scheme 1 (by replacing slots with sub-slots) for beam mapping or power control resource set mapping to sub-slots.

**Alt.2 :** No further discussion on beam mapping/power control parameter set mapping until RAN4 LS reply, and RAN1 confirm the working assumption on beam mapping.

**Dynamic switching of M-TRP/S-TRP**

Companies have proposals from last two meetings, RAN1 shall either accept that this is supported or not.

**Proposal 2.8:**

**Alt.1**

For Multi-TRP Scheme 1, supporting dynamic switching between multi-TRP PUCCH scheme and single-TRP PUCCH transmission is not restricted, and can be done by associating,

* a PUCCH resource with one or two spatial-relation-info and PRI bit-field indicating a PUCCH resource (for FR2).
* a PUCCH resource with one or two power control parameter sets and PRI bit-field indicating a PUCCH resource (for FR1)
* FFS: support of dynamic switching for Scheme 2/3 (if the schemes supported)

**Alt.2 :** For Multi-TRP Scheme 1, dynamic switching between multi-TRP PUCCH scheme and single-TRP PUCCH transmission is not supported.

Companies **who object to choose Alt1 in all the above proposals** can also suggest a way forward below.

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| **Company** | **Comments** |
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## 4.3 Proposals for Offline discussion

### 4.3.1 Stable proposals after Phase 1

*These proposals were presented for Chairman to endorse in Phase 1. Will be discussed depending on the outcome of that.*

**Proposal 2.1:** For M-TRP PUCCH scheme 1,

* Support PUCCH formats 0 and 2 (in addition to agreed PUCCH formats 1,3,4)

**Proposal 2.2:**

For M-TRP PUCCH scheme 1,

* For PUCCH formats 1/3/4, values for the total number of repetitions at least contain values 2, 4, and 8.
  + FFS: maximum repetition number can be extended to 16.
* For PUCCH formats 0/2, the total number of repetitions at least contain 2.
  + FFS: other values.
* RRC configured number of slots (repetitions) are applied across both TRPs (e.g if the number of repetitions given by *nrofSlots* in *PUCCH-config* is 8, per TRP limit is 4).

**Offline Agreement 2.5:** To support per TRP power control for multi-TRP PUCCH schemes in FR1,

* Two sets of power control parameters are used, and each set has a dedicated value of p0, pathloss RS ID and a closed-loop index.
* FFS: details on how a PUCCH resource can be linked to one or both of the two sets of power control parameters.
* FFS: whether PUCCH resource group can be linked to power control parameter sets.

**Offline Agreement 3.5:** For single-DCI based M-TRP PUSCH repetition schemes, up to two power control parameter sets (using *SRI-PUSCH-PowerControl*) can be applied when SRS resources from two SRS resource sets indicated in DCI format 0\_1/0\_2.

* FFS1: Details on linking SRI fields to two power control parameters,
  + Alt. 1: Add second *sri-PUSCH-MappingToAddModList,* andselect two *SRI-PUSCH-PowerControl* from two *sri-PUSCH-MappingToAddModList*
  + Alt. 2: Add SRS resource set ID in *SRI-PUSCH-PowerControl,* and select *SRI-PUSCH-PowerControl* from *sri-PUSCH-MappingToAddModList* considering the SRS resource set ID
  + Alt. 3: Let RAN2 handle this
  + Alt.4: Add second *sri-PUSCH-PathlossReferenceRS-Id/sri-P0-PUSCH-AlphaSetId/sri-PUSCH-ClosedLoopIndex* in *SRI-PUSCH-PowerControl*.
* FFS2: Enhancements on open-loop power control parameter set indication
* FFS3: Consideration on *srs-PowerControlAdjustmentStates*
* FFS4: Impact of multi-TRP PUSCH repetition on PHR reporting
* FFS5: Enhancement on power control parameters per TRP when SRI(s) indication of two SRS resource sets is absent.

### 4.3.2 Offline proposals for discussion

There are two pending issues (proposal 3.1 and proposal 3.3) from the phase 1 discussion, which are on SRI and TPMI indications. This issue is something critical and RAN1 cannot delay that for another meeting. Based on FL observations, there are different flavours that companies wish to consider in SRI fields, and also want to discuss them separately for codebook based on non-codebook based PUSCH. FL proposals are as below.

**Proposal 3.1-A:** For single DCI based M-TRP PUSCH repetition schemes, in codebook based PUSCH,

* Support two SRIs corresponding to two SRS resource sets are included in DCI formats 0\_1/0\_2.
  + **Option 1:** Each SRI field indicating SRI per TRP, where the SRI field based on Rel-15/16 framework
  + **Option 2**: One enhanced SRI field indicating two SRIs
    - FFS: details of enhanced SRI field including the specification effort to replace Table 7.3.1.1.2-32/32A/32B in 38.212.
* Support dynamic switching between multi-TRP and single-TRP operation
  + **For Option 1 - Alt1:** by using two SRI fields at least when there is a reserved entry for one SRI field.
    - FFS: whether to support dynamic switching if the SRI fields does not have a reserved entry
  + **For Option 1 - Alt2 :** by using two SRI fields or TPMI field(s).
    - FFS: Additional details of SRI/TPMI field interpretations
  + **For Option 2:** by using one enhanced SRI field or TPMI field(s).
    - FFS: Additional details of SRI field interpretations

**Proposal 3.1-B:** For single DCI based M-TRP PUSCH repetition schemes, in non-codebook based PUSCH,

* Support two SRIs corresponding to two SRS resource sets are included in DCI formats 0\_1/0\_2.
  + **Option 1:** Each SRI field indicating SRI per TRP, where the SRI field based on Rel-15/16 framework
  + **Option 2:** Each SRI field indicating SRI per TRP, where the first SRI field based on Rel-15/16 framework,
    - FFS: details of second SRI field including the specification change for Table 7.3.1.1.2-28/29/30/31 in 38.212.
  + **Option 3**: One enhanced SRI field indicating two SRIs
    - FFS: details of enhanced SRI field including the specification effort to replace Table 7.3.1.1.2-28/29/30/31 in 38.212.
* Support dynamic switching between multi-TRP and single-TRP operation
  + **For Option 1:** by using two SRI fields at least when there is a reserved entry for one SRI field.
    - FFS: whether to support dynamic switching if the SRI fields does not have a reserved entry
  + **For Option 2:** by using two SRI fields
    - FFS: Additional details of SRI field interpretations
  + **For Option 3:** by using one enhanced SRI field.
    - FFS: Additional details of SRI field interpretations

Please comment. Option 1 (+ alt1 in CB PUSCH) will be FL suggestion by considering the majority view.

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| --- | --- |
| **Company** | **Comments** |
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**Proposal 3.3:** For single DCI based M-TRP PUSCH repetition schemes, in codebook based PUSCH,

* **Option 1**: two TPMI fields are indicated in DCI formats 0\_1/0\_2.
  + **Alt.1** : The first TPMI field uses the Rel-15/16 TPMI field design (which includes TPMI index and the number of layers) of DCI format 0\_1/0\_2. The second TPMI field only indicates the second TPMI index. The same number of layers are applied as indicated in the first TPMI field.
    - FFS: Details of second TPMI field interpretation including changes expected in Tables 7.3.1.1.2-2/2A/2B/3/3A/4/4A/5/5A in 38.212
  + **Alt.2** : The first and second TPMI fields use the Rel-15/16 TPMI field design (which includes TPMI index and the number of layers) of DCI format 0\_1/0\_2.
* **Option 2**: enhanced TPMI field is indicated in DCI formats 0\_1/0\_2.
  + The enhanced TPMI field indicates first TPMI index, second TPMI index, and the number of layers. The same number of layers are applied for both TPMI indexes.
    - FFS: Details of TPMI field interpretation including the specification effort to replace Tables 7.3.1.1.2-2/2A/2B/3/3A/4/4A/5/5A in 38.212

Please comment. Option 1 + Alt.1 will be FL suggestion by considering the majority view.

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| **Company** | **Comments** |
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# Reference

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| --- | --- | --- | --- |
| 1 | [R1-2100344](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2100344.zip) | Enhancements on multi-TRP/panel for PDCCH, PUCCH and PUSCH | CATT |
| 2 | [R1-2100422](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2100422.zip) | Further discussion on enhancement of MTRP operation | vivo |
| 3 | [R1-2100535](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2100535.zip) | On multi-TRP enhancements for PDCCH and PUSCH | Fraunhofer IIS, Fraunhofer HHI |
| 4 | [R1-2100582](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2100582.zip) | Enhancements on Multi-TRP for PDCCH, PUSCH and PUCCH | MediaTek Inc. |
| 5 | [R1-2100619](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2100619.zip) | Enhancements on Multi-TRP for PDCCH, PUCCH and PUSCH | LG Electronics |
| 6 | [R1-2100637](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2100637.zip) | Multi-TRP enhancements for PDCCH, PUCCH and PUSCH | Intel Corporation |
| 7 | [R1-2100738](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2100738.zip) | Enhancements on Multi-TRP for PDCCH PUCCH and PUSCH | Fujitsu |
| 8 | [R1-2100784](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2100784.zip) | Discussion on enhancements on Multi-TRP for PDCCH, PUCCH and PUSCH | Spreadtrum Communications |
| 9 | [R1-2100845](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2100845.zip) | Considerations on Multi-TRP for PDCCH, PUCCH, PUSCH | Sony |
| 10 | [R1-2100950](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2100950.zip) | Discussion on multi-TRP for PDCCH, PUCCH and PUSCH | NEC |
| 11 | [R1-2100965](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2100965.zip) | Discussion on Enhancements on Multi-TRP for Uplink Channels | Asia Pacific Telecom, FGI |
| 12 | [R1-2101006](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2101006.zip) | Enhancements for Multi-TRP URLLC schemes | Nokia, Nokia Shanghai Bell |
| 13 | [R1-2101033](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2101033.zip) | Enhancements on Multi-TRP for PDCCH, PUCCH and PUSCH | CMCC |
| 14 | [R1-2101093](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2101093.zip) | Enhancements on Multi-TRP for PDCCH, PUCCH and PUSCH | Xiaomi |
| 15 | [R1-2101187](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2101187.zip) | Enhancements on Multi-TRP for PDCCH, PUCCH and PUSCH | Samsung |
| 16 | [R1-2101351](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2101351.zip) | Views on Rel-17 multi-TRP reliability enhancement | Apple |
| 17 | [R1-2101415](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2101415.zip) | Multi-TRP Enhancements for PDCCH, PUCCH and PUSCH | Convida Wireless |
| 18 | [R1-2101447](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2101447.zip) | Enhancements on Multi-TRP for PDCCH, PUCCH and PUSCH | Qualcomm Incorporated |
| 19 | [R1-2101537](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2101537.zip) | Enhancements on Multi-TRP PUSCH | Sharp |
| 20 | [R1-2101598](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2101598.zip) | Discussion on MTRP for reliability | NTT DOCOMO, INC. |
| 21 | [R1-2101653](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2101653.zip) | Discussion on enhancement on Multi-TRP PDCCH | ASUSTeK |
| 22 | [R1-2101654](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2101654.zip) | On PDCCH, PUCCH and PUSCH enhancements | Ericsson |
| 23 | [R1-2101662](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2101662.zip) | Enhancements on Multi-TRP for PDCCH, PUCCH and PUSCH | TCL Communication Ltd. |