**3GPP TSG-RAN WG1#10**
**Beijing, China, 18 Jan. - 21 Jan. 2000**

***TSGR1#10(00)0108***

**Agenda Item:** Ad Hoc 14

**Source:** Samsung Electronics Co.

**Title:** Clarification of issues on gated DPCCH transmission

**Document for:** discuss and approve

# 1. Introduction

In this document, we summarize and clarify all of the issues related to gated DPCCH transmission currently under discussion. The issues that have not been either agreed nor discussed are the random gating pattern, mandatory/optional status of gating, gating in compressed mode, and procedures in one-way (downlink only gating) operation. Although some of the aforementioned issues have been already discussed in several previous WG1 meetings, it would be better to summarize them again to help their understanding.

In the last WG1#7bis Kyongju meeting, a concern on the EMC effects of gated DPCCH transmission to the hearing aid apparatus was raised. Following that, the concept of random gating was introduced by Mitsubishi [1]. In WG1#8 New York meeting [2], the random gating pattern generation algorithm was proposed by Samsung, however, the algorithm was not approved at the meeting because the explanation of the algorithm was not so clear. In addition, there was a concern on the neutrality of the technology, that is, the degree of complexity should be the same when the algorithm is implemented with ASIC or DSP. Finally, WG1 decided to discuss further the random pattern generation method [3]. In WG1#9 Dresden meeting, the revised contribution was submitted [4], but it was not discussed due to lack of time. In order to discuss all of the outstanding issues we update the previous document by summarizing those issues.

# 2. Combination of Gating Operation Mode

For the UTRAN, the gated DPCCH transmission is an option for both uplink and downlink while, for the UE, it is optional for the uplink and mandatory for the downlink. The UTRAN and UE negotiate the combination of gating operation parameters when needed. The parameters required to be negotiated are gating rate, gating pattern, and direction as follows.

| | | | |
|---|---|---|---|
| Gating Rate | 1 | 1/3 | 1/5 |

| | | |
|---|---|---|
| Gating Pattern | Random | Regular |

| | | |
|---|---|---|
| Direction | Downlink Only | Uplink and Downlink |

If the gating transmission is disabled (i.e., gating rate = 1), then no gating pattern will be used. In the case where the gated DPCCH transmission is used only for the downlink, then the UE shall transmit the DPCCH in every time slots, and the UE shall:

- adjust the transmit power in response to the valid downlink TPC, where valid downlink TPC means the downlink TPC transmitted at the gated-on slots
- ignore any downlink TPC that are received during the gated off slot, and the uplink transmit power shall remain constant
- generate and transmit uplink TPC based on the downlink symbols if the time slot is associated with the downlink gate-on slot
- repeat the previous uplink TPC if the time slot is associated with the downlink gate-off slot

In the compressed mode, the gated DPCCH transmission shall be stopped through the higher layer signaling between UE and UTRAN. It is possible to transmit DPDCH while maintaining gating mode, directed by higher layer. During transmission of DPDCH in gating mode, all of the corresponding physical layer control information (DPCCH) shall be transmitted while the gating mode is maintained, and the receiver shall ignore the invalid part of DPCCH according to the appropriate gating pattern. In this case, TFCI and Pilot bits shall not be ignored because it provides the physical information of DPDCH.

# 3. Random Gating Pattern Generation Method

If the gated DPCCH transmission is enabled with random gating pattern, the downlink and uplink gating patterns shall be determined based on the parameters depicted in Table 1.

**Table 1. Parameters for Random Gating Pattern**

| **Parameter** | **Value** |
|---|---|

| | |
|---|---|
| CFN | 0, 1, …, 255 (8bits) |
| gating rate | 1/3 or 1/5 |
| Number of gating group( $N_G$ ) | 5, if gating rate is 1/3<br>3, if gating rate is 1/5 |
| Gating group size ( $S_G$ ) | |
| $A = (a_0, a_1, ..., a_{18})$ | 1011010011011101001 (19bits) |

In Table 1, CFN is a frame counter ranged from 0 to 255, and $N_G$ represents the number of gating groups in a frame. Each gating group consists of $S_G$ (gating group size) consecutive slots, which is the number of slots in a gating group.

Let $i$ be the CFN of the frame $(i = 0,1,...,255)$ and $j$ be the $j$ th gating group in a frame $(j = 0,1,..., N_G - 1)$, respectively, then the allocated time slot, $s(i, j)$, shall be given by

$$s(i,j) = \begin{Bmatrix} (A_j \oplus C_i)_{10} \bmod (S_G - 1) + 1, & j = 0 \\ (A_j \oplus C_i)_{10} \bmod S_G, & j = 1,..., N_G - 2 \\ S_G - 1, & j = N_G - 1 \end{Bmatrix}, \quad i = 0,1,...,255$$

where $A_j = (a_j, a_{j+1}, ..., a_{j+15}), j = 0,1,..., N_G - 2$, is a 16bit sequence constructed from $A$ in Table 1 and Figure 1, and $C_i = ((\mathrm{CFN})_2, (\mathrm{CFN})_2)$ is a 16bit sequence consists of repeated binary representation of CFN, where $(\bullet)_m$ represents the $m$-ary representation of the argument. Figure 1 shows the explanation of sequence $A$ and $A_j$.

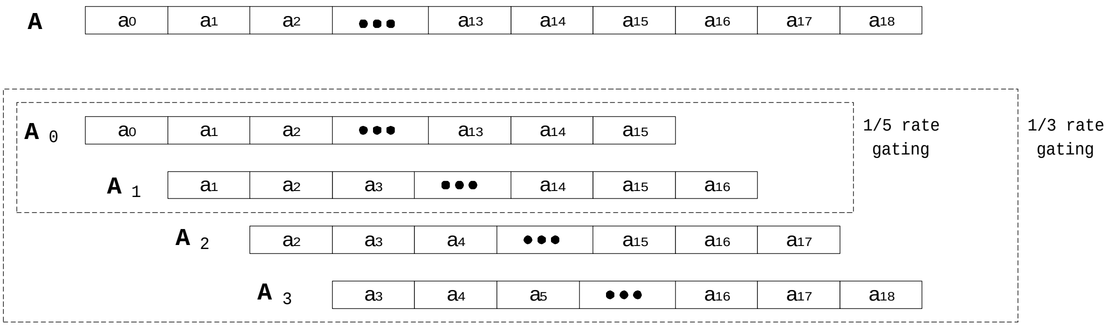
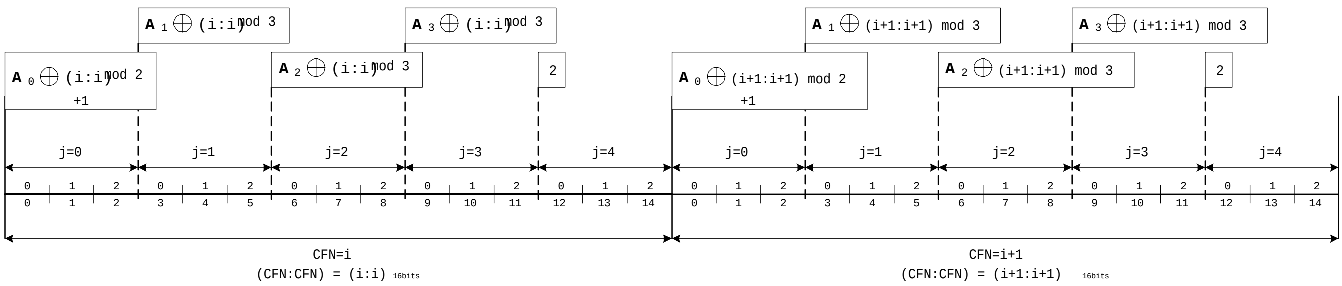
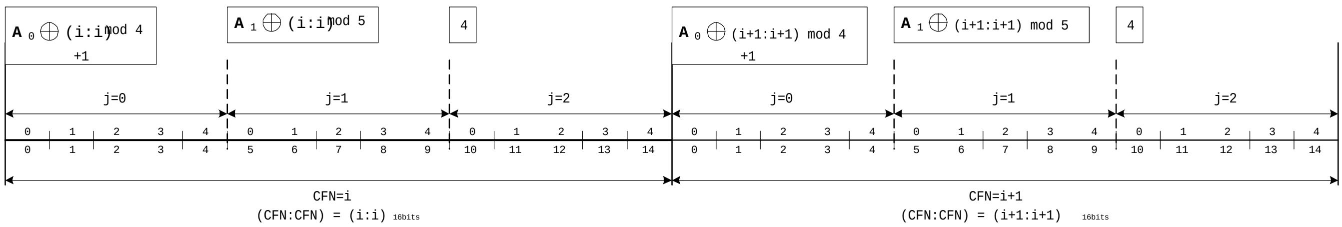



**Figure 1. Sequence $A$ and $A_j$**

The range of $s(i, j)$ is {0,1,2} in the case of 1/3 rate gating, and {0,1,2,3,4} in the case of 1/5 rate gating, except for the first and last gating groups. It is worth noting that the first time slot of each frame shall never be allocated to $s(i, j)$ ( $j = 0$ case), and the last time slot of each frame is always allocated to $s(i, j)$ ( $j = N_G - 1$ case). Figure 2 explains the method of the proposed random pattern generation for uplink DPCCH gating.




(a) s(i,j) of 1/3 rate gating




(b) s(i,j) of 1/5 rate gating

**Figure 2. Calculation of $s(i, j)$ : (a) 1/3 rate (b) 1/5 rate**

When the gated transmission mode is enabled in the downlink and uplink, UTRAN and the UE shall transmit the DPCCH in the time slots specified in Table 1 and Table 2. Only one slot per each gating group shall be gated-on.

**Table 1 : Downlink DPCCH gate on time slot allocations during gated transmission mode enabled**

| Gating Pattern | Gating Rate | Downlink DPCCH gate on time slot allocation | |
|---|---|---|---|
| | | Pilot | TPC, TFCI |
| Random Pattern | 1/3 | $j \times S_G + s(i, j) - 1$ | $j \times S_G + s(i, j)$ |
| | 1/5 | | |

* Note: i=0,1,...,255 denotes the CFN and j=0,1,2,3,4 if gating rate is 1/3, j=0,1,2 if gating rate is 1/5 denotes the gating group number.

**Table 2 : Uplink DPCCH gate on time slot allocations during gated transmission mode enabled**

| Gating Pattern | Gating Rate | Uplink DPCCH gate on time slot allocation |
|---|---|---|
| | | Pilot, TFCI, FBI, TPC |
| Random Pattern | 1/3 | $j \times S_G + s(i, j)$ |
| | 1/5 | |

* Note: i=0,1,...,255 denotes the CFN and j=0,1,2,3,4 if gating rate is 1/3, j=0,1,2 if gating rate is 1/5 denotes the gating group number.

An example of the relative timings of the downlink and uplink DPCCH transmission with random gating pattern using a hypothetical pattern is depicted in Figure 3. The gating pattern for the uplink slot in Figure 3 is (2, 0, 1, 0, 2) for 1/3 rate gating and (1, 2, 4) for 1/5 rate gating.

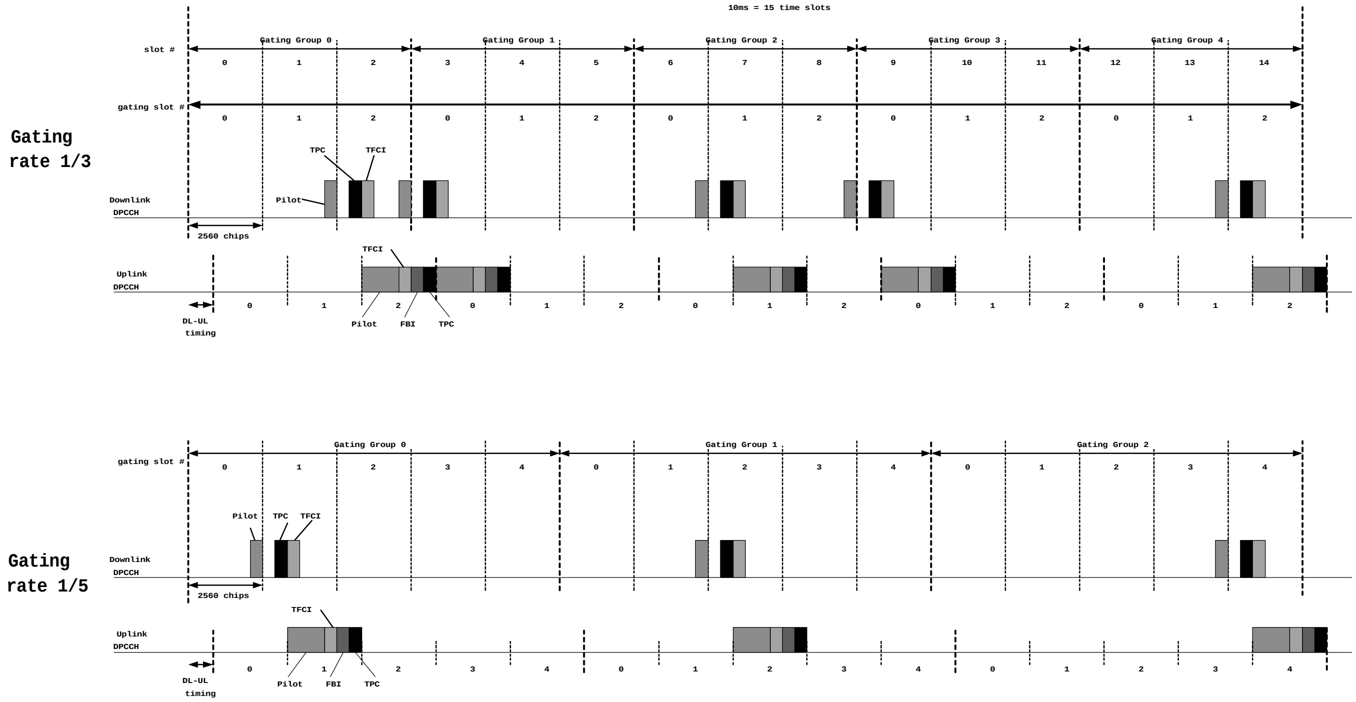



**Figure 3. Uplink and Downlink DPCCH gating with random gating pattern**

## 4. Power Spectral Density

The most important factor related to the EMC effect is the power spectral density of the gating pattern. In regular gating pattern, the periodic low frequency components are included which may result in some sound to the nearby hearing aid apparatus from UEs.. By randomizing the gating pattern, the power spectrum can be spread out over a range of frequencies making the sound heard through the hearing aid apparatus random-noise-like and hard to notice. Figure 4 shows the power spectral density of the proposed random gating pattern. In addition, the power spectral density of the regular gating pattern is also plotted to compare the spectral density.

(a) regular patter (b) random pattern

**Figure 4. Power spectral density of (1/3 rate gating): (a) regular pattern (b) random pattern**

From this figure, we can ascertain the fact that the power spectrum becomes wide spread over a range of frequencies and the peak power spectral density becomes much smaller than that of the regular gating patter. The reduction of the peak power spectral density of the proposed random gating from the regular gating is summarized in Table 2.

**Table 2. Reduction of Peak Power Spectral Density from Regular Gating**

| | 1/3 rate gating | 1/5 rate gating |
|---|---|---|
| Reduction of Peak Power Spectral Density | 11.7dB | 8.5dB |

## 5. Conclusion

In this document, issues related to the gated DPCCH transmission are summarized and clarified.

## 6. References


[1] TSGR1#8(99)f43, "Reducing EMC problem in uplink DPCCH Gated mode," Mitsubishi, New York, 12-15 Oct. 1999.

[2] TSGR1#8(99)g54, "Revised Random Pattern for DPCCH Gated Transmission (Rev. of R1-99f80)," Samsung, New York, 12-15, Oct. 1999.

[3] TSGR1#8(99)h77, "Draft minutes for 3GPP RAN-TSG 8th WG1 meeting," New York, 12-15, Oct. 1999.

[4] TSGR1#9(99)j51, "Random pattern for Gated DPCCH transmission," Dresden, ,Nov. 1999.


## 7. Contact Persons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