TSG-RAN Working Group 1(Radio) meeting #7 ***TSGR1#7(99)b53***
Hannover, Germany, 30 Aug. –03 Sep. 1999

Agenda Item: **Ad Hoc 10**

Source: **LG Information & Communications, Ltd.**

Title: **Time Delay between Physical Channels of Different Scrambling Codes**

Document for: **Proposal**

Introduction

This document includes a proposal for improved modulation method for multiple scrambling codes. The orthogonality of orthogonal variable spreading factor (OVSF) codes is not preserved between the physical channels of different scrambling codes, and the interference between physical channels of different scrambling codes is severer when those physical channels are time-synchronised

In this proposed method, the output of spreading coder is delayed for a few samples in order to make the physical channels of different scrambling codes time-asynchronous. With this proposed method, the interference between physical channels of different scrambling codes is reduced.

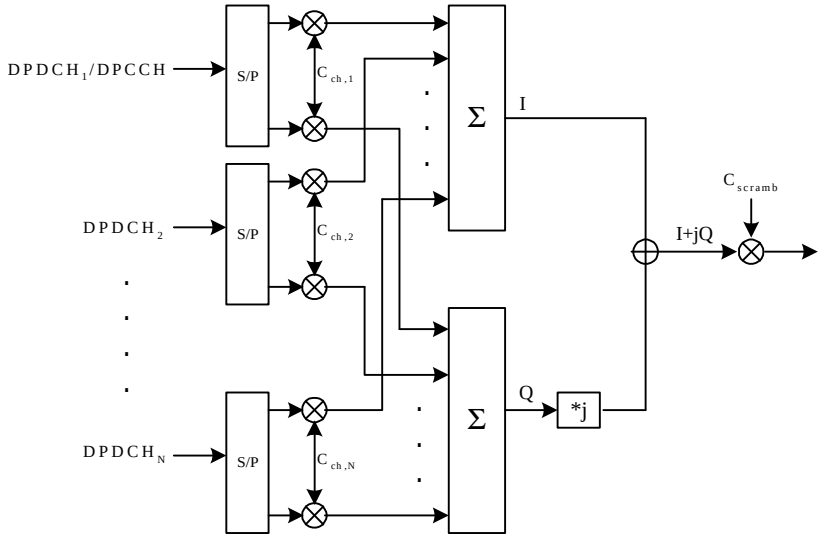
Current Method

Multiple scrambling codes on the downlink were approved at the TSG-RAN WG1 meeting #5 (June 1-4, 1999, Cheju, Korea) [1]. For each cell, one primary scrambling code (PSC) and M secondary scrambling codes (SSC) are available.

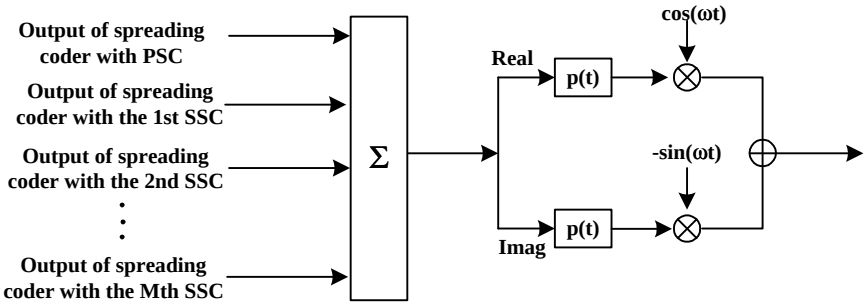
The time synchronisation between BS and MS is carried out by using synchronisation channel (SCH), and the physical channels (PCHs) scrambled by PSC and SSC are time-synchronised with SCH as illustrated in Figures 1 and 2 [2].

The PCHs scrambled by the same scrambling code should be time-synchronised to each other in order to preserve the orthogonality of OVSF codes. However, the orthogonality of OVSF codes is not preserved between the PCHs of different scrambling codes. Moreover, the interference power between the PCHs, which are not orthogonal to each other, has the maximum value when two PCHs are time-synchronised [3].

So, we introduce the time delay at the output of spreading coder to make the PCHs of different scrambling codes time-asynchronous.



(a) Spreading Coder



(b) Modulator

Figure 1. Spreading coder / Modulator for downlink DPCH (current method)

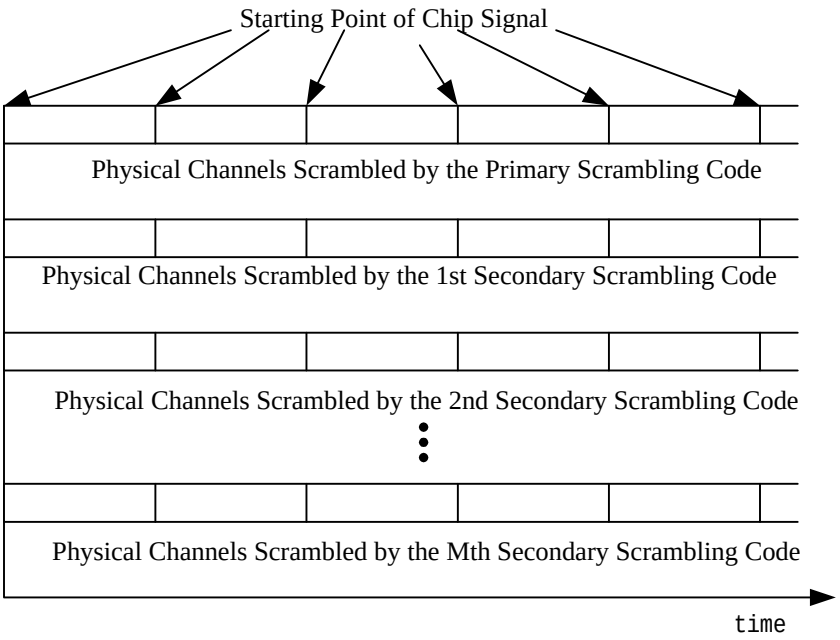


Figure 2. Timing relationship between physical channels scrambled by different scrambling codes (current method)

Proposed Method

Figures 3 and 4 illustrate the proposed method. The output of the spreading coder with the m-th SSC is time-delayed for $T_{d,m}$, where $0 \le T_{d,m} < T_c$, m = 1,2, …, M, and T_c is chip duration. When $T_{d,m} = 0$,m = 1,2, …, M, the proposed method is identical to the current method.

The advantage of proposed method is the reduction of interference between the PCHs of different scrambling codes, and the reduction of interference power is a function of time delay, $T_{d,m}$. So, the effect of time delay on the interference power will be discussed.

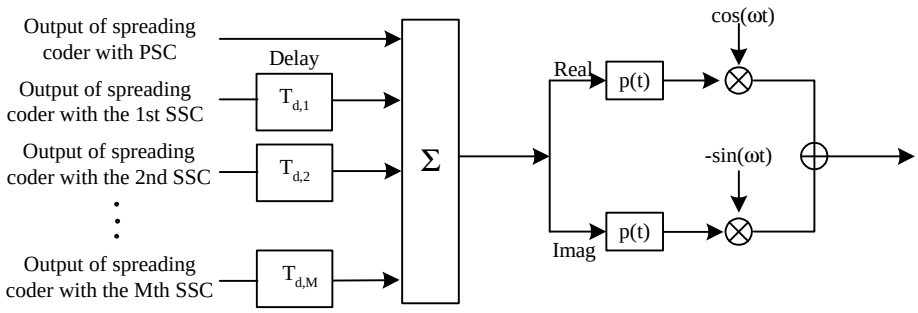


Figure 3. Modulator for downlink DPCH (proposed method)

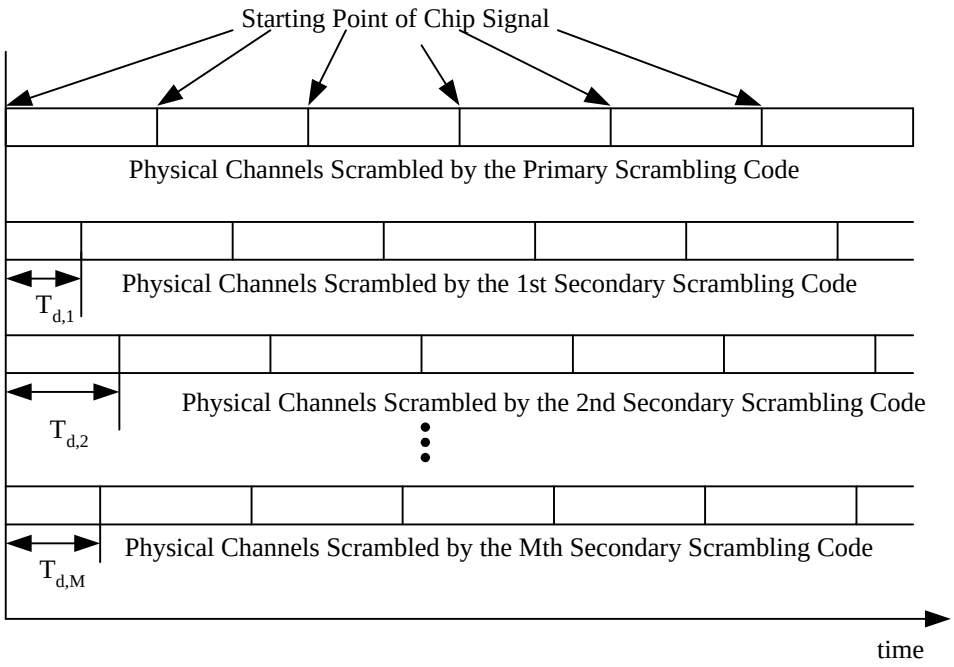


Figure 4. Timing relationship between physical channels scrambled by different scrambling codes (proposed method)

Optimal Time Delay for M=1

Interference power due to the physical channel with relative time delay T_d is proportional to $I(T_d)$ which can be expressed as

$$I(T_d) = \sum_{q=-e}^{e} \left(\int_{-\frac{eT_c}{2}}^{\frac{eT_c}{2}} P(t)P(t - qT_c - T_d)dt \right)^2 \quad (1)$$

where pulse-shaping filter P(t) is the time-limited version of the root-raised cosine (RRC), $RC_0(t)$, with roll-off α in the frequency domain [4], $e \cdot T_c$ is the non-trivial duration of pulse-shaping filter P(t). The P(t) and $RC_0(t)$ can be expressed as follows.

$$P(t) = \begin{cases} RC_o(t), & -\frac{eT_c}{2} \le t < \frac{eT_c}{2} \\ 0, & otherwise \end{cases} \quad (2)$$

$$RC_0(t) = \frac{\sin\left(p\,\frac{t}{T_C}(1-a)\right) + 4a\,\frac{t}{T_C}\cos\left(p\,\frac{t}{T_C}(1+a)\right)}{p\,\frac{t}{T_C}\left(1-\left(4a\,\frac{t}{T_C}\right)^2\right)} \quad (3)$$

The interference power $I(T_d)$ of (1) is evaluated by using numerical method and plotted as a function of T_d in Figures 5 and 6 for e = 12 and roll-off α = 0, 0.22, 0.3, and 1. As shown in Figures 5 and 6, the interference power $I(T_d)$ has the minimum value when $T_d = T_c/2$ regardless of the value of roll-off α. And, $I(T_c/2)/ I(0)$ = 0.985, 0.891, 0.850, and 0.50 for roll-off α = 0, 0.22, 0.3, and 1, respectively.

For roll-off α = 0.22, the reduction of 11% in the interference power is achieved by using our proposed method. If the roll-off value is changed to be 0.30 ((1+0.30)* 3.84cps = 5Mhz) due to the change of chip rate, the 15% reduction of interference power is shown by using this proposed method.

The normalised interference power $(I(T_d)/I(0))$ is plotted as a function of time delay for e = 4, 8, 12, and 16 in Figure 7. The interference power has the minimum value when $T_d = T_c/2$ regardless of the value of e.

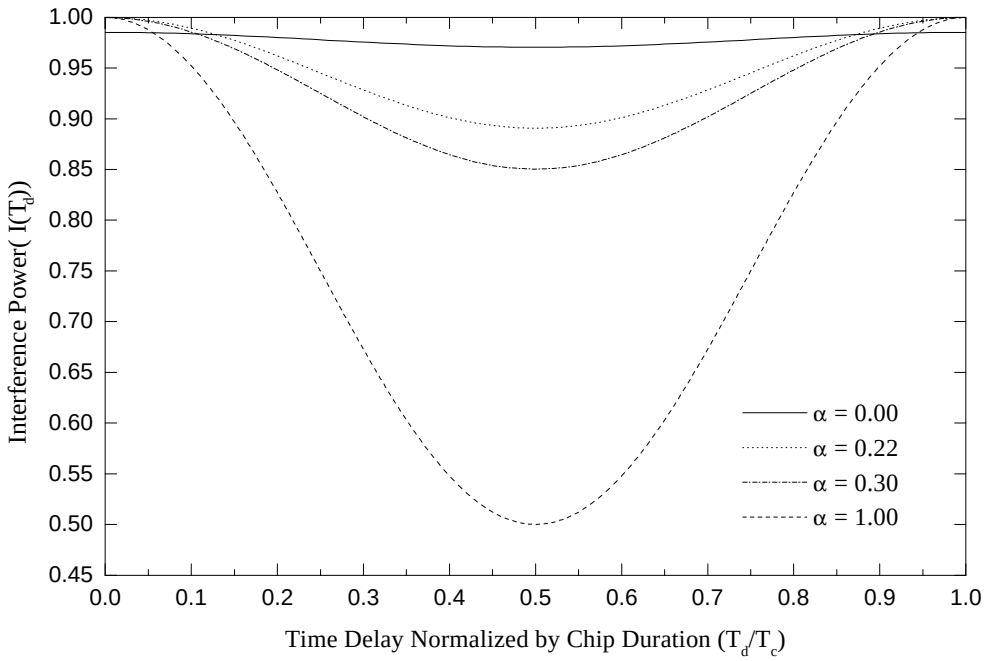


Figure 5. The interference power $(I(T_d))$

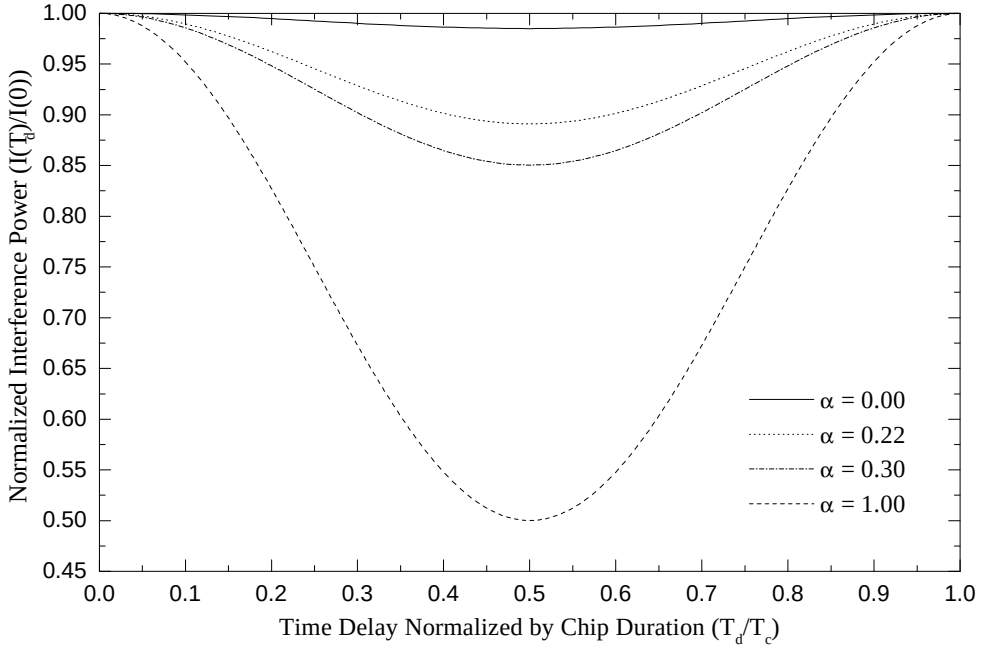


Figure 6. The normalised interference power ($I(T_d)/I(0)$)

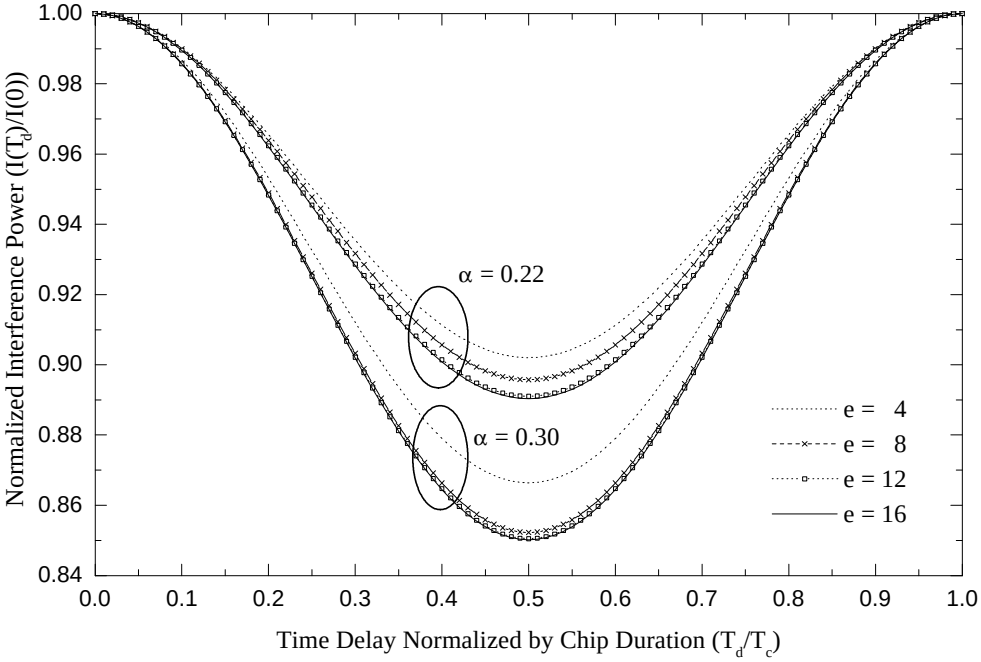


Figure 7. The normalised interference power ($I(T_d)/I(0)$) for for e = 4, 8, 12, and 16

Time Delay for M ≥ 2

Until now, we considered two physical channels that are non-orthogonal to each other (i.e., one PSC and one SSC). When multiple SSCs are used at a cell, we should set M time delay, $T_{d,m}$, m = 1,2, …, M, with considering the total interference power.

The total interference power for one PSC and M SSC is expressed as

$$S = \sum_{m=0}^{M} \sum_{\substack{n=0 \\ n \neq m}}^{M} I\left(\left|T_{d,m} - T_{d,n}\right|\right) \qquad (4)$$

where $T_{d,0}$ is the time delay for the output of the spreading coder with PSC and $T_{d,0} = 0$.

In order to make the implementation of time delay simple, the value of time delay, $T_{d,m}$, m = 1,2, …, M, is restricted by discrete value such as $T_{d,m} = g_m \cdot T_c / N$, $g_m = 0, 1, \ldots, N-1$. For N = 1, $T_{d,m}$ = 0 and this is identical to the current method. For N = 2, $T_{d,m}$ is 0 or $T_c/2$, and, for N = 4, $T_{d,m}$ is 0, $T_c/4$, $T_c/2$, or $3T_c/4$, and so on. If N is a divisor of the over-sampling rate, L (= sampling rate / chip rate), the time delay, $T_{d,m}$, is just $g_m \cdot L / N$ samples delay after spreading coder.

The time delay, $T_{d,m}$, m = 1,2, …, M, which minimizes total interference power of (4) is found out by using exhaustive search. The total interference power, S, for N = 1, 2, 4, 8 is plotted as a function of (M+1) in Figures 8 and 9 with e = 12. As we can see from Figures 8 and 9, the most of the total interference power reduction is achieved by passing from N = 1 to N = 2. When α = 0.22, the interference is reduced by 10.9% for M = 1 and 5.8% for M = 16. When α = 0.30, the interference is reduced by 15.0% for M = 1 and 7.9% for M = 16. The further interference reduction by N > 2 is negligibly small. So, we can set N = 2 (e.g., $T_{d,m} = 0$ or $T_c/2$). This property makes the implementation of time delay very simple since the sampling rate is always a multiple of both 2 and chip rate.

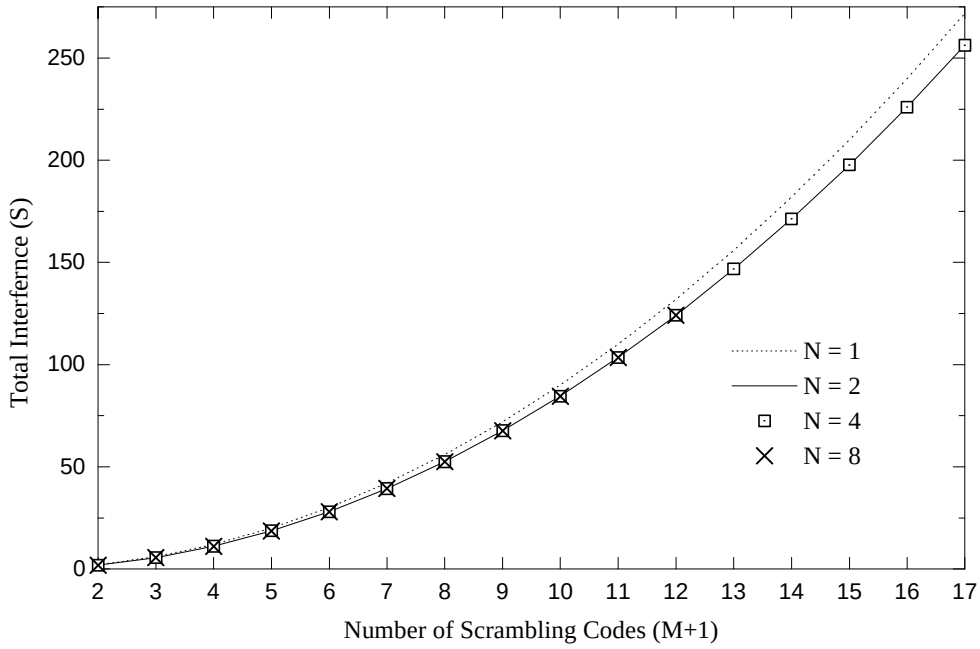


Figure 8. Total Interference Power (α = 0.22)

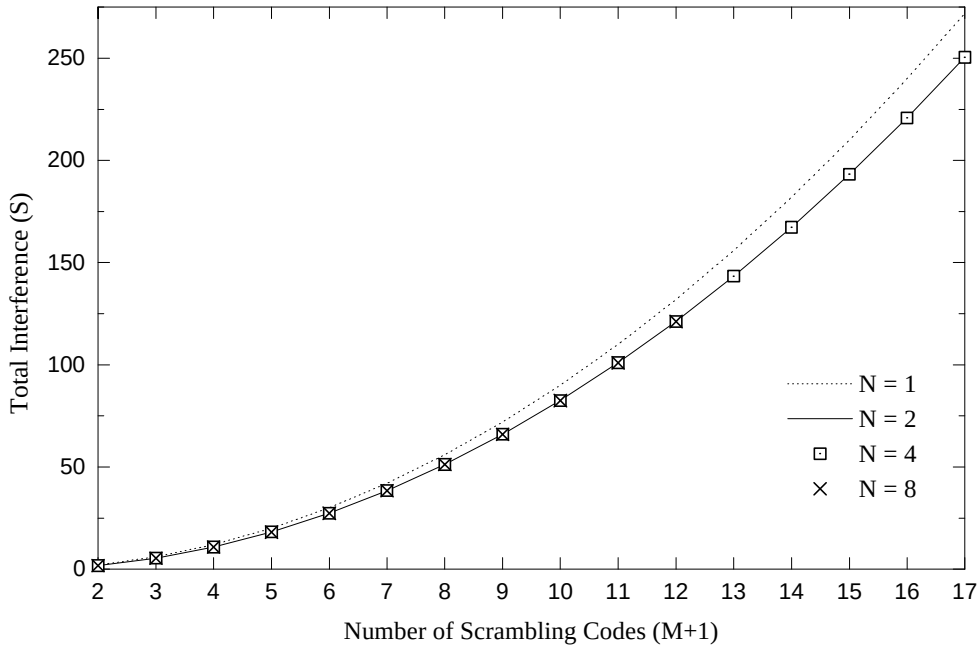


Figure 9. Total Interference Power (α = 0.30)

Time Delay for SSC

Time delay, $T_{d,m}$, can be transmitted to MS via signalling, or predefined time delay for SSC can be used. Table 1 shows the example of the time delay, $T_{d,m}$, m = 1,2, …, M, for SSC. With this table, no additional signaling of time delay is necessary between BS and MS.

Table 1. The delay for SSC

M	$T_{d,m}$
1	T_c / 2
2	0
3	T_c / 2
4	0
5	T_c / 2
6	0
7	T_c / 2
…	…
M	0 for even M and T_c/2 for odd M

Conclusions

In this document, we have proposed the improved modulation method for multiple scrambling codes which delays the output of spreading coder a few samples in order to reduce the interference power between the physical channels of different scrambling codes. The value of time delay for scrambling code is found out with considering the total interference power for all physical channels.

With this method, the total interference power is reduced by 8~15%.

References

[1] Ericsson, “Multiple scrambling codes,” TSGR1#5(99)724, Cheju, Korea, June 1-4, 1999.

[2] TS 25.213, V2.1.2, Spreading and Modulation, 3GPP TSG RAN WG1, R1-99A66.

[3] M. B. Pursley, “Performance evaluation of phase-coded spread-spectrum multiple-access communication-part I: system analysis,” IEEE Trans. Commun. Vol. COM-25, no. 8, Aug. 1977, pp. 795-799.

[4] TS 25.104, V2.0.0, UTRA (BS) FDD; Radio Transmission and Reception, 3GPP TSG RAN WG4, June 1999, RP-99362.

--- Text proposal for 25.213 ---

5 Downlink spreading and modulation

5.1 Spreading

Figure 12 illustrates the spreading and modulation for the downlink DPCH. Data modulation is QPSK where each pair of two bits are serial-to-parallel converted and mapped to the I and Q branch respectively. The I and Q branch are then spread to the chip rate with the same channelization code c_{ch} (real spreading) and subsequently scrambled by the scrambling code C_{scramb} (complex scrambling). A delay is placed after scrambling. The interval of delay is zero or one over twice chip rate. The interval of delay is the same if the same scrambling code is used.

< The interval of delay can be transmitted to UE via signalling, or a predefined interval of delay can be used.>

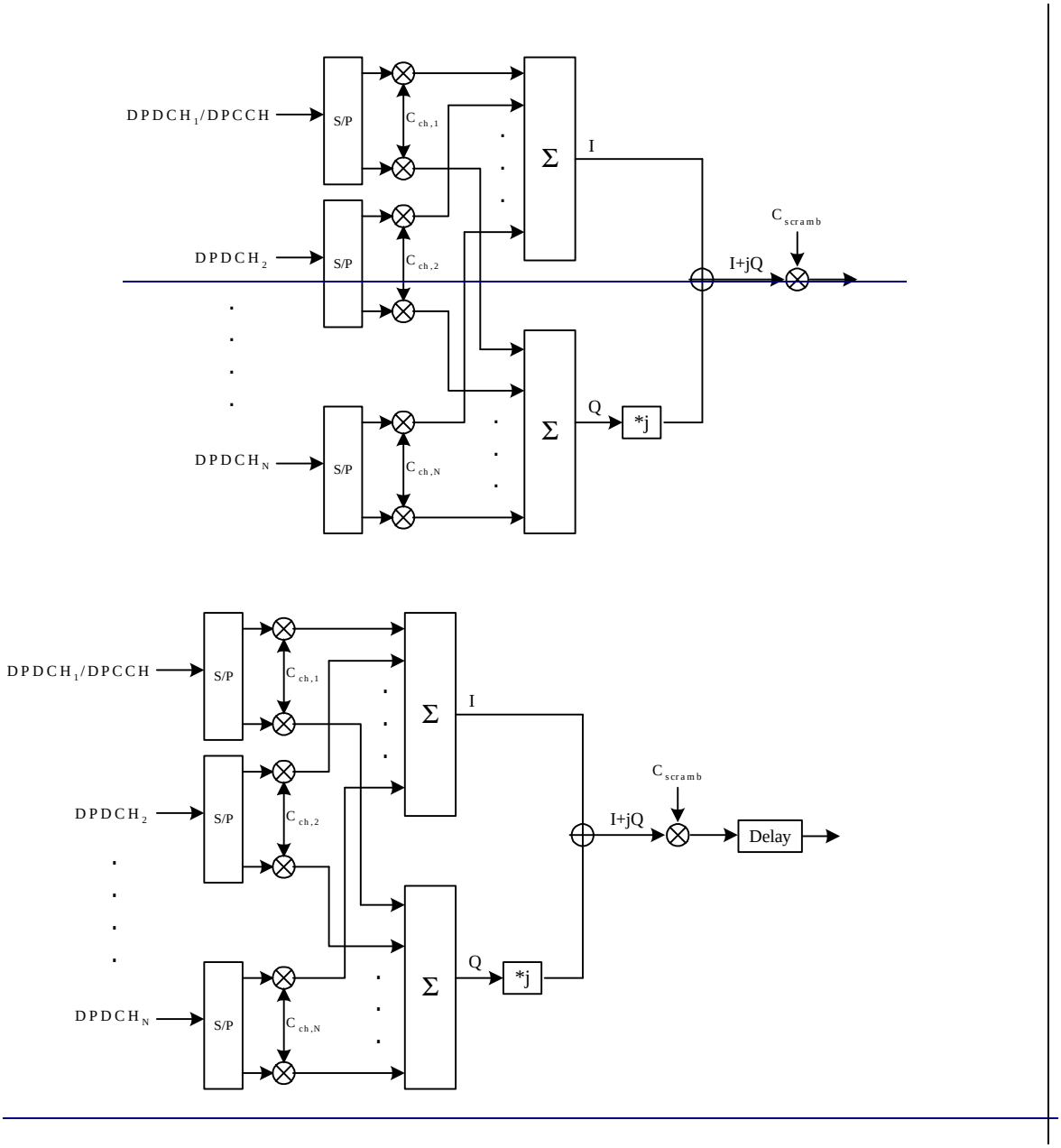


Figure 12. Spreading/modulation for downlink DPCH.