TS 25.211 V2.2.1 (1999-08)

Technical Specification

3rd Generation Partnership Project (3GPP);
Technical Specification Group (TSG)
Radio Access Network (RAN);
Working Group 1 (WG1);
Physical channels and mapping of transport channels onto physical channels (FDD)

Reference

<Workitem> (<Shortfilename>.PDF)

Keywords

<keyword[, keyword]>

3GPP

Postal address

Office address

Internet

secretariat@3gpp.org
Individual copies of this deliverable
can be downloaded from
http://www.3gpp.org

Contents

Intellectual Property Rights

<IPR notice shall be provided once correct notice is available within 3GPP>

Foreword

This Technical Specification has been produced by the 3GPP.

The contents of the present document are subject to continuing work within the TSG and may change following formal TSG approval. Should the TSG modify the contents of this TS, it will be re-released by the TSG with an identifying change of release date and an increase in version number as follows:

Version 3.y.z

where:

x   the first digit:

    1   presented to TSG for information;

    2   presented to TSG for approval;

    3   Indicates TSG approved document under change control.

y   the second digit is incremented for all changes of substance, i.e. technical enhancements, corrections, updates, etc.

z   the third digit is incremented when editorial only changes have been incorporated in the specification;

1   Scope

This specification describes the characteristics of the Layer 1 transport channels and physicals channels in the FDD mode of UTRA. The main objectives of the document are to be a part of the full description of the UTRA Layer 1, and to serve as a basis for the drafting of the actual technical specification (TS).

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

<Editor's Note: Relevant references should be discussed>

[1] TS 25.201 (V2.0.0): "Physical layer - general description"

[2] TS S1.02 (V1.0.0): "UE physical layer capabilities"

[3] TS 25.211 (V2.0.0): "Physical channels and mapping of transport channels onto physical channels (FDD)"

[4] TS 25.212 (V1.0.0): "Multiplexing and channel coding (FDD)"

[5] TS 25.213 (V2.0.0): "Spreading and modulation (FDD)"

[6] TS 25.214 (V1.0.0): "Physical layer procedures (FDD)"

[7] TS 25.221 (V1.0.0): "Transport channels and physical channels (TDD)"

[8] TS 25.222 (V1.0.0): "Multiplexing and channel coding (TDD)"

[9] TS 25.223 (V2.0.0): "Spreading and modulation (TDD)"

[10] TS 25.224 (V1.0.0): "Physical layer procedures (TDD)"

[11] TS 25.231 (V0.2.0): "Measurements"

[12] TS 25.301 (V3.0.0): "Radio Interface Protocol Architecture"

[13] TS 25.302: "Services Provided by the Physical Layer"

[14] TS 25.401: "UTRAN Overall Description"

3 Definitions, symbols and abbreviations

3.1 Definitions

For the purposes of the present document, the [following] terms and definitions [given in ... and the following] apply.

<defined term>: <definition>.

example: text used to clarify abstract rules by applying them literally.

3.2 Symbols

For the purposes of the present document, the following symbols apply:

<symbol>   <Explanation>

3.3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

<ACRONYM> <Explanation>

AI   Acquisition Indicatior
AICH   Acquisition Indication Channel

BCH   Broadcast Channel
CCPCH   Common Control Physical Channel
CCTrCH   Coded Composite Transport Channel
CPCH   Common Packet Channel
DCH   Dedicated Channel
DPCCH   Dedicated Physical Control Channel
DPCH   Dedicated Physical Channel
DPDCH   Dedicated Physical Data Channel
DSCH   Downlink Shared Channel
FACH   Forward Access Channel
FAUSCH   Fast Uplink Signalling Channel
FBI   Feedback Information
MUI   Mobile User Identifier
PCH   Paging Channel
PCPCH   Physical Common Packet Channel
PDSCH   Physical Downlink Shared Channel
PI   Page Indicatior
PICH   Page Indication Channel
PRACH   Physical Random Access Channel
PSCCCH   Physical Shared Channel Control Channel
RACH   Random Access Channel
RNC   Radio Network Controller
SCH   Synchronisation Channel
SF   Spreading Factor
SFN   System Frame Number
STTD   Space Time Transmit Diversity
TFCI   Transport Format Combination Indicator
TSTD   Time Switched Transmit Diversity
TPC   Transmit Power Control
UE   User Equipment

4   Transport channels

Transport channels are the services offered by Layer 1 to the higher layers.

A transport channel is defined by how and with what characteristics data is transferred over the air interface. A general classification of transport channels is into two groups:

- Common Channels (where there is a need for in-band identification of the UEs when particular UEs are addressed)

- Dedicated Channels (where the UEs are identified by the physical channel, i.e. code and frequency)

General concepts about transport channels are described in 3GPP RAN TS25.302 (L2 specification).

4.1   Dedicated transport channels

There exists only one type of dedicated transport channel, the Dedicated Channel (DCH).

<Note: WG1 concluded that FAUSCH will not be included in release 99.>

[There are two types of dedicated transport channel, the Dedicated Channel (DCH) and the Fast Uplink Signalling Channel (FAUSCH).]

4.1.1   DCH – Dedicated Channel

The Dedicated Channel (DCH) is a downlink or uplink transport channel that is used to carry user or control information between the network and the UE. [The DCH thus corresponds to the three channels Dedicated Traffic Channel (DTCH),

Stand-Alone Dedicated Control Channel (SDCCH), and Associated Control Channel (ACCH) defined within ITU-R M.1035.] The DCH is transmitted over the entire cell or over only a part of the cell using lobe-forming antennas. The Dedicated Channel (DCH) is characterized by the possibility of fast rate change (every 10ms), fast power control and inherent addressing of UEs.

4.1.2   FAUSCH – Fast Uplink Signalling Channel

<Note: WG1 concluded that FAUSCH will not be included in release 99.>

 The Fast Uplink Signalling Channel (FAUSCH) is an optional uplink transport channel that is used to carry control information from a UE. The FAUSCH is always received from the entire cell.

4.2   Common transport channels

There are six types of common transport channels: BCH, FACH, PCH, RACH, DSCH, and DSCH control channel.

4.2.1   BCH – Broadcast Channel

The Broadcast Channel (BCH) is a downlink transport channel that is used to broadcast system- and cell-specific information. The BCH is always transmitted over the entire cell with a low fixed bit rate.

4.2.2   FACH – Forward Access Channel

The Forward Access Channel (FACH) is a downlink transport channel that is used to carry control information to a UE when the system knows the location cell of the UE. The FACH may also carry short user packets. The FACH is transmitted over the entire cell or over only a part of the cell using lobe-forming antennas. The FACH uses slow power control and requires in-band identification of the UEs.

4.2.3   PCH – Paging Channel

The Paging Channel (PCH) is a downlink transport channel that is used to carry control information to a UE when the system does not know the location cell of the UE. The PCH is always transmitted over the entire cell and requires inband identification of the UE. The transmission of the PCH is associated with the transmission of a physical layer signal, the Paging Indicator, to support efficient sleep-mode procedures.

4.2.4   RACH – Random Access Channel

The Random Access Channel (RACH) is an uplink transport channel that is used to carry control information from the UE. The RACH may also carry short user packets. The RACH is always received from the entire cell. The RACH is characterized by a collision risk and by the use of open loop power control.

4.2.5   CPCH – Common Packet Channel

The CPCH is an uplink transport channel that is used to carry small and medium sized packets. CPCH is a contention based random access channel used for transmission of bursty data traffic. CPCH is associated with a dedicated channel on the downlink which provides power control for the uplink CPCH.

4.2.6   DSCH – Downlink Shared Channel

<Note: WG1 concluded that DSCH control channel will not be included in release 99.>

 The downlink shared channel (DSCH) is a downlink transport channel shared by several UEs carrying dedicated control or traffic data.

Two possibilities exist for the DSCH:

• the DSCH is associated with a DCH,

- the DSCH is associated with a DSCH control channel.

It is for further study whether both possibilities are needed.

4.2.7 DSCH Control Channel

<Note: WG1 concluded that DSCH control channel will not be included in release 99.>

The DSCH control channel is a downlink transport channel carrying control information to the UE for operating the DSCH when not associated with a DCH. Such control information corresponds among other things to resource allocation messages and L1 control information such as TPC, that are not available on the DSCH.

5 Physical channels

Physical channels typically consist of a three-layer structure of superframes, radio frames, and time slots, although this is not true for all physical channels. Depending on the symbol rate of the physical channel, the configuration of radio frames or time slots varies.

- - Superframe : A Superframe has a duration of 720ms and consists of 72 radio frames. The superframe boundaries are defined by the System Frame Number (SFN):

     - The head radio frame of superframe : SFN mod 72=0.

     - The tail radio frame of superframe: SFN mod 72=71.

- - Radio frame : A Radio frame is a processing unit which consists of 15 time slots.
- - Time slot   : A Time slot is a unit which consists of the set of information symbols. The number of symbols per time slot depends on the physical channel.
- - Symbol   : One symbol consists of a number of chips. The number of chips per symbol is equivalent to the spreading factor of the physical channel.

5.1 The physical resource

The basic physical resource is the code/frequency plane. In addition, on the uplink, different information streams may be transmitted on the I and Q branch. Consequently, a physical channel corresponds to a specific carrier frequency, code, and, on the uplink, relative phase (0 or $\pi/2$).

5.2 Uplink physical channels

5.2.1 Dedicated uplink physical channels

There are two types of uplink dedicated physical channels, the uplink Dedicated Physical Data Channel (uplink DPDCH) and the uplink Dedicated Physical Control Channel (uplink DPCCH).

The DPDCH and the DPCCH are I/Q code multiplexed within each radio frame (see TS 25.213).

The uplink DPDCH is used to carry dedicated data generated at Layer 2 and above, i.e. the dedicated transport channel (DCH). There may be zero, one, or several uplink DPDCHs on each Layer 1 connection.

The uplink DPCCH is used to carry control information generated at Layer 1. The Layer 1 control information consists of known pilot bits to support channel estimation for coherent detection, transmit power-control (TPC) commands, feedback information (FBI), and an optional transport-format combination indicator (TFCI). The transport-format combination indicator informs the receiver about the instantaneous parameters of the different transport channels multiplexed on the uplink DPDCH, and corresponds to the data transmitted in the same frame. It is the UTRAN that determines if a TFCI should be transmitted, hence making it is mandatory for all UEs to support the use of TFCI in the uplink. There is one and only one uplink DPCCH on each Layer 1 connection.

Figure 1 shows the frame structure of the uplink dedicated physical channels. Each frame of length 10 ms is split into 15 slots, each of length T_{slot} = 2560 chips, corresponding to one power-control period. A super frame corresponds to 72 consecutive frames, i.e. the super-frame length is 720 ms.
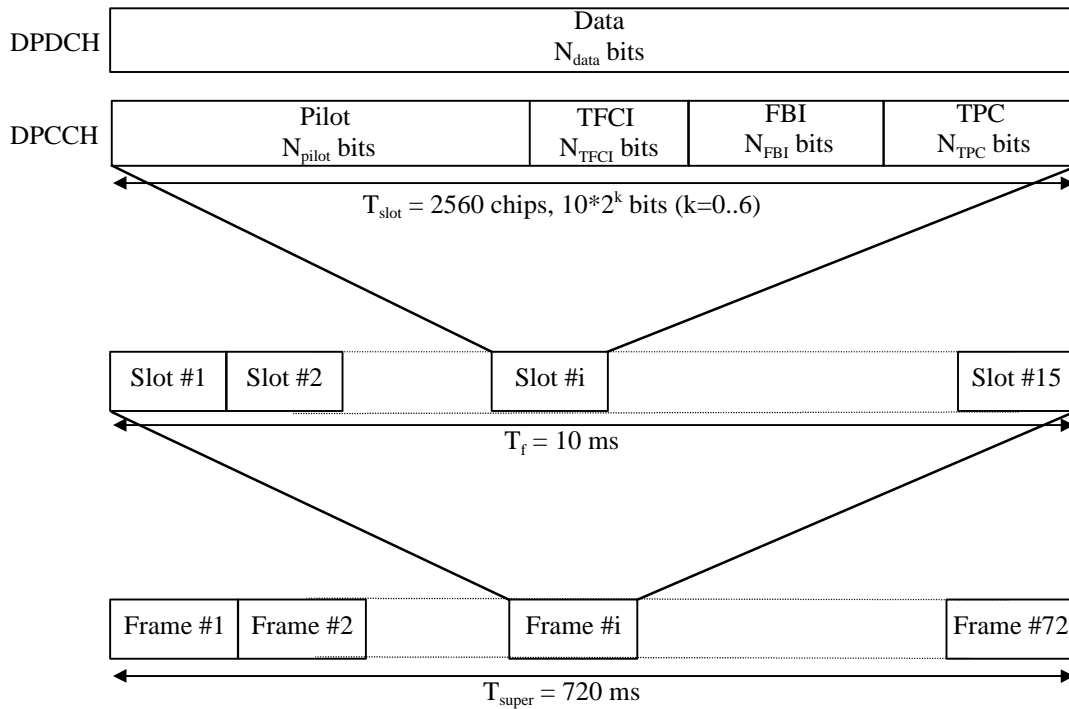
Figure 1: Frame structure for uplink DPDCH/DPCCH.

The parameter k in Figure 1 determines the number of bits per uplink DPDCH/DPCCH slot. It is related to the spreading factor SF of the physical channel as $SF = 256/2^k$. The spreading factor may thus range from 256 down to 4. Note that an uplink DPDCH and uplink DPCCH on the same Layer 1 connection generally are of different rates, i.e. have different spreading factors and different values of k.

The exact number of bits of the different uplink DPCCH fields in Figure 1 (N_{pilot}, N_{TPC}, N_{FBI}, and N_{TFCI}) is yet to be determined. The field order is fixed. A limited set of field combinations will be defined.

<Editors note: See Adhoc #7: The spreading factor for the DPCCH fields and the length (in bits) of each field is negotiated at connection set up. Both the spreading factor and the length of the fields may be negotiated during the connection through higher layer signalling.>

The values for the number of bits per field are given in Table 1 and Table 2. The channel bit and symbol rates given in Table 1 are the rates immediately before spreading. The pilot patterns are given in Table 3 and Table 4, the TPC bit pattern is given in Table 5.

The N_{FBI} bits are used to support techniques requiring feedback between the UE and the UTRAN Access Point (=cell transceiver), including feedback (FB) mode transmit diversity and site selection diversity (SSDT). The exact details of the FBI field are in the frame structure shown in Figure 2 and described below.are for further study.
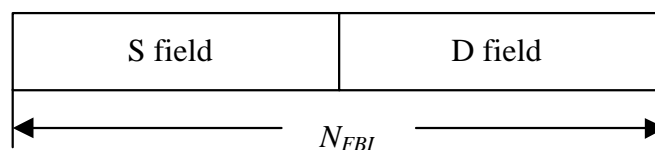
Figure 2: Details of FBI field

The S field is used for SSDT signalling, while the D field is used for FB Mode Transmit Diversity Signalling. Each of the S and D fields can be length 0,1 or 2, with a total FBI field size N_{FBI} according to Table 2 (DPCCH fields).

Simultaneous use of SSDT power control and FB Mode Transmit Diversity requires that both the S and D fields be of length 1. The use of these FBI fields is described in 25.214

Table 1: DPDCH fields

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}
15	15	256	150	10	10
30	30	128	300	20	20
60	60	64	600	40	40
120	120	32	1200	80	80
240	240	16	2400	160	160
480	480	8	4800	320	320
960	960	4	9600	640	640

There are two types of Uplink Dedicated Physical Channels; those that include TFCI(e.g. for several simultaneous services) and those that do not include TFCI(e.g. for fixed-rate services). These types are reflected by the duplicated rows of Table 2. The channel bit and symbol rates given in Table 2 are the rates immediately before spreading.

Table 2: DPCCH fields

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{pilot}	N_{TPC}	N_{TFCI}	N_{FBI}
15	15	256	150	10	6	2	2	0
15	15	256	150	10	8	2	0	0
15	15	256	150	10	5	2	2	1
15	15	256	150	10	7	2	0	1
15	15	256	150	10	6	2	0	2
15	15	256	150	10	5	1	2	2

The pilot bit pattern is described in Table 3 and Table 4. The shadowed part can be used as frame synchronization words. (The value of the pilot bit other than the frame synchronization word shall be "1".)

Table 3: Pilot bit patterns for uplink DPCCH with N_{pilot} = 5 and 6.

<Editors note: Pilot bit patterns to be updated for 15 slots/frame.>

	$N_{pilot} = 5$					$N_{pilot} = 6$					
Bit #	0	1	2	3	4	0	1	2	3	4	5
Slot #1	1	1	1	1	0	1	1	1	1	1	0
2	0	0	1	1	0	1	0	0	1	1	0
3	0	1	1	0	1	1	0	1	1	0	1
4	0	0	1	0	0	1	0	0	1	0	0
5	1	0	1	0	1	1	1	0	1	0	1
6	1	1	1	1	0	1	1	1	1	1	0
7	1	1	1	0	0	1	1	1	1	0	0
8	1	0	1	0	0	1	1	0	1	0	0
9	0	1	1	1	0	1	0	1	1	1	0
10	1	1	1	1	1	1	1	1	1	1	1
11	0	1	1	0	1	1	0	1	1	0	1
12	1	0	1	1	1	1	1	0	1	1	1
13	1	0	1	0	0	1	1	0	1	0	0
14	0	0	1	1	1	1	0	0	1	1	1
15	0	0	1	1	1	1	0	0	1	1	1

Table 4: Pilot bit patterns for uplink DPCCH with N_{pilot} = 7 and 8.

<Editors note: Pilot bit patterns to be updated for 15 slots/frame.>

	$N_{pilot} = 7$							$N_{pilot} = 8$							
Bit #	0	1	2	3	4	5	6	0	1	2	3	4	5	6	7
Slot #1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0
2	1	0	0	1	1	0	1	1	0	1	0	1	1	1	0
3	1	0	1	1	0	1	1	1	0	1	1	1	0	1	1
4	1	0	0	1	0	0	1	1	0	1	0	1	0	1	0
5	1	1	0	1	0	1	1	1	1	1	0	1	0	1	1
6	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0
7	1	1	1	1	0	0	1	1	1	1	1	1	0	1	0
8	1	1	0	1	0	0	1	1	1	1	0	1	0	1	0
9	1	0	1	1	1	0	1	1	0	1	1	1	1	1	0
10	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
11	1	0	1	1	0	1	1	1	0	1	1	1	0	1	1
12	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
13	1	1	0	1	0	0	1	1	1	1	0	1	0	1	0
14	1	0	0	1	1	1	1	1	0	1	0	1	1	1	1
15	1	0	0	1	1	1	1	1	0	1	0	1	1	1	1

The relationship between the TPC bit pattern and transmitter power control command is presented in Table 5.

Table 5: TPC Bit Pattern

TPC Bit Pattern		Transmitter power control command
$N_{TPC} = 1$	$N_{TPC} = 2$	
1	11	1
0	00	0

In each radio frame, the TFCI value corresponds to a certain combination of bit rates of the DCHs currently in use. This correspondence is (re-)negotiated at each DCH addition/removal. For default TFCI there is one code word of length 30 bits. For extended TFCI there are 2 code words of length 15 bits giving the same total number of encoded TFCI bits per frame as for default TFCI. The 30 encoded TFCI bits are divided evenly among the 15 time slots, 2 bits per slot.

Multi-code operation is possible for the uplink dedicated physical channels. When multi-code transmission is used, several parallel DPDCH are transmitted using different channelization codes, see TS 25.213. However, there is only one DPCCH per connection.

5.2.2   Common uplink physical channels

5.2.2.1   Physical Random Access Channel

The Physical Random Access Channel (PRACH) is used to carry the RACH.

[The Physical Random Access Channel (PRACH) is used to carry the RACH and the FAUSCH.]

5.2.2.1.1   RACH transmission

<Editors note: Section needs to be updated for 15 slots/frame.>

The random-access transmission is based on a Slotted ALOHA approach with fast acquisition indication. The UE can start the transmission at a number of well-defined time-offsets, relative to the frame boundary of every second frame of the received BCH of the current cell. The different time offsets are denoted *access slots*. There are 15 access slots per two frames and they are spaced 5120 chips1.25 ms apart. as illustrated in Figure 3. Figure 2 shows the access slot numbers and their spacing to each other. Information on what access slots are available in the current cell is broadcast on the BCH.
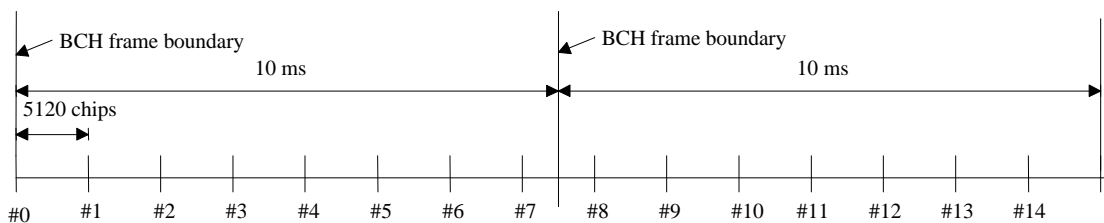
Figure 3: RACH access slot numbers and their spacing.
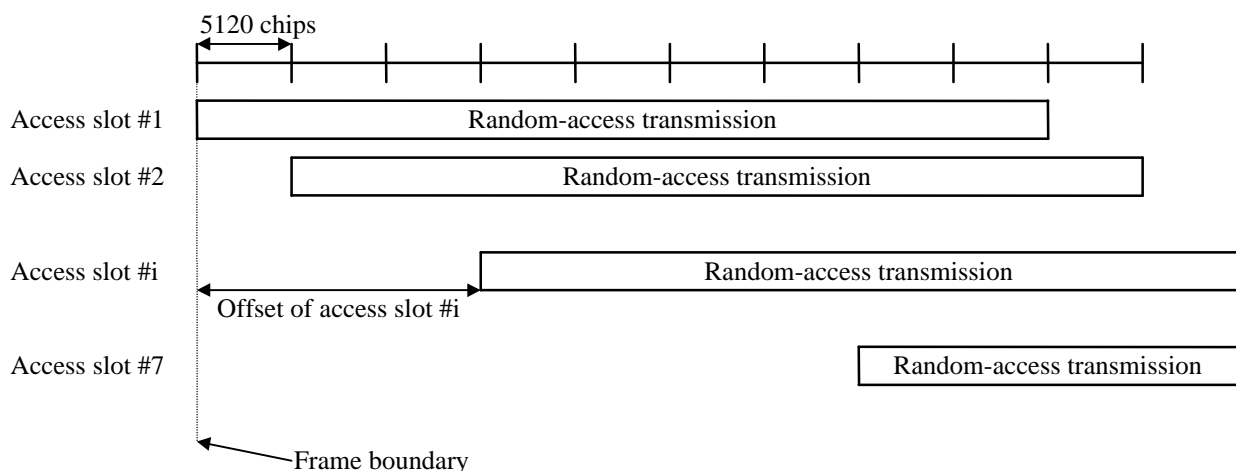
Figure 4: PRACH allocated for RACH access slots.

The structure of the random-access transmission of Figure 4, is shown in Figure 5. The random-access transmission consists of one or several *preambles* of length ~~1 ms~~4096 chips and a *message* of length 10 ms.

| Preamble | | Preamble | .... | Preamble | | Message part |

4096 chips   10 ms

Figure 5: Structure of the random-access transmission.

5.2.2.1.2   RACH preamble part

~~<Note: WG1 decided to use a different spreading code scheme. An additional set of differential signatures has been decided. A detailed description of the preamble spreading and of the signatures is given in TS 25.213.>~~

The preamble part of the random-access burst consists of <u>256 repetitions of a signature, which is comprised of</u> ~~a~~ *~~signature~~ of length* 16 complex symbols ±1(+j). There are a total of 16 different signatures, based on the <u>Hadamard</u> ~~Orthogonal Gold~~ code set of length 16 (see TS 25.213 for more details).

5.2.2.1.3   RACH message part

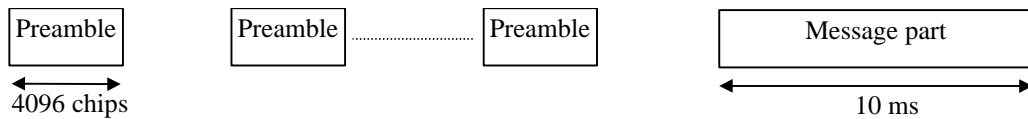Figure 6 shows the structure of the Random-access message part. The 10 ms message is split into 15 slots, each of length $T_{slot} = 2560$ chips. Each slot consists of two parts, a data part that carries Layer 2 information and a control part that carries Layer 1 control information. The data and control parts are transmitted in parallel.

The data part consists of $10*2^k$ bits, where k=0,1,2,3. This corresponds to a spreading factor of 256, 128, 64, and 32 respectively for the message data part.

The control part consists of 8 known pilot bits to support channel estimation for coherent detection and 2 bits of rate information. This corresponds to a spreading factor of 256 for the message control part. The total number of rate-information bits in the random-access message is thus $15*2 = 30$. The rate information indicates the spreading factor or, equivalently, the number of bits of the data part of the random-access message. The coding of the rate information is the same as that of the TFCI, see further TS 25.212, Section 4.3.

Data | Data N_{data} bits |

Control | Pilot N_{pilot} bits | TFCI N_{TFCI} bits |

$T_{slot} = 2560$ chips, $10*2^k$ bits (k=0..3)

| Slot #1 | Slot #2 | | Slot #i | | Slot #15 |

Random-access message $T_{RACH} = 10$ ms
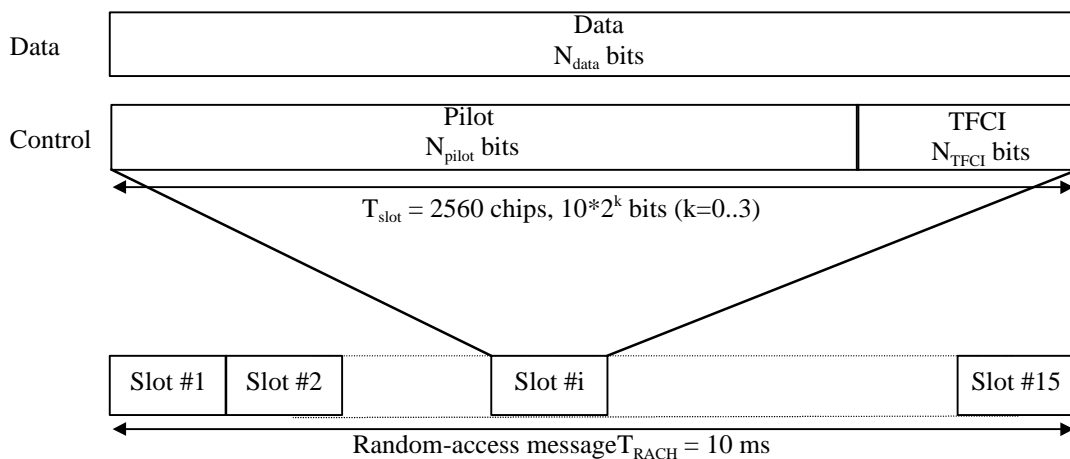
Figure 6: Structure of the random-access message part.

Table 6: Random-access message data fields.

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}
15	15	256	150	10	10
30	30	128	300	20	20
60	60	64	600	40	40
120	120	32	1200	80	80

Table 7: Random-access message control fields.

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{pilot}	N_{TFCI}
15	15	256	150	10	8	2

5.2.2.1.4 FAUSCH transmission

<Note: WG1 concluded that FAUSCH will not be included in release 99.>

<Editors note: FAUSCH sections need to be updated for 15 slots/frame.>
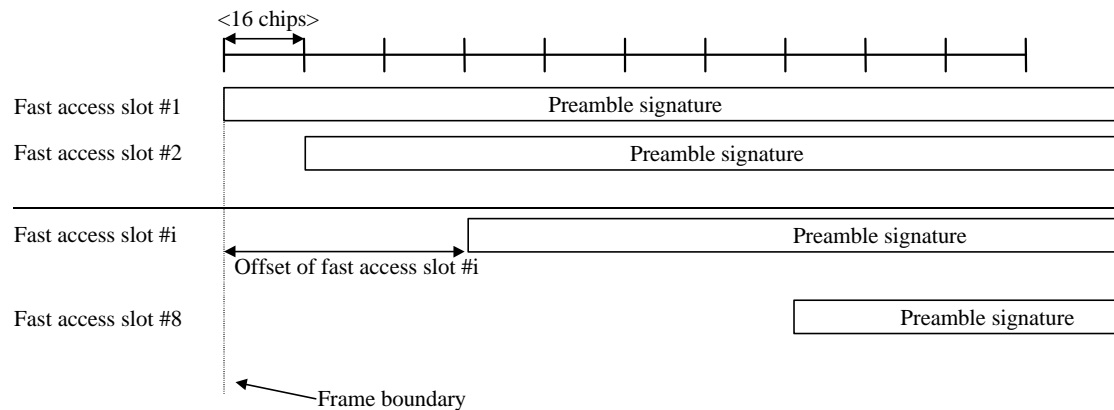
Figure 7: PRACH used for FAUSCH fast access slots.

The Fast Uplink Physical Channel (FAUSCH) is based on the transmission of a signature of length 16 complex symbols $\pm(1+j)$. The signature is one of the set of signatures used for the RACH preamble. Signature no.[8] is selected because it has the best correlation properties. Each symbol is spread with a 256 chip real Orthogonal Gold code. A time slot is allocated to the UE by the network when entering Connected Mode but the allocation may be updated with appropriate signalling. To avoid the possibility of collisions only one UE is allowed to transmit with a given signature in a particular time slot. Thus the UE can start the transmission of the FAUSCH at an assigned time offset relative to the frame boundary of the received BCH of the current cell. The different time offsets are denoted *fast access slots* and are spaced [16] chips apart as illustrated in Figure 5. To avoid possible confusion of transmissions from different UEs the separation between allocations of fast access slots to different UEs must be sufficient to allow for any round-trip delay resulting from the physical distance between network and UE. Therefore the allocation of fast access slots may be limited by the network to a subset of those available, depending on the deployment scenario.

5.2.2.1.5 Sharing of PRACH by RACH and FAUSCH

<Note: WG1 concluded that FAUSCH will not be included in release 99.>

~~FAUSCH uses only the preamble part of PRACH. The RACH and FAUSCH transmissions could use different Gold Codes for spreading the signatures, but the complexity of the uplink receiver is significantly reduced if the same Gold Code is used. Low interference between RACH and FAUSCH can then be achieved by restricting the allocation of RACH access slots and FAUSCH fast access slots so that the respective transmissions occur in different parts of the 10 ms frame. The partitioning of the frame is flexible. For example, if RACH access slots are spaced 2.5 ms apart, then FAUSCH fast access slots could be allocated in the gaps. The UE can determine the available RACH access slots my monitoring the BCH. The FAUSCH fast access slots are individually allocated to a specific UE.~~

5.2.2.2 Physical Common Packet Channel

The Physical Common Packet Channel (PCPCH) is used to carry the CPCH.

<Editors note: The detailed description of the uplink and downlink Common Packet Channels specifications will be developed as a result of further discussions on the reflector. This also includes the determination of all necessary parameters for the operation of the Common Packet Channel.

Also note that text will be developed for Section 7 containing timing issues of the uplink and downlink transmissions associated with the Common Packet Channel.>

5.2.2.3 Physical Fast Uplink Signalling Channel

<Note: WG1 concluded that FAUSCH and hence PFAUSCH will not be included in release 99.>

The Physical Fast Uplink Signalling Channel (PFAUSCH) is used to carry the FAUSCH.

5.2.2.3.1 FAUSCH transmission
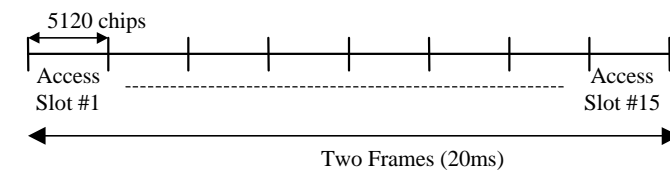
Figure 8: PFAUSCH access slots.

The PFAUSCH consists of 15 access slots, offset in time, by multiples of 5120 chips, from the boundary of every second frame of the received BCH of the current cell. Information on what access slots are available within the current cell is broadcast on the BCH.
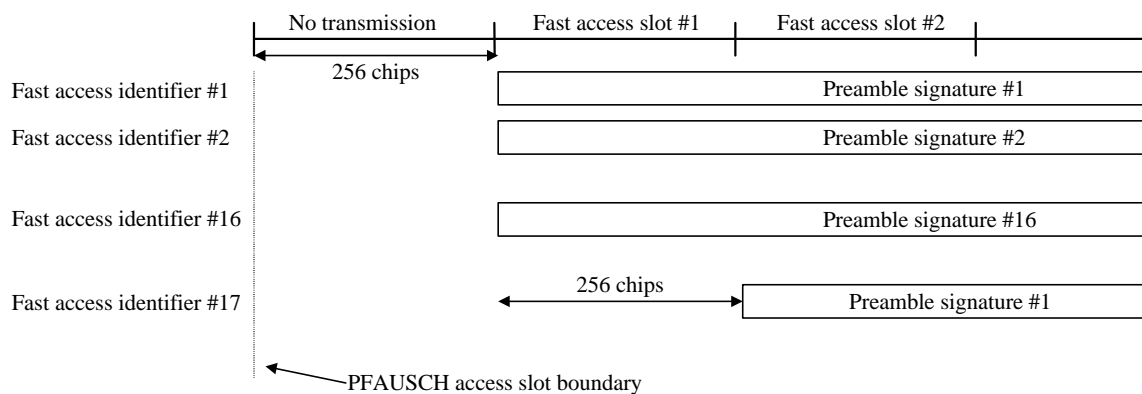
Figure 9: PFAUSCH used for FAUSCH fast access identifiers.

The Fast Uplink Physical Channel (FAUSCH) is based on the transmission of signatures of length 16 complex symbols $\pm(1+j)$. The signatures are the same set of signatures used for the RACH preamble. The signatures are spread with a 4096 Long Code, as per the RACH. A *fast access identifier*, comprising a unique combination of signature and time slot, together with a PFAUSCH access slot number, may be

allocated to the UE by the network when entering Connected Mode, but the allocation may be updated with appropriate signalling.

For fast access identifier #i, within a particular PFAUSCH access slot, the assigned fast access slot is given by int(((i-1)/16)+1), and the preamble is (i-1)mod16 + 1.

To avoid the possibility of collisions, only one UE is allowed to transmit with a given signature in a particular time slot. Thus the UE can start the transmission of the FAUSCH at an assigned time offset relative to the boundary of the PFAUSCH access slot. The different time offsets are denoted *fast access slots* and are spaced 256 chips apart as illustrated in Figure 5. To avoid possible confusion of transmissions from different UEs, the separation between allocations of fast access slots to different UEs with the same signature must be sufficient to allow for any round-trip delay resulting from the physical distance between network and UE. Therefore the allocation of fast access slots may be limited by the network to a subset of those available, depending on the deployment scenario.

5.3   Downlink physical channels

5.3.1   Downlink Transmit Diversity

Table 8 summarizes the possible application of open and closed loop Transmit diversity modes on different downlink physical channels.

Table 8: Application of Tx diversity modes on downlink physical channels.

Channel	Open loop mode	Closed loop mode	Note
PCCPCH	X	N/A	STTD applied only to data symbols. The last odd data symbol in every frame (10 msec.) is not STTD encoded.
SCH	X	N/A	TSTD used.
SCCPCH	X	N/A	
DPCH	X	X	For the 7.5 ksps channel, the last odd data symbol in every frame (10 msec.) is not STTD encoded.
PDSCH (associated with DPCH)	X	X	
AICH	X	N/A	Only if closed loop Tx diversity is used in the cell and/or open loop mode is used on PCCPCH.

N/A = Not applied
X = Can be applied

5.3.1.1   Open loop transmit diversity

5.3.1.1.1   Space time block coding based transmit antenna diversity (STTD)

The open loop downlink transmit diversity employs a space time block coding based transmit diversity (STTD). The STTD encoding is used optionally at the base station. Its use at the mobile is mandatory. A block diagram of the transmitter and a generic STTD encoder are shown in the Figure 10 and Figure 11 below. Channel coding, rate matching and interleaving is done as in the non-diversity mode.
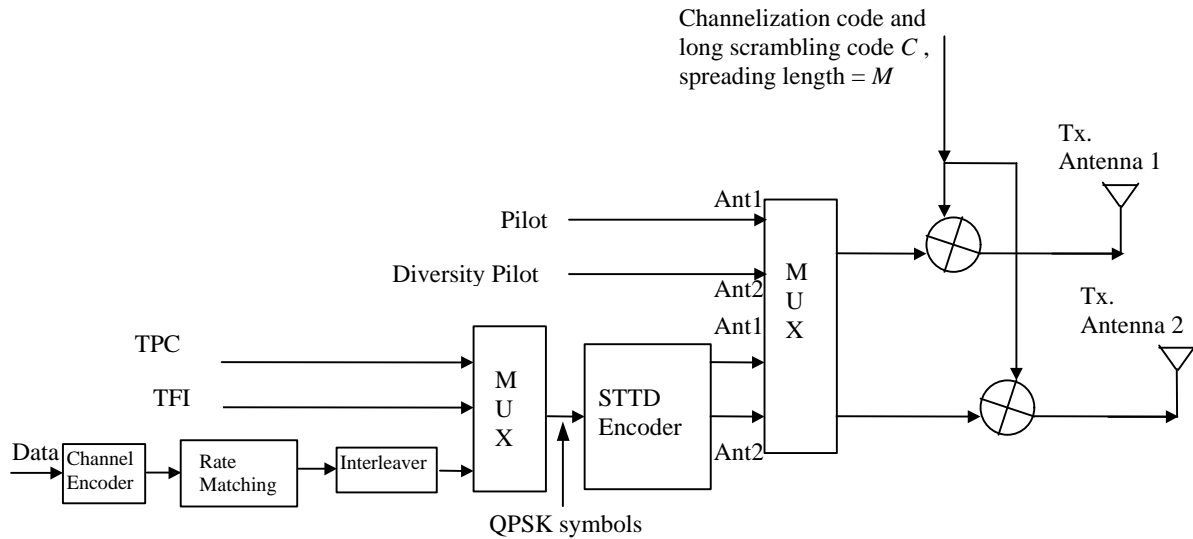
Figure 10: Block diagram of the transmitter (STTD).
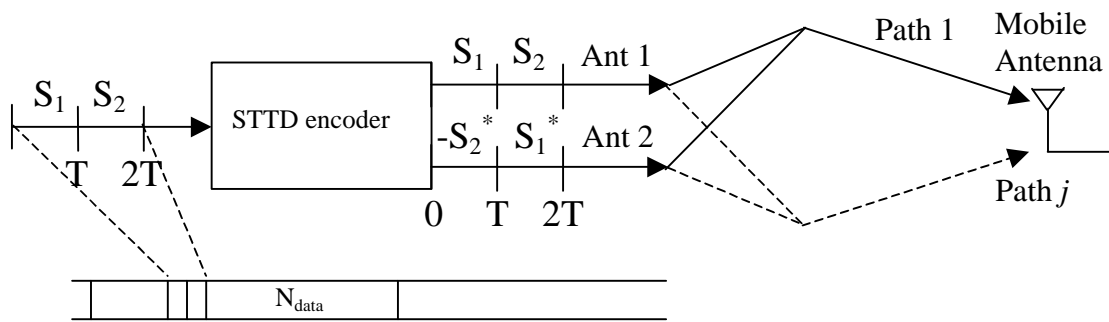
Figure 11: Block diagram of STTD encoder. The symbols S_1, S_2 are QPSK symbols and T denotes the symbol time.

5.3.1.1.2 Time Switched Transmit Diversity for SCH (TSTD)

TSTD is used optionally at the base station. Its use at the UE is mandatory. A block diagram of the transmitter using TSTD for SCH and STTD for PCCPCH is shown in Figure 12.
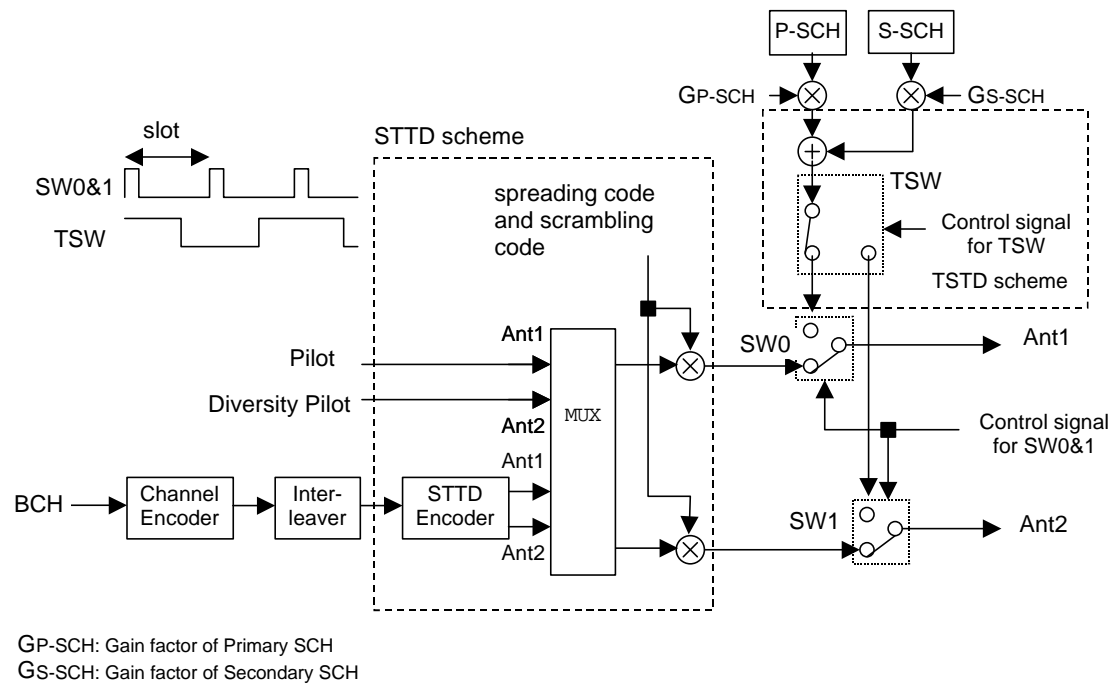
Figure 12: Multiplexing scheme of SCH (TSTD) and PCCPCH (STTD)

5.3.2   Dedicated downlink physical channels

There is only one type of downlink dedicated physical channel, the Downlink Dedicated Physical Channel (downlink DPCH).

Within one downlink DPCH, dedicated data generated at Layer 2 and above, i.e. the dedicated transport channel (DCH), is transmitted in time-multiplex with control information generated at Layer 1 (known pilot bits, TPC commands, and an optional TFCI). The downlink DPCH can thus be seen as a time multiplex of a downlink DPDCH and a downlink DPCCH, compare Section 5.2.1. It is the UTRAN that determines if a TFCI should be transmitted, hence making it is mandatory for all UEs to support the use of TFCI in the downlink.

Figure 13 shows the frame structure of the downlink DPCH. Each frame of length 10 ms is split into 15 slots, each of length T_{slot} = 2560 chips, corresponding to one power-control period. A super frame corresponds to 72 consecutive frames, i.e. the super-frame length is 720 ms.

DPCCH	DPDCH	DPCCH	DPDCH	DPCCH
TFCI N_{TFCI} bits	Data1 N_{data1} bits	TPC N_{TPC} bits	Data2 N_{data2} bits	Pilot N_{pilot} bits

T_{slot} = 2560 chips, $10*2^k$ bits (k=0..7)

| Slot #1 | Slot #2 | | Slot #i | | Slot #15 |

T_f = 10 ms

| Frame #1 | Frame #2 | | Frame #i | | Frame #72 |

T_{super} = 720 ms
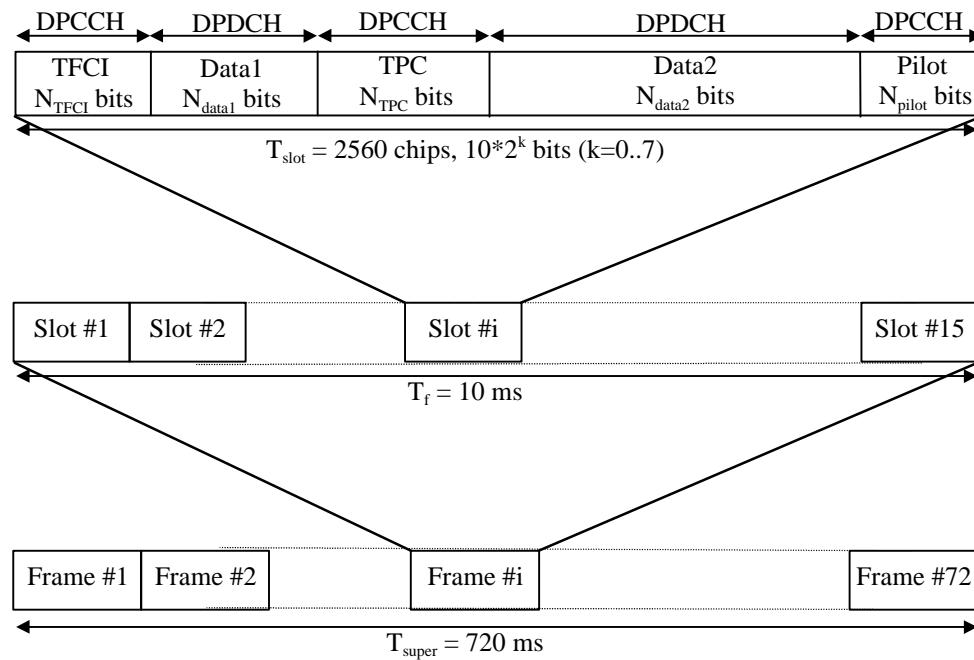
Figure 13: Frame structure for downlink DPCH.

The parameter k in Figure 13 determines the total number of bits per downlink DPCH slot. It is related to the spreading factor SF of the physical channel as $SF = 512/2^k$. The spreading factor may thus range from 512 down to 4.

The exact number of bits of the different downlink DPCH fields in Figure 13 (N_{pilot}, N_{TPC}, N_{TFCI}, N_{data1} and N_{data2}) are given in Table 9.is yet to be determined. The overhead due to the DPCCH transmission has to be negotiated at the connection set-up and can be re-negotiated during the communication, in order to match particular propagation conditions.

The DPCCH fields are spread using the same channelization code used for the DPDCH field. A channelization code for the highest bit rate to be served during the connection (for a given DPCH) should be assigned (with spreading factor SF_1).

Table 9 shows the number of bits per slot of the various fields. There are basically two types of downlink Dedicated Physical Channel; those that include TFCI (e.g. for several simultaneous services) and those that do not include TFCI(e.g. for fixed-rate services). These types are reflected by the duplicated rows of Table 9. The channel bit and symbol rates given in Table 9 are the rates immediately before spreading.

Table 9: DPDCH and DPCCH fields

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/Frame DPDCH	DPCCH	TOT	Bits/ Slot	DPDCH Bits/Slot N_{Data1}	N_{Data2}	DPCCH Bits/Slot N_{TFCI}	N_{TPC}	N_{Pilot}
15	7.5	512	60	90	150	10	2	2	0	2	4
15	7.5	512	30	120	150	10	0	2	2	2	4
30	15	256	150	150	300	20	2	8	0	2	8
30	15	256	120	180	300	20	0	8	2	2	8
60	30	128	450	150	600	40	6	24	0	2	8
60	30	128	420	180	600	40	4	24	2	2	8
120	60	64	900	300	1200	80	4	56	8*	4	8
240	120	32	2100	300	2400	160	20	120	8*	4	8
480	240	16	4320	480	4800	320	48	240	8*	8	16
960	480	8	9120	480	9600	640	112	496	8*	8	16
1920	960	4	18720	480	19200	1280	240	1008	8*	8	16

* If no TFCI, then the TFCI field is blank.

<Editors note: Additional slot formats with less pilot bits due to CPICH are FFS.>

Note: This table assumes the chip rate 3.84 Mcps i.e. it does not cover other chip rates such as 7.68 Mcps.

The pilot symbol pattern is described in Table 10. The shadowed part can be used as frame synchronization words. (The symbol pattern of the pilot symbols other than the frame synchronization word shall be "11".) In Table 10, the transmission order is from left to right. (Each two-bit pair represents an I/Q pair of QPSK modulation.)

Table 10: Pilot Symbol Pattern

<Editors note: Pilot bit patterns to be updated for 15 slots/frame.>

	$N_{pilot}=4$		$N_{pilot}=8$				$N_{pilot}=16$							
Symbol #	0	1	0	1	2	3	0	1	2	3	4	5	6	7
Slot #1	11	11	11	11	11	10	11	11	11	10	11	11	11	10
2	11	00	11	00	11	10	11	00	11	10	11	11	11	00
3	11	01	11	01	11	01	11	01	11	01	11	10	11	00
4	11	00	11	00	11	00	11	00	11	00	11	01	11	10
5	11	10	11	10	11	01	11	10	11	01	11	11	11	11
6	11	11	11	11	11	10	11	11	11	10	11	01	11	01
7	11	11	11	11	11	00	11	11	11	00	11	10	11	11
8	11	10	11	10	11	00	11	10	11	00	11	10	11	00
9	11	01	11	01	11	10	11	01	11	10	11	00	11	11
10	11	11	11	11	11	11	11	11	11	11	11	00	11	11
11	11	01	11	01	11	01	11	01	11	01	11	11	11	10
12	11	10	11	10	11	11	11	10	11	11	11	00	11	10
13	11	10	11	10	11	00	11	10	11	00	11	01	11	01
14	11	00	11	00	11	11	11	00	11	11	11	00	11	00
15	11	00	11	00	11	11	11	00	11	11	11	10	11	01

The relationship between the TPC symbol and the transmitter power control command is presented in Table 11.

Table 11: TPC Bit Pattern

TPC Bit Pattern			Transmitter power control command
$N_{TPC} = 2$	$N_{TPC} = 4$	$N_{TPC} = 8$	
11	1111	11111111	1
00	0000	00000000	0

In each radio frame, the TFCI value corresponds to a certain combination of bit rates of the DCHs currently in use. This correspondence is (re-)negotiated at each DCH addition/removal. For default TFCI there is one code word of length 30 bits. For extended TFCI there are 2 code words of length 15 bits giving the same total number of encoded TFCI bits per frame as for default TFCI. The 30 encoded TFCI bits are divided evenly among the 15 time slots, 2 bits per slot. At the channel bit rates higher than 60 ksps, each 2-bit pair is repeated four times.

<Editors note: DL Multicode transmission>

When the total bit rate to be transmitted on one downlink connection exceeds the maximum bit rate for a downlink physical channel, multicode transmission is employed, i.e. several parallel downlink DPCHs are transmitted for one connection using the same spreading factor. In this case, the Layer 1 control information is put on only the first downlink DPCH. The additional downlink DPCHs belonging to the connection do not transmit any data during the corresponding time period, see Figure 14. Multiple codes may also transmitted in order to transmit different transport channels on different codes (code multiplex). In that case, the different parallel codes may have different spreading factors and the Layer 1 control information is transmitted on each code independently.

One Slot (2560 chips)
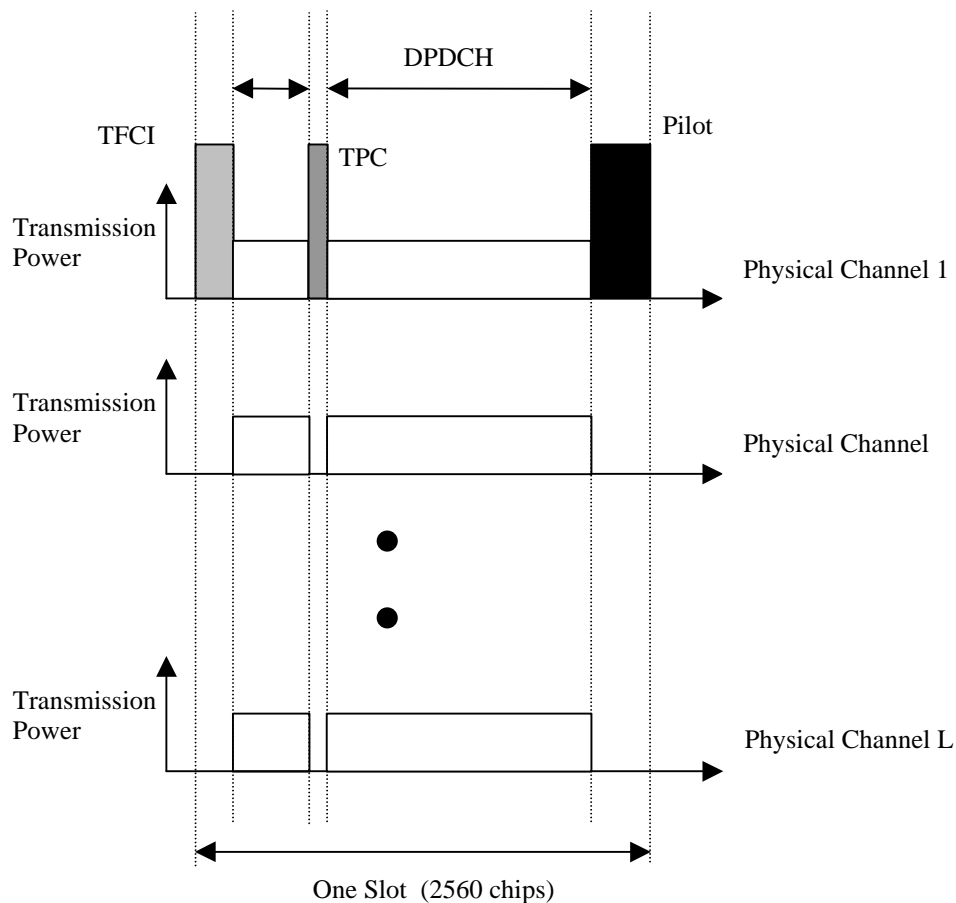
Figure 14: Downlink slot format in case of multi-code transmission.

5.3.2.1 STTD for DPCH

The block diagrams shown in Figure 10and Figure 11 are used to STTD encode the DPDCH, TPC and TFCI symbols. The pilot symbol pattern for the DPCH channel transmitted on the diversity antenna is given in Table 12. For the 7.5 ksps DPCH the last odd data symbol in every frame (10 msec.) is not STTD encoded and the same symbol is transmitted with equal power from the two antennas.

Table 12: Pilot pattern of the DPCH channel for the diversity antenna using STTD.
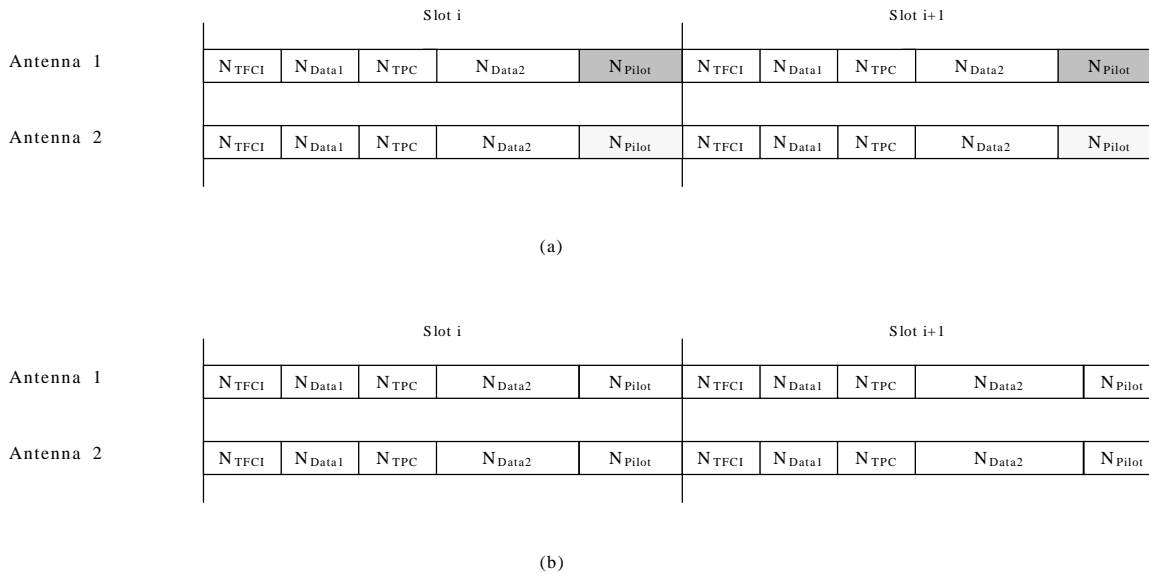
~~<Editors note: Pilot bit patterns to be updated for 15 slots/frame.>~~

	$N_{pilot} = 4$		$N_{pilot} = 8$				$N_{pilot} = 16$							
Symbol #	0	1	0	1	2	3	0	1	2	3	4	5	6	7
Slot #1	01	10	11	00	00	10	11	00	00	10	11	00	00	10
2	10	10	11	00	00	01	11	00	00	01	11	10	00	10
3	11	10	11	11	00	00	11	11	00	00	11	10	00	11
4	10	10	11	10	00	01	11	10	00	01	11	00	00	00
5	00	10	11	11	00	11	11	11	00	11	11	01	00	10
6	01	10	11	00	00	10	11	00	00	10	11	11	00	00
7	01	10	11	10	00	10	11	10	00	10	11	01	00	11
8	00	10	11	10	00	11	11	10	00	11	11	10	00	11
9	11	10	11	00	00	00	11	00	00	00	11	01	00	01
10	01	10	11	01	00	10	11	01	00	10	11	01	00	01
11	11	10	11	11	00	00	11	11	00	00	11	00	00	10
12	00	10	11	01	00	11	11	01	00	11	11	00	00	01
13	00	10	11	10	00	11	11	10	00	11	11	11	00	00
14	10	10	11	01	00	01	11	01	00	01	11	10	00	01
15	10	10	11	01	00	01	11	01	00	01	11	11	00	11

At call setup phase the UE is informed if Transmit diversity will be used on DPCH or not. If the base station allows diversity mode, the base station starts the transmission of dedicated physical channel(s) using open loop diversity mode by default. As soon as the reverse link transmission has started, the base station can command the UE to either use open loop diversity mode or feedback mode by using higher level signalling. During hand over between cells and sectors open loop antenna diversity is used on dedicated physical channels.

5.3.2.2 Dedicated channel pilots with feedback mode transmit diversity

For certain sub-modes of feedback mode transmit diversity, ~~in which transmission antennas are selected, the pilot patterns can be varied according to which antenna is transmitted upon~~ orthogonal pilot sequences can be applied between the diversity antennas (see Figure 15 a, where the different shading indicates different pilot patterns). This assists in some types of antenna verification. Pilot symbol patterns are defined in Table 10 and Table 12~~TBD~~. Otherwise, the pilot symbol patterns from both of the antennas are the same (see Figure 15 b).

(a)

	Slot i					Slot i+1				
Antenna 1	N_{TFCI}	N_{Data1}	N_{TPC}	N_{Data2}	N_{Pilot}	N_{TFCI}	N_{Data1}	N_{TPC}	N_{Data2}	N_{Pilot}
Antenna 2	N_{TFCI}	N_{Data1}	N_{TPC}	N_{Data2}	N_{Pilot}	N_{TFCI}	N_{Data1}	N_{TPC}	N_{Data2}	N_{Pilot}

(b)

	Slot i					Slot i+1				
Antenna 1	N_{TFCI}	N_{Data1}	N_{TPC}	N_{Data2}	N_{Pilot}	N_{TFCI}	N_{Data1}	N_{TPC}	N_{Data2}	N_{Pilot}
Antenna 2	N_{TFCI}	N_{Data1}	N_{TPC}	N_{Data2}	N_{Pilot}	N_{TFCI}	N_{Data1}	N_{TPC}	N_{Data2}	N_{Pilot}

Figure 15: Slot structures for downlink dedicated physical channel diversity transmission. Structure (a) may be used in conjunction with antenna verification. Structure (b) is used otherwise.

5.3.3 Common downlink physical channels

5.3.3.1 Common Pilot Channel

A Common Pilot Channel (CPICH) is a downlink physical channel with pre-defined modulation, used as a phase reference for other DL physical channels. In the normal case, the modulation on a Common Pilot Channel is the all-one sequence {…, 1, 1,…}. In case of STTD and FB TX diversity, a different modulation pattern is used for a Common Pilot Channel on a diversity antenna.

<Editors note: The exact modulation pattern is FFS.>

There may be two types of Common Pilot Channels in a cell:

- There is always one and only one Primary Common Pilot Channel in each cell. The Primary Common Pilot consists of 300 bits per frame, is spread by a pre-defined channelization code with SF=256 and is scrambled by the primary scrambling code.

   <Editors note: Which channelisation code to be used is FFS.>

- There may also be one or several Secondary Common Pilot Channels in a cell. A Secondary Common Pilot Channel may be spread by an arbitrary channelization code and is scrambled by the primary or a secondary scrambling code.

<Editors note: The code allocation for the Common Pilot Channels should be described in 25.213.>

5.3.3.2 Primary Common Control Physical Channel (CCPCH)

The Primary CCPCH is a fixed rate (30 kbps, SF=256) downlink physical channels used to carry the BCH.

Figure 16 shows the frame structure of the Primary CCPCH. The frame structure differs from the downlink DPCH in that no TPC commands, no TFCI and no pilot bits are transmitted The Primary CCPCH is not transmitted during the first 256 chips of each slot. Instead, Primary SCH and Secondary SCH are transmitted during this period (see section 5.3.3.4).
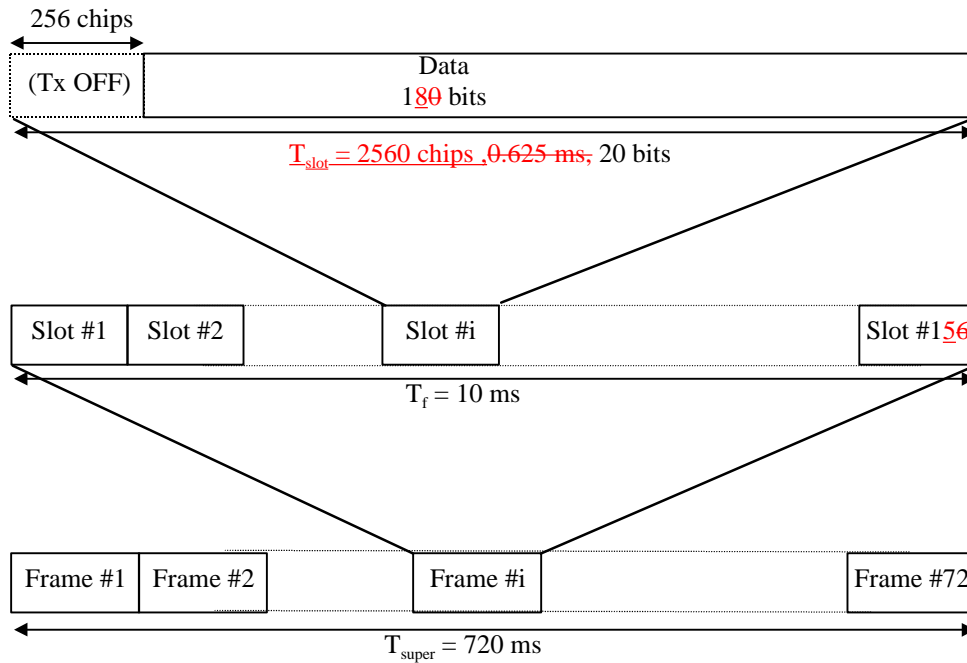
Figure 16: Frame structure for Primary Common Control Physical Channel.

<Editors note: Pilot bit patterns has been deleted.>

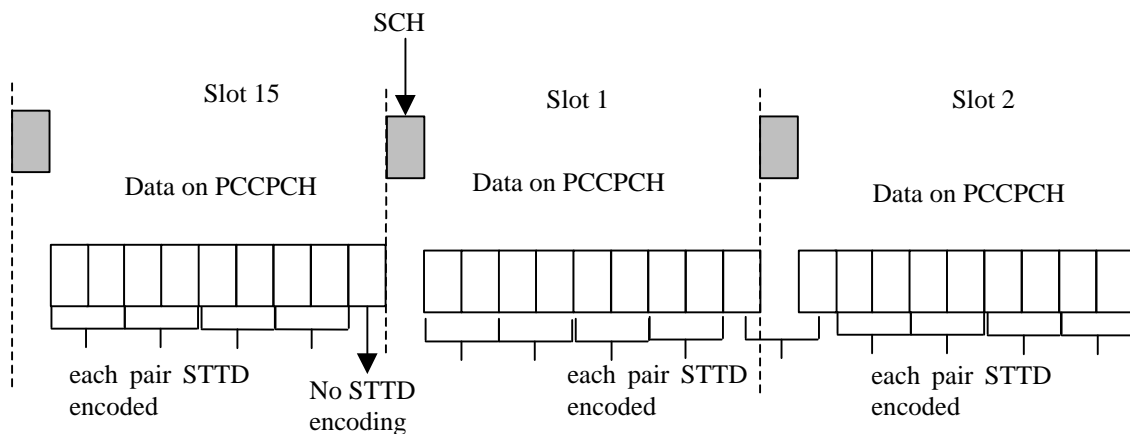### 5.3.3.2.1 Primary CCPCH structure with STTD encoding

<Editors note: Needs to be checked for pilot bits removal on PCCPCH.>

In case the diversity antenna is present at the base station and the PCCPCH is to be transmitted using open loop transmit diversity, the data symbols of the PCCPCH are STTD encoded as given in section 5.3.1.1.1, Figure 10 and Figure 11. The last odd data symbol in every frame (10 msec.) is not STTD encoded and the same symbol is transmitted with equal power from the two antennas. The base station transmits a L3 message on the broadcast channel (BCH) indicating whether STTD encoding is used for the PCCPCH or not. In addition, the base station indicates the presence/absence of STTD encoding on PCCPCH, by modulating the SCH. During power on and hand over between cells the UE determines the presence of STTD encoding on the PCCPCH, by either receiving the L3 message, by demodulating the SCH channel or by a combination of the above two schemes.

<Editors note: Pilot bit patterns has been deleted.>

The STTD encoding for the data symbols of the slots 1 and 2 of a PCCPCH frame is given in the figure below. The same procedure is used for the data symbols of slots 3 and 4, 5 and 6 and henceforth, respectively.
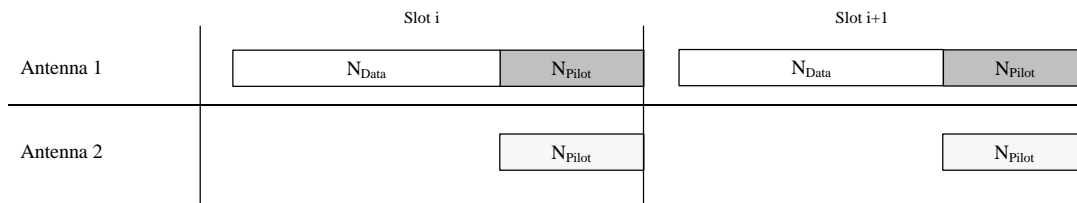
Figure 17: STTD encoding for the data symbols of the PCCPCH.

~~<Editors note: Figure to be updated to remove pilot bits due to CPICH.>~~

~~5.3.3.2.2 Primary CCPCH structure with FB mode transmit diversity~~

~~<Editors note: Needs to be checked for pilot bits removal on PCCPCH.>~~

~~**Figure 14: Slot structure of Primary CCPCH when diversity transmission is applied on dedicated channels.**~~

~~<Editors note: Figure to be deleted or changed to remove pilot bits due to CPICH.>~~

5.3.3.3 Secondary Common Control Physical Channel

<Editors note: The maximum bit rates supported by different terminal classes on the Secondary CCPCH is FFS. >

The Secondary CCPCH is used to carry the FACH and PCH. There are two types of Secondary CCPCH: those that include TFCI and those that do not include TFCI. It is the UTRAN that determines if a TFCI should be transmitted, hence making it mandatory for all UEs to support the use of TFCI. The set of possible rates is the same as for the downlink DPCH, see Section 5.3.2.

The frame structure of the Secondary CCPCH is shown in Figure 19.
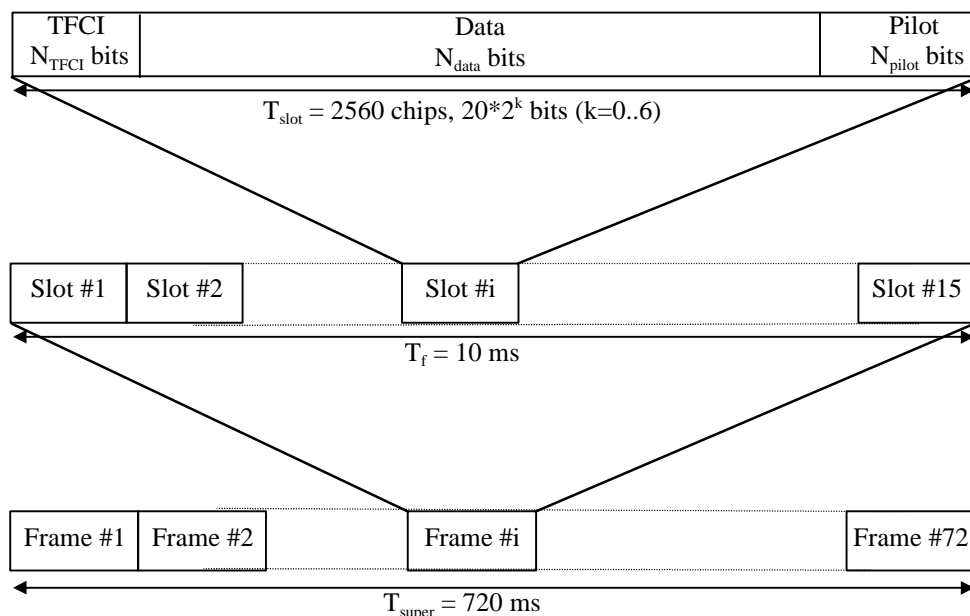
Figure 19: Frame structure for Secondary Common Control Physical Channel.

The parameter k in Figure 19 determines the total number of bits per downlink Secondary CCPCH slot. It is related to the spreading factor SF of the physical channel as $SF = 256/2^k$. The spreading factor range is from 256 down to 4.

The values for the number of bits per field are given in Table 13 and Table 14. The channel bit and symbol rates given in Table 13 are the rates immediately before spreading. The pilot patterns are given in Table 15.

The FACH and PCH can be are mapped to the same or to separate Secondary CCPCHs. The main difference between a CCPCH and a downlink dedicated physical channel is that a CCPCH is not power controlled. The main difference between the Primary and Secondary CCPCH is that the Primary CCPCH has a fixed predefined rate while the Secondary CCPCH can support variable rate with the help of the TFCI field included. Furthermore, a Primary CCPCH is continuously transmitted over the entire cell while a Secondary CCPCH is only transmitted when there is data available and may be transmitted in a narrow lobe in the same way as a dedicated physical channel (only valid for a Secondary CCPCH carrying the FACH).

The pilot symbol pattern is described in Table 15. The shadowed part can be used as frame synchronization words. (The symbol pattern of pilot symbols other than the frame synchronization word shall be "11".) In Table 15, the transmission order is from left to right. (Each two-bit pair represents an I/Q pair of QPSK modulation.)

<Editors note: The following paragraph needs to be checked for 15 slots/frame.>

In the Secondary Common Control Physical Channel, it is possible to have burst transmission based on radio frame units. When burst transmission is performed, pilot symbols shall be added to the head of the burst. The number of symbols and the symbol pattern of the pilot symbols to be attached shall take the pattern of Slot #15 in Table 15. The scrambling code phase of the pilot symbol to be added shall have continuous values from the phase of the head of the burst.

Table 13: Secondary CCPCH fields with pilot bits

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}	N_{pilot}	N_{TFCI}
30	15	256	300	20	12	8	0
30	15	256	300	20	10	8	2
60	30	128	600	40	32	8	0
60	30	128	600	40	30	8	2
120	60	64	1200	80	72	8	0
120	60	64	1200	80	64	8	8
240	120	32	2400	160	152	8	0
240	120	32	2400	160	144	8	8
480	240	16	4800	320	304	16	0
480	240	16	4800	320	296	16	8
960	480	8	9600	640	624	16	0
960	480	8	9600	640	616	16	8
1920	960	4	19200	1280	1264	16	0
1920	960	4	19200	1280	1256	16	8

Table 14: Secondary CCPCH fields without pilot bits

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}	N_{pilot}	N_{TFCI}
30	15	256	300	20	20	0	0
30	15	256	300	20	18	0	2
60	30	128	600	40	40	0	0
60	30	128	600	40	38	0	2
120	60	64	1200	80	80	0	0
120	60	64	1200	80	72	0	8
240	120	32	2400	160	160	0	0
240	120	32	2400	160	152	0	8
480	240	16	4800	320	320	0	0
480	240	16	4800	320	312	0	8
960	480	8	9600	640	640	0	0
960	480	8	9600	640	632	0	8
1920	960	4	19200	1280	1280	0	0
1920	960	4	19200	1280	1272	0	8

Table 15: Pilot Symbol Pattern

~~<Editors note: Pilot bit patterns to be updated for 15 slots/frame.>~~

	$N_{pilot} = 8$				$N_{pilot} = 16$							
Symbol #	0	1	2	3	0	1	2	3	4	5	6	7
Slot #1	11	11	11	10	11	11	11	10	11	11	11	10
2	11	00	11	10	11	00	11	10	11	11	11	00
3	11	01	11	01	11	01	11	01	11	10	11	00
4	11	00	11	00	11	00	11	00	11	01	11	10
5	11	10	11	01	11	10	11	01	11	11	11	11
6	11	11	11	10	11	11	11	10	11	01	11	01
7	11	11	11	00	11	11	11	00	11	10	11	11
8	11	10	11	00	11	10	11	00	11	10	11	00
9	11	01	11	10	11	01	11	10	11	00	11	11
10	11	11	11	11	11	11	11	11	11	00	11	11
11	11	01	11	01	11	01	11	01	11	11	11	10
12	11	10	11	11	11	10	11	11	11	00	11	10
13	11	10	11	00	11	10	11	00	11	01	11	01
14	11	00	11	11	11	00	11	11	11	00	11	00
15	11	00	11	11	11	00	11	11	11	10	11	01

5.3.3.3.1　　Secondary CCPCH structure with STTD encoding

In case the diversity antenna is present at the base station and the SCCPCH is to be transmitted using open loop transmit diversity, the data symbols of the SCCPCH are STTD encoded as given in Section 5.3.1.1.1, Figure 10 and Figure 11. The diversity antenna pilot symbol pattern for the SCCPCH is given in Table 16 below.

Table 16: Pilot symbol pattern for the diversity antenna when STTD encoding is used on the SCCPCH.

~~<Editors note: Pilot bit patterns to be updated for 15 slots/frame.>~~

	$N_{pilot} = 8$				$N_{pilot} = 16$							
Symbol #	0	1	2	3	0	1	2	3	4	5	6	7
Slot #1	11	00	00	10	11	00	00	10	11	00	00	10
2	11	00	00	01	11	00	00	01	11	10	00	10
3	11	11	00	00	11	11	00	00	11	10	00	11
4	11	10	00	01	11	10	00	01	11	00	00	00
5	11	11	00	11	11	11	00	11	11	01	00	10
6	11	00	00	10	11	00	00	10	11	11	00	00
7	11	10	00	10	11	10	00	10	11	01	00	11
8	11	10	00	11	11	10	00	11	11	10	00	11
9	11	00	00	00	11	00	00	00	11	01	00	01
10	11	01	00	10	11	01	00	10	11	01	00	01
11	11	11	00	00	11	11	00	00	11	00	00	10
12	11	01	00	11	11	01	00	11	11	00	00	01
13	11	10	00	11	11	10	00	11	11	11	00	00
14	11	01	00	01	11	01	00	01	11	10	00	01
15	11	01	00	01	11	01	00	01	11	11	00	11

5.3.3.4 Synchronisation Channel

The Synchronisation Channel (SCH) is a downlink signal used for cell search. The SCH consists of two sub channels, the Primary and Secondary SCH. Figure 20 illustrates the structure of the SCH and the transmission timing relationship with the Primary CCPCH:
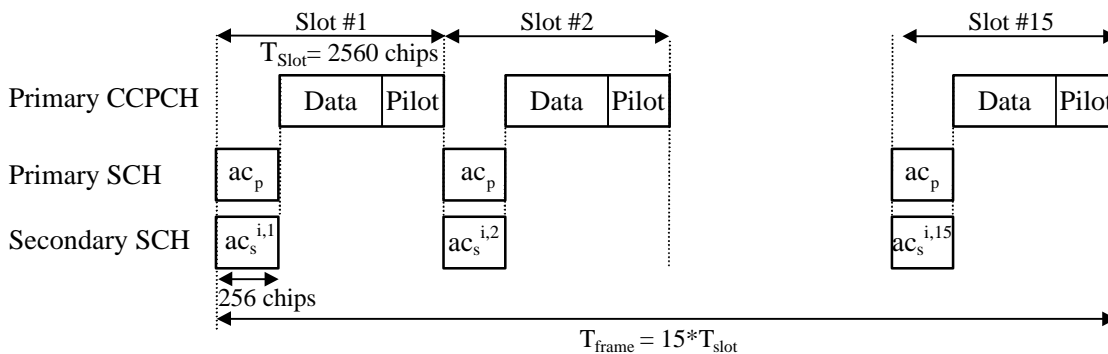
c_p : Primary Synchronization Code
$c_s^{i,k}$: One of 16 possible Secondary Synchronization Codes
$(c_s^{i,1}, c_s^{i,2}, ..., c_s^{i,15})$ encode cell specific long scrambling code group i
a: Modulation on primary and secondary synchronization codes to indicate STTD encoding on PCCPCH

Figure 20: Structure of Synchronisation Channel (SCH).

The Primary SCH consists of a modulated code of length 256 chips, the Primary Synchronisation Code, transmitted once every slot. The Primary Synchronisation Code is the same for every cell in the system and is transmitted time-aligned with the period where the Primary CCPCH is not transmitted as illustrated in Figure 20.

The Secondary SCH consists of repeatedly transmitting a length 15 sequence of modulated codes of length 256 chips, the Secondary Synchronisation Codes, transmitted in parallel with the Primary Synchronisation channel. Each Secondary Synchronisation code is chosen from a set of 16 different codes of length 256. This sequence on the

Secondary SCH indicates which of the 32 different code the cell's downlink scrambling code belongs. 32 sequences are used to encode the 32 different code groups each containing 16 scrambling codes.

The primary and secondary synchronization codes are modulated by the symbol *a* shown in Figure 20, which indicates the presence/ absence of STTD encoding on the PCCPCH and is given by the following table:

PCCPCH STTD encoded	a = +1
PCCPCH not STTD encoded	a = -1

5.3.3.4.1   SCH transmitted by TSTD

Figure 21 illustrates the structure of the SCH transmitted by the TSTD scheme. In this Figure, STTD is applied to the Primary CCPCH.
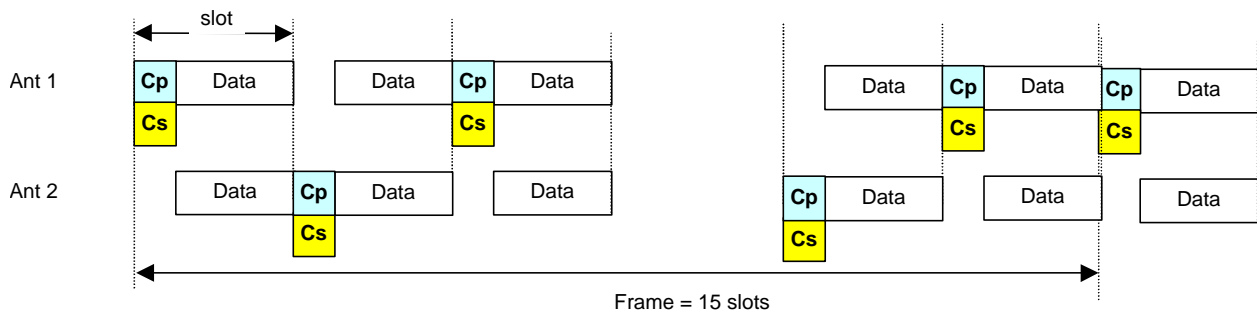

Frame = 15 slots

Figure 21: Structure of SCH transmitted by TSTD scheme

5.3.3.5   Physical Shared Channel Control Channel (PSCCCH)

<Note: WG1 concluded that PSCCCH will not be included in release 99.>
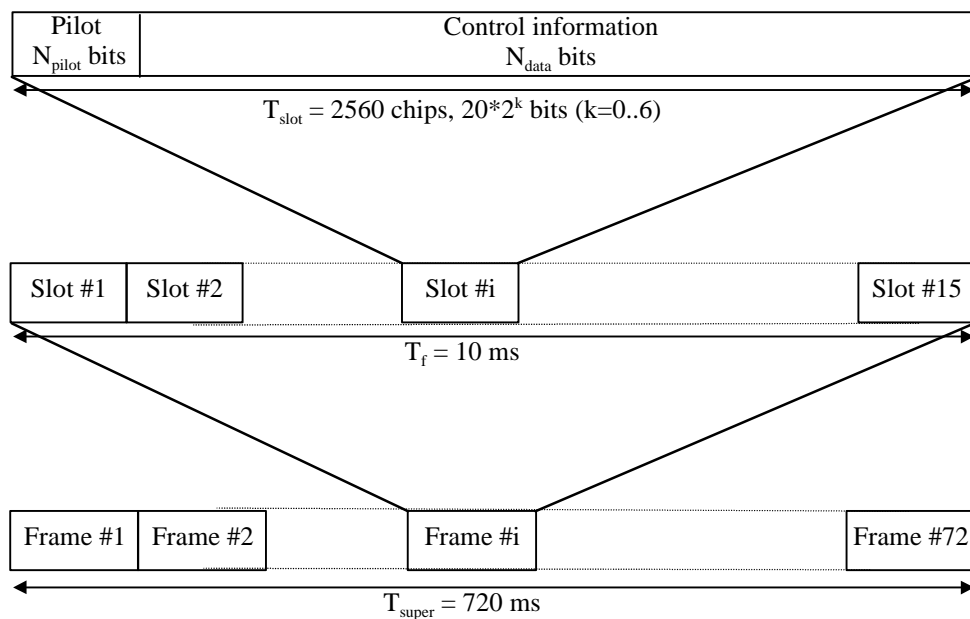
 The frame structure for the PSCCCH is shown in Figure 22.

.

Pilot N_{pilot} bits	Control information N_{data} bits

T_{slot} = 2560 chips, 20*2^k bits (k=0..6)

Slot #1 | Slot #2 | ... | Slot #i | ... | Slot #15

T_f = 10 ms

Frame #1 | Frame #2 | ... | Frame #i | ... | Frame #72

T_{super} = 720 ms

Figure 22: Frame structure of the Physical Shared Channel Control Channel (PSCCCH).

The PSCCCH contains pilot symbols, and a control information field. The control information field can include TPC commands concerning several users. Other control information includes code assignment for the DSCH, but could also

comprise other type of information if needed. The TPC commands would come in support of fast closed loop power control of the PDSCH, and thus, would have to be decoded on a slot-by-slot basis. The exact structure of the control information field is for further study.

5.3.3.6 Physical Downlink Shared Channel

<Note: WG1 concluded that DSCH control channel will not be included in release 99.>

The Physical Downlink Shared Channel (PDSCH), used to carry the Downlink Shared Channel (DSCH), is shared by users based on code multiplexing. It is always associated with another physical channel, as follows:

- If the DSCH is associated with a DCH, the PDSCH is associated with a DPCH,

- If the DSCH is associated with a DSCH control channel, the PDSCH is associated with a PSCCCH.

This is described respectively in Sections 5.3.3.6.1 and 5.3.3.6.2.

In both cases, the PDSCH does not comprise any pilot symbols, since this does not seem to be required at this stage, given information provided on the associated DPCH or PSCCCH. This still needs to be verified.

5.3.3.6.1 DSCH associated with a DCH

The frame structure of the DSCH, when associated with a DCH, is shown on Figure 23.
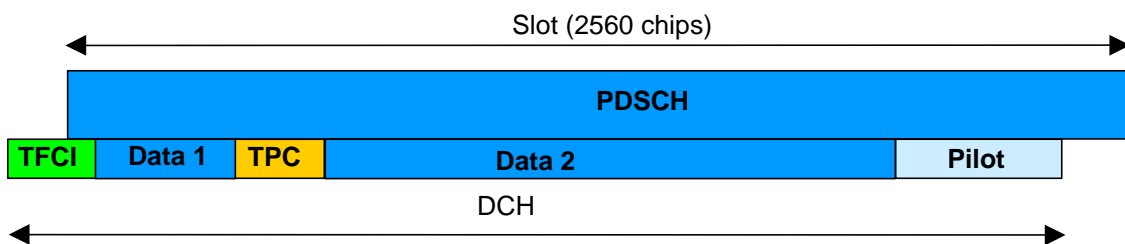
Figure 23: Frame structure for the DSCH when associated to a DCH.

To indicate for UE that there is data to decode on the DSCH, two signalling methods are possible, either using the TFCI field, or higher layer signalling.

The DSCH transmission with associated DCH is a special case of multicode transmission. The channels do not have necessary the same spreading factor and for DSCH the spreading factor may vary from frame to frame. The relevant Layer 1 control information is transmitted on DCH, the PDSCH does not contain DPCCH information.

For DSCH the allowed spreading factors may vary from 256 to 4. DSCH may consist of multiple parallel codes as well as negotiated at higher layer prior to starting data transmission. In such a case the parallel codes shall be operated with frame synchronization between each other.

5.3.3.6.2 DSCH associated with a DSCH control channel

<Note: WG1 concluded that DSCH control channel will not be included in release 99.>

The frame structure of the DSCH when associated with a DSCH control channel is shown in Figure 24.
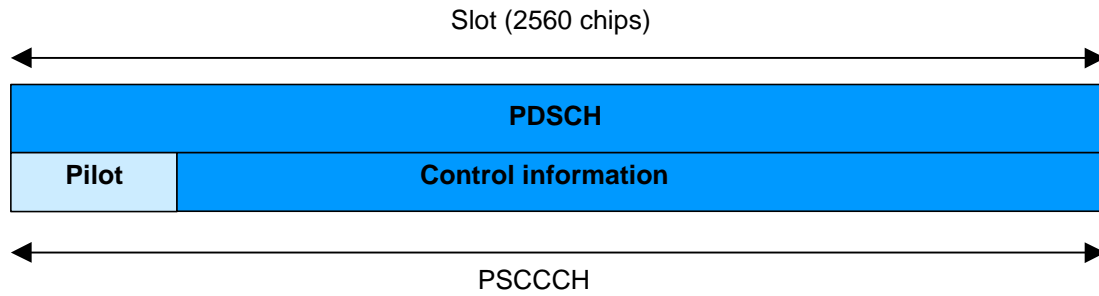
Slot (2560 chips)

PDSCH	
Pilot	**Control information**

PSCCCH

Figure 24: Frame structure for the DSCH when associated to a DSCH control channel.

5.3.3.7 Acquisition Indication Channel (AICH)

~~<Editors note: AICH timing needs to be updated according to 15 slots/frame.>~~

The Acquisition Indicator channel (AICH) is a physical channel used to carry Acquisition Indicators (AI). Acquisition Indicator AI_i corresponds to signature *i*, see further 25.213, Section 4.3.3.2

Figure 25 illustrates the frame structure of the AICH. <u>Two</u> AICH frame<u>s</u> of <u>total</u> length 2~~1~~0 ms consist~~s~~ of <u>15</u>~~8~~ *access slots* (AS), each of length 20 symbols (<u>5120 chips</u>~~1.25 ms~~). Each access slot consists of two parts, an *Acquisition-Indicator* (AI) part and an empty part.

16 symbols (4096 chips) **4 symbols (1024 chips)**

AI	empty

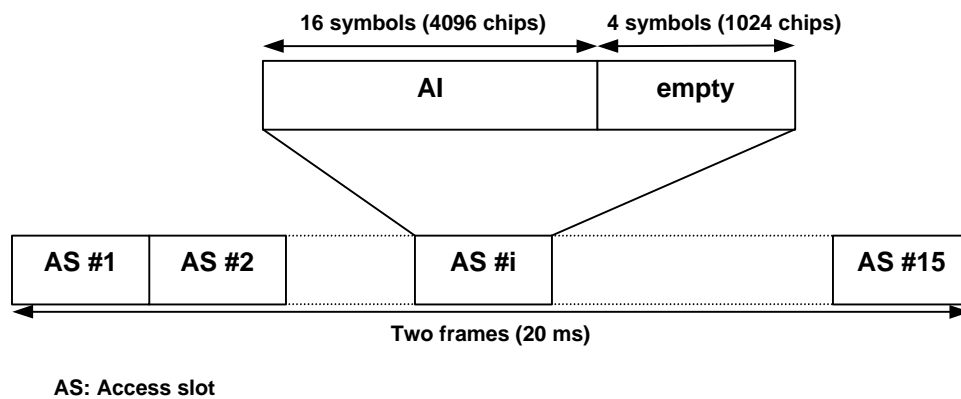| AS #1	AS #2		AS #i		AS #15

Two frames (20 ms)

AS: Access slot

Figure 25: Structure of Acquisition Indicator CHanel (AICH)

Figure 26 illustrates the detailed generation of an AICH access slot. Note that Figure 26 shows an example implementation.

The AI-part of the access slot consists of the symbol-wise sum of <u>up to</u> 16 orthogonal code words w_1-w_{16}, multiplied by the value of the corresponding acquisition indicator AI_i. The orthogonal code words $w_1,...,w_{16}$ are shown in Table 17.

The empty part of the access slot consists of 4 zeros.

The phase reference for the AICH is the <u>CPICH</u> ~~pilot symbols of the downlink PCCPCH~~.
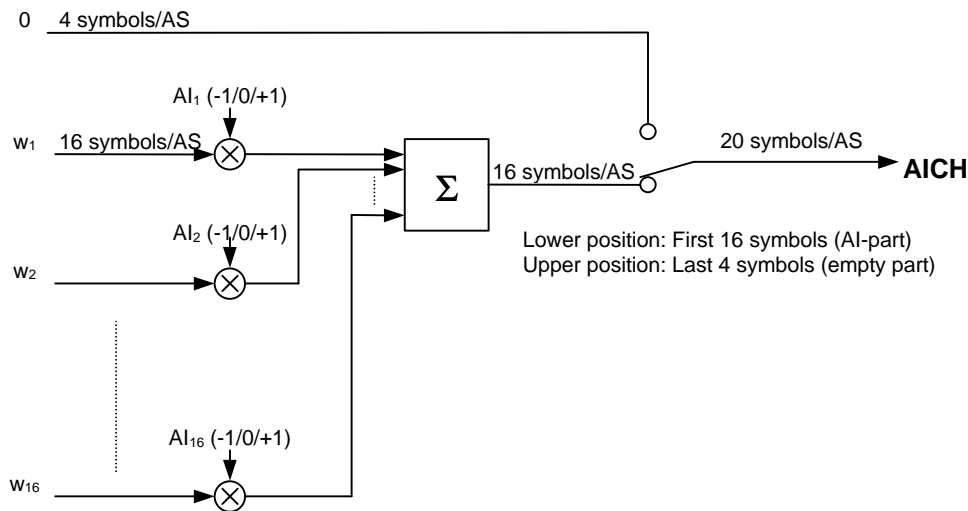
0   4 symbols/AS

AI_1 (-1/0/+1)

w_1 16 symbols/AS   ⊗

Σ   16 symbols/AS   20 symbols/AS   ▶ **AICH**

AI_2 (-1/0/+1)

w_2 ⊗

Lower position: First 16 symbols (AI-part)
Upper position: Last 4 symbols (empty part)

AI_{16} (-1/0/+1)

w_{16} ⊗

Figure 26: Schematic generation of AICH access slots.

Table 17: Definition of orthogonal vectors w_1-w_{16} used in Figure 26; A = (1+j)

i	w_i															
1	A	A	A	-A	-A	-A	A	-A	-A	A	A	-A	A	-A	A	A
2	-A	A	-A	-A	A	A	A	-A	A	A	A	-A	-A	A	-A	A
3	A	-A	A	A	A	-A	A	A	-A	A	A	A	-A	A	-A	A
4	-A	A	-A	A	-A	-A	-A	-A	-A	A	-A	A	-A	A	A	A
5	A	-A	-A	-A	-A	A	A	-A	-A	-A	-A	A	-A	-A	-A	A
6	-A	-A	A	-A	A	-A	A	-A	A	-A	-A	A	A	A	A	A
7	-A	A	A	A	-A	-A	A	A	A	-A	-A	-A	-A	-A	-A	A
8	A	A	-A	-A	-A	-A	-A	A	A	-A	A	A	A	A	-A	A
9	A	-A	A	-A	-A	A	-A	A	A	A	-A	-A	-A	A	A	A
10	-A	A	A	-A	A	A	-A	A	-A	-A	A	A	-A	-A	A	A
11	A	A	A	A	A	A	-A	-A	A	A	-A	A	A	-A	-A	A
12	A	A	-A	A	A	A	A	A	-A	-A	-A	-A	A	A	A	A
13	A	-A	-A	A	A	-A	-A	-A	A	-A	A	-A	-A	-A	A	A
14	-A	-A	-A	A	-A	A	A	A	A	A	A	A	A	-A	A	A
15	-A	-A	-A	-A	A	-A	-A	A	-A	A	-A	-A	A	-A	-A	A
16	-A	-A	A	A	-A	A	-A	-A	-A	-A	A	-A	A	A	-A	A

The spreading/scrambling of the AICH is done is the same way as the spreading/scrambling of other DL channels, compare 25.213, Section 5.1. The AICH is spread by a channelization code of length 256 and subsequently scrambled by the cell-specific scrambling code.

5.3.3.8   Page Indication Channel (PICH)

<Note: This is a working assumption which will become agreed if not challenged until the WG1#7 meeting.>

The Page Indicator Channel (PICH) is a fixed rate (SF=256) physical channel used to carry the Page Indicators (PI). The PICH is always associated with an S-CCPCH to which a PCH transport channel is mapped.
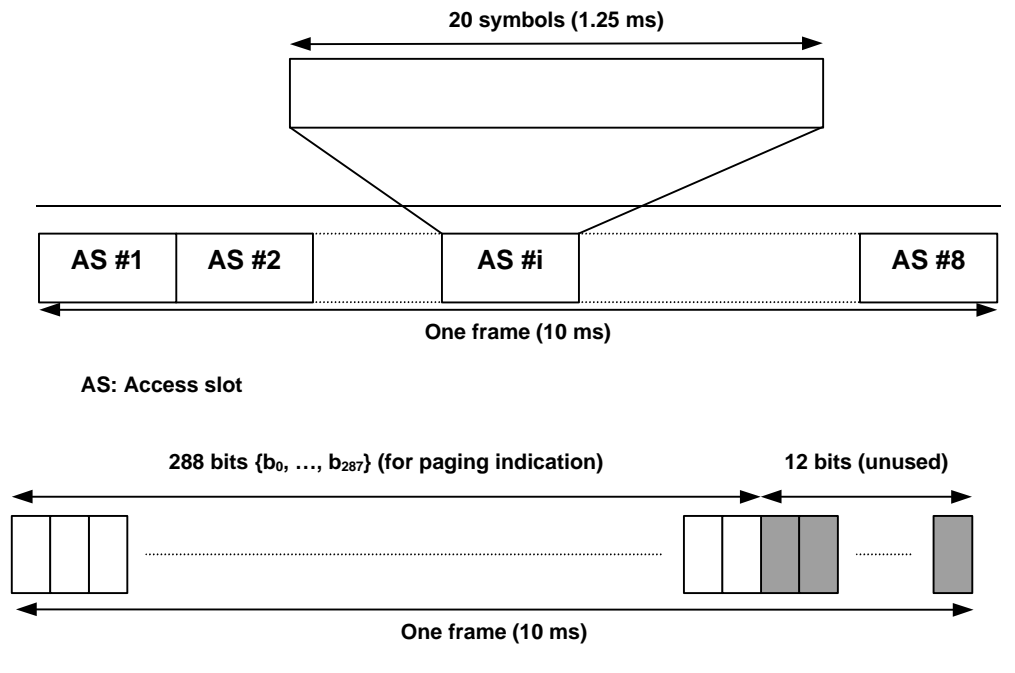
Figure 27 illustrates the frame structure of the PICH. One PICH frame of length 10 ms consists 300 bits. Of these, 288 bits are used to carry Page Indicators. The remaining 12 bits are not used.

<Editors note: PICH timing needs to be updated according to 15 slots/frame.>

<Editors note: The merge of AICH and PICH into ICH is under study.>

The Page Indication Channel (PICH) is a physical channel used to carry the Page Indicators (PI). Figure 24 illustrates the frame structure of the PICH. One PICH frame of length 10 ms consists of 8 access slots (AS), each of length 20 symbols (1.25ms).

Figure 27: Structure of Page Indicator CHannel (PICH)

~~Figure 25 illustrates the detailed generation of an PICH access slot. There are 5, 10 or 20 Page Indicators in each access slot. In case of 5 or 10 Page Indicators, repetition 4 and 2 times respectively is applied. The phase reference for the PICH is the pilot symbols of the downlink PCCPCH.~~

~~**Figure : Schematic generation of PICH access slot**~~

N Page Indicators $\{PI_0, \ldots, PI_{N-1}\}$ are transmitted in each PICH frame, where N=18, 36, 72, or 144. The mapping from $\{PI_0, \ldots, PI_{N-1}\}$ to the PICH bits $\{b_0, \ldots, b_{287}\}$ are according to Table 18.

Table 18: Mapping of Page Indicators (PI) to PICH bits

Number of PI per frame (N)	$PI_i = 1$	$PI_i = 0$
N=18	$\{b_{16i}, \ldots, b_{16i+15}\} = \{1,1,\ldots,1\}$	$\{b_{16i}, \ldots, b_{16i+15}\} = \{0,0,\ldots,0\}$
N=36	$\{b_{8i}, \ldots, b_{8i+7}\} = \{1,1,\ldots,1\}$	$\{b_{8i}, \ldots, b_{8i+7}\} = \{0,0,\ldots,0\}$
N=72	$\{b_{4i}, \ldots, b_{4i+3}\} = \{1, 1,\ldots,1\}$	$\{b_{4i}, \ldots, b_{4i+3}\} = \{0, 0,\ldots,0\}$
N=144	$\{b_{2i}, \ldots, b_{2i+1}\} = \{1,1\}$	$\{b_{2i}, \ldots, b_{2i+1}\} = \{0,0\}$

If aPaging Indicator in a certain frame is set to "1" it is an indication that UEs associated with this Page Indicator should read the corresponding frame of the associated S-CCPCH.

6 Mapping of transport channels onto physical channels

Figure 28 summarises the mapping of transport channels onto physical channels.

Transport Channels	Physical Channels
	Common Pilot Channel (CPICH)
BCH ————————	Primary Common Control Physical Channel (Primary CCPCH)
FACH ————————	Secondary Common Control Physical Channel (Secondary CCPCH)
PCH ————	
RACH ————————	Physical Random Access Channel (PRACH)
FAUSCH ————————	Physical Fast Access Signalling Channel (PFAUSCH)
CPCH ————————	Physical Common Packet Channel (PCPCH)
DCH ————————	Dedicated Physical Data Channel (DPDCH)
	Dedicated Physical Control Channel (DPCCH)
	Synchronisation Channel (SCH)
DSCH ————————	Physical Downlink Shared Channel (PDSCH)
DSCH control channel ————	Physical Shared Channel Control Channel (PSCCCH)
	Acquisition Indication Channel (AICH)
	Page Indication Channel (PICH)

Figure 28: Transport-channel to physical-channel mapping.

<Editors note: It is still under study if there should be a common physical channel ICH for the Acquisition and Page Indicators or separate Acquisition Indication and Page Indication Channels..>
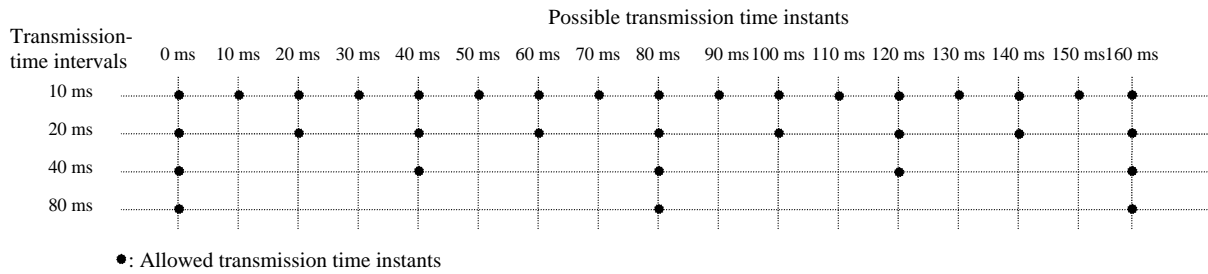
The DCHs are coded and multiplexed as described in TS 25.212, and the resulting data stream is mapped sequentially (first-in-first-mapped) directly to the physical channel(s). The mapping of BCH and FACH/PCH is equally straightforward, where the data stream after coding and interleaving is mapped sequentially to the Primary and Secondary CCPCH respectively. Also for the RACH, the coded and interleaved bits are sequentially mapped to the physical channel, in this case the message part of the random access burst on the PRACH.

6.1 Multiplexing of different transport channels onto one CCTrCH, and mapping of one CCTrCH onto physical

Different transport channels can be encoded and multiplexed together into one Coded Composite Transport Channel (CCTrCH) as described in [4]. The following rules shall apply to the different transport channels which are part of the same CCTrCH:

1) Transport channels multiplexed into one CCTrCh should have co-ordinated timings in the sense that transport blocks arriving from higher layers on different transport channels of potentially different transmission time intervals shall have aligned transmission time instants as shown in Figure 29.

2) Only transport channels with the same active set can be mapped onto the same CCTrCH.

3) Different CCTrCHs cannot be mapped onto the same DPDCH.

4) One CCTrCH shall be mapped onto one or several DPDCHs. These physical channels <u>within one CCTrCH</u> shall <u>all</u> have the same SF. ~~on the uplink. It is FFS whether one CCTrCH may be mapped onto DPDCHs with different SF on the downlink. (see Note 1)~~

Possible transmission time instants

Transmission-
time intervals   0 ms 10 ms 20 ms 30 ms 40 ms 50 ms 60 ms 70 ms 80 ms   90 ms 100 ms 110 ms 120 ms 130 ms 140 ms 150 ms160 ms

●: Allowed transmission time instants

Figure 29: Possible transmission time instants regarding CCTrCH

5) Dedicated Transport channels and common transport channels cannot be multiplexed into the same CCTrCH

6) For the common transport channels, only the FACH and PCH may belong to the same CCTrCH

~~Note 1 : The decision on the possibility to map one CCtrCH onto DPDCHs of different SFs should consider issues like code usage and physical channel segmentation rule definition and performance.~~

~~Note 2 : It is also for further study if one transport channel can be split to several CCTrCHs. However de-multiplexing might be better located in the MAC layer.~~

There are hence two types of CCTrCH

1) CCTrCH of dedicated type, corresponding to the result of coding and multiplexing of one or several DCH

2) CCTrCH of common type, corresponding to the result of the coding and multiplexing of a common channel, RACH in the uplink, DSCH , FACH or PCH for the downlink.

6.1.1   Allowed CCTrCH combinations for one UE

6.1.1.1   Allowed CCTrCH combinations on the uplink

The following CCTrCH combinations for one UE are allowed, where those are mutually exclusive :

1) one CCTrCH of dedicated type

2) one CCTrCH of common type

6.1.1.2   Allowed CCTrCH combinations on the downlink

The following CCTrCH combinations for one UE are allowed :

1) x CCTrCH of dedicated type + y CCTrCH of common type

The allowed combination of CCTrCHs of dedicated and common type are FFS.

Note 1: It is for further study if only one or several CCTrCHs of dedicated type are allowed in downlink, i.e if x is allowed to be greater than 1. The decision should consider performance of balancing using rate matching and how to code and transmit the TFCI. ~~The decision should also consider code usage if conclusion from Note 2 in previous section was that one CCTrCH was to be mapped onto DPDCHs with the same SF.~~

Note 2 : There is only one DPCCH in the uplink, hence one TPC bits flow on the uplink to control possibly the different DPDCHs on the downlink, part of the same or several CCTrCHs.

Note 3 : ~~It is for further study if several DPCCHs can be transmitted in downlink, in conjunction with one CCTrCH with multiple DPDCHs or multiple CCTrCHs.~~ There is only one DPCCH in the downlink, even with multiple CCTrCHs. With multiple CCTrCHs, the DPCCH is transmitted on one of the physical channels of that CCTrCH which has the smallest SF among the multiple CCTrCHs. ~~Even if several DPCCH on the downlink are considered,~~ Thus there is only one TPC command flow and only one TFCI word in downlink even with multiple CCTrCHs. ~~is used , with possibly the same TPC information on the different DPCCH, if applicable.~~
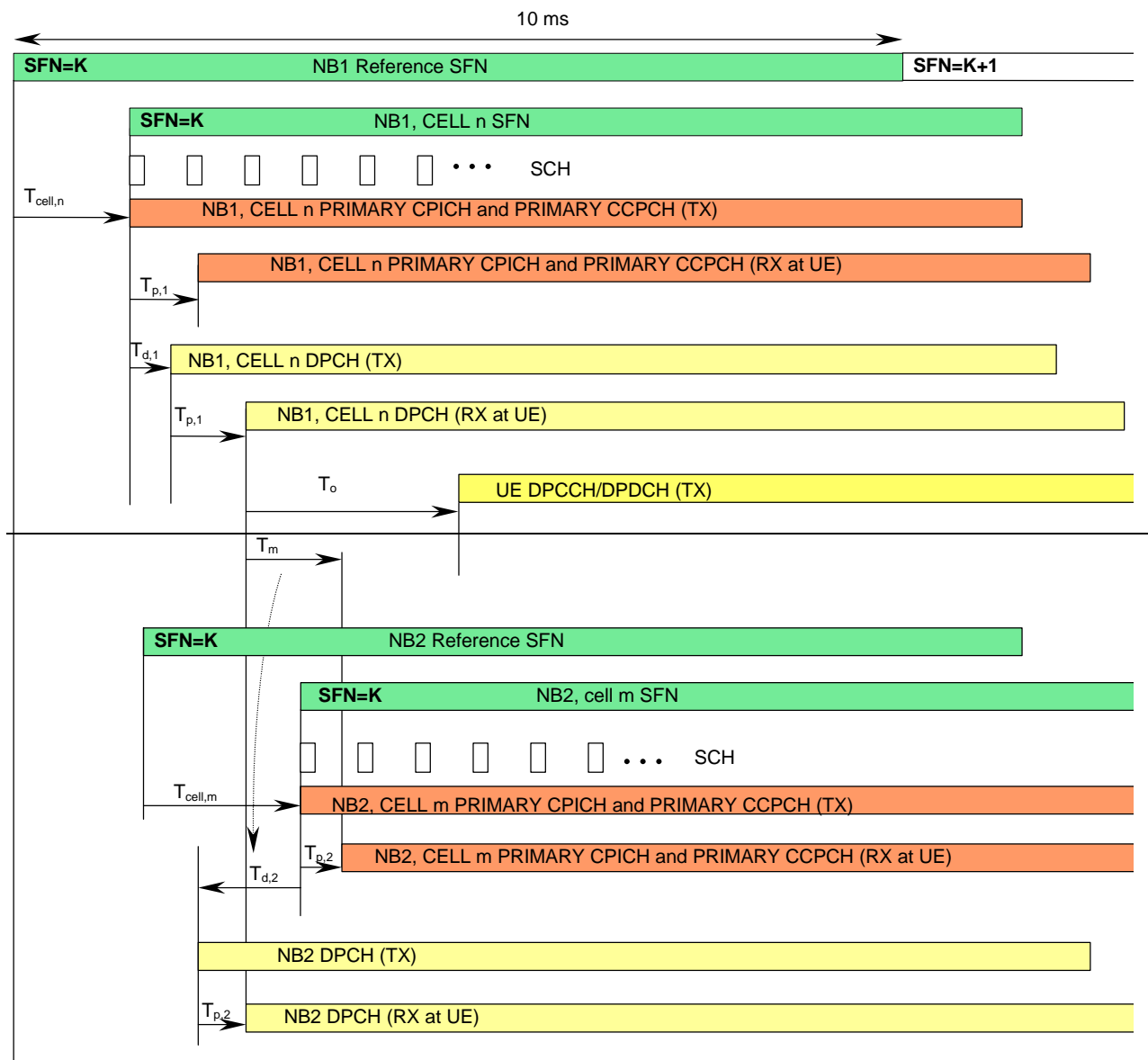
7 Timing relationship between physical channels

<Editors note: M=36864=512*72 needs to be confirmed.>

In general, a Node B covers *N* cells, where *N* ³ *1*. Each Node B has a Reference System Frame Number (SFN), which counts from *0* to *M-1* in Radio Frame (10 ms) intervals. *M* is a multiple of the superframe (72), and is TBD. The purpose of the Reference SFN is to make sure that the correct frames are combined at soft handover. Each cell has a Cell SFN, which is broadcast on the BCH.

The physical channel timing is shown in 3GPP RAN TS 25.401.

~~Figure 28 shows the proposed physical channel timing parameters in a soft handover situation including two Node Bs, NB1 and NB2. The timing parameters in Figure 28 refer to frame timing.~~

Figure 28: Physical channel timing relations.

The parameters in Figure 28 are explained below:

T_p: Propagation delay between Node B and UE.

T_{cell}: This timing offset is used for the frame timing of SCH, Primary CCPCH and the starting phase of all downlink scrambling codes in a cell. The resolution is TBD and depends on the maximum expected time dispersion. The range is one slot. T_{cell} is also the reference frame timing for the PRACH.
<Editors note: Descriptive text: The main purpose of T_{cell} is to avoid overlapping SCHs in different cells belonging to the same Node B. The resolution affects the number of possible cells in a Node B.>

T_d: This timing offset is used for the frame timing of DPCHs and Secondary CCPCHs. It can be individually set up for each DPCH and Secondary CCPCH. The T_d values for the latter may be broadcast on the BCH, or known a-priori. The resolution is 256 chips in order to maintain downlink orthogonality and the range is TBD.   <Editors note: Descriptive text: The purpose of T_d is:
—In an originating/terminating cell, to distribute discontinuous transmission periods in time, and also to distribute Node B-RNC transmission traffic in time.
—At soft handover, to synchronise downlink DPCHs to the same UE, in order to minimise the buffering requirements at the UE.>

~~T_o: This constant timing offset is used to set up the transmission frame timing of an uplink DPCCH/DPDCH in the UE. The value is TBD. The starting phase of the uplink scrambling code is synchronised with the uplink DPCCH/DPDCH frame timing.~~
~~<Editors note: Descriptive text: The uplink DPCCH/DPDCH transmission frame timing should be set to T_o seconds after the frame timing of the earliest received path of the downlink DPCH. T_o should be chosen to minimise the closed loop PC delay in as large cell-radii as possible.>~~

~~T_m: This value is measured by the UE and reported to the RNC prior to soft handover. The RNC can then notify this value to the target cell, which then knows how to set T_d to achieve proper reception and transmission frame timing of the dedicated physical channel.~~
~~<Editors note: Descriptive text: Note that since the UE reports the value T_m as the time difference between the received Primary CCPCH frame timing from the target cell and the earliest received existing DPCH path, the propagation delay to the target cell is already compensated for in the setting of T_d at the target cell. The DPCH signal from the target cell will reach the UE at the same time as the earliest received existing DPCH path. The only remaining error, besides frequency drift and UE mobility related errors, is due to a (known) rounding error at the target cell in order to maintain downlink orthogonality.>~~

7.1   DPCCH/DPDCH timing relations

7.1.1   Uplink

In uplink the DPCCH and all the DPDCHs transmitted from one UE have the same frame timing.

7.1.2   Downlink

In downlink, the DPCCH and all the DPDCHs carrying CCTrCHs of dedicated type to one UE have the same frame timing.

7.2   DSCH timing

~~<Editors note: DSCH timing needs to be checked for new chiprate.>~~

The relative timing between a DSCH and DCH is given as follows:

DSCH timing is identical to the cell primary CCPCH

DCH timing is asynchronous with max 1 slot (2560 chips) ahead or max 14 slots (35840 chips) behind. This determines explicitly which frame on DSCH carries the user data based on the TFCI or higher layer signaling on DCH.
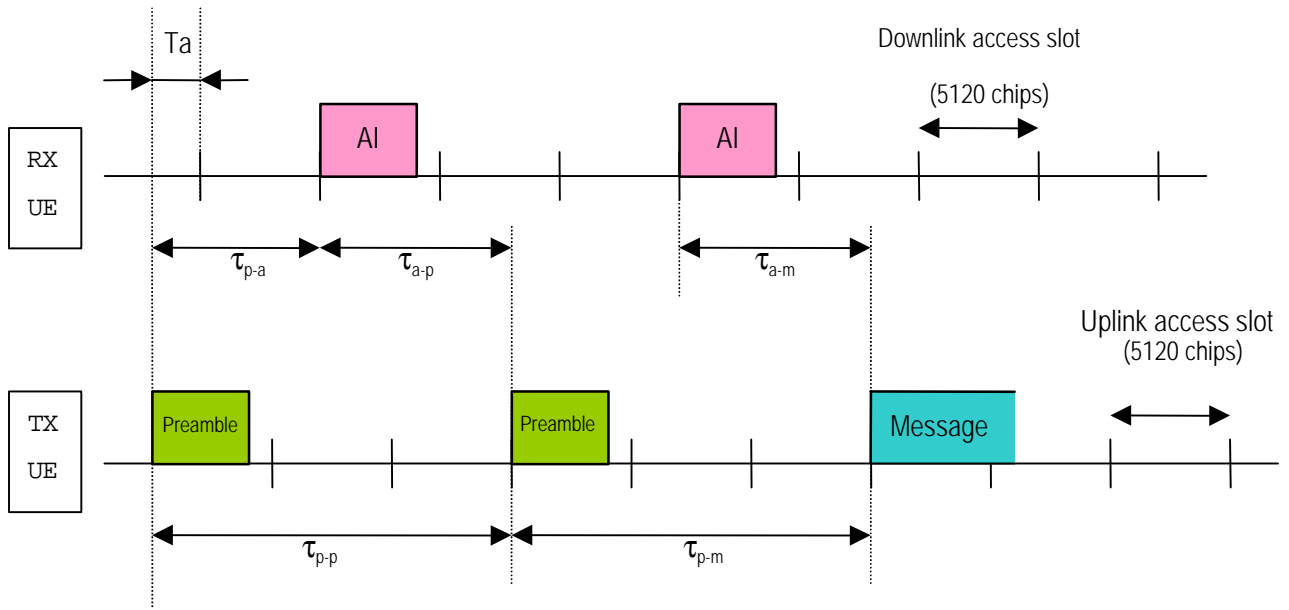
7.3   PRACH/RACH timing relation:

~~<Editors note: PRACH/RACH timing needs to be updateded for new chiprate.>~~

Figure 31: Timing of PRACH and AICH transmission as seen by the UE, with AICH transmission timing set to 0.
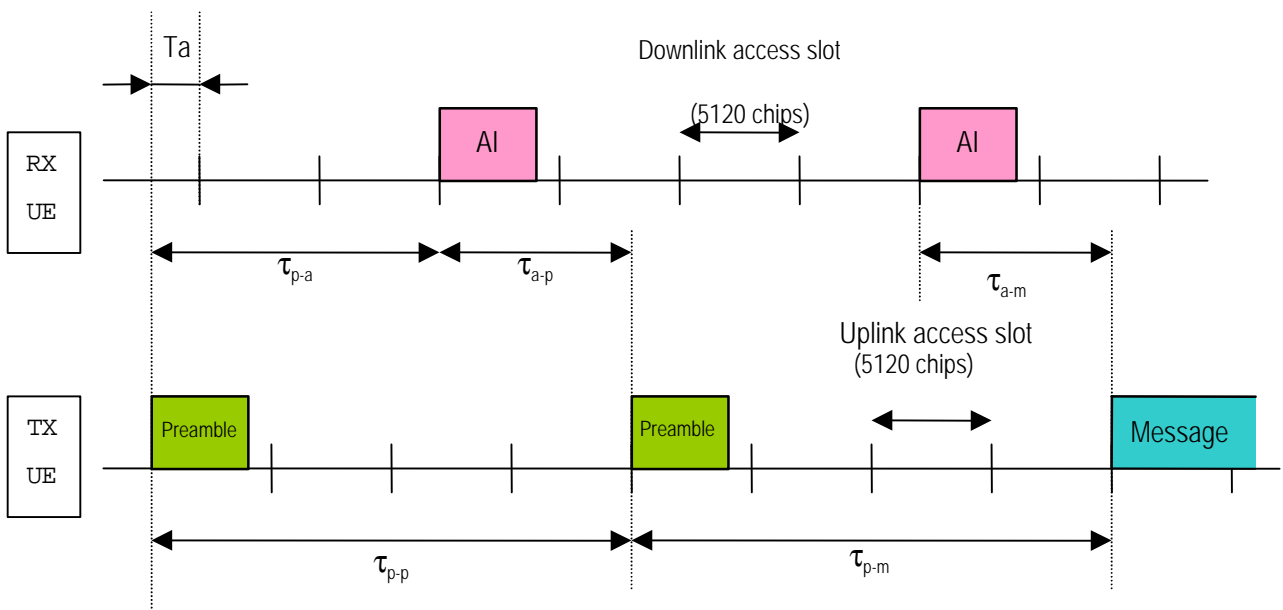

Figure 32: Timing of PRACH and AICH transmission as seen by the UE, with AICH transmission timing set to 1.

Figure 31 and Figure 32 illustrate the timing relation between PRACH and AICH as seen by the UE, with AICH transmission timing set to 0 and 1, respectively. ~~The timing figures define the case where all access slots are available. If not all access slots are available, Figure 28 and define the minimum values for~~ τ_{p-p}, τ_{p-m}, τ_{p-a} ~~and~~ τ_{a-p}.

- Both uplink and downlink access slots of length 5120 chips~~1.25 ms~~ are defined.

- For each downlink access slot there is a corresponding uplink access slot.

- The preambles are to be transmitted time aligned with the uplink access slots.

-The downlink access slots are transmitted time aligned with the PCCPCH frame boundary.

- An uplink access slot is transmitted a specified time τ_{p-a} before the corresponding downlink access slot.

- Subsequent preambles can be transmitted either three or four access slots after the latest transmitted preambles (τ_{p-p} is either 3 or 4 access slots), depending on the AICH transmission timing value.

- The message can be transmitted either three or four access slots after the latest transmitted preamble (τ_{p-m} is either 3 or 4 access slots), depending on the AICH transmission timing value.

The timing offset (T_a) between uplink and downlink access slots, as seen by the UE, is <u>the same as 1 slot duration of 2560 chips</u>0.5ms.

The timing of preamble-to-AICH (τ_{p-a}) has two alternative values: <u>7680 chips</u>1.75ms or <u>12800 chips</u>3ms, depending on the AICH transmission timing value.

The timing of AICH-to-preamble(τ_{a-p}) has one value: <u>7680 chips</u>2ms.

The timing of AICH-to-message(τ_{a-m}) has one value: <u>7680 chips</u>2ms.

7.4 Paging timing relation

<u>Figure </u>33 <u>illustrates the timing between an S-CCPCH frame and the corresponding frame of an associated PICH. The frame of the associated PICH precedes the corresponding S-CCPCH frame by $\tau_{PICH} = 3\times2560$ chips.</u>

PICH

Frame #N

S-CCPCH

Frame #N

$\tau_{PICH} = 3\times \textbf{2560 chips}$
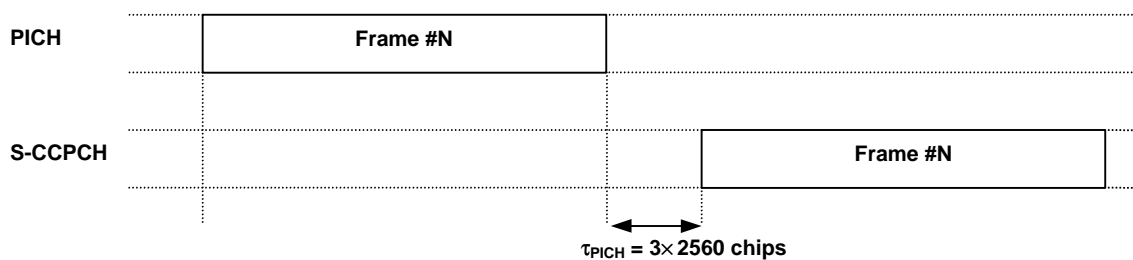
<u>Figure </u>33<u>: Timing between S-CCPCH and associated PICH</u>

Appendix A: Power Control Timing

<Editors note: Power control timing needs to be updated for new chiprate.>

<Editors note: The Power control timing described in this appendix should be seen as an example on how the control bits have to be placed in order to permit a short TPC delay. It seems appropriate to move this part later.>

In order to maximize the BTS-UE distance within which one-slot control delay is achieved, the frame timing of an uplink DPCH is delayed by 1024 chips 250μs from that of the corresponding downlink DPCH measured at the UE antenna.

Responding to a downlink TPC command, the UE shall change its uplink DPCH output power at the beginning of the first uplink pilot field after the TPC command reception. Responding to an uplink TPC command, BTS shall change its DPCH output power at the beginning of the next downlink pilot field after the TPC command reception. Note that the delay from the uplink TPC command reception to the power change timing is not specified for BTS. The UE shall decide and send TPC commands on the uplink based on the downlink SIR measurement. The TPC command field on the uplink starts, when measured at the UE antenna, 512 chips 125μs after the end of the downlink pilot field. BTS shall decide and send TPC commands based on the uplink SIR measurement. However, the SIR measurement periods are not specified either for UE nor BTS.

Fig. A-1 illustrates an example of transmitter power control timings.
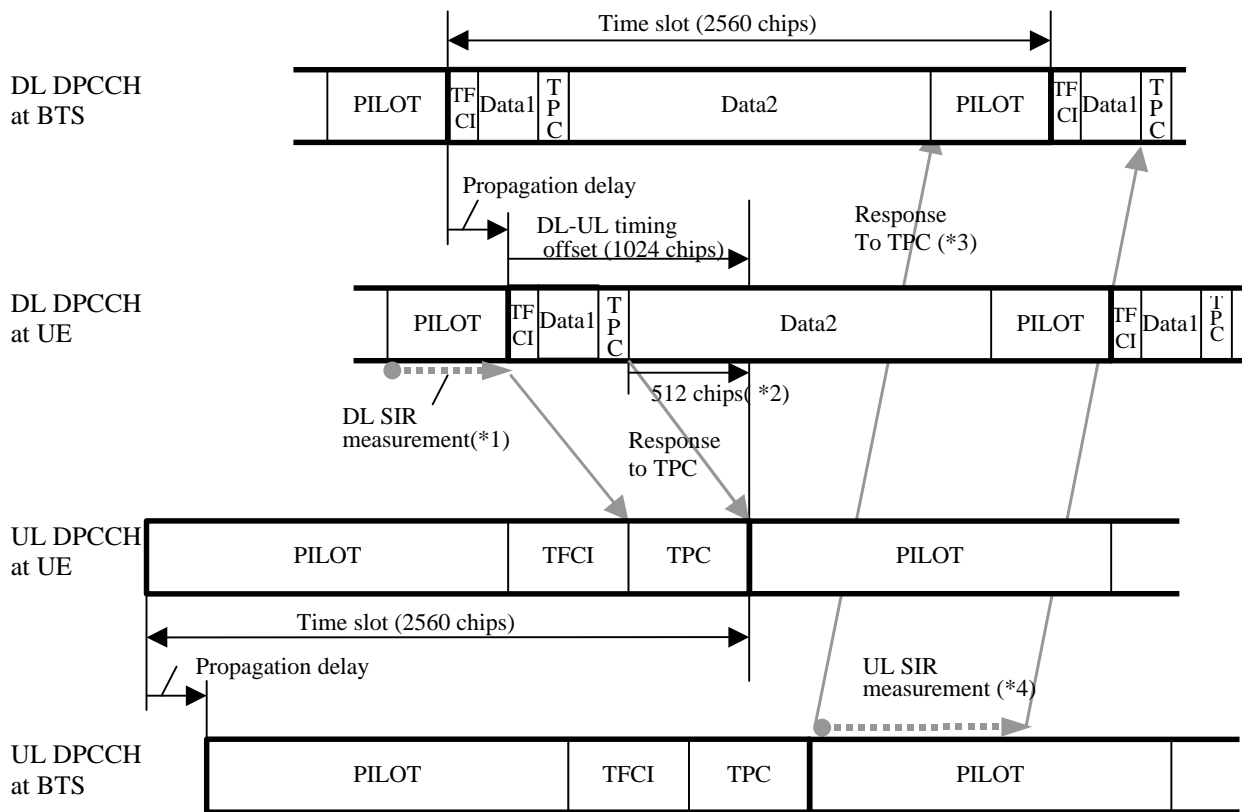
*1,4   The SIR measurement periods illustrated here are examples. Other ways of measurement are allowed to achieve accurate SIR estimation.
*2   Except the case of DL symbol rate=7.5ksps.
*3   If there is not enough time for BTS to respond to the TPC, the action can be delayed until the next slot.

Fig. A-1 Transmitter power control Timing

History

Document history		
V0.0.0	1999-02-12	Created document from UMTS XX.03, V1.3.0
V0.0.1	1999-02-18	Small changes
V0.1.0	1999-02-26	Version approved by WG1#2. The changes agreed at the meeting to incorporate e.g. ad hoc conclusions not yet included
V1.0.0	1999-03-05	Version approved by RAN. Identical to V0.1.0
V1.0.1	1999-03-17	Included adhoc conclusions from WG1#2 and editorial changes.
V1.0.2	1999-03-23	Added adhoc conclusions from WG1#3
V1.0.3	1999-03-24	Added further text from Adhoc 6
V1.1.0	1999-03-24	Version approved by WG1#3
V1.1.1	1999-04-14	Updated RACH and Tx diversity description. Updated multicode figure. Added pilot table for PCCPCH. Removed FACH mapping section.
V1.1.2	1999-04-19	Added adhoc conclusions and text proposals from WG1#4
V1.1.3	1999-04-20	Added further text proposals from WG1#4
V2.0.0	1999-04-20	Version approved by WG1#4
TS 25.211 V2.0.0	1999-04-22	Endorsed by TSG-RAN as TS 25.211 v2.0.0
V2.0.1	1999-06-04	Added adhoc conclusions and text proposals from WG1#5
V2.1.0	1999-06-04	Version approved by WG1#5
V2.1.1	1999-07-07	Updated according to chiprate change and CPICH
V2.2.0	1999-07-13	Approved by WG1#6.
V2.2.1	1999-08-12	Further changes including text proposals from WG1#6
Editor for TS 25.211 is: Andreas Wilde Nippon Ericsson K.K. Tel: +81 3 5216 9072 Fax: + 81 3 5216 9047 Email: andreas.wilde@nrj.ericsson.se This document is written in Microsoft Word 97.		