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Agenda Item:

Source: **CWTS WG1**

Title: **Method and Principle of Uplink Synchronization**

Document for: **Consideration**

Introduction

Following the harmonization of TD-SCDMA and UTRA-TDD, this document introduces the principle of uplink synchronization, which is one of the most important parts of the CWTS RTT proposal. The harmonization process was agreed among ARIB, CATT, DoCoMo, Ericsson, Nokia, Panasonic, RITT and Siemens (RP99248).

CDMA technology has been recognized as the main multiplex access technology. However, for the most CDMA systems, the uplink channels always work asynchronously. This means that the UEs' signals arrive at the Node B at different time. Thus, the asynchronous UEs are interfered with each other (Multiple-Access-Interference). It is known that CDMA is an interference-limited system, the unwanted interference may lead to the degradation of the system capacity, and then the power control scheme has to be deployed to solve this problem. For the present mobile communications systems, to estimate the locations of the UEs is difficult, to establish and maintain the uplink synchronization procedures between different UEs in a cell is also difficult because of multipath and shadow fading.

It is well known that uplink synchronization, or so-called synchronous CDMA will lead to higher capacity (theoretically 3dB when multipath could be negligible) and simplify the demodulator in Node B.

In this paper, a simple, effective and low-cost solution to establish and maintain the uplink synchronization between different UEs is presented. This technology has already been commercially used in the practical system (the SCDMA based Wireless Local Loop system deployed in China). In this method, all UEs' signals are spread with the orthogonal Walsh sequences and are sure to arrive at the demodulator in Node B at the same time.

The following contents are intended to work as the complementary material to understand the working principle of synchronous CDMA, which is adopted in the proposed TD-SCDMA RTT under consideration by ITU.

1. The frame and burst structure in TD-SCDMA (UTRA-TDD low chiprate mode) system

1.1. References

1.CWTS WG1 TS C1.21, "Physical channels and mapping of transport channels onto physical channels (TDD)"
2.CWTS WG1 TS C1.24, "Physical layer procedures (TDD)"

1.2. Frame structure

As shown in Figure 1, the frame structure of 3GPP TDD is adopted in TD-SCDMA proposal. A superframe of 720ms is divided into 72 radio frames of 10ms, and a radio frame of 10ms is then subdivided into 2 subframes of 5ms to match with the 5ms TDD interval in TD-SCDMA. The 5ms TDD interval is designed to meet the requirement of fast beamforming in high moving speed as 120km/h when the smart antenna technology is deployed.

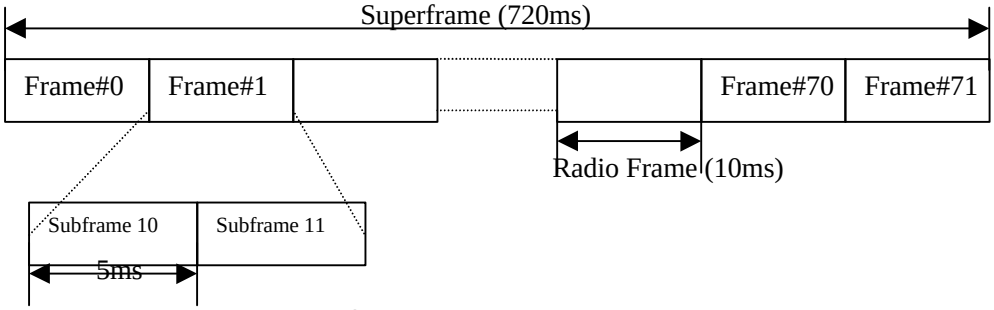
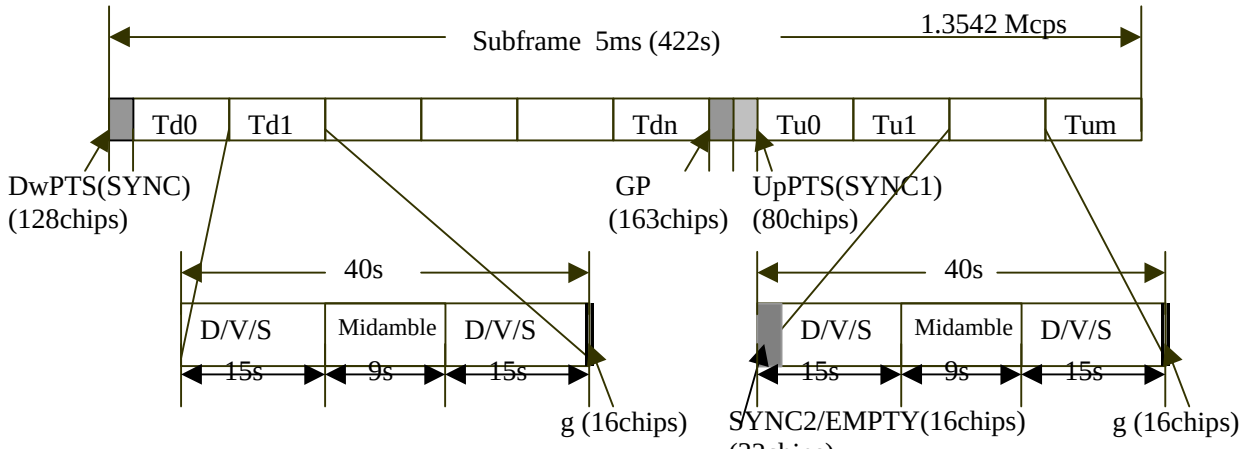


Figure 1. Frame structure

1.3. Burst structure and time slots assignment

Figure 2 shows the burst structure and the time slots assignment in one subframe.
The duration of each subframe is 5ms as shown in Figure 1. In each 5ms TDD interval, there are 10 main time slots and 3 special time slots, which are defined as follows:
DwPTS: a time slot including 64 chips of SYNC and 64 chips of guard period for downlink Pilot and downlink synchronization (SCH).
GP: a time slot including about 163 chips of guard period at Tx/Rx switching point.
UpPTS: a time slot including 48 chips of SYNC1 and 32 chips of guard period for uplink Pilot and closed loop uplink synchronization (SCH).
The location of TDD switching point (position of GP and UpPTS) may be varied depending on the uplink and downlink transmission data rate, but there is only one switching point in one subframe.
Among the 10 main time slots, all the main time slots (at least the first main time slot) before the switching point are allocated as downlink, while all the main time slots (at least the last main time slot) behind the switching point are allocated as uplink. In detail, the first code channel in time slot Td0 is allocated as BCH or PCH, and among other code channels in Td0 time slot, up to 8 code channels could be allocated as FACH. The other code channels in Td0 and other main downlink time slots could be assigned as downlink traffic channels. At the UE side, maximum 8 code channels in Tu0 time slot could be allocated as RACH. The other code channels in Tu0 and other main uplink time slots could be assigned as uplink traffic channels. The change of the subframe structure will be broadcast over the BCH. In each main time slot, there may be 1/2/4/8/16 code channels according to the spreading factor . Due to the synchronous character, only 16 chips period as guard time between each main time slot is required.



Where $n + m + 2 = 10$

Figure 2. Time slot assignment for the TDD subframe

1.4. Burst structure for uplink synchronization

Among the whole TDD time slots in a subframe with length of 5ms, only DwPTS, UpPTS time slots and SYNC2/EMPTY field in each uplink traffic channels have direct relation with the synchronization mechanism, as shown in Figure 2.

2. The establishment of the uplink synchronization

The main guard time slot (GP) is a long empty period to provide the switching from Tx to Rx in each subframe; it plays an important role in the UEs' uplink synchronization establishment procedures. Theoretically, the guard time between the uplink and downlink should be larger than the sum of the signal processing time and the $2D/C$, where D is the largest distance between the Node B and the UE (or the maximum radius of the cell), and C is the speed of light, which equals to $3\times10^8 m/s$. For the convenience of the system, it is necessary to keep the guard time constant at the side of the Node B, while the UE adjusts the Tx time according to the distance from it to the Node B. In physical layer signaling, two special fields in each main downlink time slot are designed. One is called synchronization shift (SS); the other is named as power control (PC). Once the UE's uplink synchronization sets up, the Node B can calculate the distance between the UE and the Node B based on the Tx time of the UE.

When a UE is powered on, it will search the first 4 strongest SYNC sequences from the nearby Node Bs and choose the most suitable one and try to access , i.e., it will seek the training sequence SYNC from the Node B at the first. Since the SYNC in DwPTS are always transmitted by the Node B with the specified Gold code sequences and with higher Tx power than any other main downlink time slots, the SYNC will be easily recognized by the UE . Meanwhile, the UE will try to read the contents in BCH following DwPTS to find RACH/FACH pairs and their B/I status, etc.

Although the UE can receive the downlink synchronization signal from the Node B at this moment, it is not sure when to transmit and how to establish the uplink synchronization with other UEs, because it does not know its distance from the Node B. In this case, the UE will roughly estimate its next Tx time and Tx power level, according to the detected arrival time and power level of the received training sequence (SYNC) in DwPTS. And then it will randomly choose a SYNC1 sequence in UpPTS and a pair of RACH/FACH among the idle access channel pairs, and send the SYNC1 and access request on the RACH with the estimated Tx time and Tx power level. These are the open loop uplink synchronization procedures.

The SYNC1 sequence following the guard time slot is used only in the UpPTS for uplink synchronization; it is a known orthogonal Gold code sequence. In this period, only the UEs (maximum 8 UEs) that want to establish the uplink synchronization transmit with different Gold code sequences followed by RACHs while other code channels are in their EMPTY period to avoid any interference to them. Once the Node B detects the required output from one UE, or has found the correlated peak value exceeding the minimum threshold, the SS and PC could be obtained by comparing the detected arrival time and power level of the SYNC1 with the expected arrival time and power level. Meanwhile, the Node B will try to despread the signals in the following RACH. If the following contents are verified to be correct by the CRC and other methods, the Node B will response to the UE by sending its control signaling over the chose FACH in the following subframe. The control signaling includes the packets of higher layer signaling such as Link_Grant and assigned traffic channel information, and the fields of physical layer signaling such as SS and PC, etc.

Once the UE receives the above mentioned control signaling in the chose FACH, its access request has been accepted by the Node B.. Meanwhile, it must adjust its Tx time and Tx power level according to the received SS and PC information, and then continue its access procedures in the same RACH/FACH pair of the next subframe. These are the closed loop uplink synchronization procedures.

When a collision happened or in bad propagation environment, the Node B can't receive

SYNC1 and RACH. In these cases, the UE will not get any useful response from the Node B in the FACH of next subframe, thus the UE will have to adjust it's Tx time and Tx power level based on the last received SYNC and re-send a access request after a random delay.

Besides situations mentioned above , all kinds of procedures for the UE could be concluded as follows:

1. If the UE has detected no answer or error answer in the control signaling packets in the FACH, it will abandon these packets. To avoid the risk of collision with other UEs, it will re-send the access request with the newly estimated Tx time and Tx power level based on new SYNC after a random delay.
2. If the UE has correctly received the downlink control signaling packets in the FACH, but the PID does not match, the UE will abandon these packets. To avoid the risk of collision with other UEs, it will re-send the access request with the newly estimated Tx time and Tx power level based on new SYNC after a random delay.
3. If the UE has correctly received the downlink control signaling packets in the FACH, but without PID, the UE will abandon these packets. To avoid the risk of collision with other UEs, it will adjust its Tx time and Tx power level as the SS and PC information informed by the Node B and re-send the access request after a random delay.
4. If the access request can be correctly received by the Node B, and the response from Node B in FACH is also correctly received by the UE with the PID matched, the UE understands that the Node B has accepted its access request. Then the UE will adjust its Tx time and Tx power level as the SS and PC information informed by the Node B. And it will continue its access procedures in the same RACH/FACH pair of the next subframe

If the UE can not access the Node B as the above 4 procedures within the fixed period, it will turn into standby state.

3. Maintenance of the uplink synchronization

The maintenance of the uplink synchronization is vital in the proposed system, the special field SYNC2/EMPTY is used in each traffic channel of each main uplink time slot. In each main uplink time slot, there is only one code channel can transmit SYNC2 in the SYNC2/EMPTY field when its Walsh code number matches with the Subframe Number (FN, a L1 parameter in BCH) while other code channels will be EMPTY in this period. By use of this mechanism, the Node B will successfully obtain the correlation peak value and the arrival time from the active UE. Based on the arrival time, the Node B can calculate the uplink synchronization tolerance of the UE and hence feed back the SS information to the UE in the corresponding downlink traffic channel of the next subframe, and then enable the UE to adjust its Tx time correctly. These procedures guarantee the reliability of the uplink synchronization. Obviously, the uplink synchronization will be checked once per 16 TDD intervals or 80ms. Because the accuracy in uplink synchronization is about $\pm 1/8$ chip duration, or approximately 90ns in 1.3542Mcps chiprate, the maximum distance variation between Node B and the UE will be $90\times10^{-9}\times3\times10^{8}=27\text{m}$. When the UE is moving at the speed of 120km/h, the distance variation will be 2.7m only in 80ms duration. Actually, a UE will need to adjust its Tx time once or twice per second only. In other words, some burst with error bit will not affect the maintenance of uplink synchronization.

4. Other topics related to synchronous CDMA

4.1. The accuracy in uplink synchronization

The specification for the accuracy of uplink synchronization is $\pm 1/8$ chip duration. Theoretically, when the uplink synchronization tolerance is larger than $\pm 1/4$ chip duration, the obvious Multiple-Access-Interference will appear.

4.2. Chiprate

Based on the above accuracy in uplink synchronization, the timing tolerance will be approximately 90ns for chiprate of 1.3542Mcps or 30ns for chiprate of 4.096Mcps

respectively. Since the frequency stability or timing accuracy of most proposed IMT2000 RTTs is 0.1ppm for UE, the random timing tolerance will be the same level as 100ns. Therefore, a low chiprate is better suited for the uplink synchronization.

4.3. Smart antenna

Smart antenna is a widely accepted technology in IMT2000 RTTs. It is well known that the DOA estimation and beamforming of smart antenna is performed in digital baseband (DBB). It is requested that the DBB receivers in each Rx path in Node B should bring the phase and amplitude information of the Rx signal to the DBB DSP for smart antenna processing. The simplest way to design the DBB receiver is that shown in Figure 3 as an example. It is obvious that the receiver can only be used in a CDMA system with uplink synchronization. In other words, synchronous CDMA will lead to a simplified solution to smart antenna system.

4.4. Multipath

One may find that the reported uplink synchronization technology can only guarantee the uplink synchronization between the main paths of each code channel; the multipath components are still asynchronous. The asynchronous multipath components will lead to interference as in any other CDMA RTTs. Therefore, the uplink synchronization reaches optimum performance, when combined with techniques like smart antennas and channel equalization.

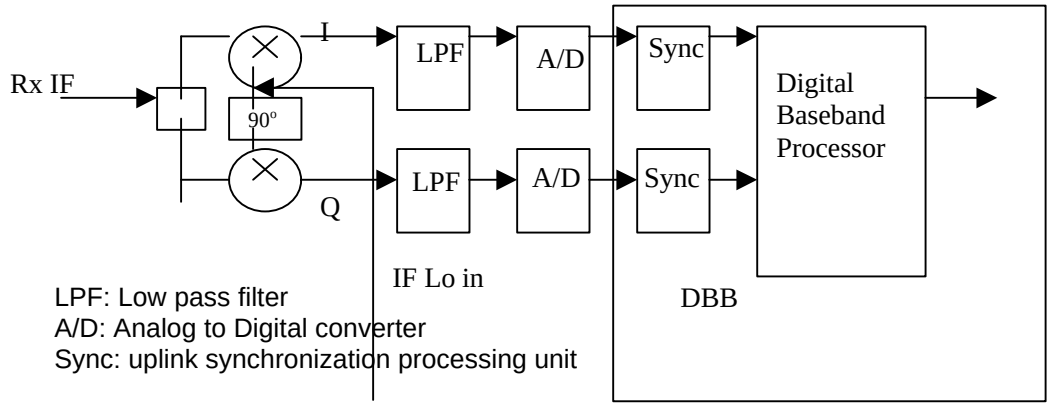
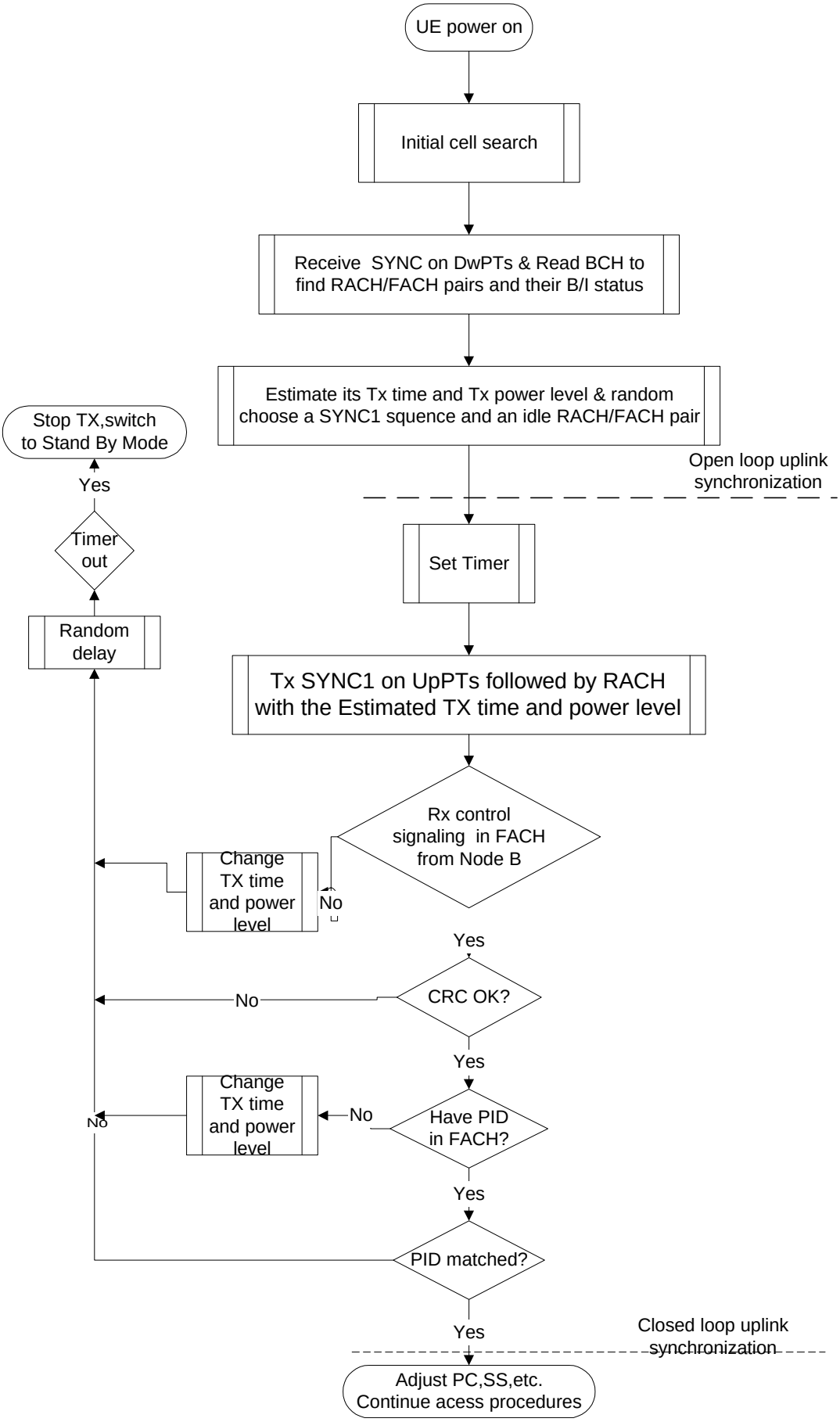


Figure 3. Example for DBB receiver used in synchronous CDMA and smart antenna system

5. Conclusion

In this working document, a basic description for establishing and maintaining of the uplink synchronization between a Node B and UEs is provided, as well as the detailed frame and burst structure used in TD-SCDMA (UTRA-TDD low chiprate mode) system. It is shown that the uplink synchronization technology will mainly benefit to simplify the receiver in Node B and to adopt the smart antenna technology.


UE power on
Initial cell search
Receive SYNC on DwPTs & Read BCH to find RACH/FACH pairs and their B/I status
Estimate its Tx time and Tx power level & random choose a SYNC1 squence and an idle RACH/FACH pair
Open loop uplink synchronization
Set Timer
Tx SYNC1 on UpPTs followed by RACH with the Estimated TX time and power level
Rx control signaling in FACH from Node B
No
Change TX time and power level
Yes
CRC OK?
No
Yes
Have PID in FACH?
No
Change TX time and power level
No
Yes
PID matched?
Yes
Closed loop uplink synchronization
Adjust PC,SS,etc. Continue acess procedures
Timer out
Yes
Random delay
Stop TX,switch to Stand By Mode