Agenda Item:

Source: **Nokia**

Title: **Text proposal for downlink scrambling code phase shift parameter**

Document for: **Discussion**

_____

Introduction

Nokia suggests that the phase shift parameter has only one value common for all chip rates. The value to use is 131072 which quanratees that both the in phase component and the quadrature component has a different segment of a Gold code. It is pointed out that there is not available a "three taps per register" structure for downlink because of different polynomials. If a simpler structure is desired the scheme of R1-99379 should be used.

Text proposal for 25.213

5.2.2 Scrambling code

The total number of available scrambling codes is 512, divided into 32 code groups with 16 codes in each group.

[In order to avoid code limitation in some cases, e.g. when increasing the capacity using adaptive antennas, the possibility to associate several scrambling codes with one cell (BCH area) has been identified as one solution. The exact implementation of such a scheme is still to be determined.]

<Editor's note: Use of multiple downlink scrambling codes to aid adaptive antennas are ffs.>

The scrambling code sequences are constructed by combining two real sequences into a complex sequence. Each of the two real sequences are constructed as the position wise modulo 2 sum of [40960 chip segments of] two binary m-sequences generated by means of two generator polynomials of degree 18. The resulting sequences thus constitute segments of a set of Gold sequences. The scrambling codes are repeated for every 10 ms radio frame. Let x and y be the two sequences respectively. The x sequence is constructed using the primitive (over GF(2)) polynomial $1+X^7+X^{18}$. The y sequence is constructed using the polynomial $1+X^5+X^7+X^{10}+X^{18}$.

<Editor's note: [ ] is due to the fact that only 4.096Mcps is a working assumptions. 1.024, 8.196, and 16.384Mcps are ffs.>

Let $n_{17} \dots n_0$ be the binary representation of the scrambling code number n (decimal) with n_0 being the least significant bit. The x sequence depends on the chosen scrambling code number n and is denoted x_n, in the sequel. Furthermore, let $x_n(i)$ and $y(i)$ denote the i:th symbol of the sequence x_n and y, respectively

The m-sequences x_n and y are constructed as:

Initial conditions:
$x_n(0)=n_0$, $x_n(1)=n_1$, $\dots =x_n(16)=n_{16}$, $x_n(17)=n_{17}$
$y(0)=y(1)=\dots =y(16)=y(17)=1$

Recursive definition of subsequent symbols:
$x_n(i+18) = x_n(i+7) + x_n(i)$ modulo 2, $i=0,...,2^{18}-20$,
$y(i+18) = y(i+10)+y(i+7)+y(i+5)+y(i)$ modulo 2, $i=0,..., 2^{18}-20$.

The n:th Gold code sequence z_n is then defined as
$z_n(i) = x_n(i) + y(i)$ modulo 2, $i=0,..., 2^{18}-2$.

These binary code words are converted to real valued sequences by the transformation '0' -> '+1', '1' -> '-1'.
Finally, the n:th complex scrambling code sequence C_{scramb} is defined as (the lowest index corresponding to the chip scrambled first in each radio frame): (see Table 1 for definition of N and M)

$C_{scramb}(i) = z'_n(i) + j\, z'_n(i+M)$, $i=0,1,...,N-1$.

<Editor's note: the values 3584 and 40960 areis based on an assumption of a chip rate of 4.096 Mcps.>
Note that the pattern from phase 0 up to the phase of 10 msec is repeated.
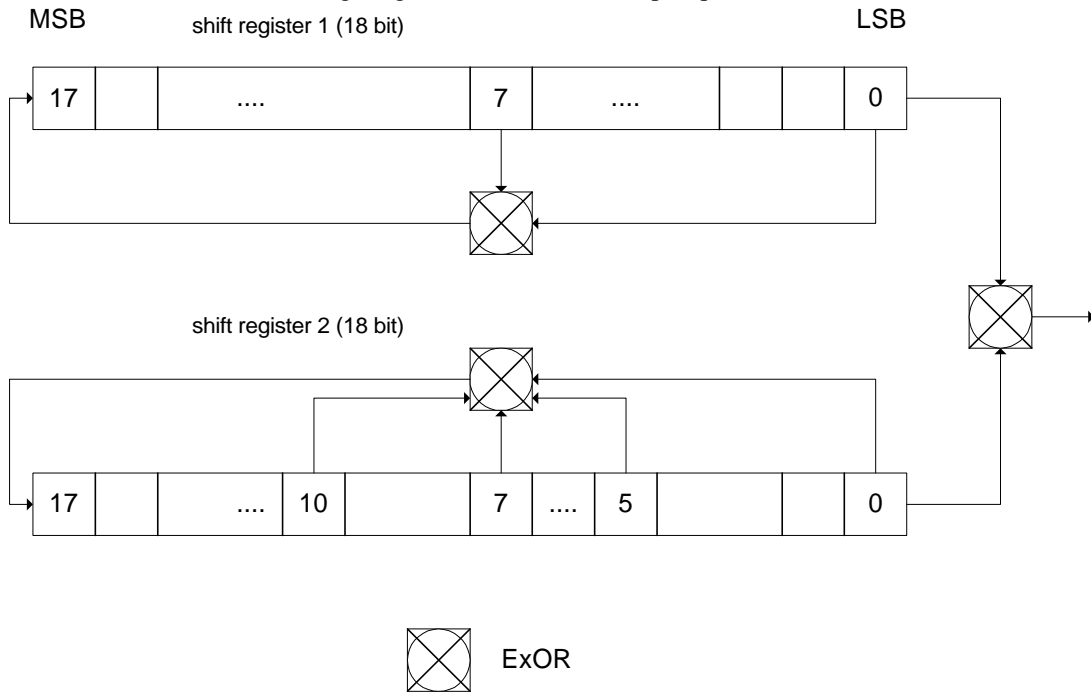The index *n* runs from 0 to 511 giving 512 distinct 40960 chip sequences.

Figure 1. Configuration of downlink scrambling code generator

Chip rate (Mcps)	Period	IQ Offset	Range of phase (chip)	
	N	M	for in-phase component	for quadrature component
[1.024]	[10240]	[896131072]	0 – N-1	M – N+M-1
4.096	40960	3584131072		
[8.192]	[81920]	[7168131072]		
[16.384]	[163840]	[14336131072]		

Table 1. Correspondence between chip rate and downlink scrambling code phase range