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Title: Further buffer complexity and processing time considerations on HARQ

Document for: Discussion

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1. Introduction

This document continues the discussion on buffer size and processing time issues that have already been adressed in [1], [2]. Whereas the concept of stop-and-wait HARQ has been discussed in the previous documents, no assumptions have yet been made on the feasible number of subchannels N and HSDPA TTI length. The implicit assumption in examples has been either N=2 or N=4. As was already shown in [2], N = 2 makes UE and RNS timing requirements very strict

2. Receiver buffer size

2.1 Buffer sizes for N=4, TTI = 5 (from HSDPA TR25.848)

As a basis for comparison, the example used in RAN WG1 TR25.848, i.e. N=4, TTI = 5 slots, is used as a frame of reference. Tables 1 and 2 show the maximum buffer size for this HARQ process assuming Chase combining.

Table 1. Buffer at soft combining stage for 10 code channels, HSDPA TTI = 5 slots

SF	Maximum buffer size for N-channel SAW HARQ, N=4, 3.33 ms frame, modulation symbols (I,Q pairs) buffered (Ksymbols)			
	QPSK	8-PSK	16-QAM	64-QAM
16, 10 code channels or 32, 20 code channels	64 (max 4.8 Mbps)	64 (max 7.2 Mbps)	64 (max 9.6 Mbps)	64 (max 14.4 Mbps)

Table 2. Memory at the input of turbo decoder for 10 code channels, HSDPA TTI = 5 slots

SF	Maximum buffer size for N-channel SAW HARQ, N=4, 3.33 ms frame, soft symbols buffered (Ksymbols)			
	QPSK	8-PSK	16-QAM	64-QAM
16, 10 code channel or 32, 20 code channels	64 (max 4.8 Mbps)	96 (max 7.2 Mbps)	128 (max 9.6 Mbps)	192 (max 14.4 Mbps)

2.2 Buffer sizes for N = 5, TTI = 3

By increasing the number of subchannels from four to five and shortening the TTI length to three slots results in maximum buffer sizes shown in tables 3 and 4. The *buffer size is about 75%* of N=4, TTI = 5 slots.

Table 3. Buffer at soft combining stage for 10 code channels, HSDPA TTI = 3 slots

SF	Maximum buffer size for N-channel SAW HARQ, N=5, 2.0 ms frame, modulation symbols (I,Q pairs) buffered (Ksymbols)			
	QPSK	8-PSK	16-QAM	64-QAM
16, 10 code channels or 32, 20 code channels	48.0 (max 4.8 Mbps)	48.0 (max 7.2 Mbps)	48.0 (max 9.6 Mbps)	48.0 (max 14.4 Mbps)

Table 4. Memory at the input of turbo decoder for 10 code channels, HSDPA TTI = 3 slots

SF	Maximum buffer size for N-channel SAW HARQ, N=5, 2.0 ms frame, soft symbols buffered (Ksymbols)			
	QPSK	8-PSK	16-QAM	64-QAM
16, 10 code channels or 32, 20 code channels	48.0 (max 4.8 Mbps)	72.2 (max 7.2 Mbps)	96.0 (max 9.6 Mbps)	144 (max 14.4 Mbps)

2.3 Buffer sizes for N = 6, TTI = 3 slots

By further increasing the number of subchannels to six and employing a TTI of three slots, maximum buffer sizes are as depicted in tables 5 and 6. In this case the *buffer size is about 90%* of N=4, TTI = 5 slots.

Table 5. Buffer at soft combining stage for 10 code channels, HSDPA TTI = 3 slots

SF	Maximum buffer size for N-channel SAW HARQ, N=6, 2.0 ms frame, modulation symbols (I,Q pairs) buffered (Ksymbols)			
	QPSK	8-PSK	16-QAM	64-QAM
16, 10 code channels or 32, 20 code channels	57.6 (max 4.8 Mbps)	57.6 (max 7.2 Mbps)	57.6 (max 9.6 Mbps)	57.6 (max 14.4 Mbps)

Table 6. Memory at the input of turbo decoder for 10 code channels, HSDPA TTI = 3 slots

SF	Maximum buffer size for N-channel SAW HARQ, N=6, 2.0 ms frame, soft symbols buffered (Ksymbols)			
	QPSK	8-PSK	16-QAM	64-QAM
16, 10 code channels or 32, 20 code channels	57.6 (max 4.8 Mbps)	86.4 (max 7.2 Mbps)	115.2 (max 9.6 Mbps)	172.8 (max 14.4 Mbps)

It can be seen that reducing the TTI length from 5 slots to 3 slots causes savings in maximum buffer size even when the number of HARQ subchannels is increased. In order to fulfill processing time considerations, the subchannels in general have to be increased when TTI length is reduced if a given time relation is to be preserved. It has to be noted that all the values presented represent soft symbols; in baseband implementation each soft symbol will require a number of bits for storage depending on desired accuracy.

3. Processing time considerations

Figure 1 shows the general concept of timing for HARQ process. After having received a packet on HSPDSCH the UE has T_{UEP} for processing and sending acknowledgement to the Node B. Based on the acknowledgement the network decides whether it resends the TTI or transmits a new packet. For the UE to know that Node B is transmitting something to it, a pointer is assumed to be transmitted in downlink. This pointer identifies the UE that will have a packet to be received in the next HSDPA TTI. The processing time available for Node B between receiving the acknowledgement and transmitting the pointer is T_{NBP}. The length of pointer directly affects the available processing time in Node B. A pointer of one time slot would relax timing requirements compared to a pointer of three time slots. However, the signaling to be included in the pointer is much more difficult to fit only in one time slot. These two issues are to be weighed in order to reach a good tradeoff.

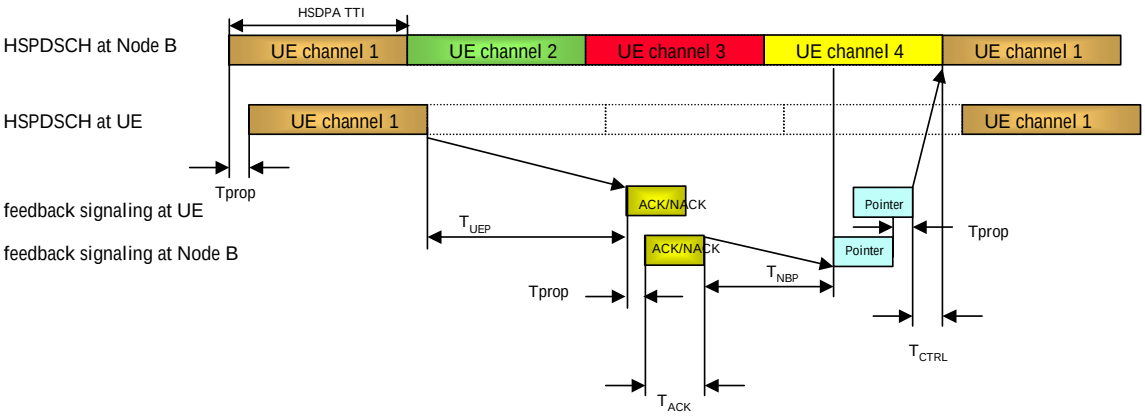

Figure 1. HARQ timing schematic for N=4

In tables 7 – 9 some estimations for available processing time is depicted for N=4, N=5 and N=6. The timing calculations assume that a pointer of length 1 slot or 3 slots is transmitted prior to the respective packet and control field – control field and data are transmitted in parallel. The acknowledgement signal from UE may be spread over one of more slots. However, the longer T_{ACK} becomes, the less processing time there is available for UE and RNS. In the tables, T_{ACK} = 1 slot is assumed. Furthermore, as one example, it is assumed that at least 2 ms is reserved for Node B processing, i.e. 3.5 slots in practise. The effect of unsynchronized DL timing of UEs is taken into account by deducting one slot from the total UE + Node B timing.

Table 7. UE and Node B processing times based on N=4.

Parameter	Sequential ptr, parallel ctrl and packets	
	3 slot TTI	**5 slot TTI**
T_{UEP}	1.00 ms (0.5xTTI)	5.00 ms (1.5xTTI)
T_{NBP}	2.33 ms	2.33 ms

Table 8. UE and Node B processing times based on N=5, N=6, pointer 1 slot.

Parameter	Sequential ptr, parallel ctrl and packets	
	3 slot TTI, N=5	**3 slot TTI, N=6**
T_{UEP}	3.00 ms (1.5xTTI)	5.00 ms (2.5xTTI)
T_{NBP}	2.33 ms	2.33 ms

Table 9. UE and Node B processing times based on N=5, N=6, pointer 3 slots.

Parameter	Sequential ptr, parallel ctrl and packets	
	3 slot TTI, N=5	**3 slot TTI, N=6**
T_{UEP}	1.67 ms (0.8xTTI)	3.67 ms (1.8xTTI)
T_{NBP}	2.33 ms	2.33 ms

The two bottom rows of the tables show the total time available from UE and Node B processing. There are many factors to be considered when evaluating whether the total time is sufficient.

- Minimum Node B processing time
- Length of pointer information field
- Length of the HSDPA TTI

Allocating the processing time between UE and Node B can be done by selecting the relative transmit instant of UE acknowledgement with respect to the transmission of HSPDSCH in downlink. The earlier the ACK is sent, the more time there is available for Node B processing. As shown in the example figures, it may be safe to reserve for example 2 ms (three time slots) for Node B processing so that there is enough time for updating all the data and scheduling for the respective UE in the network.

The selection of pointer field length is a tradeoff between Node B processing time and amount of available signaling as stated earlier. A one-slot pointer leaves most time for processing but it cannot contain a lot of information. On other hand, each additional slot for the pointer reduces available processing time by 0.67 ms. For practical reasons, we assume here that all the HSDPA feedback and information fields are multiples of a time slot – subslot divisions make processing only more difficult.

The length of the HSDPA TTI also has an impact on the processing time needed. Since a shorter TTI contains fewer bits than a longer one, the processing load for baseband processing such as interleaving and turbo decoding is smaller and less time is consumed.

3. Conclusion

The buffer size calculations show reduction in required buffer size when the number of subchannels is increased from N=4 to N=5 or N=6 while at the same time shortening TTI length from 5 slots to 3 slots. The processing time calculations give an estimate on how the available time for UE and RNS processing consequently changes. It can clearly be seen that N=4 with TTI=3 slots makes for very strict timing requirements for the baseband hardware – the processing time for UE (or Node B) can be less than one TTI. Thus, the most interesting comparison is that between N=4, TTI=5 slots and N=5&6, TTI = 3 slots. When pointer is 1 slot in length, N=6, TTI=3 slots gives the same available processing time than N=4, TTI=5 slots. N=5, TTI=3 slots provides less processing time, thus the UE has roughly one TTI length less time available for processing. The receiver buffer size for N=6, TTI=3 slots is slightly smaller than for N=4, TTI=5 slots. On the other hand, N=5, TTI=3 slots gives a 25% reduction in buffer size over N=4, TTI=5 slots and still about 17% saving over N=6, TTI=3 slots.

Naturally, the buffer sizes in practice will be considerable since the soft symbols are represented by several bits. Furthermore, with incremental redundancy combining the buffer sizes are a multiple of those for Chase combining as addressed in [2]. However, processing time considerations seem to make N=6, TTI = 3 slots favourable over N=5, TTI = 3 slots. In this way, buffer size is reduced over N=4, TTI = 5 without adverse impact on timing. It is also desirable to limit N to only one figure in order to scale down the complexity of the HSDPA concept. Thus, it is seen that N=6, TTI=3 slots presents the best tradeoff for buffer size minimization and reasonable processing timing requirements.

REFERENCES

[1] TSGR1#17, R1-00-1464, "Text proposal for HARQ complexity evaluation in HSDPA TR", Nokia.

[2] TSGR1#18, R1-01-0128, "Text proposal on HARQ complexity for TR25.848", Nokia.