TSG-RAN Working Group 1 meeting #18 ***TSGR1#18(01)0055***
Boston, USA, Jan. 15 – Jan. 18, 2001

Agenda Item:
Source: SK Telecom
Title: (Draft) Timing control issues on USTS
Document for: Discussion

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1. Introduction

Regarding timing control for USTS, the following two issues were raised in the last WG1 meeting:
- Why 20 msec for tracking process?
- Impact on the UL/DL timing?

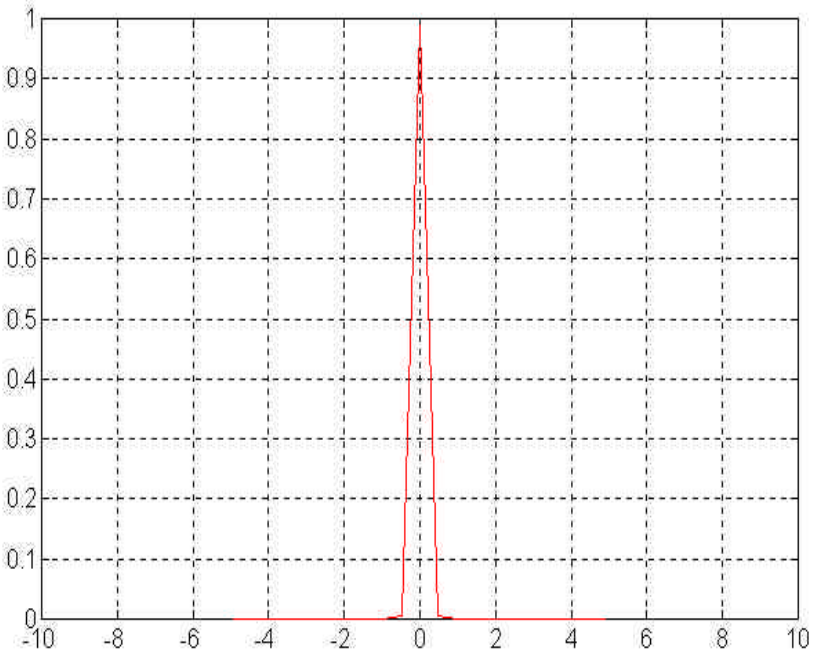
This document discusses the above two issues and also covers some comments we've got privately.

2. Choosing 20 msec for tracking process

Multipaths may exist in the range of a few seconds and we can find many results on the time-averaged or stochastic characteristic of multipath fading. However, unfortunately we have not been able to find any reports on the variation of receiving timing of multipaths so far. Samsung did measure the round trip delay (RTD) variation with current IS-95 system three years ago in the following situation.
- RTD data collected at urban area, the cell site is located at Okeum in Seoul
- Commercial IS-95 service is on over cellular band (800MHz band)
- Resolution of the RTD is Tchip/4, where the chip rate is 1.2288 Mcps
- Mobile stations are selected randomly
- 36 calls which last more than 10 seconds are examined
- 36 call data was collected from 1st FA among 4 FA(s) at 97.12.30 daytime

Figures 1 and 2 shows the results, where x-axis is the RTD variation (RTD_i ? $RTD_{i?1}$) with i and i-1 being the i-th and (i-1)-th measurement points. The measurement interval was set to 80 msec and 1000 msec for Figures 1 and 2, respectively. It can be seen that the variation of RTD of the main path is within ?1/4 chip with a very high probability when the measurement interval is 80 msec. If we take into account the different chip rates in IS-95 and W-CDMA, the arrival time variation of 1/4 chip in IS-95 corresponds to about 1 chip in W-CDMA. Hence, the RTD variation with a measurement interval of 80 msec is expected to be about 1 chip in W-CDMA. So, if we assume 1/4 chip timing control step size and 20 msec timing control interval, tracking process can catch up the less than 1 chip variation in 80 msec.

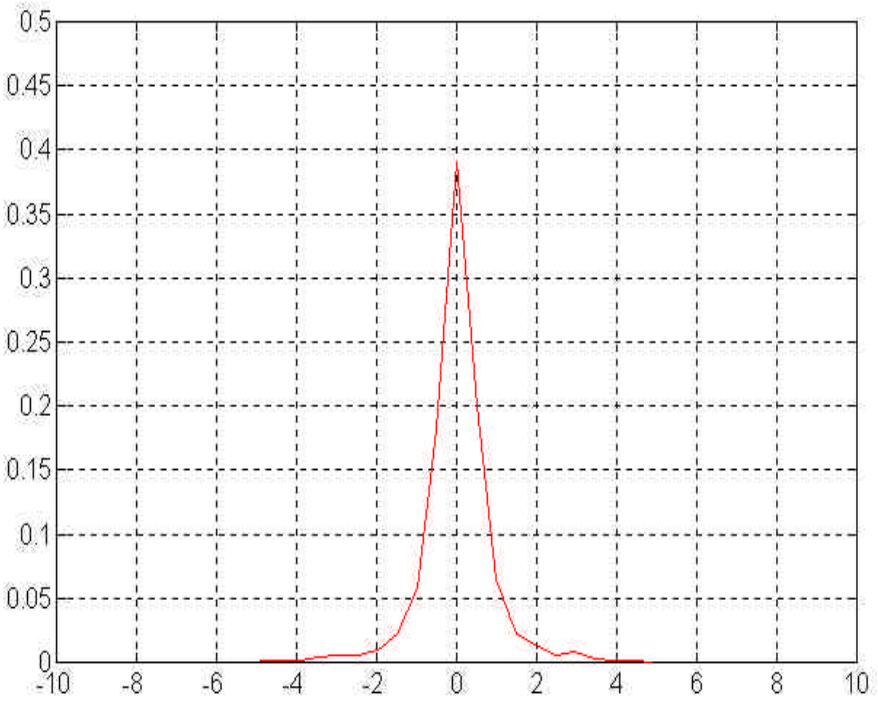
The channel variation rate (i.e., the variation of the arrival time of multipaths) mostly depends on the mobile speed and partially depends on the change of the surrounding environment. If we are focusing on the mobile speed, the channel variation rate is a function of the variation in the path distance. Even when we assume 100 km/h mobile speed, the mobile can move only 0.6 m for 20 msec. This amount of spatial change is negligible in arrival time because one chip corresponds to 78 m for 3.84 Mcps. Furthermore, even though the whole time variation of a multipath may exist within a few seconds, the arrival timing variation during a measurement interval (e.g., 80 msec) is much smaller. If USTS is catching up the variation in arriving time continuously, then the amount of timing variation for next synchronisation (tracking process in USTS) is considerably small. The update rate of 20 msec seems to be fast enough even in real systems because we randomly chose the mobiles to measure the timing variation and some of the mobiles may be high speed mobiles.



X axis: RTD_i ? $RTD_{i?1}$ (? 1/4 chip)

Y axis: Occurrence frequency

Figure 1. The variation of RTD when measured every 80 msec.



X axis: RTD_i ? $RTD_{i?1}$ (? 1/4 chip)

Y axis: Occurrence frequency

Figure 2. The variation of RTD when measured every 1000 msec.

3. Impact on the UL/DL timing

According to the current specifications, UL/DL relative timing is 1024 chips while not in SHO. But if the uplink timing is adjusted at initial synchronisation phase and during the tracking process with USTS, then the UL/DL relative timing is not maintained and varies. The range of UL/DL relative timing depends on the reference time T_{ref} . Moreover, when the UE is in SHO, the UL/DL timing is within 1024 ? 148 chips without USTS but this range may be affected with USTS. This section discusses on this issue.

3.1 Single radio link case

First, let us consider a single radio link case (i.e., when the UE is not in SHO). Since we are considering indoor and dense pedestrian environments for USTS, we assume the cell radius is 10 km (this value is sufficiently large for the above two environments considered for USTS. According to the current cell planning of SK Telecom in Seoul area, most of the cell radius is less than 2 km, even though it reaches more than 10 km in suburban or rural area). For a chip rate of 3.84 Mcps, the maximum propagation delay comes to 128 chips. So, if we set T_{ref} to be 128 chips, then the UL/DL timing becomes 1024 ? 128 chips. If the UE is near the cell site, UL/DL timing is close to 1024+128 chips. Or, it is close to 1024-128 chips. Since the UL/DL timing of 1024 chips was set by considering large cell size (i.e., 37.5 km), this amount of variation has a negligible impact on the CLPC processing both at UE and in the Node B.

3.2 Multiple radio link case (soft handover)

Now, let's proceed to the SHO case. Figure 3 shows the UE and Node B timing in case of three cells in Active set with/without USTS. The UE and any of the cell sites are the same distance apart, which corresponds to ? chips in time. ?=128 chips is assumed for 10 km cell radius, which is the maximum one-way propagation delay and also equals to T_{ref} . First, we focus on the case without USTS. As mentioned, the UL/DL timing is within T0 ? $?_{\max}$ (=1024 ? 148) chips without USTS. This is because the arriving times of DL DPCH at the UE from the cell sites in Active set may differ due to the granularity of $?_{DPCH,n}$. Therefore, the UL/DL timing is T0 chips for one of the cell sites but it may exist in the range of 1024 ? 148 chips for the others. The left and right thresholds (the maximum value of ? = $?_{\max}$ =148) come from the processing budgets in the Node B and the UE, respectively. This is well illustrated in the Figure 3, where the DL transmission time at the cell site C is assumed to be ? time earlier than that of the cell site B and the DL transmission time at the cell site A is ? time later for simplicity.

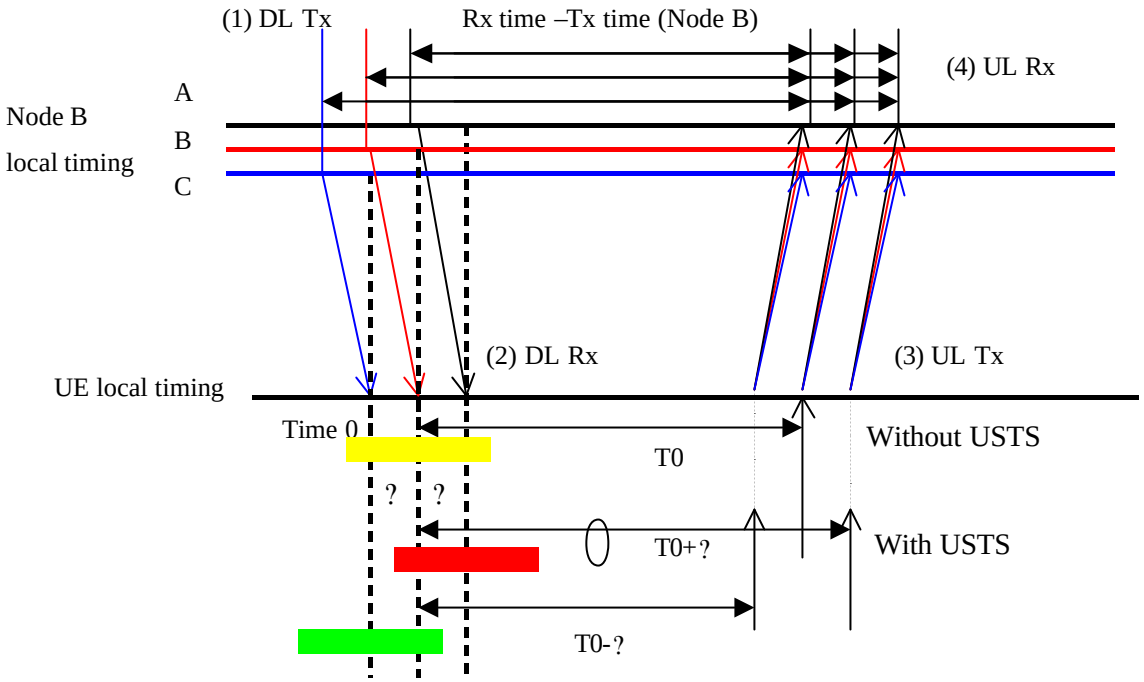


Figure 3. UE/Node B timings in case of three cells in Active set with/without USTS.

Even with USTS, the arrival times at the UE from cell sites A, B, and C are not affected at all. However, the UL/DL timing for the cell site B is not constant but now may vary within T0 ? ? chips. This variation may threaten the processing budget in either Node B or UE.

The time difference (3)-(2) corresponds to the power control processing time UE can spend, which needs to be larger than T0-$?_{max}$. The larger the difference (4)-(1), the shorter the processing time Node B can spend. According to the amount of timing adjustment ?, the range needs to be shifted. Or, even though the DL timing is within the range, the power control cannot be performed in one slot. For example, if the UL/DL relative time happens to become T0-? in the figure, then the UE power control processing time for cell A becomes shorter to be T0 - ? - ?. So it may now threaten the UE processing budget. In this case, the range needs to be shifted to the left (yellow range ✍ green range) and the DL timing of the cell A needs to be adjusted so that DL reception occurs within the shifted range. In other words, the center of the shifted range is kept at T0 times earlier from the UL DPCH transmission regardless of the amount of timing adjustment. This is the same as in the case without USTS but UL/DL relative timing is not fixed with USTS and therefore, the range is now varying as in the figure. Hence, as the amount of timing control varies faster in a wider range, the DL timing adjustment may occur more frequently. The trade-off between the performance degradation due to longer power control loop delay and the signalling load to adjust the DL timing needs to be taken into account.