TSG-RAN Working Group 1 meeting #18
Boston, USA
January 15-18, 2001

TSGR1#18(01)0038

Agenda item: Release 4

Source: Ericsson

Title: Comments on TR 25.840 Terminal Power Saving features

Document for: Discussion

Introduction

In this contribution we present some comments on the current version of TR 25.840 Terminal Power Saving features v2.0.0 [1].

Gated DPCCH transmission scheme in FDD – Terminology

A rather general comment is on the terminology used for the different states in Figure 1 and 2. In principle there is only uplink DPCCH gating, downlink DPCCH gating and no gating (normal transmission). This is similar to compressed mode, where uplink compressed mode and downlink compressed mode can be used as such or together. Introducing the terms "normal gated transmission" and "embedded gated transmission" seems to complicate the terminology and should preferably be avoided in the description of DPCCH gating. The state diagrams in Figure 1 and 2 could be simplified accordingly.
Also, it would be useful to decide upon a common term for gated transmission, instead of using either DPCCH gating, gated transmission or just gating.

Detection of DPDCH frame during gating

The UE is informed via downlink TFCI whether it needs to read the DSCH or not. For this purpose, TFCI is always transmitted in downlink frames that are defined by the DRX cycle. We assume that this is done to make sure that the UE can detect the TFCI word, as this is encoded over a frame period. However, in uplink the TFCI bits are just transmitted during the non-gated slots, i.e. no complete TFCI word can be received in the Node B and thus, no sensible TFCI detection is possible. Instead it is suggested to use pilot energy based detection in uplink, and to read the TFCI depending on energy comparisons. It is not obvious why TFCI has to be used differently in uplink and downlink. It is also not clear why the TFCI is transmitted during uplink DPCCH gating at all, if it anyway can't be detected.

Power control parameters

The power control parameters seem to be described in a similar way as done for compressed mode. However, the methods used for compressed mode are meant to overcome the impacts of short periods without TPC commands, i.e. one or two frames. These short periods occur relatively frequently. In difference to this, a far higher number of consecutive frames is affected by gating compared to compressed mode. It has not been shown that the proposed measures (different power control algorithms, recovery periods, step sizes, power offsets, etc.) result in significant performance improvements for gating. It is not mentioned in the technical report what kind of signalling would be needed to support all those features. Especially with respect to the work still to be done in other working groups, the technical report must be clearer on those details. It needs to be studied what different power control behaviours are really necessary also with respect to signalling, as it is a goal in itself to keep the parameters to a minimum.

Recovery period

As gating will be used for quite a high number of consecutive frames, it must be ensured that the power control works sufficiently well during this long period. If this is the case, we can't see any need to have any recovery period of a

couple of frames after a relatively long gating period. The full specification of a recovery period has quite some impact on the specifications (cf compressed mode).
The situation with gating is quite different from the compressed mode situation with respect to use of a recovery period. It has not been shown so far that such a period would be beneficial for DPCCH gating.

Power control step size

It is stated in the technical report that the power control step size can be different during gated transmission. It is not stated how the step size should be changed. It could be the same step size as in normal non-gated mode, it could be twice the step size of normal mode or it could be an arbitrary signalled step size. With respect to the work to be done in other WGs, it needs to be studied what is the most appropriate solution considering performance and signalling. It should be kept in mind that the number of parameters should be minimised.

Operation with other features

STTD

Four consecutive bits are STTD encoded and can possibly overlap a slot border. It is not obvious that there is no impact from gating, where DPCCH transmission changes from one slot to another.

Compressed mode

As gating can't be used during compressed mode (active TGPS), there are impacts on the practically achievable gains from DPCCH gating. This issue is discussed in [3].

SSDT

It is stated that gating shall be disabled when SSDT is initiated. It should be clarified in which way the disabling is done., e.g. whether additional signalling is to be used.

Impact to WGs

WG1

Only TS 25.214 is listed as the only affected specification. We believe that in the end modifications would be needed to most of the layer 1 specifications.
It is quite likely that some changes will be needed to the text 25.211. At least if CRC based outer loop power control [2] is introduced for gating, changes will be needed to the text TS 25.212. As done for compressed mode, some modifications will be needed for some of the measurements, i.e. TS 25.215 needs to be modified.

WG3

While the for WG2 the RRC specification is listed as being impacted by gating, it is quite likely that also WG3 specifications as NBAP would need to be modified to configure the NodeBs for gated transmission. This of course depends on the intended amount of signalling and parameters where the technical report is not very specific on yet.

WG4

Most likely, also changes to the RRM specification 25.133 will be necessary.

Performance

The impact of compressed mode on the achievable gains with DPCCH gating is discussed in [3].

UE battery life enhancements

To our understanding, the UE battery life enhancement figures given in the report are relatively implementation dependent.
Considering the TX gating figures, the gains through gating are depending on the absolute power consumption in the transmitter part in the UE and its relation to the absolute receiver part power consumption. Transmitting at higher powers and consuming more power in the UE transmitter at low RX power consumption will lead to high battery life enhancements for TX gating, while the improvements for RX gating are rather small. On the other hand, if a UE consumes

relatively high power in the receiver part and less power in the transmitter, the gains from RX gating will be higher and the TX gating gains will be lower.
The figures given in the tables should not be seen as the absolutely achievable gains, as the absolute power consumption in TX and RX will be different from one UE manufacturer to another. Thus, the achievable gains will differ for each UE manufacturer.

Reference and history sections

These comments are more of editorial nature.
It seems that in the gating TR overlapping references are used which correspond either to section 2 “References” or to section 8.1.3 “References”. This overlap should be resolved. In the history section, the comment “will be approved and placed under change control at TSG –RAN#10” should be removed.

Conclusion

To have a clear picture of the proposed solutions for DPCCH gating and also to progress the work in other WGs, clarification of the technical report is needed in the above areas.

References

[1] 3G TR 25.840 (v2.0.0), “Terminal power saving features”
[2] R1-01-0009, “Further clarifications on outer loop power control during DPCCH gating”, Nokia
[3] R1-01-0039, “Impact of compressed mode on the performance of DPCCH gating”, Ericsson