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Source:	**Panasonic**
Title:	**Proposal of bit mapping for type-III HARQ**
Agenda Item:	**AH24 (HSDPA)**
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1. Introduction

In this contribution we propose a bit-mapping scheme for type-III HARQ. Sender transmits systematic bits and parity bits on separated symbols. Receiver combines retransmitted packets' symbols before calculating the log-likelihood ratio.

This contribution shows that proposed scheme

- ? can achieve better performance than conventional type-III HARQ
- ? requires less size of receiver buffer than conventional type-III HARQ

2. Hybrid ARQ

HARQ has been proposed for HSDPA and there have been many analyses about the complexity and performance. Two types of Hybrid ARQ methods have been proposed for HSDPA. One scheme is Chase Combining(CC) and the other is Incremental Redundancy(IR). CC is simple HARQ and requires small receiver buffer. IR requires larger receiver buffer than CC but can achieve better performance than CC. Incremental Redundancy HARQ is called as type-II or type-III (when each packet is self-decodable).

? Chase Combining

This scheme is to send a number of repeats of coded data and decoders combine multiple coded packets before decoding. This scheme achieves gain with small buffer size in a receiver. The buffer size becomes the number of coded symbols of one coded packet.

? Incremental Redundancy

This scheme is to transmit additional redundant information in each retransmission and receiver decode on each retransmission. This incremental redundancy scheme is called type-II Hybrid ARQ. If each retransmission packet is self-decidable this scheme is called type-III Hybrid ARQ. IR requires larger size of buffer in a receiver than Chase Combining. The buffer size becomes the number of coded bits of total transmitted coded packets.

Simulation results on CC and IR have been shown and it has been reported that in some cases Incremental Redundancy can achieve better performance than Chase Combining. [1][2] Another contribution evaluated the complexity from the viewpoint of buffer size.

3. Sender and receiver structure

✍ Structure of sender

Fig. 1 shows the sender structure of the proposed type-III HARQ. Turbo encoder generates turbo-coded data. X is a set of systematic bits. Y and Z are sets of parity bits. Parity bits are punctured and the set of systematic bits is now called S and two sets of punctured parity bits are now called as Podd and Peven.

The turbo code rate changes from 1/3 into 1/2 with this puncturing. The puncturing pattern is shown below [figure 1]. A set of systematic bits and parity bits is selected according to the count of packet's transmission as detailed below [Fig. 2]. Then QAM modulation and spreading are employed. MCS should not be changed when proposed bit mapping method is used.
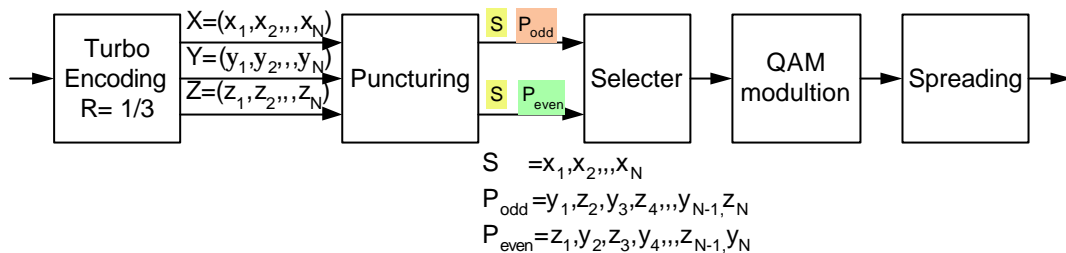

$$S = x_1, x_2, ,, x_N$$
$$P_{odd} = y_1, z_2, y_3, z_4, ,, y_{N-1}, z_N$$
$$P_{even} = z_1, y_2, z_3, y_4, ,, z_{N-1}, y_N$$

Fig. 1 Sender structure of proposed type-III HARQ

✍ Packet format

Fig. 2 shows the packet format of the proposed HARQ. Systematic bits set S is sent in each retransmission and Parity bits set Podd and Peven are sent alternately in each packet.

One symbol for systematic bits includes systematic bits only. One symbol for parity bits includes parity bits only. No symbol includes systematic bits and parity bits simultaneously. With this procedure systematic bits and parity bits are mapped on symbols separately.

If channel interleaver is used, channel interleaving should be performed with symbol unit or two channel interleavers should be used for systematic bits and parity bits respectively.
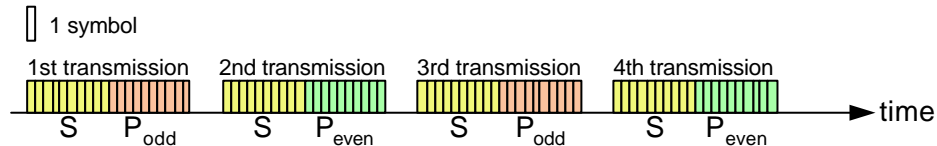
One symbol includes systematic bits only or parity bits only.
No symbol includes systematic bits and parity bits simultaneously.

Fig. 2 Packet format of proposed type-III HARQ

✍ Structure of receiver

Receiver combines every packet's systematic symbols before turbo decoding. Receiver also combines plural received Podd packet symbols and Peven packet symbols respectively before turbo decoding.

Log-likelihood ratio (LLR) of each bit is calculated after the symbol combination.

✍ Approximation in LLR calculation

Here we will explain why proposed method can achieve better performance than conventional scheme.

Conventional receiver can't combine retransmission symbols before calculates LLR of each bit, because each symbol may include systematic bit and parity bit simultaneously. But proposed receiver can combine retransmission symbols before calculates LLR.

When LLR is calculated, Max calculation is performed, which is one of approximation (please see[3]). Proposed scheme performs Max calculation only once after combination but Conventional scheme performs Max calculation twice before combination. So proposed scheme can reduce the error in LLR calculation than conventional scheme.
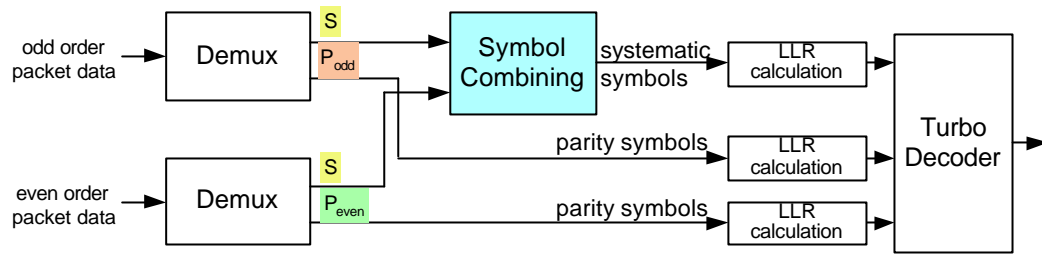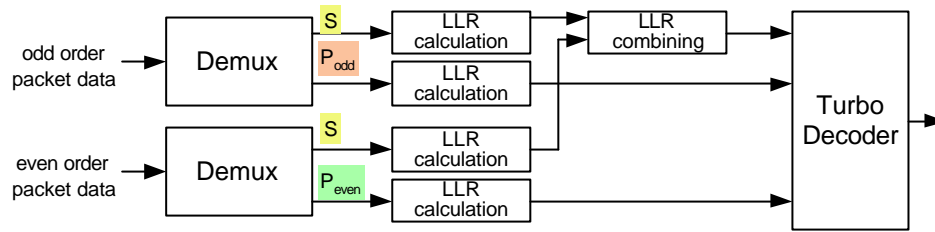
Fig. 3 Receiver structure of PROPOSED type-III HARQ

Fig. 4 Receiver structure of CONVENTIONAL type-III HARQ

4. Simulation Assumptions

The simulation assumptions are listed in Table. 1.

Table. 1

Parameter	Value	Comment
Chip-rate	3.84Mcps	
Spreading Factor	32	
Number of code for HS-DSCH	1	
TPC	Off	
CPICH Ec/Ior	-10dB(10% of Ior)	
DSCH Ec/Ior	-1dB (80% of Ior)	
Channel Model	AWGN	
Channel Estimation	Ideal	
HSDPA Frame Length	3.33ms(5 slots)	transmission unit interval.
Number of CRC bits	16	
Tail bits	6	in each transmission unit.
Max Number of Iterations for Turbo Decoding	8	
Metric for Turbo Code	Max	
HARQ structure	Dual Stop and Wait	
Number of maximum retransmission	10	
STTD	Off	
Code Rate	1/2	in each transmission unit. Generated from rate 1/3 Turbo Code.

MCSs used in the simulations are shown in Table. 2.
Two types of MCS are evaluated in this link level simulation.

Table. 2

MCS	Modulation	Code Rate	Information bits per packet	Coded bits per packet
2	16 QAM	1/2	800	1600
1	QPSK	1/2	400	800

5. Simulation results

 Fig. 5 and Fig. 6 show the frame error rate comparison. The proposed scheme can achieve better performance than conventional type-III HARQ. In each retransmission packet the proposed scheme can achieve about 0.5dB gain from conventional scheme.
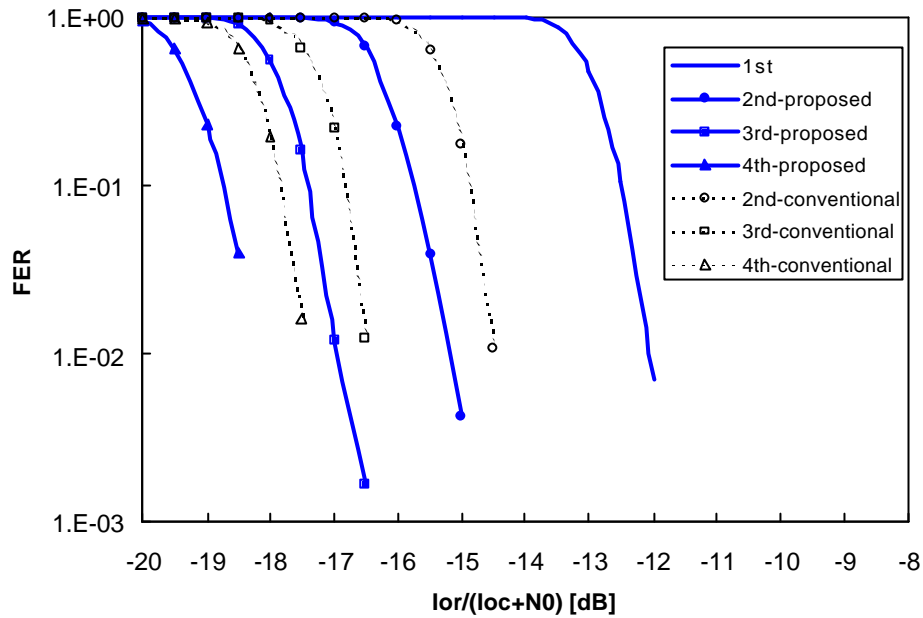

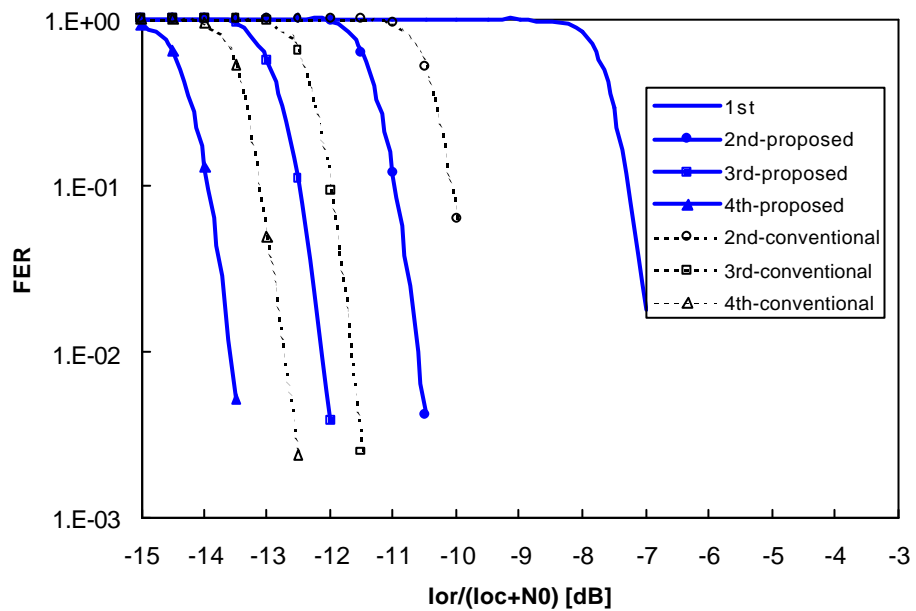**Fig. 5 Frame error rate QPSK R=1/2 AWGN channel (MCS 1)**

Fig. 6 Frame error rate 16QAM R=1/2 AWGN channel (MCS 2)

Fig. 7 and Fig. 8 show the throughput analysis. The proposed scheme can achieve better performance than the conventional scheme.
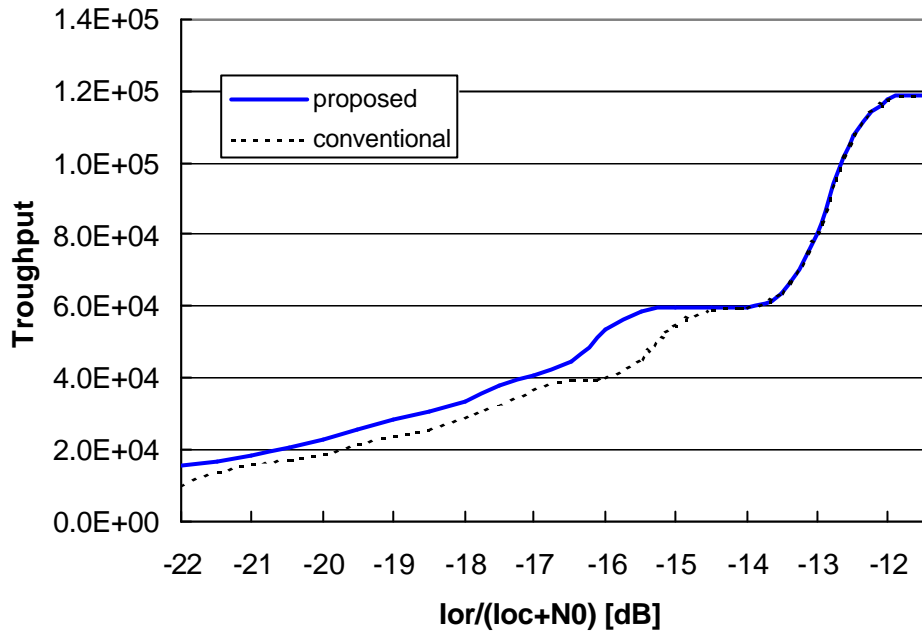

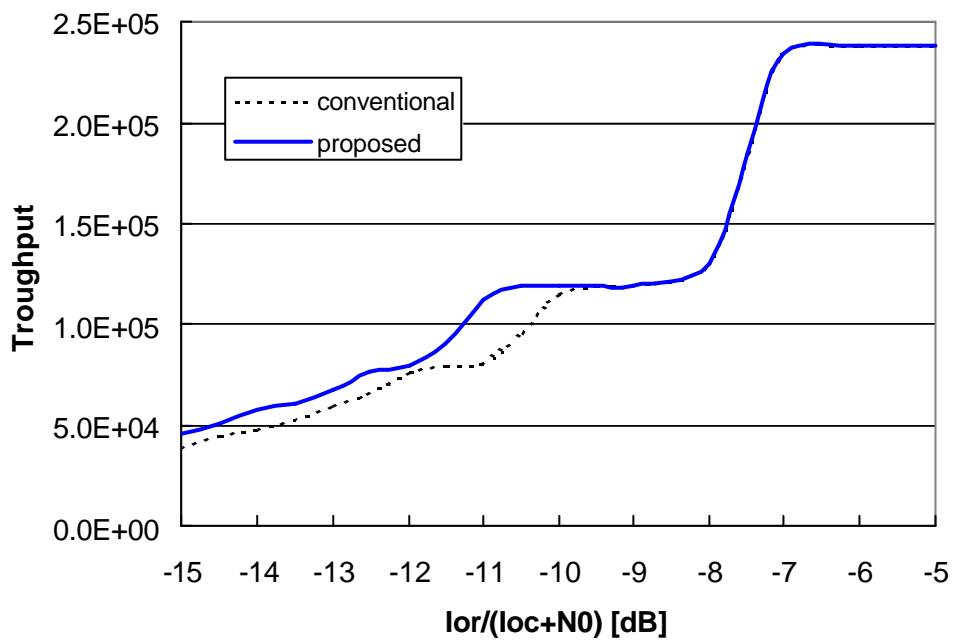**Fig. 7 Throughput QPSK R=1/2 AWGN channel (MCS 1)**

Fig. 8 Throughput 16QAM R=1/2 AWGN channel (MCS 2)

6. Receiver's buffer size consideration

The proposed scheme requires less size of receiver buffer than conventional scheme.
Proposed and conventional scheme's receiver buffer size is as follows.

$$Buffer_{conventional} ? \, {}^{'}\!(N_{systematic} ? N_{parity} {}^{'}\!) ? N_{type} \tag{1}$$

$$Buffer_{proposed} ? \, N_{systematic} ? N_{parity} ? N_{type} \tag{2}$$

$Buffer_{conventional}$ buffer size of conventional HARQ

$Buffer_{proposed}$ buffer size of proposed HARQ

$N_{systematic}$ number of systematic symbols in one HS-DSCH packet

N_{parity} number of parity symbols in one HS-DSCH packet

N_{type} number of different type of packet in HARQ retransmission

Conventional receiver has to store each retransmission packet, the buffer size is the number shown in equation (1), while proposed scheme has to prepare only the size of one packet regarding systematic symbols. So proposed scheme can reduce receiver's buffer.

Table. 3 Buffer size comparison

Code rate in each retransmission unit	$N_{systematic}$	N_{parity}	N_{type}	$Buffer_{conventional}$	$Buffer_{proposed}$	reduction to conventional method
1/2	200	200	2	800symbols	600symbols	33.3%
3/4	300	100	6	2400symbols	900symbols	62.5%

7. Conclusion

We proposed a bit-mapping scheme for type-III HARQ.
 The characteristic of this scheme is that sender transmits systematic bits and parity bits on separated symbols. Receiver combines retransmitted packets' symbols before calculating the log-likelihood ratio.
This contribution showed that proposed scheme

  ✍ can achieve better performance than conventional type-III HARQ

  ✍ requires less size of receiver buffer than conventional type-III HARQ

References

[1] R1-00-1428,Ericsson "Performance Comparison of Chase Combining and Incremental Redundancy for HSDPA" Stockholm, Sweden, November 21-24, 2000.
[2] R1-00-1396,Motorla "Performance Comparison of Hybrid-ARQ Schemes" Stockholm, Sweden, November 21-24, 2000.
[3] R1-00-1093, Ericsson, Motorola and Nokia "Link Evaluation Methods for High Speed Downlink Packet Access (HSDPA)" Berlin, Germany, August 21-24, 2000.