**3GPP TSG RAN WG1** ***TSGR1#15(00)1082***
**Berlin, Germany, 22nd – 25th August, 2000**

**Agenda item:** **R99**

**Source:** **Panasonic**

**Title:** **Clarification of FBI field**

**Document for:** **Decision**

## Introduction

Current spec does not specify FBI field if N_FBI is larger than sum of S field and D field. In other words, if there remains the FBI field not used both SSDT and closed loop Tx-div, filling bits is not specified.

In addition, the position of filling bits is not specified.

The attached CR for 25.211 aims to clarify this uncertainness in Release 99.

## Background

The total FBI field size changes from 0 to 2 bit. The S field for SSDT consists of 0,1 or 2bits. The D field for Tx-div consists of 0 or 1 bit.

From our understanding, current specification does not require FBI field is filled with S bit or D bit because of the flexible usage of SSDT setting and Tx-div setting. This means the possibility of remaining bits.

## About bit pattern

We don't have a special opinion for filling bit pattern. For simplicity, we propose with "1".

In RAN1 reflector, it was suggested for filled with TPC. At least we cannot agree 7th and 8th bits with TPC. Because filling 7th and 8th bits with TPC changes power control timing relation between uplink and downlink. Concerning 9th bit, we would like to hear other member's opinion. At this document, we propose filling with "1" for simplicity.

## About filling bit position

When NFBI is 2bits, S field is 0bit and D field is 1bit, there is a choice of position of filling bit.

a) Total FBI field: 2bit, S field: 1bit, D field: 1bit, Filling bit: 0bit. There is no difference between two methods.

Method A "S" "D"

Method B "S" "D"

b) Total FBI field: 2bit, S field: 1bit, D field: 0bit, Filling bit: 1bit. There is no difference between two methods.

Method A "S" "F"

Method B "S" "F"

c) Total FBI field: 2bit, S field: 0bit, D field: 1bit, Filling bit: 1bit. The position of D bit is different.

Method A "D" "F"

Method B "F" "D"

Not depending on the usage of SSDT, method B can keep the position of D field. So we propose method B.

Above discussion is based with filling "1"(i.e. fixed pattern). If we choose filling 9th bit as TPC, we should select method B and the position of D field moves according the usage of SSDT.

## Conclusion

According above discussion, we propose following CR for 25.211.

**3GPP TSG RAN WG1 Meeting #15**
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***Document R1-00-1082***
*e.g. for 3GPP use the format TP-99xxx*
*or for SMG, use the format P-99-xxx*

# CHANGE REQUEST

*Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.*

| 25.211 | CR | 077 | Current Version: | 3.3.0 |
|---|---|---|---|---|

*GSM (AA.BB) or 3G (AA.BBB) specification number ↑* *↑ CR number as allocated by MCC support team*

| For submission to: | RAN #9 | for approval | X | strategic | | (for SMG use only) |
|---|---|---|---|---|---|---|
| *list expected approval meeting # here ↑* | | for information | | non-strategic | | |

*Form: CR cover sheet, version 2 for 3GPP and SMG* *The latest version of this form is available from:* ftp://ftp.3gpp.org/Information/CR-Form-v2.doc

**Proposed change affects:** *(at least one should be marked with an X)* (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]

**Source:** Panasonic **Date:** 2000-08-18

**Subject:** Clarification of FBI field

**Work item:**

**Category:** *(only one category shall be marked with an X)*

| | | | | | |
|---|---|---|---|---|---|
| F | Correction | X | **Release:** | Phase 2 | |
| A | Corresponds to a correction in an earlier release | | | Release 96 | |
| B | Addition of feature | | | Release 97 | |
| C | Functional modification of feature | | | Release 98 | |
| D | Editorial modification | | | Release 99 | X |
| | | | | Release 00 | |

**Reason for change:** Current specification does not specify the FBI field if not used Sfield or Dfield. It should be clarified.

**Clauses affected:** 5.2.1

**Other specs affected:**

| | | |
|---|---|---|
| Other 3G core specifications | | → List of CRs: |
| Other GSM core specifications | | → List of CRs: |
| MS test specifications | | → List of CRs: |
| BSS test specifications | | → List of CRs: |
| O&M specifications | | → List of CRs: |

**Other comments:**

help.doc

<--------- double-click here for help and instructions on how to create a CR.

# 5.2 Uplink physical channels

## 5.2.1 Dedicated uplink physical channels

There are two types of uplink dedicated physical channels, the uplink Dedicated Physical Data Channel (uplink DPDCH) and the uplink Dedicated Physical Control Channel (uplink DPCCH).

The DPDCH and the DPCCH are I/Q code multiplexed within each radio frame (see [4]).

The uplink DPDCH is used to carry the DCH transport channel. There may be zero, one, or several uplink DPDCHs on each radio link.

The uplink DPCCH is used to carry control information generated at Layer 1. The Layer 1 control information consists of known pilot bits to support channel estimation for coherent detection, transmit power-control (TPC) commands, feedback information (FBI), and an optional transport-format combination indicator (TFCI). The transport-format combination indicator informs the receiver about the instantaneous transport format combination of the transport channels mapped to the simultaneously transmitted uplink DPDCH radio frame. There is one and only one uplink DPCCH on each radio link.

Figure 1 shows the frame structure of the uplink dedicated physical channels. Each radio frame of length 10 ms is split into 15 slots, each of length $T_{slot}$ = 2560 chips, corresponding to one power-control period.

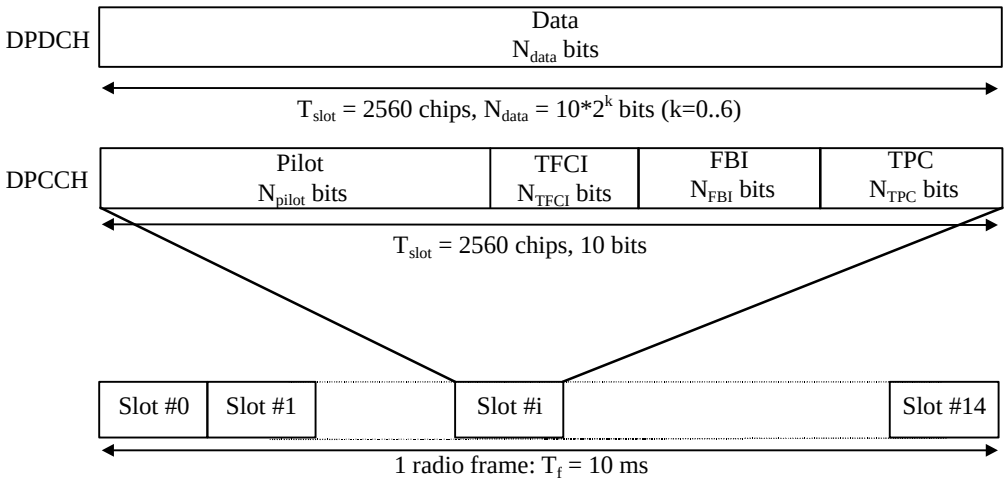


**Figure 1: Frame structure for uplink DPDCH/DPCCH**

The parameter k in figure 1 determines the number of bits per uplink DPDCH slot. It is related to the spreading factor SF of the DPDCH as SF = $256/2^k$. The DPDCH spreading factor may range from 256 down to 4. The spreading factor of the uplink DPCCH is always equal to 256, i.e. there are 10 bits per uplink DPCCH slot.

The exact number of bits of the uplink DPDCH and the different uplink DPCCH fields ($N_{pilot}$, $N_{TFCI}$, $N_{FBI}$, and $N_{TPC}$) is given by table 1 and table 2. What slot format to use is configured by higher layers and can also be reconfigured by higher layers.

The channel bit and symbol rates given in table 1 and table 2 are the rates immediately before spreading. The pilot patterns are given in table 3 and table 4, the TPC bit pattern is given in table 5.

The FBI bits are used to support techniques requiring feedback from the UE to the UTRAN Access Point, including closed loop mode transmit diversity and site selection diversity transmission (SSDT). The structure of the FBI field is shown in figure 2 and described below.

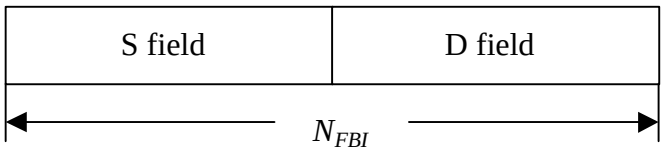


**Figure 2: Details of FBI field**

The S field is used for SSDT signalling, while the D field is used for closed loop mode transmit diversity signalling. The S field consists of 0, 1 or 2 bits. The D field consists of 0 or 1 bit. The total FBI field size $N_{FBI}$ is given by table 2. If total FBI field is not filled with S field or D field, FBI field is filled with "1". When $N_{FBI}$ is 2bits, S field is 0bit and D field is 1bit, the earliest position bit is filled with "1". Simultaneous use of SSDT power control and closed loop mode transmit diversity requires that the S field consists of 1 bit. The use of the FBI fields is described in detail in [5].

**Table 1: DPDCH fields**

| Slot Format #i | Channel Bit Rate (kbps) | Channel Symbol Rate (ksps) | SF | Bits/ Frame | Bits/ Slot | $N_{data}$ |
|---|---|---|---|---|---|---|
| 0 | 15 | 15 | 256 | 150 | 10 | 10 |
| 1 | 30 | 30 | 128 | 300 | 20 | 20 |
| 2 | 60 | 60 | 64 | 600 | 40 | 40 |
| 3 | 120 | 120 | 32 | 1200 | 80 | 80 |
| 4 | 240 | 240 | 16 | 2400 | 160 | 160 |
| 5 | 480 | 480 | 8 | 4800 | 320 | 320 |
| 6 | 960 | 960 | 4 | 9600 | 640 | 640 |

There are two types of uplink dedicated physical channels; those that include TFCI (e.g. for several simultaneous services) and those that do not include TFCI (e.g. for fixed-rate services). These types are reflected by the duplicated rows of table 2. It is the UTRAN that determines if a TFCI should be transmitted and it is mandatory for all UEs to support the use of TFCI in the uplink. The mapping of TFCI bits onto slots is described in [3].

In compressed mode, DPCCH slot formats with TFCI fields are changed. There are two possible compressed slot formats for each normal slot format. They are labelled A and B and the selection between them is dependent on the number of slots that are transmitted in each frame in compressed mode.

**Table 2: DPCCH fields**

| Slot Format #i | Channel Bit Rate (kbps) | Channel Symbol Rate (ksps) | SF | Bits/ Frame | Bits/ Slot | $N_{pilot}$ | $N_{TPC}$ | $N_{TFCI}$ | $N_{FBI}$ | Transmitted slots per radio frame |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 15 | 15 | 256 | 150 | 10 | 6 | 2 | 2 | 0 | 15 |
| 0A | 15 | 15 | 256 | 150 | 10 | 5 | 2 | 3 | 0 | 10-14 |
| 0B | 15 | 15 | 256 | 150 | 10 | 4 | 2 | 4 | 0 | 8-9 |
| 1 | 15 | 15 | 256 | 150 | 10 | 8 | 2 | 0 | 0 | 8-15 |
| 2 | 15 | 15 | 256 | 150 | 10 | 5 | 2 | 2 | 1 | 15 |
| 2A | 15 | 15 | 256 | 150 | 10 | 4 | 2 | 3 | 1 | 10-14 |
| 2B | 15 | 15 | 256 | 150 | 10 | 3 | 2 | 4 | 1 | 8-9 |
| 3 | 15 | 15 | 256 | 150 | 10 | 7 | 2 | 0 | 1 | 8-15 |
| 4 | 15 | 15 | 256 | 150 | 10 | 6 | 2 | 0 | 2 | 8-15 |
| 5 | 15 | 15 | 256 | 150 | 10 | 5 | 1 | 2 | 2 | 15 |
| 5A | 15 | 15 | 256 | 150 | 10 | 4 | 1 | 3 | 2 | 10-14 |
| 5B | 15 | 15 | 256 | 150 | 10 | 3 | 1 | 4 | 2 | 8-9 |

The pilot bit patterns are described in table 3 and table 4. The shadowed column part of pilot bit pattern is defined as FSW and FSWs can be used to confirm frame synchronization. (The value of the pilot bit pattern other than FSWs shall be "1".)

**Table 3: Pilot bit patterns for uplink DPCCH with $N_{pilot}$ = 3, 4, 5 and 6**

| | $N_{pilot}$ = 3 | | | $N_{pilot}$ = 4 | | | | $N_{pilot}$ = 5 | | | | | $N_{pilot}$ = 6 | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit # | 0 | 1 | 2 | 0 | 1 | 2 | 3 | 0 | 1 | 2 | 3 | 4 | 0 | 1 | 2 | 3 | 4 | 5 |
| Slot #0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 2 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 3 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 4 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 5 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 6 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 7 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 8 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 9 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 10 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 11 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 12 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 13 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 14 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |

**Table 4: Pilot bit patterns for uplink DPCCH with $N_{pilot}$ = 7 and 8**

| | $N_{pilot}$ = 7 | | | | | | | $N_{pilot}$ = 8 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit # | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Slot #0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 2 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 3 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 4 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 5 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 6 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 7 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 8 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 9 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 10 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 11 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 12 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 13 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 14 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

The relationship between the TPC bit pattern and transmitter power control command is presented in table 5.

**Table 5: TPC Bit Pattern**

| TPC Bit Pattern | | Transmitter power control command |
|---|---|---|
| $N_{TPC}$ = 1 | $N_{TPC}$ = 2 | |
| 1 | 11 | 1 |
| 0 | 00 | 0 |

Multi-code operation is possible for the uplink dedicated physical channels. When multi-code transmission is used, several parallel DPDCH are transmitted using different channelization codes, see [4]. However, there is only one DPCCH per radio link.

A power control preamble may be used for initialisation of a DCH. Both the UL and DL DPCCHs shall be transmitted during the power control preamble. The length of the power control preamble is a UE-specific higher layer parameter, $N_{pcp}$ (see [5], section 5.1.2.4), signalled by the network. The UL DPCCH shall take the same slot format in the power control preamble as afterwards, as given in table 2. When, $N_{pcp} > 0$ the pilot patterns from slot #(15- $N_{pcp}$) to slot #14 of table 3 and table 4 shall be used. The timing of the power control preamble is shown in Figure 33 in subclause 7.7. The TFCI field is filled with "1" bits.