TSG-RAN WG1, Meeting #15 R1-00-1100
Berlin, Germany, 22-25 August, 2000

Agenda item:

Source: QUALCOMM Europe

Title: UE Timing related issues

Document for: Discussion & Action

Introduction

This contribution is an attempt to consolidate the information on UE timing related issues found in various RAN specifications and highlight a number of potential undefined areas and inconsistencies. It is for discussion and decision on necessary actions (CR on R1 specifications or LS to other groups) to clarify and/or complete the specification in this area. Although it covers specifications which are under the responsibility of other groups, we submit this contribution to R1 as the leading group on UE timing related issues.

Our discussion on UE timing is based on the following principles :

- The procedures and measurement related to the UE timing have to be applicable and perform flawlessly in both asynchronous and synchronous networks (where synchronous network means a network in which base stations timing is based on a common time reference).
- The UE timing has to be based on the received downlink signal in order to avoid very stringent clock requirement in the terminal or time drifts when using typical oscillators.
- Reference points in time may have different meanings or implications depending on the context. For example the term “first significant path” has a different meaning is the demodulation and LCS context.

“First Significant” path

The terminology “first significant path” is used throughout RAN specifications and in particular in TS 25.211, TS 25.215 and TS 25.331. The meaning of “First Significant” may be ambiguous as it is not clear whether the classification is in the time domain, the power domain or some other dimension. This issue is also described in [1]. Since the reason for considering “First Significant” paths is related to timing aspects (Tx-Rx timing relation) it should be clarified that “First” is to be interpreted in the time domain, i.e. it means “earliest”. ***This requires a change in TS 25.211 and TS 25.215 as proposed in [1] as well as liaison to other RAN working groups to ensure consistency across RAN specification.***

The above clarification is not sufficient as “Earliest Significant” is very vague and subject to interpretation. Although the exact definition of “earliest significant” path is a sensitive implementation related issue and should not be specified in the text, we believe that the UE should be allowed to use different criteria (i.e. thresholds) depending on the context. In particular the UE should be allowed to identify different “first significant” paths whether operating in the SHO receiver context or in the LCS context. This applies in particular to the “Rx-Tx delay” measurement defined in TS 25.215.

TS 25.215 defines the "Rx-Tx delay" measurement as the time difference between UL transmission time instant and the corresponding time instant in the "first significant" DL path of a given cell in the active set. The "Rx-Tx delay" measurements are used for at least two different purposes. The first use is related to the addition of new cells to the active set and allows the network to determine the time offset to be applied to the DL transmission of that new cell. In that context the "first significant" path is likely (implementation choice) the first path which could/would be used for demodulation. The second use of the measurement relates to the LCS context, in particular to the RTT (Round Trip Time) determination. In that context, the "first significant" path should be the earliest path that the UE can detect with a certain confidence level (implementation dependent). Although it may happen that the earliest detectable path could also be used for demodulation, this is not always the case and we believe that the ***system should be able to differentiate the "Rx-Tx delay" measurement for those two contexts as is done for the other time related measurements (i.e. SFN-SFN Type 1 and SFN-SFN Type 2 measurements defined in TS 25.133, section 8.1.10). This would require a change to TS 25.215 and TS 25.133 which is under the responsibility of WG4***. We therefore suggest to send a liaison to R4 and R2 on this issue requesting differentiation of the "Rx-Tx delay" measurement based on the context (LCS or preparation of cell addition).

We also noted that there is currently an inconsistency between 25.133 and 25.331 regarding the resolution of the "Rx-Tx time difference" measurement. 25.133 section 8.1.11 calls for a 0.25 chip resolution while 25.331 only supports 1 chip resolution.

"Valid" Rx timing range

TS 25.214, section 4.3.4

During a connection the UE may adjust its DPDCH/DPCCH transmission time instant.

If the receive timing for any downlink DPCCH/DPDCH in the current active set has drifted, so the time between reception of the downlink DPCCH/DPDCH in question and transmission of uplink DPCCH/DPDCH lies outside the valid range, L1 shall inform higher layers of this, so that the network can be informed of this and downlink timing can be adjusted by the network.

NOTE: The maximum rate of uplink TX time adjustment, and the valid range for the time between downlink DPCCH/DPDCH reception and uplink DPCCH/DPDCH transmission in the UE is to be specified by RAN WG4.

TS 25.214 describes the UE behavior when the timing of a cell in the active set drifts outside the valid range. In essence the UE shall report this event to the network and the network is expected to adjust the timing of that cell so that the cell appears again in the valid range. The valid range is said to be defined in R4. We could not find any definition of a "valid range" in R4 specification. However, TS 25.331 (R2 RRC) defines a procedure where the network can request the UE to report events such as "Rx-Tx" threshold crossing. Although it looks as if a reference correction in 25.214 would solve the issue, there are a few more issues to be considered.

TS 25.331
14.5.2.6, Reporting event 6F: The UE Rx-Tx time difference for a RL included in the active set becomes larger than an absolute threshold

When this event is ordered by UTRAN in a MEASUREMENT CONTROL message, the UE shall send a MEASUREMENT REPORT message when the UE Rx-Tx time difference becomes larger than the threshold defined by the IE "UE Rx-Tx time difference threshold".

14.5.2.7, Reporting event 6G: The UE Rx-Tx time difference for a RL included in the active set becomes less than an absolute threshold

When this event is ordered by UTRAN in a MEASUREMENT CONTROL message, the UE shall send a MEASUREMENT REPORT when the UE Rx-Tx time difference becomes less than the threshold defined by the IE "UE Rx-Tx time difference threshold"

Information Element/Group name	Need	Multi	Type and reference	Semantics description
>UE Rx-Tx time difference threshold	CV - clause 2		Integer(769..1280)	Time difference in chip. In event 6f, 6g.

TS 25.331 section 10.3.7.105 (see above table) also defines the actual range for reporting threshold values. The threshold for reporting the event could be as high as 256 chips away (plus or minus) from the UE DL reference timing (i.e. Tx_timing – T0). Assuming DL timing adjustment procedure in the network may lead to an additional 20 chip drift [2] until the DL timing is adjusted and assuming a worst case delay spread of 128 chips (higher spreads are possible although not likely) this would leave less than 108 chips for PC command derivation and modulation (DL) or PC command demodulation and Tx power adjust (UL) in order to meet the 1 slot power control loop delay target. In addition this would require the deskew buffer size to be at least 512+128+40 chip long. We believe this puts some unnecessary burden on the UE design while the benefit of allowing such a large "valid" range is not obvious. We nevertheless agree that the network should be allowed to include some hysteresis in the threshold in order to avoid some ping-pong effects in the timing of DL cells. ***Assuming R1 agrees with the above we suggest that R1 sends a liaison to R2 on this issue, suggesting that the range for UE Rx-Tx time difference threshold be reduced.***

TS 25.133
8.1.11.2UE Rx-Tx time difference measurement report mapping
The reporting range is for UE Rx-Tx time difference is from 876 ... 1170 chip.

TS 25.133 defines the valid measurement range. As explained above it possible that the actual "Rx-Tx" range is wider than 1024+/-128 chips. The current text in R4 allows to report delays within 148 chips of the DL reference timing (i.e. 20 chip margin) which corresponds to the potential extra drift which may happen during the timing adjustment procedure. As discussed above the actual "Rx-Tx" value may be higher depending on how the network sets the reporting threshold and on how long it takes to adjust the DL timing of a cell. Since "Rx-Tx" is a critical measurement from LCS and DL timing selection point of view we believe that the measurement range should cover all possible valid scenarios including transient situations. ***Depending on whether and how the reporting threshold range is modified in 25.331 the "Rx-Tx" measurement range in TS 25.331 should be extended to reflect all possible valid "Rx-Tx" values. This would require a LS to R4.***

Finally it is possible due to a number of reasons (network configuration, UE configuration, UE limitations) that the UE can not process the power control information related to a cell (DL power control command decision & modulation and UL power control command demodulation and Tx power adjustment) to meet the 1 slot power control delay target. It is currently not specified how the UE should behave in such a case. The two obvious options are to ignore that cell or to use the information from the previous slot on that cell (i.e. 2 slot power control delay on that cell). Note that independent of the power control delay issue the UE may be able to use that cell for demodulation as the delay requirement is not as tight. ***Although we don't have a particular preference on that issue, we believe that the UE behavior should be clarified.***

DL timing selection for cell addition

TS 25.214 specifies that the network shall select the DL timing of a RL (when adding a cell to the active set or adjusting the timing of a cell in the active set) such that the UE receives the RL within (i.e. plus or minus) 148 chips of its DL time reference (UL_Tx – T0). Assuming the network has up to date information on the timing at the UE, it is not clear why the network should not ensure that the

timing of the new cell is within 128 chips of the UE DL time reference and therefore minimize the Rx time range in the UE (which itself maximizes the chance to maintain a 1 slot delay in the power control loop).

25.214, section 4.3.2.3

"b) UTRAN starts the transmission of the downlink DPCCH/DPDCH at a frame timing such that the frame timing received at the UE will be within T0 ± 148 chips prior to the frame timing of the uplink DPCCH/DPDCH at the UE. …"

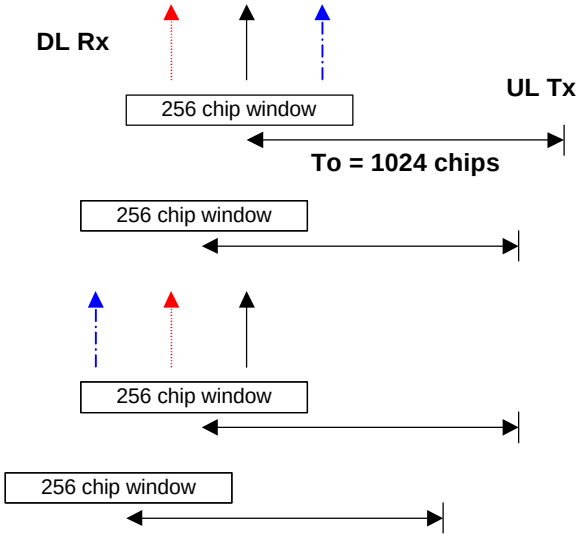
History [2] reveals that the 20 chip margin should actually not be used by the network in its time offset calculation but should be assumed in the UE receiver design in order to account for the potential additional drift between the time when the UE reports a cell being out of the "valid range" and the time the network adjusts the timing of that cell.

As discussed earlier, the UE design should account for an hysteresis in the "out of range" event reporting as well as for the additional drift which could happen while the network adjusts the DL timing of the "faulty" cell or computes the DL timing of a new cell. However, we believe that based on the information available (i.e. the measurements reports) ***the network should derive the DL RL timing so that it is received within 128 chips (and not 148 chips) of the UE DL reference timing. This requires a change to TS 25.214.***

We suggest to clarify the text to ensure that the network computes the DL timing of RL (either the initial timing or adjusted timing) such that based on the information available to the network the UE would receive the link within 128 chips of its DL time reference. Due the delays involved with the procedure and hysteresis to avoid ping pong effects the UE shall be able to accommodate an additional drift of up to [Td_adjust_delay + hysteresis] chips, that is the UE shall be able to process a RL arriving within 148+hysteresis chips of its DL time reference. We need to decide whether the 20 chip margin (derived based on Td_adjust_delay considerations) includes provision for the hysteresis or whether the UE shall be able to accommodate additional drift.

UE timing adjustment (slewing)

TS 25.133 defines a performance requirement which ensures that the UE adjusts its timing as the timing of the earliest cell drifts, the earliest received cell disappears or a new cell appears. The current text requires the UE to adjust its UL Tx timing so that it happens exactly (within 1.5 chip tolerance) 1024 chips after the earliest received DL path amongst cells in the active set. Although it seems to be the right thing to do (center of the "valid" range) this may lead to some problem in the asynchronous scenario.



Let's consider an active set with three cells each with a DL timing such that they are received 85 chips apart at the UE (see figure). Based on the requirement in TS 25.133, the UE would start adjusting its timing so that its transmit timing would happen 1024 chips after it receives cell 1. Assuming the "valid" windows is 256 chip wide, at some point cell 3 will go out of the "valid" window and the UE will report the event to the network which in turn will adjust cell 3 timing so that it appears in the "valid" windows again. The UE will then start to adjust its timing so that the transmit timing would be 1024 chips after it receives cell 3. Then cell 2 will go out of the window and so on and so forth. The UE would consequently continuously slew its timing. Although this is not a critical issue from signaling point of view (maximum slewing rate is ¼ chip per 200 ms which would result in one event every minute) it may still be preferable if this scenario is avoided. ***This can be achieved it the UE transmit timing happens 1024+128 chips after the first significant path is received. This would require a change to TS 25.133 and TS 25.211.***

References

[1] R1-00-1049, Ericsson

[2] R1-99-c89, R3 liaison statement

3GPP TS 25.211 v3.3.0

3GPP TS 25.133 v3.2.0

3GPP TS 25.331 v3.3.0