3GPP TSG RAN WG1#12

Seoul, Korea April 10th - 14th, 2000

Agenda Item:

Source: Nokia

Title: 25.215-049r1, 25.211-048 : Propagation delay for PCPCH (revision1)

Document for: Decision

1 Introduction

In its last meeting, RAN WG3 included Propagation delay measurement also for PCPCH. Since RAN WG3 uses the same data frame structure for RACH /CPCH, it is proposed that in TS25.215, there is also only one measurement defined for PRACH and PCPCH. The idea to define the propagation delay measurement for PCPCH, is that PCPCH can also be used for DPCH setup. The propagation delay measurement allows to minimise the search window , when setting up the uplink DPCH. The attached CR contains the proposed definition of Propagation delay measurement for PCPCH.

2 PCPCH propagation delay definition

Proposed definition to TS 25.215 is given below. It is aligned with the PRACH propagation delay definition as much as possible. However, the measurement definition for PCPCH is now defined so generically, that several measurements are possible, since each Iub frame contains the field for Propagation delay.

PCPCH:

Propagation delay = $(T_{RX} - T_{TX} - (L_{pc\text{-preamble}} + 1)*2560 - (k-1)*38400)/2$, where

 T_{TX} = The transmission time of CD-ICH at access slot (n-2- T_{cpch}), where $0 \le (n-2-T_{cpch}) \le 14$ and T_{cpch} can have values 0 or 1.

 T_{RX} = The time of reception of the first chip (the first significant path) of the kth frame of the PCPCH message from the UE, where k \in {1,..., N_Max_frames}.

 N_{max} frames is a higher layer parameter and defines the maximum length of the PCPCH message. The PCPCH message begins at uplink access slot (n+L_{pc-preamble}/2),

where $0 \le (n + L_{pc\text{-preamble}}/2) \le 14$ and where $L_{pc\text{-preamble}}$ can have values 0 or 8.

Note: The definition of "first significant path" needs further elaboration.

3 Changes needed in other specs

This means that TS25.211 has to contain following sentence in section "7.4 PCPCH/AICH timing relation", in the similar way that section "7.3 PRACH/AICH timing relation" now defines the timing relationship of the uplink access slot number n and downlink access slot n. Otherwise the PCPCH propagation delay definition is not clear. The CR for that is attached here also.

Uplink access slot number n is transmitted from the UE τ_{p-a1} chips prior to the reception of downlink access slot number n, n =0, 1, ...,14.

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Source:	Nokia			Date:	2000-04-12			
Subject:	Propagation delay for PC	PCH						
Work item:	UTRAN							
Category: F A (only one category shall be marked with an X)	Correction Corresponds to a correct Addition of feature Functional modification of Editorial modification			Release:	Phase 2 Release 96 Release 97 Release 98 Release 99 Release 00	X		
Reason for change:	RAN WG3 has included I needed modifications are				CPCH. The			
Clauses affecte	5.2.10 Propagation of	delay						
Other specs affected:	Other 3G core specification Other GSM core specifications MS test specifications BSS test specifications O&M specifications	$\begin{array}{c} \rightarrow \\ \rightarrow \\ \rightarrow \\ \rightarrow \end{array}$	List of CRs: List of CRs: List of CRs: List of CRs: List of CRs:					
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5.2.10 PRACH/PCPCH Propagation delay

B 0 10						
Definition	Propagation delay is defined as one-way propagation delay as measured during either PRA					
	or PCPCH access:					
	PRACH:					
	Propagation delay = $(T_{RX} - T_{TX} - 2560)/2$, where					
	T _{TX} = The <u>transmission</u> time of AICH access slot (n-2-AICH transmission timing), where 0≤(n-2-					
	AICH Transmission Timing)≤14 and AICH_Transmission_Timing can have values 0 or 1.					
	T _{RX} = The time of reception of the beginning (the first significant path) of the PRACH message					
	from the UE at PRACH access slot n.					
	Note: The definition of "first significant path" needs further elaboration.					
	rede. The definition of first significant pair freeds futurel elaboration.					
	PCPCH:					
	FUFUR.					
	Dropogation delay (T. T. (I. 14)*2560 (k 4)*29400)/2 pubara					
	Propagation delay = $(T_{RX} - T_{TX} - (L_{pc-preamble} + 1)*2560 - (k-1)*38400)/2$, where					
	T_{TX} = The transmission time of CD-ICH at access slot (n-2- T_{cpch}), where $0 \le (n-2-T_{cpch}) \le 14$					
	T _{cpch} can have values 0 or 1.					
	T_{RX} = The time of reception of the first chip (the first significant path) of the kth frame of the					
	PCPCH message from the UE, where k ∈ {1, 2,, N Max frames}.					
	N max frames is a higher layer parameter and defines the maximum length of the PCPCH					
	message. The PCPCH message begins at uplink access slot (n+Lpc-preamble/2),					
	where $0 \le (n + L_{pc\text{-preamble}}/2) \le 14$ and where $L_{pc\text{-preamble}}$ can have values 0 or 8.					
	Note: The definition of "first significant path" needs further elaboration.					
Range/mapping	The Propagation delay is given with the resolution of 3 chips with the range [0,, 765] chips.					
	The Propagation delay shall be reported in the unit PROP_DELAY where:					
	PROP_DELAY_000: 0 chip ≤ Propagation delay < 3 chip					
	PROP_DELAY_001: 3 chip ≤ Propagation delay < 6 chip					
	PROP_DELAY_002: 6 chip ≤ Propagation delay < 9 chip					
	NOI_DELAT_002. 0 GIIIP \(\sigma\) FTOPAYALION WEIAY \(\frac{3}{2}\) GIIIP					
	DDOD DELAY 250, 750 ahis < Drangastion delay , 750 ahis					
	PROP_DELAY_252: 756 chip ≤ Propagation delay < 759 chip					
	PROP_DELAY_253: 759 chip ≤ Propagation delay < 762 chip					
	PROP_DELAY_254: 762 chip ≤ Propagation delay < 765 chip					
	PROP_DELAY_255: 765 chip ≤ Propagation delay					

6 Measurements for UTRA FDD

6.1 UE measurements

6.1.1 Compressed mode

6.1.1.1 Use of compressed mode/dual receiver for monitoring

A UE shall, on higher layers commands, monitor cells on other frequencies (FDD, TDD, GSM). To allow the UE to perform measurements, higher layers shall command that the UE enters in compressed mode, depending on the UE capabilities.

In case of compressed mode decision, UTRAN shall communicate to the UE the parameters of the compressed mode.

A UE with a single receiver shall support downlink compressed mode.

Every UE shall support uplink compressed mode, when monitoring frequencies which are close to the uplink transmission frequency (i.e. frequencies in the TDD or GSM 1800/1900 bands).

All fixed-duplex UE shall support both downlink and uplink compressed mode to allow inter-frequency handover within FDD and inter-mode handover from FDD to TDD.

Monitoring frequencies outside TDD and GSM 1800/1900 bands without uplink compressed mode is a UE capability.

UE with dual receivers can perform independent measurements, with the use of a "monitoring branch" receiver, that can operate independently from the UTRA FDD receiver branch. Such UE do not need to support downlink compressed mode.

The UE shall support one single measurement purpose within one compressed mode transmission gap. The measurement purpose of the gap is signalled by higher layers.

The following section provides rules to parametrise the compressed mode.

6.1.1.2 Parameterisation of the compressed mode

In response to a request from higher layers, the UTRAN shall signal to the UE the compressed mode parameters.

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CHANGE REQUEST Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.								
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For submission to: TSG RAN #8 for approval for information strategic for SMG use only) Form: CR cover sheet, version 2 for 3GPP and SMG The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.c								nly)
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Propagation delay measurement for PCPCH in TS25.215. Clauses affected: 7.4 PCPCH / AICH timing relation								
Other specs affected:	Other 3G co Other GSM of specifica MS test specifica BSS test specifical	tions cifications ecifications		List of CF	Rs:			
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- when AICH_Transmission_Timing is set to 0, then

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	au_{p\text{-p,min}} = 15360 \text{ chips (3 access slots)} 	au_{p\text{-a}} = 7680 \text{ chips} 	au_{p\text{-m}} = 15360 \text{ chips (3 access slots)}
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- when AICH_Transmission_Timing is set to 1, then

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\tau_{p\text{-}p,min} = 20480 \text{ chips (4 access slots)} \tau_{p\text{-}a} = 12800 \text{ chips} \tau_{p\text{-}m} = 20480 \text{ chips (4 access slots)}
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The parameter AICH_Transmission_Timing is signalled by higher layers.

7.4 PCPCH/AICH timing relation

The uplink PCPCH is divided into uplink access slots, each access slot is of length 5120 chips. Uplink access slot number n is transmitted from the UE τ_{p-al} chips prior to the reception of downlink access slot number n, n =0, 1, ...,14.

The timing relationship between preambles, AICH, and the message is the same as PRACH/AICH. Note that the collision resolution preambles follow the access preambles in PCPCH/AICH. However, the timing relationships between CD-Preamble and CD-ICH is identical to RACH Preamble and AICH. The timing relationship between CD-ICH and the Power Control Preamble in CPCH is identical to AICH to message in RACH. The T_{cpch} timing parameter is identical to the PRACH/AICH transmission timing parameter. When T_{cpch} is set to zero or one, the following PCPCH/AICH timing values apply.

Note that a1 corresponds to AP-AICH and a2 corresponds to CD-ICH.

 τ_{p-p} = Time to next available access slot, between Access Preambles.

Minimum time = 15360 chips + 5120 chips X Tcpch

Maximum time = 5120 chips X 12 = 61440 chips

Actual time is time to next slot (which meets minimum time criterion) in allocated access slot subchannel group.

- $au_{p-al} = ext{Time between Access Preamble and AP-AICH has two alternative values: 7680 chips or 12800 chips, depending on <math>T_{cpch}$
- $\tau_{a1\text{-cdp}}$ = Time between receipt of AP-AICH and transmission of the CD Preamble $\tau_{a1\text{-cdp}}$ has a minimum value of $\tau_{a1\text{-cdp, min}}$ =7680 chips.
- $\tau_{p\text{-cdp}} = \text{Time between the last AP and CD Preamble.} \ \tau_{p\text{-cdp}} \ \text{has a minimum value of} \ \tau_{p\text{-cdp-min}} \ \text{which is either 3 or} \ 4 \ \text{access slots, depending on} \ T_{cpch}$
- τ_{cdp-a2} = Time between the CD Preamble and the CD-ICH has two alternative values: 7680 chips or 12800 chips, depending on T_{cpch}
- $\tau_{cdp\text{-pcp}}$ = Time between CD Preamble and the start of the Power Control Preamble is either 3 or 4 access slots, depending on T_{cpch} .

The message transmission shall start 0 or 8 slots after the start of the power control preamble depending on the length of the power control preamble.

Figure 30 illustrates the PCPCH/AICH timing relationship when T_{cpch} is set to 0 and all access slot subchannels are available for PCPCH.