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*Technical Report*

**3<sup>rd</sup> Generation Partnership Project (3GPP);  
Technical Specification Group (TSG);  
Radio Access Network (RAN);  
1.28Mcps functionality for UTRA TDD Physical Layer**

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# Foreword

This Technical Report has been produced by the 3GPP.

The contents of the present document are subject to continuing work within the TSG and may change following formal TSG approval. Should the TSG modify the contents of this TS, it will be re-released by the TSG with an identifying change of release date and an increase in version number as follows:

Version 3.y.z

where:

- x the first digit:
  - 1 presented to TSG for information;
  - 2 presented to TSG for approval;
  - 3 Indicates TSG approved document under change control.
- y the second digit is incremented for all changes of substance, i.e. technical enhancements, corrections, updates, etc.
- z the third digit is incremented when editorial only changes have been incorporated in the specification.

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## 1 Scope

This Technical Report describes the 1.28Mcps functionality for UTRA TDD physical layer, identifies commonalities and explains the differences to the 3.84Mcps chip rate. Suggestions for alignment will be provided too.

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## 2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, the latest version applies.

- [1] TS 25.201: "Physical Layer - General Description"
- [2] TS 25.221: "Physical channels and mapping of transport channels onto physical channels (TDD)"
- [3] TS 25.222: "Multiplexing and channel coding (TDD)"
- [4] TS 25.223: "Spreading and modulation (TDD)"
- [5] TS 25.224: "Physical layer procedures (TDD)"
- [6] TS 25.225: "Physical layer – Measurements (TDD)"

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## 3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

CDMA	Code Division Multiple Access
PN	Pseudo Noise
QPSK	Quadrature Phase Shift Keying
RACH	Random Access Channel



## 4 Radio Requirements

### 4.1 Radio environments

### 4.2 Services

### 4.3 Operational requirements

#### 4.3.1 Deployment scenarios

In this section a number of deployment scenarios for NB TDD and mixed NB/WB TDD scenarios are described. The physical layer of the WB option is described in detail in 3GPP TSG RAN TS25.221-225 and the NB option is described in detail elsewhere in this document.

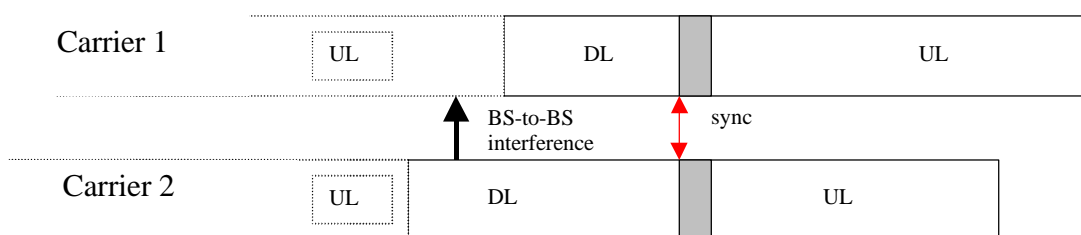
Co-ordinated operation is understood as relating to co-ordination between the nodeBs involved in the scenarios (e.g. synchronisation, knowledge of cell planning etc.). Uncoordinated operation is understood as that there is no co-ordination between the nodeBs involved in the scenarios. In both co-ordinated and uncoordinated cases the nodeBs can be from the same or a different operator.

The purpose of this section is to show potential usage of the currently defined NB option and provide a background for the standardisation discussions.

#### Scenario 1: NB TDD vs. co-ordinated NB TDD in adjacent bands

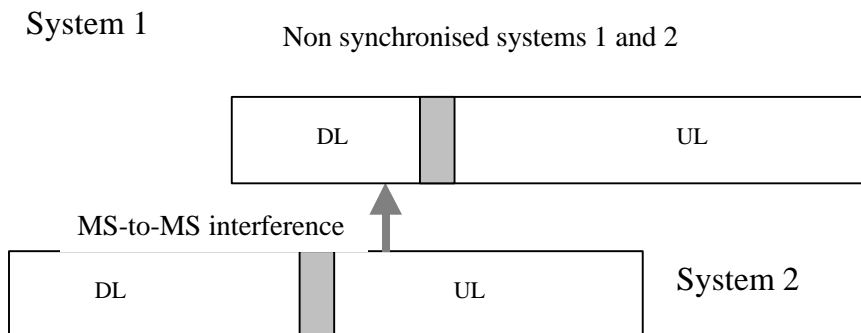
In this basic operation scenario the NB TDD carriers are used in a co-ordinated way, that is, the control slots of the systems are aligned to minimise the interference between the two systems. This means that the respective signalling slots are aligned in both the systems regardless of the current configuration of up- and downlink slots. That is, the configuration changes by shifting of the start of the sub frame boundaries.

Synchronised carriers 1 and 2. Synchronisation of signaling slots



### Scenario 2: NB TDD vs. uncoordinated NB TDD in adjacent bands

In this scenario different operators run the two interfering NB TDD systems in adjacent bands. The relative frame boundaries are unknown and there is no synchronisation between the two systems.

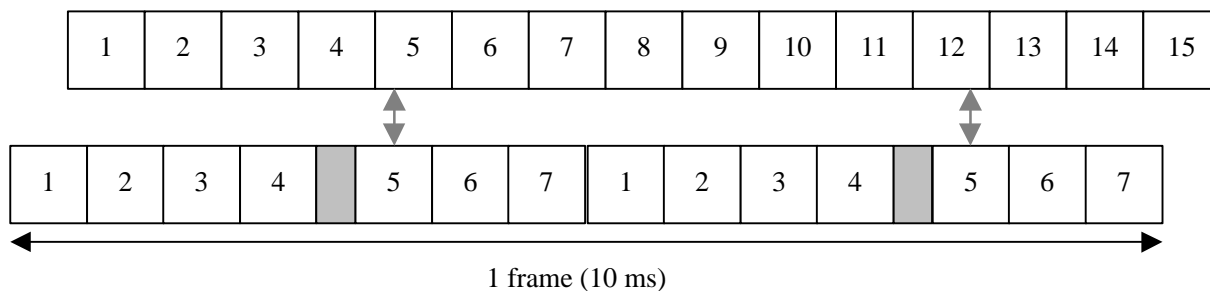


### Scenario 3: NB TDD vs. uncoordinated NB TDD in same band

This scenario is feasible when one operator owns a spectrum band and rents it out to private operators for example running corporate business systems. These systems are run in an uncoordinated way but possibly with some geographical distance between them.

### Scenario 4: NB TDD vs. WB TDD in uncoordinated operation in adjacent bands

Scenario 4 is similar to Scenario 2 except that we consider a WB TDD and a NB TDD system and the cross interference between them. The top frame structure is the WB TDD and the one below is the NB TDD.



### Scenario 5: NB TDD vs. WB TDD in uncoordinated operation in same band

The business model behind this scenario is similar as for Scenario 3 but with different types of interfering TDD systems.

4.4 Handover and Cell selection/reselection

4.5 Particular characteristics of the low chip rate TDD

---

## 5 High level characteristics

## 6 Physical layer - General description

### 6.1 General description of Layer 1

### 6.2 Document structure of the physical layer specification

## 7 Physical channels and mapping of transport channels onto physical channels

### 7.1 Transport channels

#### 7.1.1 Transport channels

##### 7.1.1.1 Dedicated transport channels

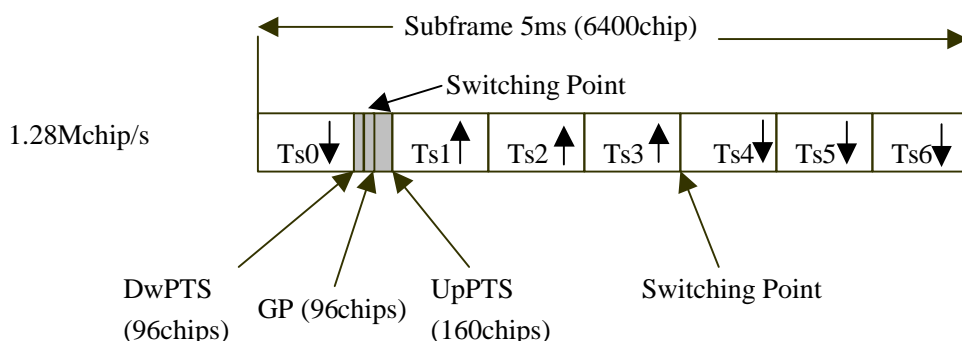
##### 7.1.1.2 Common transport channels

### 7.2 Physical channels

#### 7.2.1 Frame structure

[Description:]

For low chip rate option, the frame length is 10ms and the 10ms frame is divided into 2 sub-frames of 5ms. The frame structure for each sub-frame in the 10ms frame length is the same.



The frame structure for each sub-frame is shown in Figure 1

Figure 1 Structure of the sub-frame for low chip rate option

Tsn (n from 0 to 6): the nth normal time slot, 864 chips duration;

DwPTS: downlink pilot time slot, 96 chips duration;

UpPTS: uplink pilot time slot, 160 chips duration;

GP: main guard period for TDD operation, 96 chips duration;

[Rationale:]

In Figure 1, the total number of normal traffic time slot for uplink and downlink is 7, and the length for each normal time slot is 864 chips duration. Among the 7 normal traffic time slot, Ts0 is always allocated as downlink while Ts1 is always allocated as uplink. The time slots for the uplink and the downlink are separated by a switching point. Between the downlink time slots and uplink time slots, the special period is the switching point to separate the uplink and downlink. In each sub-frame of 5ms for low chip rate option, there are two switching points (uplink to downlink and vice versa). The proposed frame structure has taken

some new technologies into consideration, either the smart antenna (beam forming) technology or the uplink synchronization will be well supported.

Using the above frame structure, the low chip rate TDD option can operate on both symmetric and asymmetric mode by properly configuring the number of downlink and uplink time slots; (note that whatever the time slot configuration will be, the GP and DwPTS position within the frame should not change in order not to desynchronise the UEs and in order to allow Node B on air synchronisation procedures which make use of the DwPTS channel!) . It should be noted that in asymmetric operation mode, at least one normal uplink time slot and one downlink time slot will be allocated for traffic (Ts0 for downlink and Ts1 for uplink). The guard period GP of 96 chips can support the cell radius of up to about 11 km for uplink synchronization operation where the uplink transmission is advanced in macro-, micro- and pico- cell of small cells in cities or large cells in rural areas. Here the GP insures that an UE transmitting the UpPTS does not disturb the reception of the DwPTS for other UEs being close by. If this distortion is accepted in the network the cell radius can be bigger. (Note that the UpPTS is not continuously transmitted and the DwPTS is not continuously received.)

The only difference to the last version of the frame structure proposal for low chip rate is the improving of the numbering of the time slots. The physical layer behavior does not change.

[Explanation of difference:]

For both high chip rate option and low chip rate option, the frame length is 10 ms , But for low chip rate option the 10 ms length is divided into 2 sub-frame of 5 ms to allow the fast update of power control, uplink synchronization, and smart antenna beamforming.

For high chip rate option , each 10 ms frame consists of 15 time slots, each allocated to either the uplink or the downlink . So it has both single and multiple-switching point configuration both for symmetric and asymmetric allocation. While in the low chip rate option, the position of the big Guard Period GP and of the DwPTS and UpPTS physical channels, is always between Ts0 and Ts1 whatever the level of asymmetry be.

## 7.2.2 Dedicated physical channel (DPCH)

### 7.2.2.1 Spreading

#### 7.2.2.1.1 Spreading for Downlink Physical Channels

#### 7.2.2.1.2 Spreading for Uplink Physical Channels

### 7.2.2.2 Burst Types

[Description:]

In correspondence to the frame structure described above, the burst structures for Tsn, DwPTS and UpPTS are proposed. The burst structure for normal time slot (Tsn) is described in Figure 2.

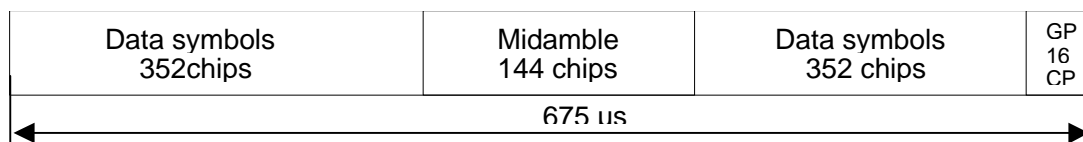


Figure 2 Burst structure for normal traffic time slot

The structure for DwPTS and UpPTS is described in Figure 3 and Figure 4.

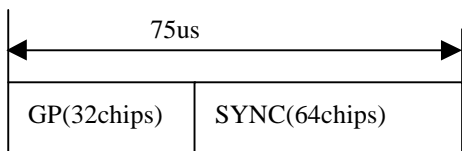


Figure 3 Structure for DwPTS

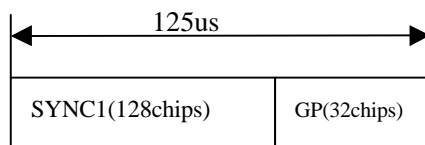


Figure 4 Structure for UpPTS

[Rationale:]

In Figure 2, the data symbols in each side of the midamble are 352 chips. The TPC bits for power control, the TFCI bits and the additional uplink synchronization bits (synchronization shift) are included in the Data symbols fields of the burst if they are needed. The amount of TFCI bits used is depending on the service and the details for TFCI, synchronization shift and TPC bits should be provided later with service mapping. For the power control symbols, the uplink synchronization control symbols and the TFCI the symbols around the midamble are used.

The GP field in Figure 2 for each time slot is used for protection between time slots to avoid the long delay multi-path interference. It should be noted that the GP of the TS0 together with the guard period in DwPTS is 48 chips long which is different with other normal guard period of 16 chips between time slots. This 'super long' guard period can be used to avoid the interference between the last normal downlink time slot and the downlink synchronization pilot burst. Otherwise, the interference to the last downlink time slot from the strong powered pilot will be serious to the traffic; and vice versa, the interference to the downlink pilot burst from the last downlink time slot will decrease the performance on downlink synchronization and cell search. Note that if the UEs serving Node B is far away and the UE makes handover measurements it will receive the beginning of the DwPTS of a close by Node B inside these 48 chip. 48 chip corresponds to 11 km difference in distance to the Node B. If the other Node B is more distant to the serving Node B, big guard period can be used for receiving the DwPTS of the handover candidate Node B.

In DwPTS and UpPTS, the content of SYNC and SYNC1 field are used for downlink and uplink pilot. The GP fields are used to separate the downlink (uplink) pilot from the normal downlink (uplink) time slot.

It should be pointed out that the uplink synchronization burst (SYNC1) is not followed by a RACH immediately. First the UL synchronization burst UpPTS is sent by the UE. This UpPTS is used for Node B to determine the received power level and the received timing. Second, the Node B transmits timing and power control information to the UE using the P-FACH (one burst message) within the next 4 frames. Then the P-RACH is transmitted. Both P-FACH and P-RACH are carrying single burst messages transmitted on a normal traffic time slot (see Fig. 2). This two phase procedure which is different with the GSM of one phase procedure has better performance than the classical approach as used in GSM. In this case, the normal traffic burst and access burst can be active in the same time slot and the interference is reduced for each other if they are time-aligned.

Note that the UpPTS has to be transmitted by the UE in advance (starting in the big GP) to arrive at the Node B at the position indicated in Figure 2. The UpPTS can also be received at a different position if the UE cannot or does not aim at the RX position indicated in Figure 2. Thus, the UpPTS can also start within the guard interval (RX, TX), depending on the situation in the system. This means relaxation to estimate timing in UE, e.g. from pathloss on P-CCPCH.

And the proposed frame structure can support all the environments of macro-, micro- and pico- cells. In vehicular environment, the speed can be more than 120km/h. Also in the proposed frame structure, some specific properties for low chip rate option such as smart antenna technology, uplink synchronisation, beamforming, etc can be well supported.

[Explanation difference:]

In high chip rate option, there are 2 burst types of DPCH. They have different midamble lengths. And there is only one burst type of DPCH in the low chip rate option. The use of the same burst structure for RACH and for traffic will guarantee that the RACH can be handled with conventional traffic on the same UL time slots since the RACH is already UL synchronised.



- 7.2.2.2.1 Transmission of TFCI
- 7.2.2.2.2 Transmission of TPC
- 7.2.2.2.3 Timeslot formats
  - 7.2.2.2.3.1 Downlink timeslot formats
  - 7.2.2.2.3.2 Uplink timeslot formats
- 7.2.2.3 Training sequences for spread bursts
  - 7.2.2.3.1 Midamble Transmit Power
- 7.2.2.4 Beamforming and Transmit Diversity

[Description:]

A smart antenna system is composed of an array of multiple antenna elements and coherent transceivers with advanced digital signal processing algorithms. Instead of a single fixed beam pattern from a traditional antenna, the smart antenna can dynamically generate multiple beam patterns, each of them is pointed to a particular UE, and such beam patterns can adapt to follow any UE intelligently. On the Rx side of Node B, such a feature, i.e., spatial selective reception at the Node B can greatly minimize co-channel interference from the co-channel UEs at different locations, thus increase the Rx sensitivity and lead to higher capacity. It can also effectively incorporate multipath components to combat multipath fading. On the Tx side of Node B, intelligent spatially selective Tx (downlink) beamforming can also greatly reduce the interference to other co-channel UEs, then dramatically save the output power requirement and lead to higher capacity. It should be noted that this section only describes a preferred approach to beamforming, other high performance techniques may also be applicable.

The low chip rate option is mainly based on the smart antenna technology. Some main technical features of the low chip rate TDD option such as 5 ms sub-frame structure are based on the smart antenna request. These technical relationships will be explained in details in other TRs which mention these features.

When DL beamforming or TX Diversity is used, at least for the resource units beamforming/Tx Diversity is applied to and which are allocated to dedicated channels, the resource units shall get one individual midamble per user or per resource unit according to midamble generation, even in DL.

[Rationale:]

The smart antenna array is composed of  $N$  antenna elements,  $N$  related feed cables and  $N$  coherent RF transceivers in RF part. By use of the A/D converters or D/A converters in analog baseband (ABB), the Rx and Tx analog signals are interfaced to the digital baseband (DBB) part over the high-speed data bus. In this model, all antenna elements related feed cables and coherent RF transceivers will be calibrated before operating.

## Beamforming

For the Node B is equipped with smart antenna array and DBB DSP, when a signal comes from one UE within the coverage of the Node B, each antenna element and coherent RF receiver will get it. Because of the different location of the different antenna element, the phase of the Rx signal will be different. In case of multipath propagation, each path will come from different directions with different amplitude and delay.

Then the Rx signal at each antenna element will show different phase and amplitude. After the front-end processing in RF part and A/D converters processing in ABB, digitized Rx signal with the phase and amplitude information will be sent to DSP in DBB part. After despreading in the DBB processor, the Rx data of each code channel may be obtained. The purpose of smart antenna in uplink is to find the best  $E_b/I_0$  after the combination. Theoretically, spatial reception at Node B can add up all useful signals while canceling all multipath interference. The next step is to realize downlink beamforming. The Tx signal of the each code channel is got by some algorithms that enable the UE to obtain the best  $E_b/I_0$ . In TDD system, because of the symmetrical performance in wave propagation, it is possible to directly use the spatial reception at Node B results to downlink beamforming.

## Fast beamforming

It is always very important to reach fast beamforming to catch the time variation in mobile network. The Node B should have a in-time reaction to the fast changing beam patterns. And this is the reason that the TDD interval in low chip rate option is 5ms while 10ms in high chip rate option. This value is a compromise in considering both the number of time slots and the switching speed of RF components.

In smart antenna system, the BTS need receive the UpLink data first, then decide the UE's position, and then beamform to UE in Downlink, but the UE does not need to transmit regularly for the Node B to determine the antenna weights when it is in idle mode.

[Explanation difference:]

For high chip rate option, the chapter about beamforming is already existed. Like the high chip rate option is that not only each user can get one midamble but also each resource allocated to that user can (but need not to) get an individual midamble. The benefit of this is that the signaling overhead is reduced.

## 7.2.3 Primary common control physical channel (P-CCPCH)

### 7.2.3.1 Primary common control physical channel (P-CCPCH)

#### 7.2.3.1.1 P-CCPCH Spreading

#### 7.2.3.1.2 P-CCPCH Burst Types

#### 7.2.3.1.3 P-CCPCH Training sequences

#### 7.2.3.1.4 Block STTD antenna diversity for P-CCPCH

### 7.2.3.2 Secondary common control physical channel (S-CCPCH)

#### 7.2.3.2.1 S-CCPCH Spreading

#### 7.2.3.2.2 S-CCPCH Burst Types

#### 7.2.3.2.3 S-CCPCH Training sequences

### 7.2.3.3 The physical random access channel (PRACH)

#### 7.2.3.3.1 PRACH Spreading

#### 7.2.3.3.2 PRACH Burst Types

#### 7.2.3.3.3 PRACH Training sequences

#### 7.2.3.3.4 Association between Training Sequences and Channelisation Codes

### 7.2.3.4 The physical synchronisation channel (PSCH)

### 7.2.3.5 Physical Uplink Shared Channel (PUSCH)

### 7.2.3.6 Physical Downlink Shared Channel (PDSCH)

### 7.2.3.7 The Page Indicator Channel (PICH)

## 7.2.4 Beacon function of physical channels

### 7.2.4.1 Location of physical channels with beacon function

### 7.2.4.2 Physical characteristics of the beacon function

## 7.2.5 Midamble Allocation for Physical Channels

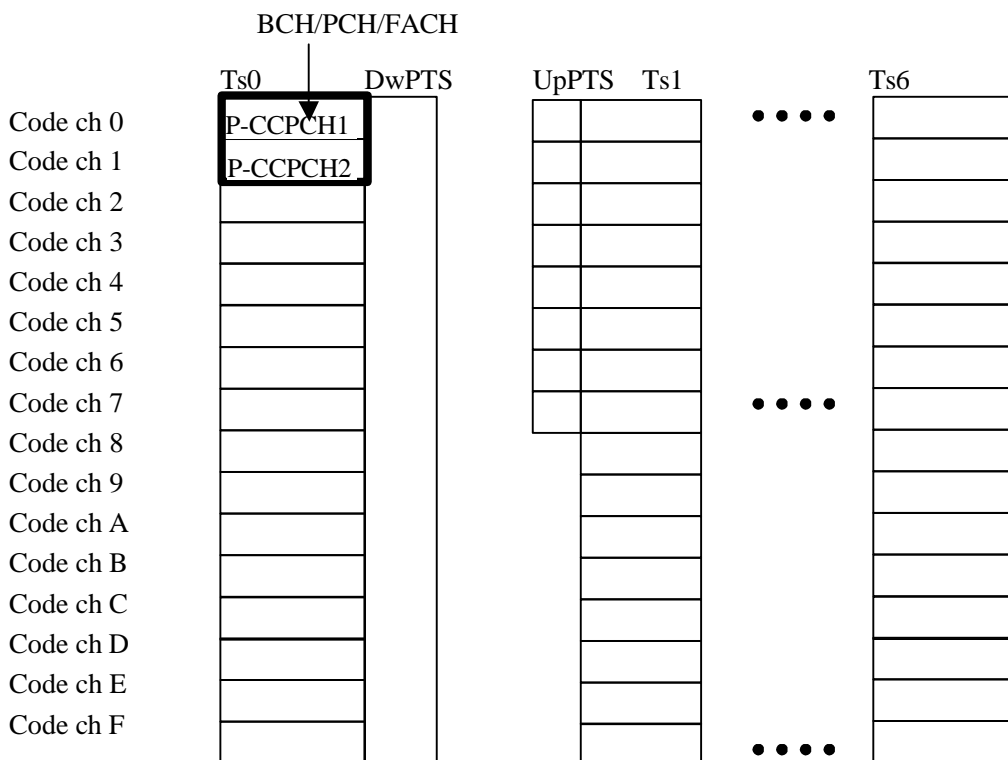
## 7.3 Mapping of transport channels to physical channels

### 7.3.1 Dedicated Transport Channels

### 7.3.2 Common Transport Channels

[Description:]

The following figure shows the mapping of BCH, FACH and PCH transport channels onto the P-



CCPCHs :

Figure 1 Transport channels mapping onto the physical channels

In low chip rate option, There are two P-CCPCH, P-CCPCH 1 and P-CCPCH 2 which are mapped onto i channelisation codes 0 and 1 (spreading factor 16) A cell should always contain P-CCPCH 1 and P-CCPCH 2 The transport channels mapped onto the P-CCPCH shall effectively be mapped onto P-CCPCH 1 and P-CCPCH 2 using the multi-code function in the channel coding and multiplexing (See physical channel segmentation in 25.222). As far as the SCCPCH is concerned, two cases can be considered. Either there are as well two SCCPCH, S-CCPCH 1 and SCCPCH 2 mapped onto two codes of spreading factor 16 or there is a single SCCPCH corresponding to a single code of spreading factor 8. The SCCPCHs may be mapped on any DL time slot. (as show in the figure 1). More details are giving as following:

The BCH is mapped on a pre-defined number of RUs/physical channels, so that the UE can unambiguously decode it. As it is for the TDD high chip rate option and for FDD mode, the low chip rate option as well foresees for one P-CCPCH only. On the combined P-CCPCH1+P-CCPCH2, different logical channels can be mapped according to the multi-frame structure.

[Rational:]

### 7.3.2.1 The Broadcast Channel (BCH)

The BCH is always mapped on the P-CCPCH1+P-CCPCH2. Due to the adoption of smart antenna, in order to provide the coverage of the whole cell, the P-CCPCHs must have in general higher transmission power level with omni-directional or sectorial pattern (without adaptive beamforming) compared with the other physical channels which can be adaptively beamformed. The BCH is time multiplexed with other channels in the multi-frame.

The UE can find the beginning of each block which is delivered on the P-CCPCHs; that is the beginning of the interleaving period, through the DwPTS sequence and its relative phase with respect to the P-CCPCHs midamble sequences. Each DwPTS can have 4 different phases and can be independently assigned by the Node B. Several continues different phase DwPTSs's combination can indicate the BCH's position in the multi-frame and the start position of the interleaving period. Also the beginning of the control multiframe can be detected from phase relations. To ensure correct decisions, an additional bit coded together with a BCH block, allows the UE to know the BCH interleaving block in P-CCPCHs.

### 7.3.2.2 The Paging Channel (PCH)

The PCH is a special broadcast channel used to page UEs from RNC. As mentioned above, it can also be mapped onto the P-CCPCHs time multiplexed with the BCH, FACH( see figure 1) , and, therefore, transmitted with the same power level and antenna pattern as those of the BCH. PCH, FACH and BCH will occupy their own blocks in the multi-frame structure. And this is the preferred way, in some condition, the PCH can be mapped onto a different physical channel (S-CCPCH or SCCPCH1+SCCPCH2, on any DL time slot but not on the codes used for the P-CCPCHs.) , the location of PCH is indicated on the BCH.( This gives more flexibility to the system.)

### 7.3.2.2 The Forward Channel (FACH)

The FACH is used to carry control information to a mobile station when the system knows the location cell of the mobile station. The FACH may also carry short user packets. The FACH can be mapped onto the P-CCPCHs time multiplexed with the BCH and PCH( see figure 1) , and, therefore, transmitted with the same power level and antenna pattern as those of the BCH. PCH, FACH and BCH will occupy their own blocks in the multi-frame structure. And this is the preferred way, in some condition, the FACH can be mapped onto a different physical channel (S-CCPCH or SCCPCH1+SCCPCH2 , on any DL time slot but not on the codes used for the P-CCPCHs.) , the location of FACH is indicated on the BCH.( This gives more flexibility to the system.)

[Explanation difference:]

In high chip rate option, the BCH is always mapped onto P-CCPCH and the PCH/FACH onto the S-CCPCH. The P-CCPCH always contains only the BCH . The secondary SCH indicates in which timeslot a mobile can find the PCCPCH containing BCH. And the location of PCH is indicated on the BCH.

In low chip rate option, the BCH is mapped only onto the P-CCPCHs (Primary Common Control Physical CHannel). The P-CCPCHs can also contain the PCH and FACH as well as the BCH. The P-CCPCHs are mapped onto the DL time slot preceding the DwPTS using two codes of that time slot (as shown in the figure 1) as described above. According the frame structure, P-CCPCHs carrying the BCH is followed by DwPTS, so when the UE detects the SYNC word, it can immediately find the BCH.

### 7.3.2.3 The Random Access Channel (RACH)

[Description:]

The RACH is mapped onto the P-RACH physical channel. The P-RACH configuration (time slot number and assigned spreading codes) is broadcast through the BCH information.

[Rationale:]

The RACH is mapped onto the P-RACH physical channel. The P-RACH can be configured by the network operator.

The P-RACHs can use either any spreading factor 16 RU or any spreading factor 8 RU in any UL time slot of the sub-frame. The spreading codes and time slots assigned to the P-RACHs are broadcast by the cell from the BCH. The capability of mapping RACH onto any UL time slot offers more flexibility to the system. The interference handling is then configurable. As the RACH is different from the other traffic it may be advantageous to distribute the RACH resources on several time slots.

The uplink sync codes (SYNC1 sequences) used by the UEs for UL synchronisation have a well known association to the P-RACHs, as broadcast by the BCH.

On the P-RACH, both power control and uplink synchronisation control is used.

The burst type used on the P-RACH is the same as for a traffic channel.

[Explanation difference:]

In low chip rate TDD option the random access procedure has two-step approach. The PRACH uses the close loop power control algorithm which is similar with the traffic channel..

In high chip rate TDD option the PRACH uses open loop power control. The details of the employed open loop power control algorithm may be different from the corresponding algorithm on other channels.

In low chip rate TDD option the burst type used on the P-RACH is the same as for a traffic channel while in high chip rate TDD option the burst type of the PRACH is a little different from the traffic channel.

- 7.3.2.4 The Synchronisation Channel (SCH)
- 7.3.2.5 Common Transport Channels for ODMA networks
- 7.3.2.6 The Uplink Shared Channel (USCH)
- 7.3.2.7 The Downlink Shared Channel (DSCH)

## Annex A (Normative): Basic Midamble Codes

- A.1 Basic Midamble Codes for Burst Type 1 and PRACH Burst Type
- A.2 Basic Midamble Codes for Burst Type 2
- A.3 Association between Midambles and Channelisation Codes
  - A.3.1 Association for Burst Type 1 and K=16 Midambles
  - A.3.2 Association for Burst Type 1 and K=4 Midambles
  - A.3.4 Association for Burst Type 2 and K=6 Midambles
  - A.3.5 Association for Burst Type 2 and K=3 Midambles

## Annex B (Informative): CCPCH Multiframe Structure

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## 8 Multiplexing and channel coding

### 8.1 Transport channel coding/multiplexing

#### 8.1.1 Error detection

##### 8.1.1.1 CRC calculation

##### 8.1.1.2 Relation between input and output of the Cyclic Redundancy Check

#### 8.1.2 Transport block concatenation and code block segmentation

##### 8.1.2.1 Concatenation of transport blocks

##### 8.1.2.2 Code block segmentation

#### 8.1.3 Channel coding

##### 8.1.3.1 Convolutional Coding

##### 8.1.3.2 Turbo coding

###### 8.1.3.2.1 Turbo coder

###### 8.1.3.2.2 Trellis termination in turbo code

###### 8.1.3.2.3 Turbo code internal interleaver

#### 8.1.4 Radio frame size equalisation

#### 8.1.5 1st interleaving

#### 8.1.6 Radio frame segmentation

#### 8.1.7 Rate matching

##### 8.1.7.1 Determination of rate matching parameters

##### 8.1.7.2 Bit separation for rate matching

##### 8.1.7.3 Rate matching pattern determination

#### 8.1.8 TrCH multiplexing

#### 8.1.9 Physical channel segmentation



## 8.1.10 2nd interleaving

8.1.10.1 Frame related 2nd interleaving

8.1.10.2 Timeslot related 2<sup>nd</sup> interleaving

## 8.1.11 Physical channel mapping

8.1.11.1 Mapping scheme after frame related 2<sup>nd</sup> interleaving

8.1.11.2 Mapping scheme after timeslot related 2<sup>nd</sup> interleaving

## 8.1.12 Multiplexing of different transport channels onto one CCTrCH, and mapping of one CCTrCH onto physical channels

8.1.12.1 Allowed CCTrCH combinations for one UE

8.1.12.1.1 Allowed CCTrCH combinations on the uplink

8.1.12.1.2 Allowed CCTrCH combinations on the downlink

## 8.1.13 Transport format detection

8.1.13.1 Blind transport format detection

8.1.13.2 Explicit transport format detection based on TFCI

8.1.13.2.1 Transport Format Combination Indicator (TFCI)

## 8.2 Coding for layer 1 control

8.2.1 Coding of transport format combination indicator (TFCI)

8.2.1.1 Default TFCI word

8.2.1.2 Coding of short TFCI lengths

8.2.2 Coding of Paging Indicator (PI)

8.2.3 Coding of Transmit Power Control (TPC)

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## 9 Spreading and Modulation

### 9.1 Data modulation

#### 9.1.1 Symbol rate

#### 9.1.2 Mapping of bits onto signal point constellation

### 9.2 Spreading modulation

#### 9.2.1 Basic spreading parameters

#### 9.2.2 Spreading codes

#### 9.2.3 Scrambling codes

#### 9.2.4 Spread and scrambled signal of data symbols and data blocks

### 9.3 Synchronisation codes

#### 9.3.1 Code Generation

#### 9.3.2 Code Allocation

##### 9.3.2.1 Code allocation for Case 1:

##### 9.3.2.2 Code allocation for Case 2:

##### 9.3.2.3 Code allocation for Case 3:

#### 9.3.3 Evaluation of synchronisation codes

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## 10 Physical layer procedures

### 10.1 Transmitter Power Control

#### 10.1.1 General Parameters

#### 10.1.2 Uplink Control

##### 10.1.2.1 Common Physical Channel

##### 10.1.2.2 Dedicated Physical Channel

#### 10.1.3 Downlink Control

##### 10.1.3.1 Common Physical Channel

##### 10.1.3.2 Dedicated Physical Channel

### 10.2 Timing Advance

#### 10.2.1 With UL Synchronization

[Description:]

This section described the detail description on the UL synchronization including the establishment of UL synchronization and maintenance of the UL synchronization.

[Rationale:]

##### 10.2.1.1 The establishment of uplink synchronization

###### 10.2.1.1.1 Preparation of uplink synchronization (downlink synchronization)

When a UE is powered on, it first needs to establish the downlink synchronisation with the cell as describe in paper about cell search procedure. Only after the UE can establish and maintain the downlink synchronisation, it can start the uplink synchronisation procedure.

###### 10.2.1.1.2 Establishment uplink synchronisation

Although the UE can receive the downlink synchronization signal from the Node B, the distance to Node B is still uncertain which would lead unsynchronized uplink transmission. Therefore, the first transmission in uplink direction is performed in a special time-slot UpPTS to reduce interference in traffic time-slots.

The timing used for the SYNC1 burst are set e.g. according to the received power level of DwPTS and/or P-CCPCH.

At the detection of the SYNC1 sequence in the searching window, the Node B will evaluate the received power levels and timing, and reply by sending the adjustment information to UE to modify its timing and power level for next transmission and for establishment of the uplink synchronisation procedure. Within the next 4 sub-frames, the Node B will send the adjustment information to the UE (in a single subframe message in the P-FACH) The uplink synchronisation procedure, normally used for a random access to the system, can also be used for the re-establishment of the uplink synchronisation when uplink is out of synchronisation.

### 10.2.1.2. Maintenance of uplink synchronisation

For the maintenance of the uplink synchronization, the midamble field of each uplink burst can be used.

In each uplink time slot the midamble in each UE is different. The Node B can estimate the power level and timing shift by measuring the midamble field of each UE in the same time slot. Then, in the next available downlink time slot, the Node B will signal the Synchronisation Shift (SS) and the Power Control (PC) commands to enable the UE to properly adjust respectively its Tx timing and Tx power level.

These procedures guarantee the reliability of the uplink synchronisation. The uplink synchronization can be checked once per TDD sub-frame. The step size in uplink synchronization is configurable and re-configurable and can be adapted from 1/8 chip to 1 chip duration. The following updates for UL synchronization are possible: 1 step up; 1 step down; no update.

[Explanation difference:]

For high chip rate option, uplink synchronisation is mentioned in 4.3 of TS25.224. But the implementation method is a little different with the low chip rate option. For low chip rate option, the establishment of the UL synchronization is done by using the UpPTS and the P-FACH.

It allocates a unique time slot UpPTS for UE to establish uplink synchronisation in the access procedure. The benefit of this method is when the UE wants to do random access, the P-RACH will have minimum interference to other traffic channel. Vice versa, it will also reduce the interference from traffic channels to P-RACH.

## 10.3 Synchronisation and Cell Search Procedures

### 10.3.1 Cell Search

[Description:]

In this section, a 4-step cell search procedure for low chip rate TDD option is described which is a slightly different with the current 3 step cell search procedure for high chip rate TDD option.

[Rational:]

During the initial cell search, the UE searches for a cell. It then determines the DwPTS synchronization, scrambling and basic midamble code identification, control multi-frame synchronisation and then reads the contents in BCH. This initial cell search is carried out in 4 steps:

#### Step 1: Search for DwPTS

During the first step of the initial cell search procedure, the UE uses the SYNC (in DwPTS) to acquire DwPTS synchronization to a cell. This is typically done with one or more matched filters (or any similar device) matched to the received SYNC which is chosen from PN sequences set. A single or more matched filter (or any similar device) is used for this purpose. During this procedure, the UE needs to identify which of the 32 possible SYNC sequences is used.

#### Step 2: Scrambling and basic midamble code identification

During the second step of the initial cell search procedure, the UE receives the midamble of the P-CCPCH. The P-CCPCH is followed by the DwPTS. In the current low chip rate TDD option each DwPTS code corresponds to a group of 4 different basic midamble code. Therefore there are total 128 midamble codes and these codes are not overlapping with each other. Basic midamble code number divided by 4 gives the SYNC code number. Since the SYNC and the group of basic midamble codes of the P-CCPCH are related one by one (that is, once the SYNC is detected, the 4 midamble codes can be determined), the UE knows which 4 basic midamble codes is used. Then the UE can determine the used basic midamble code using a try and error technique. The same basic midamble code will be used throughout the frame. As each basic midamble code is associated with a scrambling code, the scrambling code is also known by that time. According to the result of the search for the right midamble code, UE may go to next step or go back to step 1.

#### Step 3: Control multi-frame synchronisation

During the third step of the initial cell search procedure, the UE searches for the head of multi-frame indicated by QPSK phase modulation of the DwPTS with respect to the P-CCPCH midamble. The control multi-frame is positioned by a sequence of QPSK symbols modulated on the DwPTS. [n]consecutive DwPTS are sufficient for detecting the current position in the control multi-frame. To ensure correct decisions, an additional bit coded together with a BCH block, allows the UE to know the BCH interleaving block in P-CCPCH. According to the result of the control multi-frame synchronisation for the right midamble code, UE may go to next step or go back to step 2.

#### Step 4: Read the BCH

The (complete) broadcast information of the found cell in one or several BCHs is read. According to the result the UE may move back to previous steps or the initial cell search is finished. [Explanation difference:]

The initial cell search procedure is optimized considering the frame structure that is needed to enable UL synchronization and other specific features and properties for low chip rate option .

For high chip rate option , the three steps are : slot synchronisation, frame synchronisation and code-group identification, scrambling code identification.

For low chip rate option , the four steps are : search for DwPTS , scrambling and basic midamble code identification, control multi-frame synchronisation and the read of BCH information.

## 10.4 Discontinuous transmission (DTX) of Radio Frames

## 10.5 Downlink Transmit Diversity

### 10.5.1 Transmit Diversity for DPCH

#### 10.5.1.1 Determination of Weight Information

##### 10.5.1.1.1 STD Weights

##### 10.5.1.1.2 TxAA Weights

### 10.5.2 Transmit Diversity for SCH

#### 10.5.2.1 SCH Transmission Scheme

### 10.5.3 Transmit Diversity for P-CCPCH

#### 10.5.3.1 P-CCPCH Transmission Scheme

## 10.6 Random Access Procedure

[Description:]

The random access procedure and the collision problems for low chip rate option are described here. It include the preparation of random access, the random access procedure and the procedure for random access collision.

Note:

In this paper, the P-FACH is just a physical channel used to carry one burst message responding to SYNC1 during random access procedure. There is no mapping relationship between FACH and P-FACH. The P-FACH here is a little like the AICH in FDD.

[Rationale:]

### 10.6.1 Preparation of random access

When the UE is in Idle mode, it will keep the downlink synchronisation and read the cell broadcast information. From the used DwPTS, the UE will get the code set of 8 SYNC1 codes (signatures) assigned to UpPTS physical channel for random access. There are total 256 different SYNC1 sequences. SYNC1 sequences number divided by 8 gives the DwPTS sequences number. From the cell broadcast information, the UE will get to know the used SYNC1 sequences within the code set to be used; the description (codes, spreading factor, midambles, time slots) of the P-RACH channels, the description (codes, spreading factor, midambles, time slots) of the P-FACH channels, and other information (if needed ) related to random access.

In the BCH it is described what SYNC1 sequences are associated with what P-FACH resources; what P-FACHs are associated with what P-RACH resources and what P-RACH resources are associated with what (P/S-)CCPCH (carrying the FACH logical channel) resources.

Thus, when sending a SYNC1 sequence, the UE knows which P-FACH resources, P-RACH resources and CCPCH resources will be used for the access.

## 10.6.2 Random access procedures

The SYNC1 sequence in UpPTS following the guard time slot is used only for uplink synchronisation. The UE randomly selects one of the 1-8 possible signatures of the cell it wants to access to and sends it on the UpPTS physical channel.

Then the UE determines the timing and the Tx power level (open loop procedure) for the UpPTS and transmits the selected signature on the UpPTS.

Once the Node B detects the UpPTS transmission from an UE, the arrival time and the received power are known. The Node B determines the Tx power update and timing adjustment and sends them to the UE within the next four frames through the P-FACH (in a single burst/sub-frame message). Note that the P-FACH also contains the signature reference and the relative frame number (number of frames passed after the reception of the acknowledged signature) for cross check with the UE.

Once the UE receives the above mentioned control signalling from the chosen P-FACH (i.e. the P-FACH which is associated to the selected signature), its UpPTS sequence has been accepted by the Node B. Then the UE will adjust its timing and power level and send the RACH (also as a single burst/sub-frame message) on the P-RACH channel corresponding to the P-FACH exactly two frames later. In this step, the RACH sent to Node B by UE will have high synchronisation precision.

After that, the UE will receive a response from the network from the CCPCH associated to the P-RACH (by the FACH logical channel) indicating whether the UE random access has been accepted or not. In case it has been accepted the further signalling for establishing the link will take place on UL and DL dedicated channels assigned by the network through the FACH.

The UE can transmit a second UpPTS and wait for the response from the P-FACH for a further power and SS update before transmitting on the assigned resources.

## 10.6.3 Random access collision

When a collision is very likely or in bad propagation environment, the Node B does not transmit the P-FACH or cannot receive the SYNC1. In this case, the UE will not get any response from the Node B. Thus the UE will have to adjust its Tx time and Tx power level based on a new measurement and send a SYNC1 again after a random delay.

Note that at each (re-)transmission, the SYNC1 burst will be randomly selected again by the UE.

Due to the two-step approach a collision most likely happens on the UpPTS. The RACH RUs are virtually collision free. This two-step approach will guarantee that the RACH RUs can be handled with conventional traffic on the same UL time slots.

[Explanation difference:]

Different from the high chip rate option, the random access procedure of low chip rate option has two-step approach. The SYNC1 word is used to carry out uplink synchronisation and to resolve the access collision. This two-step procedure enables the RACH RUs to be handled with conventional traffic on the same UL time slots.

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- 11 Physical layer measurements
    - 11.1 Control of UE/UTRAN measurements
      - 11.1.1 General measurement concept
      - 11.1.2 Measurements for cell selection/reselection
      - 11.1.3 Measurements for Handover
      - 11.1.4 Measurements for DCA
      - 11.1.5 Measurements for timing advance
    - 11.2 Measurement abilities for UTRA TDD
      - 11.2.1 UE measurement abilities
        - 11.2.1.1 PCCPCH RSCP
        - 11.2.1.2 CPICH RSCP
        - 11.2.1.3 RSCP
        - 11.2.1.4 Timeslot ISCP
        - 11.2.1.5 UTRA carrier RSSI
        - 11.2.1.6 GSM carrier RSSI
        - 11.2.1.7 SIR
        - 11.2.1.8 CPICH Ec/No
        - 11.2.1.9 Physical channel BER
        - 11.2.1.10 Transport channel BLER
        - 11.2.1.11 UE transmitted power
        - 11.2.1.12 SFN-SFN observed time difference
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      - 11.2.2 UTRAN measurement abilities



- 11.2.2.1 RSCP
- 11.2.2.2 Timeslot ISCP
- 11.2.2.3 RSSI
- 11.2.2.4 SIR
- 11.2.2.5 Physical channel BER
- 11.2.2.6 Transport channel BLER
- 11.2.2.7 Transmitted carrier power
- 11.2.2.8 Transmitted code power
- 11.2.2.9 RX Timing Deviation

## Annex A (informative): Monitoring GSM from TDD: Calculation Results

- A.1 Low data rate traffic using 1 uplink and 1 downlink slot
  - A.1.1 Higher data rate traffic using more than 1 uplink and/or 1 downlink TDD timeslot

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## 12 Performance analysis of the low chip rate

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## 13 History

<b>Document history</b>		
V0.0.1	January 2000	Created in WG#10 in Beijing, Table of contents approved, R1-00-149
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V0.0.3	March 2000	Document renamed according to the conclusions in RAN#8, Madrid
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