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Agenda Item:
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Title: Cell search procedures for low chip rate TDD option
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Introduction

In 3GPP, there are two options for TDD mode. They are high chip rate option (3.84Mcps) and low chip rate option (1.28Mcps). The initial cell search procedure for low chip rate option is carried out in 4 steps. It is different from the high chip rate option because the low chip rate option has its own features and properties.

Conclusion

This document describes the cell search procedure of low chip rate option, it's proposed to include this cell search procedure for low chip rate TDD option in sub-clause 10.3 of TR 25.928

---------- changes to 25.928 begin ----------

10.3 Synchronisation and Cell Search Procedures

10.3.1 Cell Search Procedures

[Description:]

In this section, a 4-step cell search procedure for low chip rate TDD option is described which is a slightly different with the current 3 step cell search procedure for high chip rate TDD option.

[Rational:]

Cell Search Procedures

During the initial cell search, the UE searches for a cell. It then determines the DwPTS synchronization, scrambling and basic midamble code identification, control multi-frame synchronisation and then reads the contents in BCH. This initial cell search is carried out in 4 steps:

Step 1: Search for DwPTS

During the first step of the initial cell search procedure, the UE uses the SYNC (in DwPTS) to acquire DwPTS synchronization to a cell. This is typically done with one or more matched filters (or any similar device) matched to the received SYNC which is chosen from PN sequences set. A single or more matched filter (or any similar device) is used for this purpose. During this procedure, the UE needs to identify which of the 32 possible SYNC sequences is used.

Step 2: Scrambling and basic midamble code identification

During the second step of the initial cell search procedure, the UE receives the midamble of the P-CCPCH.The P-CCPCH is followed by the DwPTS. In the current low chip rate TDD option each

DwPTS code corresponds to a group of 4 different basic midamble code. Therefore there are total 128 midamble codes and these codes are not overlapping with each other. Basic midamble code number divided by 4 gives the SYNC code number. Since the SYNC and the group of basic midamble codes of the P-CCPCH are related one by one (that is, once the SYNC is detected, the 4 midamble codes can be determined), the UE knows which 4 basic midamble codes is used. Then the UE can determine the used basic midamble code using a try and error technique. The same basic midamble code will be used throughout the frame. As each basic midamble code is associated with a scrambling code, the scrambling code is also known by that time. According to the result of the search for the right midamble code, UE may go to next step or go back to step 1.

Step 3: Control multi-frame synchronisation

During the third step of the initial cell search procedure, the UE searches for the head of multi-frame indicated by QPSK phase modulation of the DwPTS with respect to the P-CCPCH midamble. The control multi-frame is positioned by a sequence of QPSK symbols modulated on the DwPTS. [n]consecutive DwPTS are sufficient for detecting the current position in the control multi-frame. To ensure correct decisions, an additional bit coded together with a BCH block, allows the UE to know the BCH interleaving block in P-CCPCH. According to the result of the control multi-frame synchronisation for the right midamble code, UE may go to next step or go back to step 2.

Step 4: Read the BCH

The (complete) broadcast information of the found cell in one or several BCHs is read. According to the result the UE may move back to previous steps or the initial cell search is finished.

[Explanation difference:]

The initial cell search procedure is optimized for low chip rate option to enable its specific features and properties (e.g. UL synchronization).

For high chip rate option , the three steps are : slot synchronisation, frame synchronisation and code-group identification, scrambling code identification.

For low chip rate option , the four steps are : search for DwPTS , scrambling and basic midamble code identification, control multi-frame synchronisation and the read of BCH information.

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