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Agenda Item:
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To: TSG RAN WG1
Title: Uplink synchronization for low chip rate TDD option
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Introduction

Uplink synchronization is one of the most important features of low chip rate TDD option. It will lead to an improved performance (lower interference) for the detector in the Node B, and thus, to higher capacity.

This paper gives an introduction to the establishment and maintenance of the uplink synchronization.

Conclusion

This paper is proposing to discuss and to include the following text proposal for UL synchronization in TR25.928.

--------------------- text proposal for TR25.928 begin ----------------------

[Description:]

this section described the detail description on the UL synchronization including the establishment of UL synchronization and maintenance of the UL synchronization.

[Rational:]

10.2.1 with Uplink Synchronization

10.2.1.1 The establishment of uplink synchronization

10.2.1.1.1 Preparation of uplink synchronization (downlink synchronization)

When a UE is powered on, it first needs to establish the downlink synchronisation with the cell as describe in paper about cell search procedure. Only after the UE can establish and maintain the downlink synchronisation, it can start the uplink sychronisation procedure.

10.2.1.1.2 Establishment uplink synchronisation

Although the UE can receive the downlink synchronization signal from the Node B, the distance to Node B is still uncertain which would lead unsynchronized uplink transmission. Therefore, the first transmission in uplink direction is performed in a special time-slot UpPTS to reduce interference in traffic time-slots.

The timing used for the SYNC1 burst are set e.g. according to the received power level of DwPTS and/or P-CCPCH.

At the detection of the SYNC1 sequence in the searching window, the Node B will evaluate the received power levels and timing, and reply by sending the adjustment information to UE to modify its timing and power level for next transmission and for establishment of the uplink

synchronisation procedure. . Within the next 4 sub-frames, the Node B will send the adjustment information to the UE (in a single subframe message in the P-FACH)

The uplink synchronisation procedure, normally used for a random access to the system, can also be used for the re-establishment of the uplink synchronisation when uplink is out of synchronisation.

10.2.1.2. Maintenance of uplink synchronisation

For the maintenance of the uplink synchronization, the midamble field of each uplink burst can be used.

In each uplink time slot the midamble in each UE is different. The Node B can estimate the power level and timing shift by measuring the midamble field of each UE in the same time slot. Then, in the next available downlink time slot, the Node B will signal the Synchronisation Shift (SS) and the Power Control (PC) commands to enable the UE to properly adjust respectively its Tx timing and Tx power level.

These procedures guarantee the reliability of the uplink synchronisation. The uplink synchronization can be checked once per TDD sub-frame. The step size in uplink synchronization is configurable and can be adapted from 1/8 chip to 1 chip duration. The following updates for UL synchronization are possible: 1 step up; 1 step down; no update.

[Explanation difference:]

For high chip rate option , uplink synchronisation is mentioned in 4.3 of TS25.224. But the implementation method is a little different with the low chip rate option. For low chip rate option, the establishment of the UL synchronization is done by using the UpPTS and the P-FACH.

It allocates a unique time slot UpPTS for UE to establish uplink synchronisation in the access procedure. The benefit of this method is when the UE wants to do random access, the P-RACH will have minimum interference to other traffic channel. Vice versa, it will also reduce the interference from traffic channels to P-RACH.

---------------------- text proposal for TR25.928 end ----------------------