**3GPP TSG RAN WG1 Meeting #107-e R1-21xxxxx**

**e-Meeting, November 11th – 19th, 2021**

**Source: Moderator (vivo)**

**Title: Discussion summary #1 of [107-e-NR-52-71GHz-05]**

**Agenda item: 8.2.5**

**Document for:** [Status]

# Introduction

In this contribution, we summarize issues regarding PDSCH/PUSCH enhancements for new SCSs on supporting NR from 52.6 GHz to 71 GHz for the following email discussion in RAN1 #107-e.

[107-e-NR-52-71GHz-05] Email discussion/approval on timeline related aspects adapted to each of the new numerologies 480kHz and 960kHz with checkpoints for agreements on November 15 and 19 – Huaming (vivo)

Note that the scope of agenda 8.2.5 including defining maximum bandwidth for new SCSs, time line related aspects adapted to each of the new numerologies 480kHz and 960kHz, reference signals, scheduling particularly w.r.t. multi-PDSCH/PUSCH with a single DCI, HARQ, etc. In this summary, only issues related to bandwidth for new SCSs, time line related aspects adapted to each of the new numerologies 480kHz and 960kHz and reference signals are summarized. Issues related to scheduling particularly w.r.t. multi-PDSCH/PUSCH with a single DCI, HARQ are not in the scope of this summary.

# PDSCH/PUSCH enhancements for new SCSs

In this section, we provide a summary of issues, observations and proposals related to PDSCH/PUSCH enhancements for new SCSs discussed in the submitted contributions.

As in WID, the related objectives for this summary of agenda 8.2.5 are the following.

* Physical layer aspects including [RAN1]:
	+ In addition to 120kHz SCS, specify new SCS, 480kHz and 960kHz, and define maximum bandwidth(s), for operation in this frequency range for data and control channels and reference signals, only NCP supported.

Note: Except for timing line related aspects, a common design framework shall be adopted for 480kHz to 960kHz

* + Time line related aspects adapted to 480kHz and 960kHz, e.g., BWP and beam switching timing, HARQ timing, UE processing, preparation and computation timelines for PDSCH, PUSCH/SRS and CSI, respectively.
	+ Evaluate, and if needed, specify the PTRS enhancement for 120kHz SCS, 480kHz SCS and/or 960kHz SCS, as well as DMRS enhancement for 480kHz SCS and/or 960kHz SCS.

## 2.1. Timeline

### Individual observations/proposals

The following are individual observations and proposals from the contributions.

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| Sources | Observations/proposals |
| [1, Huawei] | Proposal 1: The absolute time of 120 kHz SCS timelines should be adopted as the baseline to solve the left timeline issues in Rel-17.Proposal 2: For the value range of k1 defined for DCI format 1\_0, option 1 is preferred.Proposal 3: For NR operation with 480 kHz and/or 960 kHz SCS, CSI computation delay requirement 2 is always applied to the case of mixed SCS of PDCCH, CSI-RS and PUSCH.Proposal 4: For NR operation with 480 kHz and/or 960 kHz SCS, d1,1 and d2 (to derive Tproc,1 in PDSCH processing time) and d2,1 and d2 (to derive Tproc,2 in PUSCH preparation time) are scaled by 4 and 8 for 480kHz and 960kHz, respectively. |
| [2, Futurewei] | Proposal 1. For NR operation with 480 kHz and/or 960 kHz SCS, the CSI computation delay requirement 2 is also applied in the case of mixed SCS of PDCCH, CSI-RS and PUSCH.Proposal 2. To determine the minimum time gap (X) for wake-up and Scell dormancy indication, RAN1 can send an LS to RAN4 with a 4x/8x scaled reference value corresponding to 480kHz/960kHz SCS.Proposal 3. For the set of values for PDSCH-to-HARQ\_feedback timing indicator field in DCI format 1\_0, recommend adopting the Option 1: {4, 8, 12, 16, 20, 24, 28, 32} for 480 kHz and {8, 16, 24, 32, 40, 48, 56, 64} for 960 kHz.  |
| [3, vivo] | Proposal 1: For NR operation with 480 kHz and/or 960 kHz SCS, support the set of values below for PDSCH-to-HARQ\_feedback timing indicator field in DCI format 1\_0 in Rel-17.{7, 8, 9, 10, 12, 16, 20, 24} for 480 kHz, {13, 14, 15, 16, 24, 32, 40, 48} for 960 kHz.Proposal 2: For NR operation with 480 kHz and/or 960 kHz SCS, scale the corresponding values of 120 kHz SCS by 4x/8x for 480 kHz and 960 kHz SCS respectively for d1,1, d2, d2,1.Proposal 3: For NR operation with 480 kHz and/or 960 kHz SCS, scale the corresponding values of 120 kHz SCS by 4x/8x for 480 kHz and 960 kHz SCS respectively for the following UE timeline parameters for single and multi-PDSCH/PUSCH scheduling to maintain the same absolute time duration as that of 120 kHz SCS in FR2.* HARQ-ACK information in response to a SPS PDSCH release, N in 38.213 Section 10.2
* HARQ-ACK information in response to a detection of a DCI format 1\_1 indicating SCell dormancy, N in 38.213 Section 10.3
* Determination of the resource allocation table to be used for PUSCH, Δ in 38.214 Section 6.1.2.1.1
* UE PDSCH reception preparation time with cross carrier scheduling with different subcarrier spacings for PDCCH and PDSCH, Npdsch in 38.214 Section 5.5
* Application delay of the minimum scheduling offset restriction, Zµ in 38.214 Section 5.3.1

Proposal 4: For NR operation with 480 kHz and/or 960 kHz SCS, scale the corresponding values of 120 kHz SCS by 4x/8x for 480 kHz and 960 kHz SCS respectively for the minimum time gap for wake-up and Scell dormancy indication (DCI format 2\_6) to maintain the same absolute time duration as that of 120 kHz SCS in FR2. |
| [4, ZTE] | Observation 1: For 480kHz/960kHz SCS, the extra symbol has little effect on the total processing time.Proposal 7: For the PDSCH-to-HARQ\_feedback timing indicator field in DCI format 1\_0, Option 1 should be adopted.Proposal 8: For NR FR2-2, it is necessary to consider increasing the number of bits of PDSCH-to-HARQ\_feedback timing indicator field to 4 or 5 bits at least for DCI format 1\_1.Proposal 9: For NR operation with 480 kHz and/or 960 kHz SCS, d1,1 and d2 (to derive Tproc,1 in PDSCH processing time) and d2,1 and d2 (to derive Tproc,2 in PUSCH preparation time) are scaled by 4 and 8 for 480kHz and 960kHz, respectively.Proposal 10: * For NR operation with 480 kHz and/or 960 kHz SCS, scale the corresponding values of 120 kHz SCS by 4x/8x for 480 kHz and 960 kHz SCS respectively for the following UE timeline parameters for single and multi-PDSCH/PUSCH scheduling to maintain the same absolute time duration as that of 120 kHz SCS in FR2.
	+ HARQ-ACK information in response to a SPS PDSCH release, N in 38.213 Section 10.2
	+ HARQ-ACK information in response to a detection of a DCI format 1\_1 indicating SCell dormancy, N in 38.213 Section 10.3
	+ Determination of the resource allocation table to be used for PUSCH, Δ in 38.214 Section 6.1.2.1.1
	+ UE PDSCH reception preparation time with cross carrier scheduling with different subcarrier spacings for PDCCH and PDSCH, Npdsch in 38.214 Section 5.5
	+ Application delay of the minimum scheduling offset restriction, Zµ in 38.214 Section 5.3.1

Proposal 11: Minimum time gap for wake-up and Scell dormancy indication (DCI format 2\_6): X in 38.213 Section 10.3 for 480 kHz and 960 kHz SCS can be scaled by 4x/8x according to the value of 120kHz SCS, and X in 38.133 Section 8.2.1.2.7 is up to RAN4 |
| [6, Nokia] | Proposal 1: For NR operation with 480 kHz and/or 960 kHz SCS, the set of values for PDSCH-to-HARQ\_feedback timing indicator field in DCI format 1\_0 are* {6, 8, 12, 16, 20, 24, 28, 32} for 480 kHz and
* {12, 16, 24, 32, 40, 48, 56, 64} for 960 kHz.

Observation 1: There is no need to to scale parameters d1,1 and d2 (to derive Tproc,1 in PDSCH processing time) and d2,1 and d2 (to derive Tproc,2 in PUSCH preparation time)Observation 2: Rel-15/16 schemes for CPU can be reused for 480kHz and/or 960kHz SCS. Proposal 9: Define Δ values for 480 kHz and 960 kHz SCSs (in Table 6.1.2.1.1-5, TS 38.214). Consider the following values:* Δ = 12 for 480 kHz SCS
* Δ = 24 for 960 kHz SCS.

Proposal 10: Define Npdsch values for 480 kHz and 960 kHz SCSs (in Table 5.5-1, TS 38.214). Consider the following values:* + Npdsch = 28 for 480 kHz SCS
	+ Npdsch =56 for 960 kHz SCS.

Proposal 11: Define N for 480 kHz and 960 kHz SCSs in Section 10.2, TS 38.213. Consider the following values: N= 50 for 480 kHz SCS, and Npdsch = 100 for 960 kHz SCS.Proposal 12: Define N for 480 kHz and 960 kHz SCSs in Section 10.3, TS 38.213. Consider the following values: N= 62 for 480 kHz SCS, and Npdsch = 128 for 960 kHz SCS.Proposal 13: Define Zµ = 4 for both 480 kHz and 960 kHz SCSs in Section 5.3.1, TS 38.214. Proposal 14: CSI computation delay requirement 2 is always applied in the case of mixed SCS of PDCCH, CSI-RS and PUSCH* µ of table 5.4-1 and table 5.4-2 corresponds to the min (µPDCCH, µCSI-RS, µUL) where the µPDCCH corresponds to the subcarrier spacing of the PDCCH with which the DCI was transmitted and µUL corresponds to the subcarrier spacing of the PUSCH with which the CSI report is to be transmitted and µCSI-RS corresponds to the minimum subcarrier spacing of the aperiodic CSI-RS triggered by the DCI
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| [7, CATT] | Proposal 1: It is understood that there is no necessity to define N1/N2 for capability2 for 480 and/or 960 kHz SCS in Rel-17.Proposal 2: option 2 or option 2a can be supported for default k1 value, and words modified as following* Option 2: {7, 8, 9, 10, 11, 12, 13, 14} for 480 kHz and {~~13,~~14, 15, 16, 17, 18, 19, 20,21} for 960 kHz
* Option 2a: {1, 2, 3, 4, 5, 6, 7, 8} (same as in existing specification)

Note: the actual slot offset of k1 is the indicated value + offset where offset is ~~ceil~~ floor(N1/14)Proposal 3: for multi-PUSCHs transmission, the same rule for PUSCH preparation procedure time in section 6.4 of TS38.214 is applied.Proposal 4: for multi-PDSCHs transmission, the same rule for PDSCH processing procedure time in section 5.3 of TS 38.214 is applied. |
| [10, Ericsson] | Proposal 10 Adopt Option 1 for PDSCH-to-HARQ\_feedback timing indication in DCI format 1\_0. I.e., the K1 value in number of slots is directly indicated by the PDSCH-to-HARQ\_feedback timing indicator field value, scaled by 4 and 8 for 480 and 960 kHz SCS respectively. |
| [13, Lenovo] | Proposal 6: For supporting NR between 52.6 GHz and 71 GHz with high subcarrier spacing values including 480kHz and 960kHz, following enhancements should be supported to efficiently utilize UE’s limited processing capability to reduce latency and efficiently handle processing/preparation of CSI reports associated with multiple numerologies in parallel:* Same reference symbols duration (possibly the shortest duration corresponding to maximum supported SCS value) could be used for checking CPU availability corresponding to different CSI reports associated with different SCS values
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| [15, Samsung] | Proposal 1: Support Option 2 for default K1 value in DCI format 1\_0.Proposal 2: Support that the following parameters are scaled by 4 or 8 for 480kHz or 960kHz, respectively.* HARQ-ACK information in response to a SPS PDSCH release, N in 38.213 Section 10.2
* HARQ-ACK information in response to a detection of a DCI format 1\_1 indicating SCell dormancy, N in 38.213 Section 10.3
* Determination of the resource allocation table to be used for PUSCH, Δ in 38.214 Section 6.1.2.1.1
* UE PDSCH reception preparation time with cross carrier scheduling with different subcarrier spacings for PDCCH and PDSCH, Npdsch in 38.214 Section 5.5
* Application delay of the minimum scheduling offset restriction, Zµ in 38.214 Section 5.3.1

Proposal 3: Do not introduce additional scaling for d1,1 and d2 (to derive Tproc,1 in PDSCH processing time) and d2,1 and d2 (to derive Tproc,2 in PUSCH preparation time) for 480kHz and 960kHz. |
| [17, Apple] | Proposal 1: For NR operation with 480 kHz and/or 960 kHz SCS, scale the corresponding values of 120 kHz SCS by 4x/8x for 480 kHz and 960 kHz SCS respectively for the following UE timeline parameters for single and multi-PDSCH/PUSCH scheduling to maintain the same absolute time duration as that of 120 kHz SCS in FR2.* HARQ-ACK information in response to a SPS PDSCH release, N in 38.213 Section 10.2
* HARQ-ACK information in response to a detection of a DCI format 1\_1 indicating SCell dormancy, N in 38.213 Section 10.3
* Determination of the resource allocation table to be used for PUSCH, Δ in 38.214 Section 6.1.2.1.1
* UE PDSCH reception preparation time with cross carrier scheduling with different subcarrier spacings for PDCCH and PDSCH, Npdsch in 38.214 Section 5.5
* Application delay of the minimum scheduling offset restriction, Zµ in 38.214 Section 5.3.1
* FFS: Minimum time gap for wake-up and Scell dormancy indication (DCI format 2\_6): X in 38.213 Section 10.3 and 38.133 Section 8.2.1.2.7

Proposal 2: For NR operation with 480 kHz and/or 960 kHz SCS, the set of values for PDSCH-to-HARQ-feedback timing indicator field in DCI format 1\_0 is of the form offset + multiplier \* parameter.* The offset and multiplier can be either pre-defined in the specifications or configured via higher layer signaling

Proposal 3: The slot configuration period and the existing FR2 TD UL/DL configuration using either 60 kHz or 120 kHz is reused for 480kHz/960kHz SCS and the number of configuration slots is scaled accordingly.  |
| [18, LG] | Proposal #16: Introduce an extra symbol for ICI compensation in Tproc,1 calculation in order to cope with the case in which PDSCH processing may take a lot of time due to the severe influence of phase noise, e.g., for 120 kHz SCS and 64 QAM.Proposal #17: Consider scaling values for the extra symbols (e.g. d1,1 and d2 to derive Tproc,1) which are added to N1 when the PDSCH processing procedure time is calculated.Proposal #18: Consider scaling values for the extra symbols (e.g. d2,1 and d2 to derive Tproc,2) which are added to N2 when the PUSCH preparation procedure time is calculated.Proposal #19: The set of values for PDSCH-to-HARQ\_feedback timing indicator field in DCI format 1\_0, should be adjusted to practical value considering the increased N1, e.g., ceil(N1/14) or floor(N1/14).Proposal #20: Support the following set of values as PDSCH-to-HARQ\_feedback timing indicator field in DCI format 1\_0 for 480/960 kHz, respectively,* + {7, 8, 11, 12, 15, 16, 19, 20} for 480 kHz,
	+ {13, 14, 21, 22, 29, 30, 37, 38} for 960 kHz.

Proposal #21: CSI calculation delay requirement 2 is always applied for the mixed SCS case with 480/960 kHz SCS at any one of the SCSs for PDCCH, CSI-RS, or PUSCH.Proposal #22: Adopt the following CR so that in FR2-2 operation, all CPUs are not occupied even when UE processes the CSI report corresponding to the delay requirement 1 which is defined for FR1 and FR2-1.

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| A UE is not expected to be configured with an aperiodic CSI trigger state containing more than $N\_{CPU}$ Reporting Settings. Processing of a CSI report occupies a number of CPUs for a number of symbols as follows:- $O\_{CPU}=0 $for a CSI report with CSI-ReportConfig with higher layer parameter reportQuantity set to 'none' and CSI-RS-ResourceSet with higher layer parameter trs-Info configured- $O\_{CPU}=1 $ for a CSI report with CSI-ReportConfig with higher layer parameter reportQuantity set to 'cri-RSRP', 'ssb-Index-RSRP', 'cri-SINR', 'ssb-Index-SINR' or 'none' (and CSI-RS-ResourceSet with higher layer parameter trs-Info not configured)- for a CSI report with CSI-ReportConfig with higher layer parameter reportQuantity set to 'cri-RI-PMI-CQI', 'cri-RI-i1', 'cri-RI-i1-CQI', 'cri-RI-CQI', or 'cri-RI-LI-PMI-CQI', - if max{ µPDCCH, µCSI-RS, µUL} ≤ 3, and if a CSI report is aperiodically triggered without transmitting a PUSCH with either transport block or HARQ-ACK or both when L = 0 CPUs are occupied, where the CSI corresponds to a single CSI with wideband frequency-granularity and to at most 4 CSI-RS ports in a single resource without CRI report and where codebookType is set to 'typeI-SinglePanel' or where reportQuantity is set to 'cri-RI-CQI', $O\_{CPU}=N\_{CPU}$$O\_{CPU}=N\_{CPU}$,- otherwise, $O\_{CPU}=K\_{s}$$O\_{CPU}=K\_{S}$, where $K\_{s} $$K\_{s} $is the number of CSI-RS resources in the CSI-RS resource set for channel measurement. |

Proposal #23: Consider CSI processing timeline enhancements for better availability for CPUs for multiple CSI reports associated with different numerologies. |
| [20, Qualcomm] | Proposal 14: For NR operation with 480 kHz and/or 960 kHz SCS, consider the set of values for PDSCH-to-HARQ\_feedback timing indicator field in DCI format 1\_0 to be {7, 8, 12, 16, 20, 24, 28, 32} for 480 kHz and {13, 16, 24, 32, 40, 48, 56, 64} for 960 kHz.Proposal 15: Do not change k0/k2 range of values for the single PDSCH/PUSCH RRC TDRA tables. * The interpretation of the k2 value is done by applying an additional offset 11/21 for SCS 480kHz/960kHz.
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| [21, MediaTek] | Proposal 8: For determining the processing timelines for 480kHz and 960kHz, the following parameters are scaled by 4 and 8 for 480kHz and 960kHz, respectively.* $d\_{1,1} , d\_{2}$ (in PDSCH processing time)
* $d\_{2,1} , d\_{2}$ (in PUSCH preparation time)
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### Summary on timeline

#### PDSCH-to-HARQ\_feedback indicator

The following were agreed in RAN1#106bis-e.

Agreement:

For NR operation with 480 kHz and/or 960 kHz SCS, the value range of k1 indicated in RRC is -1 ~ 127 for DCI format 1\_1 and 0 ~ 127 for DCI format 1\_2.

* Note: this does not imply that DCI format 1\_2 supports multi-PDSCH scheduling

Agreement:

For NR operation with 480 kHz and/or 960 kHz SCS, decide the set of values for PDSCH-to-HARQ\_feedback timing indicator field in DCI format 1\_0in RAN1#107-e.

* Option 1: {4, 8, 12, 16, 20, 24, 28, 32} for 480 kHz and {8, 16, 24, 32, 40, 48, 56, 64} for 960 kHz
* Option 2: {7, 8, 9, 10, 11, 12, 13, 14} for 480 kHz and {13, 14, 15, 16, 17, 18, 19, 20} for 960 kHz
* Option 2a: {1, 2, 3, 4, 5, 6, 7, 8} (same as in existing specification)
	+ Note: the actual slot offset of k1 is the indicated value + offset where offset is ceil(N1/14)
* Other options are not precluded

Regarding the remaining issue of the set of values for PDSCH-to-HARQ\_feedback timing indicator field in DCI format 1\_0, the following contribution expressed their views.

[1, Huawei], [2, Futurewei], [4, ZTE], [10, Ericsson] support Option 1 as it is. Stated supporting reasons for Option 1 and/or concerns on Option 2/2a are:

* DCI format 1\_0 won’t support multi-PDSCH scheduling, and the TDD configuration should be aligned among different SCSs to maintain the same absolute HARQ feedback delay as 120 kHz SCS
* The maximum values of Option 2/2a are too low for gNB to schedule the nearest PUCCH resource when considering some typical DL/UL switching patterns with low ratios of UL slots
* Since the maximum HARQ process ID is extended to 32, thus the number of PDSCH-to-HARQ\_feedback timing indicator should be extended accordingly. From this point of view, the values in Option 1 have wider range and it should be adopted

On the other hand, [7, CATT], [15, Samsung], [18, LG] prefers Option 2/2a. Stated supporting reasons for Option 2/2a and/or concerns on Option 1 are:

* The scaled scheme (i.e. Option 1) has a limitation on scheduling flexibility where the distance between two scheduled last valid PDSCH shall be 4 or multiple of 4, if different HARQ-ACK feedback information of multi-PDSCHs are scheduled to one PUCCH resource
* The k1 value of 4 for 480 kHz and 8 for 960 kHz cannot be used in actual scheduling progress, since the delay of PUCCH transmission is less than duration of N1 symbols defined for 480 or 960 kHz
* Option 2/2a can provide more flexible PUCCH scheduling because one DL slot can be associated to more than one UL slot
* There is no need to increase the range of values significantly in situations where other DCI formats can already provide a sufficiently large value (0-127)

It is observed that both Option 1 and Option 2/2a impose certain constraints on scheduling of PDSCH and the associated HARQ-ACK. Some companies proposed some new options which are intended to combine the benefits of Option 1 and 2/2a or addressing some of disadvantages of each option.

[3, vivo] proposed to support {7, 8, 9, 10, 12, 16, 20, 24} for 480 kHz and {13, 14, 15, 16, 24, 32, 40, 48} for 960 kHz arguing that value 9 and 10 for 480 kHz and value 14 and 15 have more frequent use than value 28 and 32 in 480 kHz and value 56 and 64 in 960 kHz.

[6, Nokia] proposed a modified Option 1 with {6, 8, 12, 16, 20, 24, 28, 32} for 480 kHz and {12, 16, 24, 32, 40, 48, 56, 64} for 960 kHz given the smallest values of Option 1 can never be used. Similarly, [20, Qualcomm] proposed modifying the first value of each set in Option 1 to be {7, 8, 12, 16, 20, 24, 28, 32} for 480 kHz and {13, 16, 24, 32, 40, 48, 56, 64} for 960 kHz, to ensure that all the values are usable.

[17, Apple] proposed the set of values for PDSCH-to-HARQ-feedback timing indicator field in DCI format 1\_0 is of the form offset + multiplier \* parameter where the offset and multiplier can be either pre-defined in the specifications or configured via higher layer signalling and parameter is the same as the existing specification.

[18, LG] also proposed {7, 8, 11, 12, 15, 16, 19, 20} for 480 kHz and {13, 14, 21, 22, 29, 30, 37, 38} for 960 kHz if it is indeed to support larger values of PDSCH-to-HARQ\_feedback timing indicator field in DCI format 1\_0.

Moderator’s comment:

This issue was discussed in last RAN1 meeting and concerns on both Option 1 and Option 2/2a were expressed. Most supporting/opposing arguments for Option 1 and Option 2/2a were already expressed in the last RAN1 meeting. Based on the contributions, no clear majority for Option 1 or Option 2/2a can be claimed. It seems there’re strong arguments against either Option 1 or Option 2/2a.

Note that several new options are proposed in this meeting and hopefully to address concerns on both side. With that, moderator formulate the following proposal and encourage companies to indicate their 1st and 2nd preference (if any) to all options especially toward any of those new options to see if it can resolve the concerns and move forward as a compromise.

##### Proposal 1-1 (high priority)

For NR operation with 480 kHz and/or 960 kHz SCS, select one of the following options as the set of values for PDSCH-to-HARQ\_feedback timing indicator field in DCI format 1\_0 in RAN1#107e.

* Option 1: {4, 8, 12, 16, 20, 24, 28, 32} for 480 kHz and {8, 16, 24, 32, 40, 48, 56, 64} for 960 kHz
* Option 2: {7, 8, 9, 10, 11, 12, 13, 14} for 480 kHz and {13, 14, 15, 16, 17, 18, 19, 20} for 960 kHz
* Option 2a: {1, 2, 3, 4, 5, 6, 7, 8} (same as in existing specification)
	+ Note: the actual slot offset of k1 is the indicated value + offset where offset is ceil(N1/14)
* Option 3: {6, 8, 12, 16, 20, 24, 28, 32} for 480 kHz and {12, 16, 24, 32, 40, 48, 56, 64} for 960 kHz
* Option 4: {7, 8, 12, 16, 20, 24, 28, 32} for 480 kHz and {13, 16, 24, 32, 40, 48, 56, 64} for 960 kHz
* Option 5: {7, 8, 9, 10, 12, 16, 20, 24} for 480 kHz and {13, 14, 15, 16, 24, 32, 40, 48} for 960 kHz
* Option 6: {7, 8, 11, 12, 15, 16, 19, 20} for 480 kHz and {13, 14, 21, 22, 29, 30, 37, 38} for 960 kHz

Companies are encouraged to provide comments and/or to indicate 1st and 2nd preference (if any).

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| --- | --- |
| Company Name | Comments/Views |
| Samsung | Our preference is option 2. For new options (3/4/5/6), it is not essential to optimize default K1 values for DCI format 1\_0 because gNB can configure K1 values for DCI format 1\_1 by taking into account the CORESET/SS configuration and the TDRA configuration. |
| Lenovo, Motorola Mobility | Support Option 1 is it scales and have similar absolute duration as 120kHz. |
| Qualcomm | We prefer option 4 |
| Xiaomi | Option 1 is more preferred. |
| LG Electronics | In general, it is not necessary to put unused values into a very limited set of values. Considering the N1 values for 480/960 kHz SCS, the smallest value in Option 1 may never be used. For this reason, we oppose Option 1.**Our first preference is Option 2/2a**. Although it does not provide a larger scheduling range compared to Option 1, it is the simplest way to maintain the scheduling granularity with 1 slot just like the legacy default k1 values. The only concern mentioned at the last meeting about Option 2/2a is that the scheduling range is too small. If companies prefer a larger scheduling range to the scheduling granularity, (we still believe it is more important to have a high scheduling granularity than a larger range though), a midpoint between the range and the granularity could be a better way to compromise. In that respect, **our second preference is Option 6**. Comparing the scheduling granularity in units of slots corresponding to 120 kHz SCS, Option 6 can provide one more slot in which PDSCH is scheduled compared to Option 1. In other words, Option 6 could provide some degree of scheduling flexibility between Option 1 and Option 2.  |
| ZTE, Sanechips | We prefer Option1. Moreover, we wonder why the set of values for PDSCH-to-HARQ\_feedback timing indicator field in DCI format 1\_1 is not discussed. |
| Huawei, HiSilicon | We prefer Option 1 because it can be directly scaled from the field value without saving another table. The smallest value can be kept if higher UE capability is introduced in future release. |
| Apple | Given the options, our 1st preference will be option 2 and second will be option 4 i.e. option 1 with the smallest (non-usable) value removed.  |
| Futurewei | Several of the seven options are similar to each other, for example, Option 1, Option 3, and Option 4, where they have relatively larger range of values for both 480kHz and 960kHz than the other options. Considering the handling of other timeline parameters with 4x/8x scaling, we prefer these three options where K1 values have larger range for a uniform design. |

#### k0 and k2 for single PDSCH/PUSCH scheduling

In RAN1#106bis-e, the following were agreed.

Agreement:

For NR operation with 480 kHz and/or 960 kHz SCS, the value range of k0 is 0 ~ 128.

Agreement:

For NR operation with 480 kHz and/or 960 kHz SCS, the value range for k2 is 0 ~ 128.

[20, Qualcomm] raised an issue saying that the above agreements require revisiting all the RRC TDRA tables even if these TDRA tables are dedicated for single PDSCH/PUSCH grants. It argued that this will imply a lot of changes in the specifications, while the main motivation of introducing the new range of k0/k2 was to support multi-PDSCH/PUSCH scheduling via a single DCI. It proposed to keep the legacy ranges for k0/k2 for the legacy RRC TDRA tables, e.g., PUSCH-TimeDomainResourceAllocation and PDSCH-TimeDomainResourceAllocation. Furthermore, if legacy value ranges were kept for legacy RRC TDRA tables, [20, Qualcomm] also proposed that the interpretation of k2 value can be adjusted based on SCS, for example, an offset of 11/21 can be added to k2 configured value to determine the slot offset of the PUSCH for SCS 480kHz/960kHz.

Moderator’s comment:

Moderator’s understanding is that to support multi-PDSCH/PUSCH scheduling by a single DCI is one of the motivations introducing the new range of k0/k2. Other motivations to increase the value ranges were indeed mentioned during RAN1#106bis-e discussion, for example, to accommodate the increased values of N1 and N2.

Moderator would also like to remind that during RAN1#106bis-e discussion, existing range of k2 as in Rel-15/16+ SCS-specific offset was an option for consideration but was not agreed by companies. Furthermore, it is not clear to moderator that specification changes (e.g., re-interpretation of k2 value) is needed to address k2 value smaller than N2 timeline as that would be mis-configuration.

On the stated issue where a lot of specification changes are expected for revisiting all the RRC TDRA tables even if these TDRA tables are dedicated for single PDSCH/PUSCH grants, it is not clear to the moderator what are those expected changes and why those changes are expected.

Formulate the following discussion point so that the proponent can clarify and other companies can provide input.

##### Discussion point 1-2

Q1: Do you think k0 and k2 value ranges agreed in RAN1#106bis-e are not be applicable to single PDSCH/PUSCH scheduling? Please elaborate your reasoning.

Q2: Do you think re-interpretation of k2 value (with explicit RAN1 specification impact) is needed to address indicated k2 value smaller than N2 timeline? If so, for which case (single PDSCH/PUSCH scheduling and/or multi-PDSCH/PUSCH scheduling)? Please elaborate your reasoning.

Companies are encouraged to provide answers to above questions and/or input to the issue of k0/k2 value ranges for single PDSCH/PUSCH scheduling.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Samsung | Q1: k0 and k2 value ranges can be applicable to both single PDSCH/PUSCH scheduling and multi-PDSCH/PUSCH scheduling. It is unclear to us that the agreed k0/k2 value ranges make additional RAN1 specification works. Q2: No. gNB can configure k2 values accordingly.  |
| Lenovo, Motorola Mobility | Q1: In our view, k0 and k2 values can be also applicable to single PDSCH/PUSCH scheduling as we don’t see any additional effortsQ2: No |
| Qualcomm | Q1: As mentioned in our paper, we do not see strong gain from increasing the range for single PDSCH/PUSCH TDRA tables, will result in a lot of unnecessarily spec. changes. Q2: The re-interpretation of k2 is only needed when the range of k2 is up to 32  |
| Xiaomi | Agree with Samsung |
| ZTE, Sanechips | Q1: No, we think the agreed values in RAN1#106bis-e can be applicable to single PDSCH/PUSCH scheduling.Q2: No. |
| Huawei, HiSilicon | Q1: Same values set of k0 and k2 can be applied to single and multiple PXSCH scheduling. There seems no difference in the preparation time between these two scheme.Q2: No, it can be achieved by gNB’s configuration in TDRA table. |
| Apple | Q1. Applicable to both single and multiple PxSCH schedulingQ2: No |
| Futurewei | Q1: k0/k2 value extensions can be applied to single PDSCH/PUSCH scheduling.Q2: No.  |

#### CSI computation delay requirement

The following was agreed in RAN1#106-e.

Agreement:

For NR operation with 480 kHz and/or 960 kHz SCS, only value(s) for CSI computation delay requirement 2 are to be defined.

* FFS: The specific values

In RAN1#106bis-e, the following were agreed.

Agreement:

Remove [] from previous agreed Z3 values for NR operation with 480 and 960 kHz SCS. That is,

For NR operation with 480 and 960 kHz SCS, adopt at least the values of Z1, Z2 and Z3 as in the following table for single and multi-PDSCH/PUSCH scheduling to maintain the same absolute time duration as that of 120 kHz SCS in FR2.

* Note: $Xµ $is UE reported capability *beamReportTiming*; KB3 and KB4 is UE reported capability *beamSwitchTiming* for 480 and 960 kHz SCS respectively.

Table:  CSI computation delay requirement 2

|  |  |  |  |
| --- | --- | --- | --- |
|  | ***Z1* [symbols]** | ***Z2* [symbols]** | ***Z3* [symbols]** |
| *Z1* | *Z’1* | *Z2* | *Z’2* | *Z3* | *Z’3* |
| 5 | 388 | 340 | 608 | 560 | min(388, *X*5+ KB3) | *X*5 |
| 6 | 776 | 680 | 1216 | 1120 | min(776, *X*6+ KB4) | *X*6 |

Agreement:

For NR operation with 480 kHz and/or 960 kHz SCS, CSI computation delay requirement 2 is always applied at least for the case of same SCS operation.

* FFS: whether CSI computation delay requirement 2 is always applied in the case of mixed SCS of PDCCH, CSI-RS and PUSCH.

Regarding the remaining issue of whether CSI computation delay requirement 2 is always applied in the case of mixed SCS of PDCCH, CSI-RS and PUSCH, [1, Huawei], [2, Futurewei], [6, Nokia] and [18, LG] investigated this issue and all supported to always assume CSI computation delay requirement 2 in case of mixed SCS of PDCCH, CSI-RS and PUSCH. Their reason is that always applying CSI computation delay requirement 2 is compatible with existing specification.

Moderator’s comment:

According to TS 38.214, the CSI computation delay is determined as the minimum SCS of (1) aperiodic CSI-RS, (2) PDCCH scheduling the CSI-RS, and (3) PUSCH with corresponding CSI report. If the minimum SCS is determined as the timeline for CSI processing, the absolute time is the same as other SCSs if delay requirement 2 is applied. Formulate an explicit agreement to align the interpretation.

##### Proposal 1-3

For NR operation with 480 kHz and/or 960 kHz SCS, CSI computation delay requirement 2 is always applied in the case of mixed SCS of PDCCH, CSI-RS and PUSCH.

* Note: this applies when any one of the SCSs for PDCCH, CSI-RS, and PUSCH is 480 kHz or 960 kHz

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | Support the proposal  |
| Qualcomm | We are okay with the proposal  |
| LG Electronics | We support the Proposal 1-3 |
| ZTE, Sanechips | We support Proposal 1-3. |
| Huawei, HiSilicon | We support proposal 1-3 |
| Apple | We support the proposal |
| Futurewei | We support the Proposal 1-3.  |

[18, LG] also raised an associated issue on CPU when CSI computation delay requirement 2 is applied. It is observed that in existing specification of TS 38.214, UE should occupy all CPUs to compute the aperiodic CSI report which satisfies the condition of CSI computation delay requirement 1. When CSI computation delay requirement 2 is always applied to 480/960 kHz SCS, such behavior does not need to be applied for 480/960 kHz SCS since all CPUs are occupied for a (relatively) long time defined as requirement 2, which may reduce the CPU usage efficiency of the UE. Therefore, for 480/960 kHz SCS, a specification change is proposed so that all CPUs are not occupied even when UE processes the CSI report corresponding to the delay requirement 1. The relevant specification is in Clause 5.2.1.6 of the 38.214.

|  |
| --- |
| A UE is not expected to be configured with an aperiodic CSI trigger state containing more than $N\_{CPU}$ Reporting Settings. Processing of a CSI report occupies a number of CPUs for a number of symbols as follows:... - if a CSI report is aperiodically triggered without transmitting a PUSCH with either transport block or HARQ-ACK or both when *L* = 0 CPUs are occupied, where the CSI corresponds to a single CSI with wideband frequency-granularity and to at most 4 CSI-RS ports in a single resource without CRI report and where *codebookType* is set to 'typeI-SinglePanel' or where *reportQuantity* is set to 'cri-RI-CQI', $O\_{CPU}=N\_{CPU}$$O\_{CPU}=N\_{CPU}$,- otherwise, $O\_{CPU}=K\_{s}$$O\_{CPU}=K\_{S}$, where $K\_{s} $$K\_{s} $is the number of CSI-RS resources in the CSI-RS resource set for channel measurement. |

Moderator’s comment:

It is also moderator’s understanding that the CSI computation delay requirement 1 is not applicable for NR operation with 480 and/or 960 kHz SCS. With that, it makes sense to clarify UE behavior where all CPUs are occupied when UE processes the CSI report corresponding to the delay requirement 1 is not applicable for NR operation with 480 kHz and/or 960 kHz SCS. Formulate the following proposal.

##### Proposal 1-4

UE behavior where all CPUs are occupied when UE processes the CSI report corresponding to the delay requirement 1 is not applicable for NR operation with 480 kHz and/or 960 kHz SCS.

* The following example change to 38.214 Section 5.2.1.6 can be recommended to the editor to use at the editor’s discretion

 --- Unchanged parts omitted ---

if max{ *µPDCCH*, *µCSI-RS, µUL*} ≤ 3, and if a CSI report is aperiodically triggered without transmitting a PUSCH with either transport block or HARQ-ACK or both when *L* = 0 CPUs are occupied, where the CSI corresponds to a single CSI with wideband frequency-granularity and to at most 4 CSI-RS ports in a single resource without CRI report and where *codebookType* is set to 'typeI-SinglePanel' or where *reportQuantity* is set to 'cri-RI-CQI', $O\_{CPU}=N\_{CPU}$$O\_{CPU}=N\_{CPU}$,

--- Unchanged parts omitted ---

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | Support the proposal |
| Qualcomm | We are okay with the proposal  |
| LG Electronics | We support the Proposal 1-4 |
| ZTE, Sanechips | We are OK with this proposal. |
| Huawei, HiSlicon | We support the proposal |
| Apple | We are fine with the proposal |
| Futurewei | We are OK with the proposed changes. |

#### Other timeline parameters

Multiple contributions looked at other timeline parameters.

[1, Huawei] proposed that in general, the absolute time of 120 kHz SCS timelines should be adopted as the baseline to solve the left timeline issues in Rel-17.

For 480kHz and 960kHz, [1, Huawei], [3, vivo], [4, ZTE], [18, LG] and [21, MediaTek] all proposed that *d1,1* and *d2* (to derive *Tproc,1* in PDSCH processing time) and *d2,1* and *d2* (to derive *Tproc,2* in PUSCH preparation time) are scaled by 4 and 8 for 480kHz and 960kHz, respectively. Their reason is that if these extra symbols are simply added without scaling, the ratio of the increased processing time for 480/960 kHz will be smaller compared to 120kHz, which does not meet the original purpose for 480/960 kHz SCS with the same absolute time for 120 kHz SCS.

On the other hand, [6, Nokia] and [15, Samsung] thought there is no need to scale parameters d1,1 and d2 (to derive Tproc,1 in PDSCH processing time) and d2,1 and d2 (to derive Tproc,2 in PUSCH preparation time). [6, Nokia] thought the impact is neglectable in any case (due to the large parameter values defined for N1/N2) and not scaled according to SCS in Rel-15/16. [15, Samsung] argued that additional processing time relaxation does not provide any gains with the loose *N1*/*N2*/*N3* timeline given *d*1,1 (*d2,1*) and *d*2 is introduced in Rel-15/16 to provide additional processing time taking into account DM-RS position and UCI multiplexing.

Companies’ view to scale *d*1,1 (*d2,1*) and *d*2

Yes: [1, Huawei], [3, vivo], [4, ZTE], [18, LG], [21, MediaTek]

No: [6, Nokia], [15, Samsung]

Moderator’s comment:

Considering more companies prefer to scale *d*1,1 (*d2,1*) and *d*2, formulate the following proposal.

##### Proposal 1-5

For NR operation with 480 kHz and/or 960 kHz SCS, *d1,1* and *d2* (to derive *Tproc,1* in PDSCH processing time) and *d2,1* and *d2* (to derive *Tproc,2* in PUSCH preparation time) are scaled by 4 and 8 for 480kHz and 960kHz, respectively.

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Samsung | Not support. Further processing time relaxation is not helpful given that the loose N1/N2/N3 timeline.  |
| Qualcomm | We are okay with the proposal to unify the design strategy for the timelines of 480kHz/960kHz  |
| LG Electronics | We support the Proposal 1-5. By scaling these extra symbols, the purpose of their existence can be preserved and the unified design for the timelines of 480/960 kHz could be achieved. We would like to know if there is any special reason that these values (i.e., *d1,1*, *d2,1* and *d2*) should be kept small compared to N1. |
| ZTE, Sanechips | We are OK with this proposal. |
| Huawei, HiSilicon | We support the proposal 1-5. |
| Apple | We are fine with the proposal. |
| Futurewei | We are fine with the proposal with 4x/8x scaling for 480kHz/960kHz.  |

During last RAN1 meeting, there’s a discussion whether to scale the corresponding values of 120 kHz SCS by 4/8 for 480 kHz and 960 kHz SCS respectively for the following UE timeline parameters

* HARQ-ACK information in response to a SPS PDSCH release, N in 38.213 Section 10.2
* HARQ-ACK information in response to a detection of a DCI format 1\_1 indicating SCell dormancy, N in 38.213 Section 10.3
* Determination of the resource allocation table to be used for PUSCH, Δ in 38.214 Section 6.1.2.1.1
* UE PDSCH reception preparation time with cross carrier scheduling with different subcarrier spacings for PDCCH and PDSCH, Npdsch in 38.214 Section 5.5
* Application delay of the minimum scheduling offset restriction, Zµ in 38.214 Section 5.3.1

In this meeting, multiple companies investigated on this aspect and expressed their views. Summary of companies’ views:

Scale 4x/8x: [1, Huawei], [3, vivo], [4, ZTE], [15, Samsung], [17, Apple]

[6, Nokia] proposed to scale 2x/4x for first 4 parameters in above list and scale 2x/2x for Zµ in 38.214 Section 5.3.1

Moderator’s comment:

Given all but one company support to scale 4x/8x of the values of 120 kHz SCS for 480 kHz and 960 kHz SCS, formulate the following proposal.

##### Proposal 1-6

For NR operation with 480 kHz and/or 960 kHz SCS, scale the corresponding values of 120 kHz SCS by 4 and 8 for 480 kHz and 960 kHz SCS respectively for the following UE timeline parameters for single and multi-PDSCH/PUSCH scheduling to maintain the same absolute time duration as that of 120 kHz SCS in FR2.

* + HARQ-ACK information in response to a SPS PDSCH release, *N* in 38.213 Section 10.2
	+ HARQ-ACK information in response to a detection of a DCI format 1\_1 indicating Scell dormancy, *N* in 38.213 Section 10.3
	+ Determination of the resource allocation table to be used for PUSCH, *Δ* in 38.214 Section 6.1.2.1.1
	+ UE PDSCH reception preparation time with cross carrier scheduling with different subcarrier spacings for PDCCH and PDSCH, *Npdsch* in 38.214 Section 5.5
	+ Application delay of the minimum scheduling offset restriction, *Zµ* in 38.214 Section 5.3.1

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Samsung | Support |
| Lenovo, Motorola Mobility | Support the proposal |
| Qualcomm  | We support the proposal  |
| Xiaomi | Support |
| LG Electronics | We support the Proposal 1-6 |
| ZTE, Sanechips | We support the proposal. |
| Huawei, HiSilicon | We support the proposal |
| Apple | We support the proposal |
| Futurewei | We support the Proposal 1-6.  |

During last RAN1 meeting, there’s a discussion whether to scale the corresponding values of 120 kHz SCS by 4 and 8 for 480 kHz and 960 kHz SCS respectively for the following UE timeline parameter which appears in both RAN1 and RAN4 specifications.

* Minimum time gap for wake-up and Scell dormancy indication (DCI format 2\_6): X in 38.213 Section 10.3 and 38.133 Section 8.2.1.2.7

In this meeting, multiple companies expressed their views. [2, Futurewei] proposed that to determine the minimum time gap (X) for wake-up and Scell dormancy indication, RAN1 can send an LS to RAN4 with a 4x/8x scaled reference value corresponding to 480kHz/960kHz SCS. [3, vivo] and [4, ZTE] also proposed that minimum time gap for wake-up and Scell dormancy indication (DCI format 2\_6): X in 38.213 Section 10.3 for 480 kHz and 960 kHz SCS can be scaled by 4x/8x according to the value of 120kHz SCS.

Moderator’s comment:

Further input from RAN4 may be needed to make final decision on the value of this parameter. As proposed by [2], to make progress in RAN1 without waiting for RAN4’s reply, it is suggested to discuss in RAN1#107-e whether values of this parameter can be agreed in RAN1 and if so send an LS to RAN4 informing the reference values and asking RAN4 to decide. Otherwise, if no agreement of values can be made in RAN1, the values of this parameter is up to RAN4’s decision without any RAN1 input.

##### Proposal 1-7

From RAN1 perspective, for NR operation with 480 kHz and/or 960 kHz SCS, the value of minimum time gap for wake-up and Scell dormancy indication (DCI format 2\_6) is scaled by 4 and 8 of the corresponding value of 120 kHz SCS for 480 kHz and 960 kHz SCS respectively.

* Note: X in 38.213 Section 10.3 and 38.133 Section 8.2.1.2.7.
* Send LS to RAN4 to inform about RAN1’s agreement of the reference values and ask RAN4 to make final decision

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Samsung  | Support |
| Qualcomm  | We are okay with the proposal  |
| Xiaomi | support |
| LG Electronics | We are fine with the proposal, although still believe that it’s up to RAN4’s decision. |
| ZTE, Sanechips | We are OK with this proposal. |
| Huawei, HiSilicon | We support the proposal |
| Apple | We support the proposal |
| Futurewei | We support the Proposal 1-7.  |

#### CSI processing unit

Several contributions discussed issues related to CSI processing unit (CPU).

Regarding CPU, [6, Nokia] argued that CPU is the UE capability for simultaneous CSI calculations which is indicated as $N\_{CPU}$ and is related to channel variation or UE mobility rather than scheduling/subcarrier spacings. Therefore, there is no reason to increase the frequency of CSI reporting or rule for calculation of CSI occupancy. Given $N\_{CPU}$ is independent from numerology, [6, Nokia] observed that the existing specification for CPU can be reused for 480kHz and 960kHz SCS.

[13, Lenovo] raised an issue and thought it is critical to handle CPU availability check for UEs when it is required to process multiple CSI reports associated with different SCS values ranging from 15kHz to 960kHz in a parallel manner. It proposed same reference symbols duration (possibly the shortest duration corresponding to maximum supported SCS value) could be used for checking CPU availability corresponding to different CSI reports associated with different SCS values.

[18, LG] also looked into CPU availability check for multiple numerologies across active BWPs in different component carriers. It observed that in case multiple CSI reports are configured with multiple SCSs, the chance for high SCS to get available CPU at the time of checking unoccupied CPU may be less than that for low SCS. One mentioned solution for that is use of reference SCS for all CPU availability check regardless of actual SCS where reference SCS can be the lower SCS than the configured SCS, especially when high SCS is configured for UE.

Moderator’s comment:

Two companies proposed to enhance CPU availability check and one company thought existing specification can be reused with no enhancement. Note that the same issue has been discussed in RAN1#106bis-e where only the same three companies provided input on this aspect [22]. It seems no change of company views based on the contributions. Suggest other companies to provide input for discussion. Unless companies’ views changed in this meeting, moderator’s suggestion is to de-prioritize this discussion.

##### Discussion point 1-8

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | We support to have a reference SCS for CPU availability check regardless of the actual CPU for CSI – this would allow for fair opportunity to check availability for different CSI associated with different SCS.Considering the range from 15kHz to 960kHz, the issue is much prominent now |
| LG Electronics | We share the same view with Lenovo that the use of a reference SCS for CPU availability check would allow for fair opportunity for different CSI with different SCS. In addition, many timelines including CSI computation for 480/960 kHz SCS have been aligned with those for 120 kHz SCS and the intervals at which CPU availability is checked is also related to symbol duration. So, having same interval/granularity for CPU availability check regardless of SCS would further reduce the UE’s burden of continuous processing for every symbol for 480/960 kHz SCS. This is quite a simple enhancement and doesn’t impact how the actual processing timeline, but just fairer in terms of CPU availability check for all SCS. |
| ZTE, Sanechips | We agree to de-prioritize this discussion. |

## 2.2. Other issue(s)

### Individual observations/proposals

The following are individual observations/proposals from the contributions.

|  |  |
| --- | --- |
| Sources | Observations/proposals |
| [6, Nokia] | Observation 3:  Due to numerology difference between initial access and connected mode operations, residual timing error may cause a problem for PDCCH/PDSCH reception or PUSCH transmission.Proposal 14: Consider residual timing error problem and related potential solutions for >52.6 GHz operation in upcoming releases when optimizing its performance.  |
| [11, Intel] | Proposal 10: RAN1 to introduce UE capability of supporting high MCS/rank combinations in FR2-2. Observation 1: the maximal supported MCS indices reported as the UE capability can be in the range of [23, … 28] for {120kHz, rank 1}, [18, … 28] for {120kHz, rank 2}, [27, … 28] for {960kHz, rank 1}, [22, … 28] for {960kHz, rank 2}. Proposal 11: RAN1 to send LS to RAN4 about the modification needed for the UE capability of supporting high MCS/rank combinations in FR2-2.  |
| [13, Lenovo] | Observation 1: For supporting NR between 52.6 GHz and 71 GHz with high subcarrier spacing values including 480kHz and 960kHz, the selection of SCS value should not limited based on the frequency range. Other factors of channel conditions such as phase noise, ICI, Doppler, CQI, etc. plays an important role in determining the SCS value:* For DL channel, UE has all the required estimates related to channel, receiver phase noise and other impairments, etc.

Proposal 7: For supporting NR between 52.6 GHz and 71 GHz with high subcarrier spacing values including 480kHz and 960kHz, UE assistance for SCS/BWP selection should be supported to take in to account all the channel measurements and receiver impairments that are more prominent at higher frequency range* CSI reporting should be enhanced to report back suitable subcarrier spacing value based on measurements and receiver characteristics at UE
 |
| [15, Samsung] | Proposal 4: For multiple PUSCHs in in FR2-2, support DMRS bundling across the multiple PUSCHs introduced in Rel-17 Coverage enhancement WI. |
| [19, NTT DOCOMO] | Observation 1: The maximum gain of JCE over multi-PDSCH scheduling is about 0.41dB and 0.63dB in SCS of 480kHz and 960kHz, respectively.  Proposal 7: No need to support JCE for multi-PDSCH scheduling due to no significant gain. |
| [20, Qualcomm] | Proposal 5: Introduce new TRS configuration with higher frequency densities, 6 or 12 tones per RB to increase the TTL pull-in range when SCS of SSB is lower than the SCS of the data transmission.  |

### UE capability of supporting high MCS/rank combinations

[11, Intel] argued that phase noise is one of the main performance limiting factors in FR2-2 comparing to the lower NR bands. Given support of SCS 120kHz is mandatory for FR2-2 devices, and that PT-RS enhancements for FR2-2 are not supported in Rel-17, a UE capability of supporting certain MCS/rank combinations in FR2-2 is proposed as support of all 64QAM MCSs and transmission ranks is challenging without PT-RS enhancements.

[11, Intel] looked at existing UE capability signaling, *supportedModulationOrderDL*, *supportedModulationOrderUL*, *scalingFactor*, and observed that existing modulation order indication is only used to determine the max data rate and not used to explicitly limit MCSs that the gNB can use for scheduling. [11, Intel] thought the decision on the new UE capability should be made in RAN1, because it is needed from RAN1 perspective and it requires changes to RAN1 specification (38.214, section 6.1.4). Furthermore, [11, Intel] proposed to send LS to RAN4 about the modification needed for the UE capability of supporting high MCS/rank combinations in FR2-2 given the final values of maximum supported MCS index should be decided by RAN4 for each {SCS, rank} based on the set of reference hardware implementations the vendors consider.

Moderator’s comment:

Note that the same issue was raised in RAN1#106bis-e. At that time, companies expressed different preference on whether to define a new UE capability indicating supported high MCS/rank combinations and hence no agreement/conclusion was reached. Based on companies’ views expressed in RAN1#106bis-e [22], there’re several options can be considered on this aspect. Formulate the following for discussion.

##### Proposal 2-1

Regarding the potential sets of {SCS, MCS, rank} not supported by UE for NR operation in FR2-2, select one of the following options in RAN1#107-e

* Option 1: Introduce a new UE capability indicating the maximum supported MCS/rank combination for each SCS with corresponding RAN1 specification changes. Inform RAN4 about this new UE capability.
* Option 2: Leave the handling of the unsupported sets of {SCS, MCS, rank} to RAN4 without any RAN1 input
* Option 3: RAN1 send LS to RAN4 informing that UEs may not be able to support the target BLER for some sets of {SCS, MCS, rank}, and asking RAN4 to determine the sets of {SCS, MCS, rank} with which performance requirements can be defined.

Companies are encouraged to provide comments and indicate their preference on the above options.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| LG Electronics | We prefer Option 2 without further discussion in RAN1. |
| ZTE, Sanechips | In general, this kind of MCS, Rank, MCS should belong to RAN4 demod study, this can be discussed in RAN4. We prefer Option 2 and simply left this issue to RAN4. |
| Futurewei | Prefer that the issue is left for RAN4 to study.  |

### UE-assisted SCS adaptation

It is observed in [13, Lenovo] that for supporting NR between 52.6 GHz and 71 GHz with high subcarrier spacing values including 480kHz and 960kHz, the selection of SCS value should not limited based on the frequency range. Other factors of channel conditions such as phase noise, ICI, Doppler, CQI, etc. plays an important role in determining the SCS value. It further argued that UE is in a better position compared to gNB to make corresponding decision on which SCS value is more suitable given the UE estimates DL channel conditions such as phase noise, ICI, Doppler, CQI etc., and some other impairments based on the supported receiver algorithm. It then proposed that CSI reporting should be enhanced to report back suitable subcarrier spacing value based on measurements and receiver characteristics at UE.

Moderator’s comment:

Note that this is a single company proposal and the exact same aspect was discussed in RAN1#106bis-e. There was very limited input/interest from other companies in RAN1#106bis-e where only two companies commented on this aspect and both are not supporting this proposal stated either don’t see the reason for enhancement or feel it’s not a simple optimization [22]. Unless companies’ views are changed in this meeting, moderator suggest to de-prioritize this discussion.

##### Discussion point 2-2

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| ZTE, Sanechips | Agree with the moderator’s suggestion. |
| Futurewei | Ok with de-prioritizing the issue.  |
|  |  |

### DMRS bundling across the multiple PUSCHs

It is observed in [15, Samsung] that since the slot duration is smaller and the typical scenario is stationary scenario in 52.6~71GHz, coherent time may be longer compared with the slot duration. At least for multiple PDSCHs/PUSCHs with contiguous time domain resource, DMRS time domain density can be lower than one DMRS per PUSCH/PDSCH to reduce DMRS overhead without channel estimation performance degradation and equivalently improves PUSCH/PDSCH efficiency. [15, Samsung] proposed to support DMRS bundling across the multiple PUSCHs introduced in Rel-17 Coverage enhancement WI for NR operation in FR2-2.

Moderator’s comment:

Note that this issue was raised in RAN1#106bis-e during discussion for DMRS for multi-PDSCH/PUSCH scheduling. At that time, there’s a comment that transport block over multiple slots (TBoMS) was considered (in Rel-17 Coverage enhancement WI) which is different from multi-PUSCH scheduling, especially when the latter can have slot gaps [22].

Furthermore, it is also not clear to the moderator what specification impact is expected if this proposal is agreed. Suggest the proponent company to clarify and other companies to provide input for discussion.

##### Discussion point 2-3

Q1: Do you think DMRS bundling across the multiple PUSCHs introduced in Rel-17 Coverage enhancement WI can be applied for NR operation in FR2-2? Please elaborate your reasoning.

Q2: If the answer to Q1 is yes, is there any additional specification impact other than what has been specified for Rel-17 Coverage enhancement WI? If so, please elaborate the expected additional specification changes to support DMRS bundling across multiple PUSCHs for NR operation in FR2-2.

Companies are encouraged to provide comments/answers to above questions.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Samsung | Q1: According to the objective in Rel-17 Coverage enhancement WID, RP-211566, the features introduced in Rel-17 CovEnh WI is for both FR1 and FR2. The issue is whether FR2\_2 is included FR2 or not. We hope it is clarified. At least, since 120kHz SCS is applicable both FR2\_1 and FR2\_2, the features can be used for a serving cell with 120kHz SCS in FR2\_2. Q2: No additional specification impact is expected at least for 120kHz SCS. If it is identified that substantial specification works are needed, we are ok to not introduce DMRS bundling for FR2\_2.  |
| Qualcomm | Q1: Yes, as mentioned by Samsung at least for 120kHz SCS the DMRS bundling across the multiple PUSCHs should be supported for FR2-2Q2: No additional specification work should be needed.  |
| Huawei, HiSilicon | Q1: Yes. It can be extended to FR2-2. It could also be discussed in UE feature.Q2: No additional specification. |
| Apple | Q1: Yes, especially for 120 kHz. Agree that it should be a UE feature.Q2: No additional specification |
| Futurewei | Q1: Yes, DMRS bundling for SCS 120kHz can be applied for FR2-2;Q2: No specification effort for SCS 120kHz. |

### TRS enhancements

In [20, Qualcomm], it is observed that for PDSCH with high SCS (e.g., 960 kHz), the time tracking loop (TTL) may not be able to correct the typical timing error resulted from the 120kHz SSB detection as it may be out of its pull-in range. It then proposed to introduce new TRS configuration with higher frequency densities, 6 or 12 tones per RB to increase the TTL pull-in range when SCS of SSB is lower than the SCS of the data transmission.

[6, Nokia] also looked at the impact of residual timing error based SSB/SSS. It is observed that due to numerology difference between initial access and connected mode operations, residual timing error may cause a problem for PDCCH/PDSCH reception or PUSCH transmission. To address such issue, RS enhancement may be required. [6. Nokia] proposed to consider this more in detail in upcoming releases when optimizing performance of above 52.6GHz operation since this is the last RAN1 meeting for Rel-17 WI.

Moderator’s comment:

Note that this issue was discussed in RAN1#106bis-e with very limited input from companies. Suggest other companies to provide input for discussion.

Given this is the last RAN1 meeting of Rel-17 WI and no time for other companies to investigate this issue, moderator’s suggestion is to de-prioritize this discussion and consider it in future release as suggested by [6].

##### Discussion point 2-4

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| ZTE, Sanechips | Agree with the moderator’s suggestion. |
|  |  |
|  |  |

# Conclusion

TBD

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